Contribution à l'intégration 3D de composants passifs pour l'électronique de puissance

Thi Bang Doan

Université de Toulouse

THÈSE

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JURY

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M. Thierry LEBEY	*Directeur de Rechercher CNRS, Toulouse*	Directeur de thèse
M. François FOREST	*Professeur à l'Université Montpellier 2*	Codirecteur de thèse
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M. Charles JOUBERT	*Professeur à l'Université Lyon 1*	Rapporteur
M. Pierre BIDAN	*Professeur à l'université Paul Sabatier, Toulouse,*	Examinateur

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Ecole doctorale : *GEET*
Unité de recherche : *LAPLACE*
Directeur de Thèse: *Dr.Thierry LEBEY,* **Co-directeur de Thèse :** *Pr.François FOREST*
Rapporteurs : *Pr. Éric LABOURÉ et Pr. Charles JOUBERT*

THESIS

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COMMITTEE

Pr. Jean-Paul FERRIEUX	*Professor University Grenoble-G2ELab*	Chair
Dr. Thierry LEBEY	*Senior research scientist, CNRS of Laplace, Toulouse*	Supervisor
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Pr. Charles JOUBERT	*Professor University Lyon 1-Ampere*	Referee
Pr. Pierre BIDAN	*Professor University Paul Sabatier, Laplace, Toulouse*	Examiner

---

Doctoral school :*GEET*
Unit of research :*LAPLACE*
Supervisor: *Dr.Thierry LEBEY.* **Co-supervisor:** *Pr.François FOREST*
Referees: *Pr. Éric LABOURÉ* ***and*** *Pr.Charles JOUBERT*

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To my family
My parents
My husband
My daughter
And my sisters and brothers

Abstract

The performance of power electronics systems has been driven by relentless progress in semiconductor component integration over the past many years. Assemblies of active power switches and their drive circuits in compact modules enable miniaturization of the power switching part of the converters. However, the number of interconnections and discrete passive electromagnetic components such inductors, capacitors, and transformers, still limit the performance and possibilities for three-dimensional (3D) integration. An evolutionary new trend will require substantial reduction in the structural passives associated with active devices and system-level packaging to support increased demands for miniaturization, high performance, high reliability, and cost-effectiveness for power electronics.

The designs of 3-Dimensional Integrated Passive and Active Component (3D IPAC) modules are being developed thanks to advances in integrated technology and high dielectric permittivity materials, which are the focus of this dissertation. This work is performed mainly on capacitors because they are widely-used passive components, found in almost all electronic circuits with high volume and large footprint. High permittivity ferroelectric material is selected for compatibility with a simple and economical screen-printing technology aimed at fabricating planar integrated capacitors for different application purposes. Semiconductor dies and their drivers, placed directly on the surface of multilayer capacitive substrates, make it possible to reduce the size and interconnection lengths between active and passive devices, thus increasing reliability as well as performance of power electronic modules. The decoupling and flying functions of planar multilayer integrated capacitors are verified through experimentation thanks to two proposed DC-DC converter topologies.

Further study is also carried out to observe the effects of the cold isostatic pressing (CIP) process on dielectric properties of ferroelectric thick films. Under high pressure on multiple directions, the dielectric layer thickness is reduced, resulting in a higher capacitance value. Comparisons between compressed and uncompressed capacitors with the same configuration show that CIP is an effective way to increase capacitance value. This benefit suggests the opportunity for a design trend using a high capacitance value for greater filtering efficiency and decoupling purposes.

Keywords: *Passive component integration, Integrated multilayer capacitors, DC-DC integrated converter, Screen printing technique, Ferroelectric ceramic materials, Cold isostatic pressing*

Résumé

L'intégration des composants à semi-conducteur, qui s'est développée depuis de nombreuses années, a conduit à une augmentation des performances des systèmes électroniques. L'intégration d'un module compact, regroupant le composant actif et son circuit de commande, permet d'atteindre une réduction du volume de la partie liée à la commutation de puissance. Cependant, les interconnexions et les composants passifs tels que les inductances, les condensateurs ou les transformateurs constituent encore une limite tant pour les performances que pour l'intégration (3D ou non) des systèmes de puissance. La tendance actuelle est à la réduction substantielle du volume occupé par les composants passifs associés aux composants actifs, ceci afin d'augmenter la miniaturisation, les performances, la fiabilité tout en réduisant les coûts.

La conception de modules intégrant des composants actifs et des composants passifs qui soient de plus intégrés en 3D peut maintenant être envisagée en raison des progrès technologiques réalisés dans le domaine de l'intégration et par l'utilisation de matériaux présentant de fortes permittivités. Notre thèse s'inscrit dans cette démarche en se focalisant plus particulièrement sur les condensateurs, très largement utilisés et consommateurs de volume importants dans le convertisseur. Les matériaux ferroélectriques sont choisis en raison de leurs fortes permittivités, leur compatibilité avec la technique de sérigraphie, procédé relativement simple et économique permettant de réaliser des composants planaires. En plaçant les semi-conducteurs et leurs circuits de commande directement sur les condensateurs multicouches sérigraphiés, il en résulte une réduction des boucles d'interconnexions, une diminution du volume et une augmentation de la fiabilité et des performances. Des fonctions de découplage et de stockage ont été expérimentalement vérifiées dans deux topologies de convertisseurs continu-continu (DC-DC).

Une étude a également été menée afin de statuer sur l'impact du pressage isostatique à froid (CIP) sur les propriétés diélectriques des couches ferroélectriques. Outre la réduction de l'épaisseur des couches diélectriques, et ainsi, une augmentation de la valeur du condensateur, la comparaison entre des condensateurs ayant subis ou non le CIP montre que c'est une méthode efficace pour augmenter la valeur de leur capacité. L'intérêt de cette méthode est substantiel pour des applications nécessitant de fortes valeurs de capacités en vue d'un meilleur découplage et filtrage.

Mots-clés: *Intégration des composants passifs, Condensateurs multicouches intégrés, Convertisseur intégrés DC-DC, Sérigraphique, Matériaux céramiques ferroélectriques, Pressage isostatique à froid*

Résumé en Français

Introduction Général

L'électronique de puissance joue aujourd'hui un rôle important dans la conversion d'énergie. Ses domaines d'application se sont considérablement diversifiés allant de puissance de quelques Watts (alimentations pour systèmes nomades, domotique, automobile,…) jusqu'à plusieurs dizaines de MW (industrie lourde, traction ferroviaire, propulsion maritime, ...). Les convertisseurs de puissance tels que les convertisseurs continu-continu, les redresseurs, les onduleurs en interface entre le réseau et les applications (éclairage, actionneurs, machines…) minimisent les besoins en ressources fossiles. Une diminution du volume des structures de conversion, du cout de fabrication, et l'amélioration de leur rendement constituent les principaux axes de recherche du domaine, avec des répercussions sur de très larges gammes d'applications. Par conséquent, il est essentiel d'avoir une bonne maitrise de la technologie, de disposer d'un processus fiable et robuste associé à des matériaux performants. Le but est de répondre aux besoins et exigences croissantes d'un marché en perpétuelle évolution.

Au cours de ces dernières années, l'électronique de puissance a été sans relâche entraînée par les progrès de l'intégration des dispositifs actifs, par l'amélioration des topologies, des composants et du packaging. Bien que l'intégration des dispositifs semi-conducteurs permette de réduire la part liée aux composants actifs, la majeure partie du volume du convertisseur est souvent occupée par les composants passifs. Par conséquent, afin d'améliorer les performances, d'augmenter leur taux de fabrication (et de réduire les coûts) des dispositifs de l'électronique de puissance, l'accent a été mis sur l'amélioration de l'intégration des composants passifs. Parmi les composants passifs, les condensateurs occupent généralement le volume le plus important des circuits de l'électronique de puissance. Cette thèse se concentre sur l'intégration de ces composants. Les matériaux ferroélectriques sont choisis pour leur haute permittivité, pour leur compatibilité avec la technique de sérigraphie, procédé relativement simple et économique permettant de réaliser des composants planaires pour une grande gamme d'application

Le premier objectif de cette thèse consiste à développer et valider une technologie de substrats plats à proximité du "busbar" intégrant des couches capacitives. Ces couches capacitives peuvent être utilisées pour réaliser le condensateur de découplage requis par toutes les cellules de commutation sur leur bus continu et/ou pour réaliser les condensateurs d'un filtre de mode commun placé sur le même bus continu. Le procédé de fabrication a été optimisé afin de réaliser des condensateurs céramiques ferroélectriques multicouches présentant de bonnes performances électriques. Ces nouveaux composants passifs intégrés sont ensuite utilisés pour la réalisation du substrat multicouche plan intégré capacitif utilisé dans un convertisseur continu-continu.

Le deuxième objectif est de réaliser la fonction « condensateur flottant » intégré d'un convertisseur multiniveaux continu-continu. L'intégration de ces condensateurs sérigraphiés

permet de réduire l'inductance parasite du circuit de puissance à base de composants GaN. Elle permet aussi d'envisager un refroidissement par les deux faces. Un prototype de type hacheur 3-niveaux 48V-5V avec des condensateurs sérigraphies flottants est construit pour illustrer la faisabilité d'une telle solution.

Un autre axe de recherche concerne la mise en œuvre de matériaux ferroélectriques. Afin d'améliorer les caractéristiques et les performances des condensateurs intégrés, l'influence du pressage isostatique à froid (CIP) durant le procédé de fabrication a été analysé et son impact évalué. L'objectif principal de cette partie est d'étudier les caractéristiques des matériaux ferroélectriques sous pression isostatique et de proposer des alternatives afin d'améliorer la densité des condensateurs pour diverses applications.

Le manuscrit est composé de cinq chapitres qui vont être résumés succinctement:

- Chapitre I : Etat de l'art de l'intégration des composants passifs 3D.
- Chapitre II : Sélection de technologie et matériaux pour l'intégration
- Chapitre III : Analyse et caractérisation de condensateurs intégrés
- Chapitre IV : Impact du pressage isostatique à froid (CIP) sur les propriétés des couches ferroélectriques
- Chapitre V : Application à l'électronique de puissance

Chapitre I : Etat de l'art de l'intégration des composants passifs 3D

I. Raisons d'intégrer des composants passifs

Un convertisseur de puissance est constitué de différents composants actifs et passifs, montés en surface, interconnectés sur une carte de circuit imprimé ou sur un substrat. Une approche pour construire des convertisseurs de puissance plus compacts vise à accroître le niveau d'intégration des composants, qu'ils soient actifs ou passifs, via une augmentation de la fréquence de commutation, qui conduit à une réduction ou une atténuation des inductances ou des capacités les plus encombrantes. La structure 3D favorise l'assemblage de composants actifs et passifs permettant de miniaturiser les modules et les interconnexions simultanément. Réduire les longueurs d'interconnexion entre composants actifs et passifs augmente le niveau de performance, la fiabilité et permet de gagner de l'espace au niveau de la carte et du module. Pour répondre aux besoins sans cesse croissants de l'électronique de puissance, l'intégration de composants passifs doit suivre le rythme des progrès réalisés dans le domaine des composants actifs. Les facteurs suivants permettent de répondre à cette problématique :

1 Réduire la masse, le volume et la surface occupée:

- Éliminer les packagings des composants élémentaires

2 Améliorer les performances électriques:

- Réduire les longueurs de connexions aux condensateurs
- Réduire l'inductance parasite
- Réduire les surfaces (EMI)
- Améliorer l'intégrité du signal

3 Augmenter la flexibilité de conception

- Améliorer la conception des composants passifs pour n'importe quelle valeur comprise dans l'intervalle de la technologie.

4. Amélioration de la fiabilité

- limiter le nombre de brasures
- Réduire le nombre des trous et des vias
- Permettre un bon transfert de chaleur

5. Réduire le coût unitaire

- Éliminer les composants discrets
- Améliorer la robustesse
- Augmenter les possibilités de production de masse
- Augmenter la manufacturabilité (modularité et normalisation)

II. Comment intégrer des composants passifs en électronique de puissance ?

Par composants passifs, on entend les inductances, les condensateurs et les résistances. Ils peuvent se rencontrer sous la forme de composants discrets, de composants intégrés/embarqués (enfouis) et des réseaux passifs. Durant ces dernières années, les composants passifs se présentent essentiellement sous formes de composants discrets montés sur un même substrat que les composants actifs. Les inconvénients de l'utilisation de composants discrets résident dans le fait que: 1) des centaines de composants sont présents dans un circuit et leur assemblage discret occupe un espace important : 2) la présence de centaines de points de brasure est susceptible d'engendrer un problème crucial de fiabilité. Pour pallier ces inconvénients liés à l'occupation d'espace et à la fiabilité, de nombreuses recherches explorent le domaine de leur miniaturisation, ce qui a conduit à l'élaboration du concept de composants intégrés passifs qui consiste à fabriquer ces composants sous forme de groupe dans ou sur un substrat commun au lieu de les fabriquer de façon individuelle. La figure 1 vise à comparer des composants intégrés dans le PCB à des composants passifs discrets montés à sa surface. Il parait alors évident que le "circuit intégré " présente une plus grande miniaturisation par rapport au circuit discret.

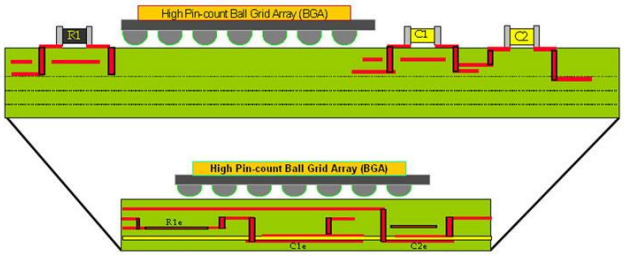


Figure 1: PCB classique avec des composants passifs discrets (en haut) et passifs intégrés dans le substrat (en bas).

III. État de l'intégration des composants passifs

Bien que l'intégration des composants actifs ait conduit à de nombreuses innovations dans l'amélioration des performances et dans la réduction de leur encombrement l'intégration des composants passifs doit faire face à des inconvénients similaires à ceux connus par l'intégration des composants actifs il y a de cela un demi-siècle :

1. Indétermination sur la nature des matériaux et des technologies: les recherches se poursuivent sur plusieurs types de matériaux résistifs et magnétiques ainsi que sur les matériaux diélectriques.
2. Le manque d'outils de conception: à la fois pour le dimensionnement des composants et leur positionnement.
3. Le besoin d'intégration « verticale »: le même fabriquant doit être capable de concevoir à la fois les substrats et les composants passifs.
4. Le problème du rendement : si un composant est défaillant, tout le substrat doit être remplacé.
5. Le problème de tolérance aux pannes.
6. L'absence de standardisation: il n'existe pas encore de standardisation commune entre les différents segments de l'industrie des composants passifs pour leur intégration.
7. La technologie du montage en surface s'améliore constamment.
8. Le manque d'un modèle de coût: la plupart des recherches se concentre sur la validation de la performance et la réduction de taille des composants passifs intégrés.

Il est donc difficile de savoir quand et comment l'utilisation de composants passifs intégrés peut être plus intéressante tant techniquement qu'économiquement.

IV. Principaux objectifs

1. Raisons pour l'intégration de condensateurs

Parmi les composants passifs, les condensateurs discrets utilisés dans diverses fonctions (filtrage, découplage, contrôle,...) occupent généralement le plus d'espace et sont les composants les plus volumineux dans les circuits de puissance. Une façon simple de construire un convertisseur d'encombrement plus faible consiste à intégrer une ou plusieurs couches capacitives directement dans le substrat. La mise en œuvre simple et la limitation du nombre d'interconnexions contribuent à réduire la présence de composants parasites (inductance et résistance) des condensateurs intégrés comparés à ceux montés en surface.
Par conséquent, les condensateurs intégrés tendent à présenter des caractéristiques proches de celles de composants "purs" avec moins de propriétés indésirables qui doivent être prises en compte lors de la phase de conception. Les condensateurs intégrés à faible inductance parasite possèdent des fréquences de résonance propre plus élevées. Ils offrent donc une plus grande gamme de fréquence de fonctionnement que ce qui est possible avec des

condensateurs discrets. Ceci est un facteur particulièrement important dans des applications haute fréquence tels que le découplage et le filtrage RF.

En outre, le principal obstacle à la conception de condensateurs intégrés adaptés pour des applications électroniques réside dans la difficulté d'indentifier les matériaux appropriés et les technologies adéquates parmi la vaste gamme de matériaux diélectriques disponibles et des technologies pour leur intégration. Par conséquent, cette thèse est fortement motivée par le désir de trouver des matériaux et des technologies appropriées pour fabriquer des condensateurs plans, multicouches intégrés directement sur le substrat. Ces condensateurs intégrés sont ensuite démontré avec les fonctions suivantes:

2. Fonction de découplage classique sur le bus DC

Toutes les topologies de convertisseurs de puissance reposent sur l'association de cellules commutation à l'aide de 2 à 2n (deux niveaux à n + 1 niveaux) composants de puissance. Dans la plupart des cas, les cellules de commutation sont reliées à un bus continu-continu. A titre d'exemple, la figure 2 montre une cellule de commutation « de base » à deux niveaux qui peut être réalisée avec à peu près n'importe quel type de semi-conducteur de puissance (seul les MOSFET ou les options IGBT + diode sont considérés ici).

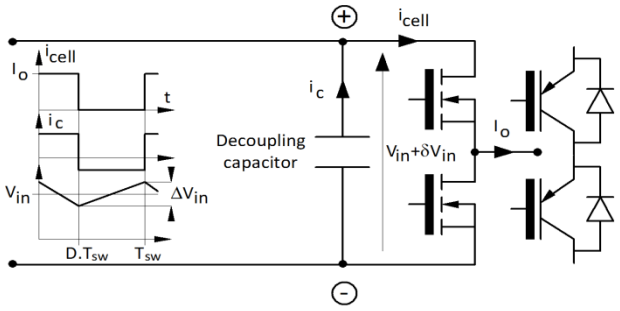


Figure 2: Fonctionnement de condensateur de découplage

Dans tous les cas, la cellule de commutation requiert l'intégration de condensateurs de découplage sur le bus continu, aussi proche que possible des interrupteurs de puissance, afin de minimiser l'inductance de fuite de la boucle de commutation et par conséquent de minimiser la surtension lors du blocage. Ce travail se concentre principalement sur cette fonction de découplage capacitif. Des condensateurs supplémentaires peuvent être introduits sur le bus continu afin de faire partie d'un filtre de mode commun, si nécessaire. Les deux fonctions capacitives, le découplage et le filtrage de mode commun, sont pris en compte dans le démonstrateur final.

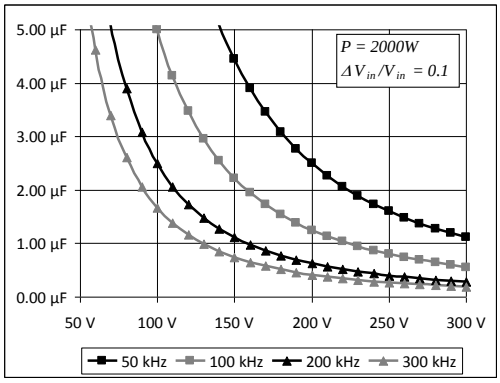


Figure 3 : Détermination de la valeur de la capacité en fonction de la tension du convertisseur pour différentes fréquences de commutation

Le but de ce travail est de mettre en œuvre des substrats capacitifs sur des surfaces relativement importantes (quelques cm²) et d'obtenir des valeurs de capacité spécifique élevées avec un faible nombre de couches en utilisant des matériaux de permittivité élevée. Les problèmes relatifs à l'interconnexion et la gestion thermique ne sont pas considérés ici. Toutefois, il est nécessaire de valider la technologie proposée dans une configuration comprenant des dispositifs de puissance à semi-conducteur: par conséquent, une cellule de commutation simplifiée a été choisie et est présentée dans le chapitre 5 de cette thèse. La cellule en question est définie pour fonctionner avec les caractéristiques suivantes:

$$P = 2000W,\ V_{in} = 200V,\ I_{on} = 10A,\ F_{sw} = 100kHz$$

Ce choix entraîne des valeurs significatives pour le condensateur de découplage: environ 1 à 2 µF pour une ondulation de la tension relative de 10% (voir figure 3). Il semble approprié d'évaluer les limites du concept si les matériaux diélectriques actuels sont utilisés.

3. La fonction de découplage dans un convertisseur à condensateur "flottant"

Les convertisseurs DC-DC de type ‘Point-Of-Load’ (POL) sont utilisés dans une large gamme d'applications, des appareils portables aux applications de l'énergie renouvelable, en passant par les véhicules électriques, et les dispositifs de commande dans l'automobile. Ces applications exigent en permanence une densité de puissance de plus en plus élevée, des convertisseurs de rendement de conversion plus élevés, de taille plus petite, plus léger et à moindre coût. Les technologies d’intégration sont les facteurs clés pour permettre une plus grande efficacité et des niveaux plus élevés d'intégration. Les défis pour l'obtention d'une densité de puissance plus élevée dans l'intégration de convertisseur de POL concernent:

- Le fait que les pertes de commutation augmentent avec les fréquences de commutation élevées.
- Les difficultés d'intégration à la fois des composants semi-conducteurs et des passifs tout en minimisant l’effet de capacité parasite et en gardant un rendement élevé.

Afin de remédier aux problèmes ci-dessus, la seconde topologie est présentée sur la Figure 4 pour démontrer la fonction flottante de condensateurs intégrés.

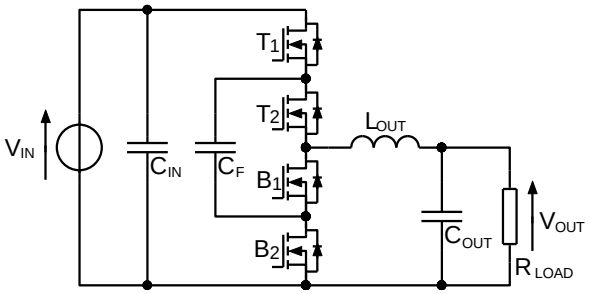


Figure 4: Schéma d'un convertisseur trois niveaux à condensateur flottant.

En général, les condensateurs utilisés dans cette topologie sont montés en surface des composants discrets, ce qui tend à occuper davantage de volume (et entraine un coût élevé pour le convertisseur). Ainsi, il convient d'intégrer les condensateurs d'entrée et C_{IN}, flottant C_F sur un substrat céramique primaire et de les relier par des vias au PCB portant les composants actifs.

L'objectif ici est de démontrer la faisabilité des condensateurs intégrés dans un convertisseur POL utilisant des composants à base de nitrure de gallium avec un refroidissement double face. Des avantages peuvent être obtenus en utilisant un convertisseur à deux cellules au lieu d'un convertisseur à une cellule classique. Le convertisseur abaisseur de tension DC-DC possède une tension d'entrée de 48 V et une tension de sortie de 5 V. En utilisant une topologie à condensateur flottant à deux cellules (FC), la tension appliquée sur l'inductance de sortie est inférieure à celle mesurée aux bornes d'un convertisseur abaisseur de tension d'une cellule classique pour cette même conversion 48V-5V. Ainsi, les contraintes sur les composants actifs sont réduites, et le compromis entre valeur de l'inductance et ondulation de courant est amélioré.

Chapitre II : Sélection de technologie et matériaux

Ce chapitre présente les solutions technologiques actuellement disponibles pour intégrer les composants passifs.

Les défis à relever afin de réaliser des condensateurs intégrés multicouches à forte capacité pour la conversion DC-DC sont :

- d'obtenir une conception flexible avec des performances prédictibles. La forte densité de capacité doit garantir une valeur variant de quelques centaines de nanofarads pour le filtrage à quelques microfarads pour le découplage. Les condensateurs ainsi réalisés doivent posséder un faible courant de fuite, un facteur de qualité élevé, de faibles valeurs d'ESR et d'ESL. Leur tenue en tension doit dépasser 100 V et leur fréquence d'utilisation doit se situer dans la gamme de quelques centaines de kHz.
- d'atteindre une faible épaisseur, une masse faible et un faible coût.
- d'être adapté à une production en grande série et offrir une possibilité de test. Cette dernière est nécessaire pour vérifier la valeur de la capacité, de l'inductance et de la résistance ainsi que pour évaluer la réponse fréquentielle.
- de réduire les défauts au cours du processus de fabrication: augmenter le rendement total de la carte.

- d'être adapté à une fabrication de type planar. Les couches sont d'autant plus minces que la capacité désirée est élevée.
- de minimiser la longueur de connexion afin de réduire l'ESL, l'ESR et d'augmenter la fréquence de résonance (SRF).

Les technologies aujourd'hui disponibles pour l'intégration des composants passifs comprennent la technologie céramique de cofrittage à basse température (LTCC), la technologie des couches minces/épaisses, la haute densité d'interconnexion (HDI) ainsi que d'autres fonctions réalisables sur un circuit imprimé. Les avantages et les inconvénients de chaque technologie sont donnés dans le Tableau 1, dans le cadre de la fabrication d'un substrat pour une capacité plane, intégrée et multicouches utilisée dans une application de conversion DC-DC.

Tableau 1: Comparaison des technologies

	LTCC	HDI	PCB	Couche mince	Couche épaisse (*sérigraphie*)
Réduction de la taille	+	-	-	++	+++
Processus	Complexe	Complexe	Complexe	Complexe	Relativement facile
Tolérance	10%-20%	10%-20%	10%-20%	5-10%	10-20%
Densité Fonctionnelle	++	--	--	++	+++
Fiabilité	-	---	---	--	++
Méthodologie de conception	Complexe	Complexe	Complexe	Complexe	Facile et flexible

La technologie "couche épaisse" associée à la technique de sérigraphie (SPT) semble la meilleure option pour ce travail. Une raison importante est que la technologie SPT est bon marché en plus d'être d'utilisation aisée; elle ne nécessite donc pas de main d'œuvre qualifiée. En outre, il est facile d'imprimer un film diélectrique, conducteur ou résistif de grande épaisseur dans des conditions usuelles tandis que les autres technologies exigent des conditions particulières d'environnement (salle blanche, éclairage,…).

Afin de réaliser des capacités de forte valeur fabricables par sérigraphie, l'encre commerciale 4212C a été choisie. Elle offre une forte permittivité allant de 2000 jusqu'à 12000, une forte rigidité diélectrique, et une faible température de frittage (900°C). Une pâte d'argent (ELS 9160) à forte conductivité et chimiquement stable a été retenue pour les électrodes afin d'éviter des problèmes mécaniques avec les couches de diélectrique durant le procédé de cofrittage. Des substrats de l'alumine (96%) sont utilisés en raison de leur grande stabilité thermique et la qualité (faible rugosité) de leur surface.

Pour limiter les défauts dans les couches diélectriques tout en augmentant la tenue en tension et en réduisant le facteur de pertes, un procédé optimisé est proposé (voir Figure 5). Deux couches diélectriques sont imprimées pour chaque couche de la capacité. La première est imprimée, séchée et cuite alors que la seconde est imprimée, séchée, et ensuite cofrittée avec la seconde électrode. Ceci permet d'éviter des problèmes de court-circuit et augmente le taux de réussite du procédé. Nous avons utilisé ce procédé pour fabriquer avec succès un grand nombre d'échantillons présentant un nombre différent de couches.

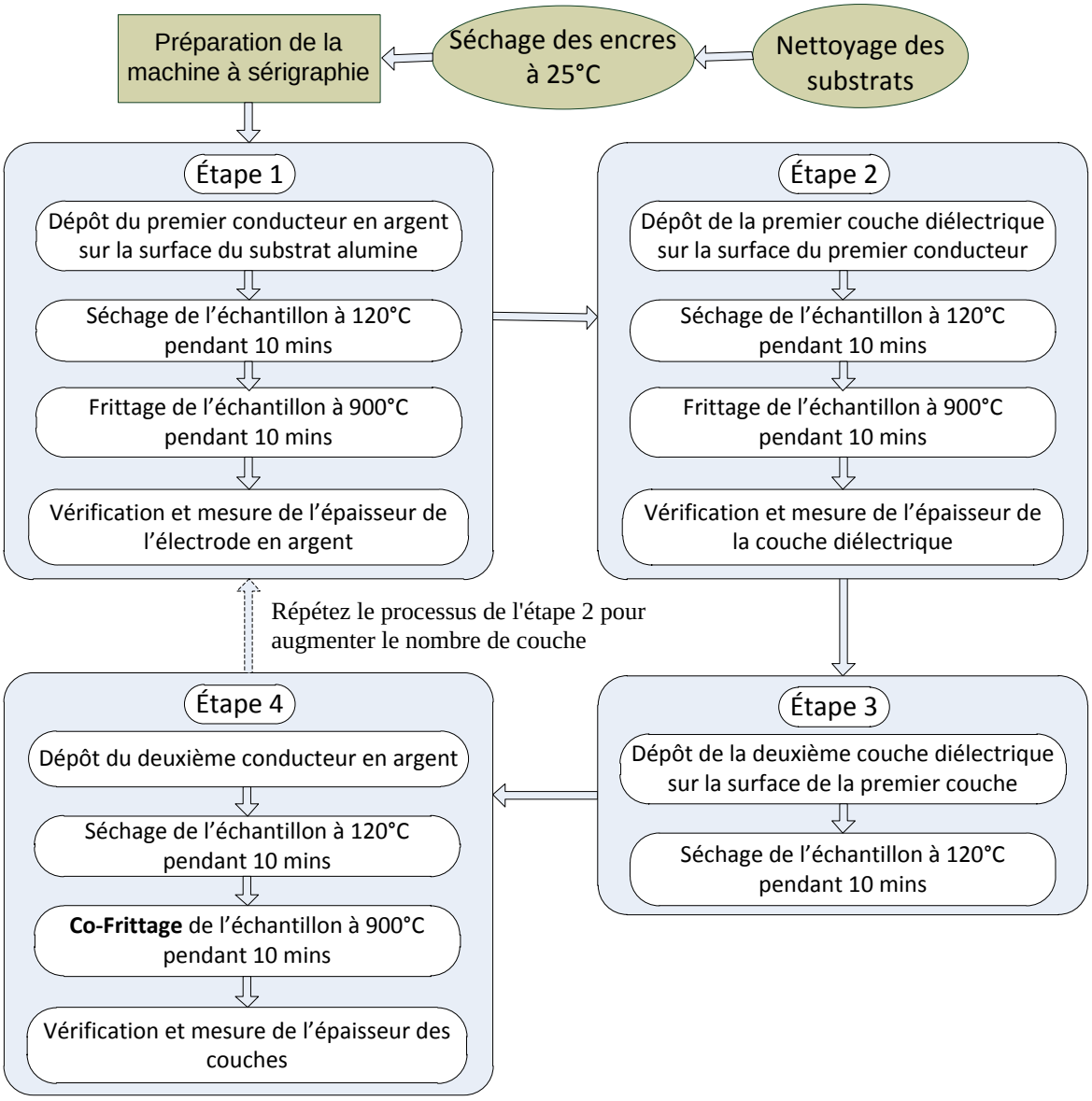


Figure 5 : Résumé du procédé suivi pour fabriquer des condensateurs intégrés.

Chapitre III : Analyse et caractérisation de condensateurs intégrés

I. Méthodes de mesures

Dans ce chapitre, les méthodes d'analyse physico-chimique et de caractérisation électrique sont sélectionnées et décrites. Les images (les vues en coupe, la microstructure) et les compositions chimiques des matériaux conducteurs et diélectriques sont observées et analysées en utilisant un microscope électronique à balayage (MEB) ou un microscope électronique en transmission (MET). L'analyseur d'impédance de HP4191A (40 Hz-110MHz) est utilisé pour caractériser les principaux paramètres des condensateurs tels que la capacité, l'impédance, l'inductance série équivalente (ESL), la résistance série équivalente (ESR), la fréquence de résonnance propre (SRF), tandis qu'une station sous pointe (Signatone) reliée à une unité KEITHLEY 2410 a été utilisée pour mesurer le courant de fuite et la tension de

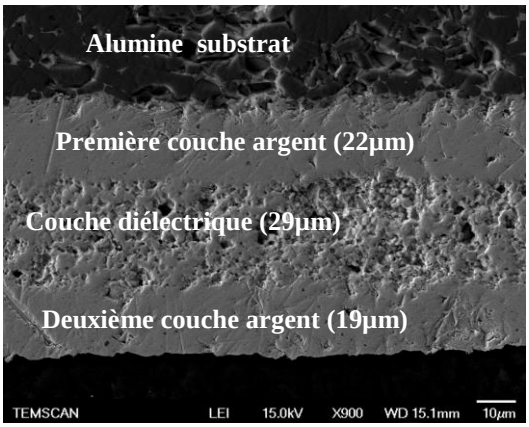
claquage du condensateur. La dépendance des caractéristiques du condensateur en fonction de sa température est obtenue en mettant la cellule de mesure dans une chambre de test de température (Heraeus HT 7010) reliée directement à un analyseur d'impédance HP 4284A (20Hz-1MHz). La dépendance en fonction de la tension de polarisation est également caractérisée à l'aide du même équipement.

II. Résultats et discussions

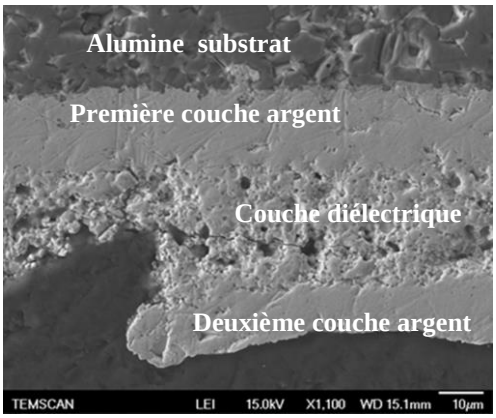
1. Analyse physico-chimique

Les condensateurs MIM

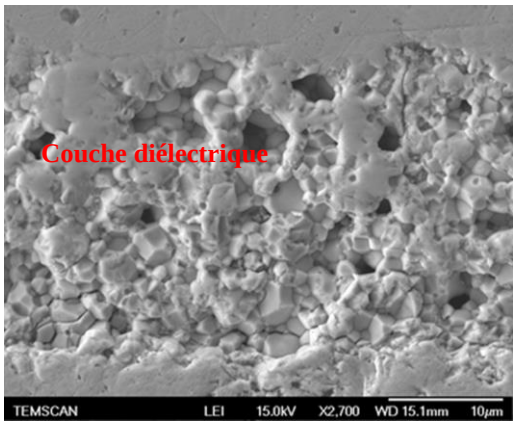
La microstructure du condensateur Metal Isolant Metal (MIM) est représentée dans les figures 6(a) et (b). L'épaisseur varie entre 15-25µm et 25-35µm pour les électrodes en argent et la couche diélectrique, respectivement. La morphologie des grains de la couche diélectrique visible à la figure 6(c) montre l'uniformité des deux couches diélectriques sans délamination, même si elles sont fabriquées de manière différente. L'absence de diffusion entre la deuxième couche diélectrique et la couche d'argent de l'électrode supérieure est également visible bien qu'elles soient cofrittées. Ceci peut éliminer le risque de rupture prématurée du condensateur lors de son utilisation.



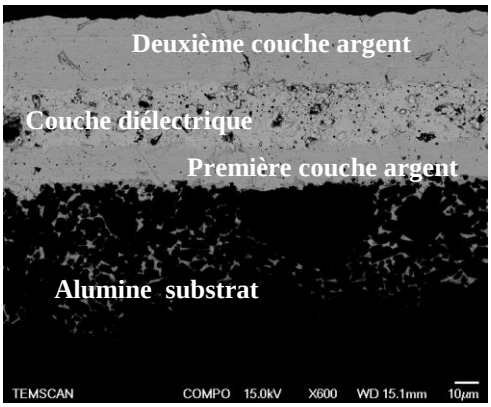
a) Microstructure de condensateur MIM.



b) Interface de la seconde électrode en argent.



c) Morphologie des particules de la couche diélectrique.



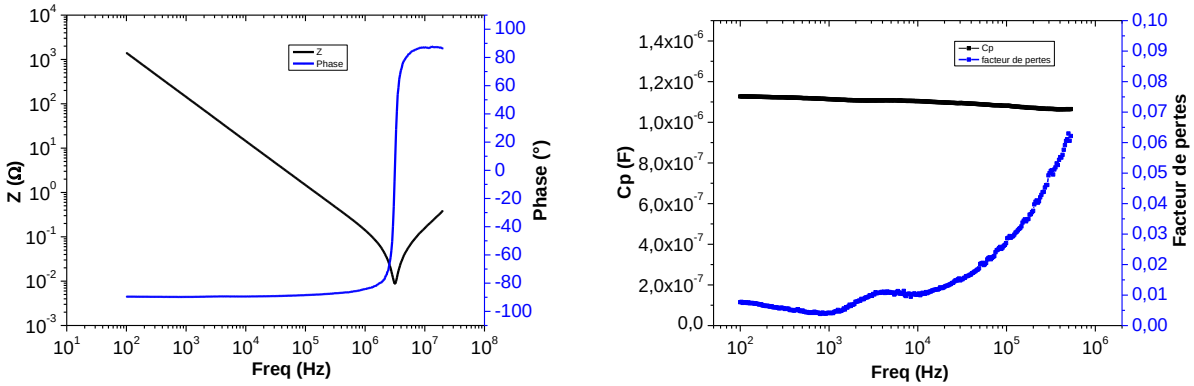
d) Diffusion dans le substrat d'alumine.

Figure 6: Observation MET des condensateurs MIM.

2. Caractéristiques électriques

a. Réponses en fréquence

La réponse en fréquence des condensateurs MIM est donnée dans la figure 7(a) montrent que, pour une fréquence inférieure à la fréquence de résonance propre (SRF environ 1MHz), l'impédance est inversement proportionnelle à la fréquence. Au point de SRF, l'ESR peut être déterminée. Pour une fréquence supérieure à SRF, le comportement du condensateur devient selfique. Le condensateur MIM S_{M2}, avec une surface utile de 33mmx19mm, présente une densité de capacité élevée (1.9nF/mm^2 pour une épaisseur diélectrique de 30µm) et un facteur de pertes faible, comme le montre la figure 7(b).

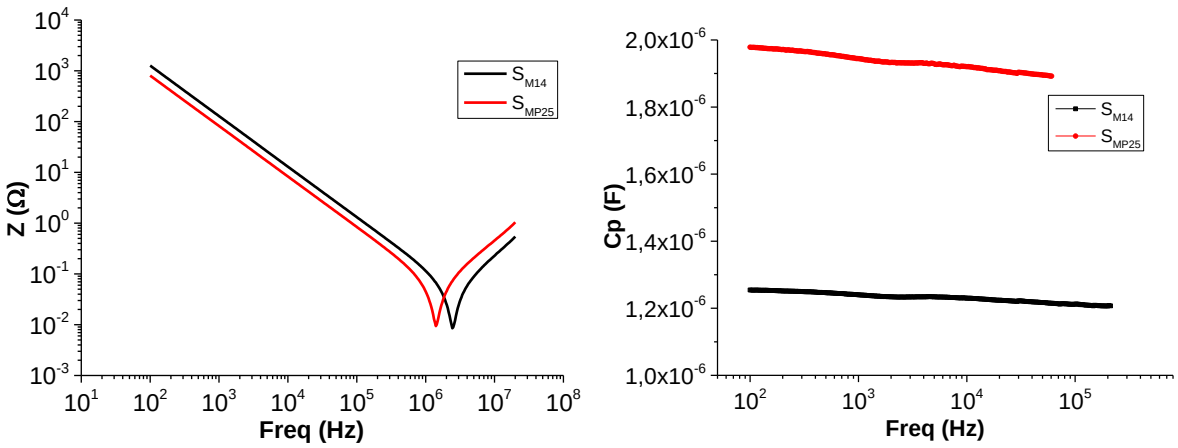


(a) (b)

Figure 7: Réponses en fréquence du condensateur MIM : a) variation de l'impédance et de la phase. b) Variation de de la capacité et du facteur de perte.

b. Les condensateurs interdigités

Des couches capacitives empilées et interconnectées alternativement permettent de créer une structure multicouche et d'augmenter la valeur du condensateur MIM. La comparaison de l'impédance d'un condensateur MIM S_{M14} et d'un condensateur multicouche S_{M25} (Figure 8) démontre que la qualité des interconnexions entre les électrodes permet de réaliser un condensateur multicouche, et que l'utilisation de couches interdigitées permet d'augmenter la valeur du condensateur.



(a) (b)

Figure 8: Comparaison de la réponse en fréquence entre le condensateur MIM et le condensateur interdigité.

c. Le courant de fuite

Cette partie est consacrée à la mesure du courant de fuite des condensateurs intégrés. Une bonne résistance d'isolement (rapport de la tension aux bornes du condensateur et du courant le parcourant (R = V/I_L)) est nécessaire afin de limiter l'autodécharge des condensateurs et donc de garantir un niveau de tension relativement invariant lorsqu'ils ne sont pas sollicités (ou un niveau d'énergie quasi-constant lorsqu'ils sont utilisés pour stocker de l'énergie électromagnétique).

Dans le cas le plus simple, le courant de fuite I_L d'un condensateur dépend de la tension appliquée à ses bornes. La courbe présentée sur la figure 9 montre les variations du courant de fuite pendant les 200 premières secondes après l'application de la tension. L'ordre de grandeur de ce courant est la dizaine de nano Ampère en régime permanent qui intervient relativement rapidement. Le rapport du courant de fuite et de la tension aux bornes du condensateur correspondant au précédent graphe montre une valeur d'isolement élevée (de l'ordre du GΩ).

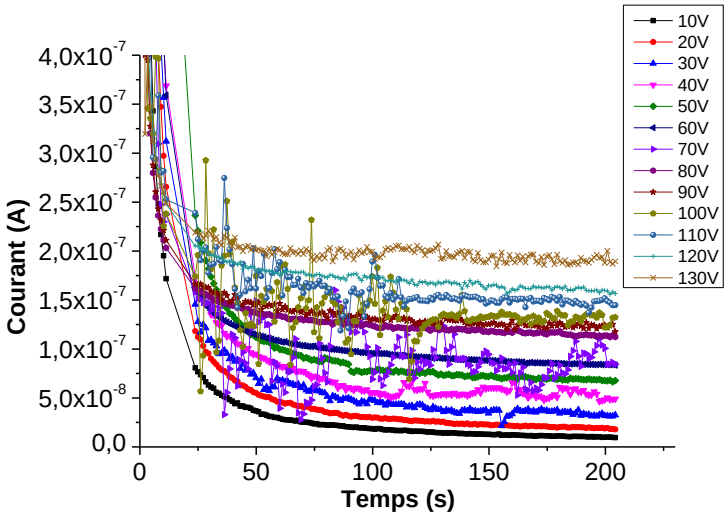


Figure 9: Exemple de détermination du courant de fuite dans un condensateur

d. Mesure de la tension de tenue et de claquage

Il s'agit ici d'étudier la tension que peut supporter le condensateur. Les tests de tenue en tension ont été réalisés sur deux condensateurs MIM S_{M1} et S_{M2} à température ambiante, et plongés dans un liquide diélectrique FC72 afin de s'affranchir des paramètres environnementaux. Les résultats montrent que la tension de claquage des condensateurs intégrés peut atteindre dans cette géométrie plus de 300.

e. Dépendance des caractéristiques avec la température

La stabilité thermique est un des facteurs clé des condensateurs. Ainsi, les propriétés diélectriques des condensateurs MIM ont été mesurées en fonction de la température, comme le montre la figure 10. Etant donné la nature du diélectrique, et comme il était attendu, la valeur du condensateur a tendance à augmenter à la température de Curie – point auquel la valeur du condensateur est maximale ce qui est causé par la transition de phase – qui correspond approximativement à la température ambiante, 23°C. Ces variations des caractéristiques avec la température nous conduisent à penser qu'une utilisation dans des environnements particulièrement chauds pourrait s'avérer délicate. En revanche, il est à noter que les pertes sont faibles sur les plages de températures et de fréquences étudiés ici.

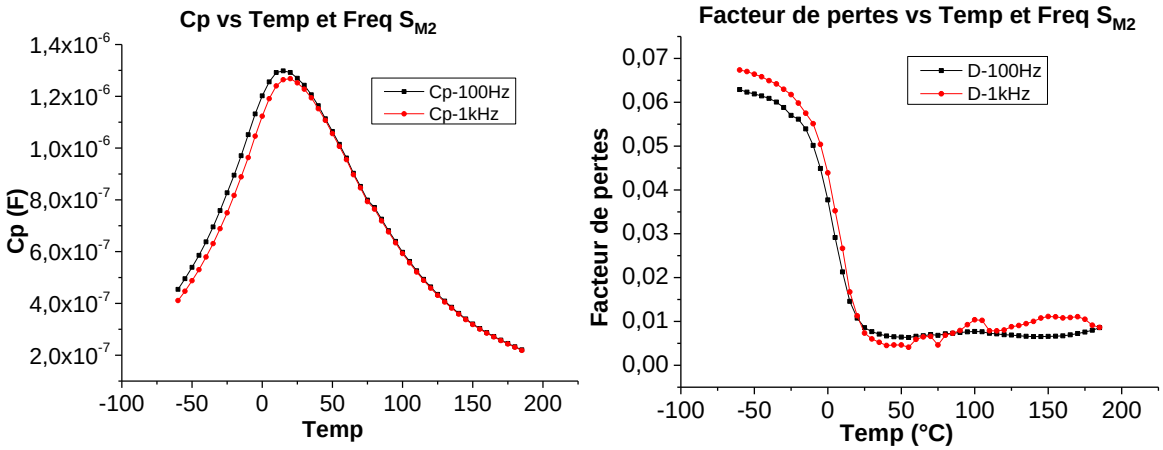
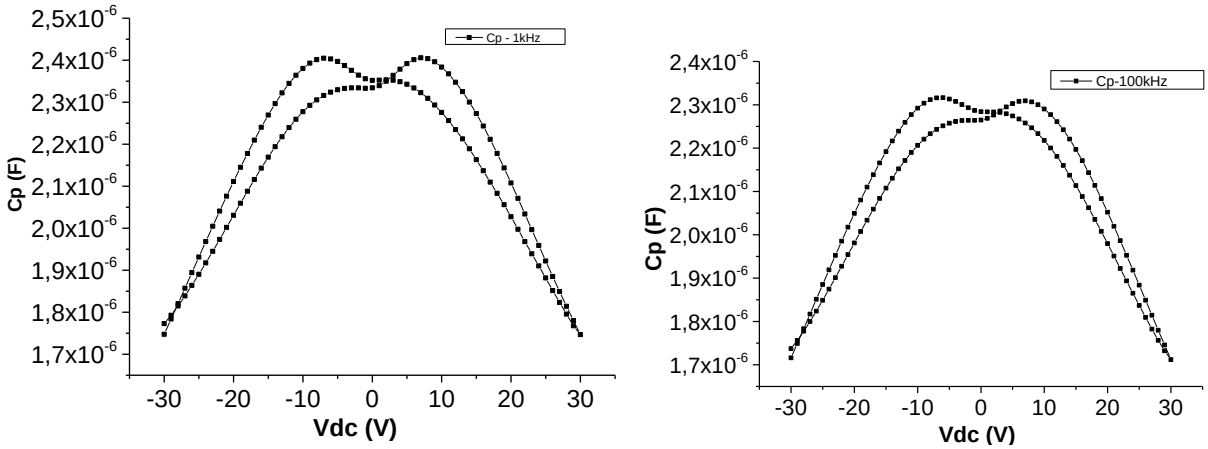


Figure 10: Influence de la température sur les caractéristiques de condensateurs MIM à 100 Hz et 1 kHz.

f. Dépendance des paramètres avec la tension de polarisation

Les résultats des mesures à température ambiante, figure 11, montrent l'évolution typique de la valeur des condensateurs intégrés ferroélectriques avec une tension de polarisation VDC entre -30 et +30 V. La valeur diminue significativement lorsque la tension de polarisation augmente. Ce comportement est relié à la nature ferroélectrique du matériau et peut être considéré comme limitant pour une utilisation en électronique de puissance.



(a) (b)

Figure 11: DC dépendance de polarisation de condensateurs intégrés (a) 1 kHz, et (b) 100 kHz

Chapitre IV: Impact du pressage isostatique à froid (CIP) sur des couches épaisses ferroélectriques

Les concepteurs ont tendance à utiliser des condensateurs à forte capacité pour obtenir un meilleur découplage et un filtrage plus efficace. Par conséquent, afin d'augmenter la capacité d'un condensateur intégré, des matériaux de permittivité diélectrique plus élevée doivent être utilisés et les surfaces des électrodes doivent être augmentées. Ce chapitre présente une méthode alternative simple pour obtenir une capacité élevée en réduisant en plus l'épaisseur de la couche diélectrique grâce au pressage isostatique à froid (CIP). L'étude porte sur l'impact de différents traitements CIP sur l'épaisseur de la couche ferroélectrique des condensateurs sérigraphiés.

I. Procédures de CIP proposées

Procédés étudiés

Le procédé sans prétraitement CIP réalisé dans le chapitre 2 est noté P1. Nous avons proposé trois autres procédés P2; P3; P4 utilisant différents prétraitements CIP. Ces processus sont résumés dans le tableau 2.

Tableau 2 : Étapes de préparation des échantillons pour la fabrication de condensateurs MIM Ag : Argent ; CD : couche diélectrique ; D= dépôt; S=séchage; F= frittage ; CIP : pressage isostatique à froid

Nome	Couche	Processus	La durée (jour)	Note
P1	1ère Ag	D/S/F	1	Pas de CIP
	1ère CD	D/S/F	1	
	2ème CD	D/S	1	
	2ème Ag	D/S/CF		
P2	1ère Ag	D/S/F	1	CIP appliqué uniquement sur la 1er CD
	1ère CD	D/S/CIP/F	1	
	2ème CD	D/S	1	
	2ème Ag	D/S/F		
P3	1ère Ag	D/S/F	1	CIP appliqué au 1er CD puis CIP appliqué sur les 2ème CD et 2ème Ag
	1ère CD	D/S/CIP/F	1	
	2ème CD	D/S	1	
	2ème Ag	D/S/C-CIP/CF		
P4	1ère Ag	D/S/F	1	CIP appliqué sur la 1ère CD et 2ème CD, séparément
	1ère CD	D/S/ CIP/F	1	
	2ème CD	D/S/CIP/F	1	
	2ème Ag	D/S/F	1	

Traitement CIP

L'étude a porté sur des condensateurs MIM utilisant la configuration dans laquelle le diélectrique est pris en sandwich entre deux couches d'argent. Une fois que la couche diélectrique sérigraphiée est séchée, les échantillons sont emballés dans un sac en plastique présentant une excellente ténacité. Le sac a été scellé à l'aspirateur et emballé hermétiquement à l'aide d'un appareil à vide, comme représenté sur la figure 12(b), (c). Le sac en plastique est ensuite totalement immergé dans le liquide de la presse isostatique à froid. Pour former une couche densifiée à faible porosité et à rugosité de surface réduite sur la couche diélectrique, la pression a été appliquée dans la gamme de 600-3000 bars, et maintenue pendant 5 minutes, comme le montre la figure 12(d). Après le prétraitement CIP, le sac en plastique est retiré et les échantillons sont frittés à 900°C pendant 10 minutes.

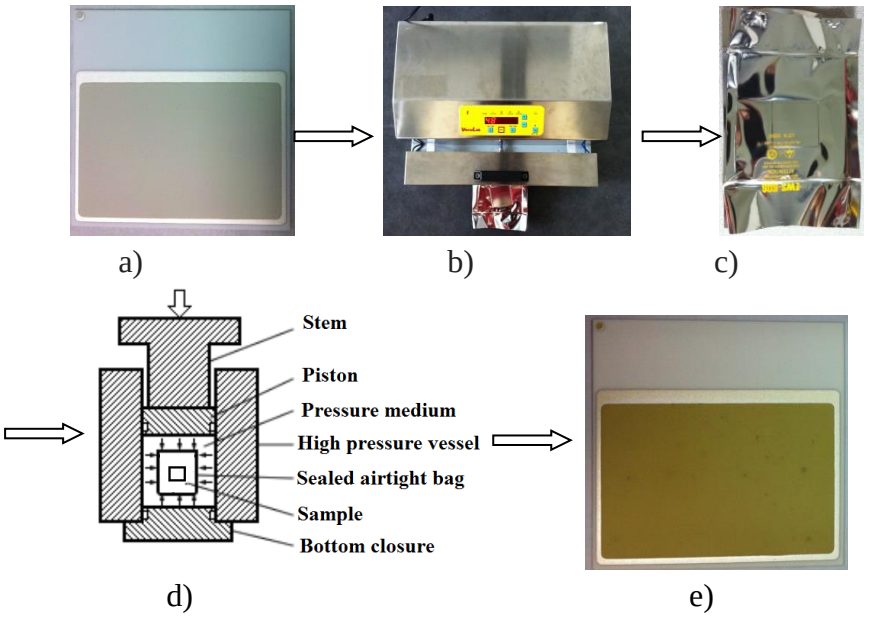


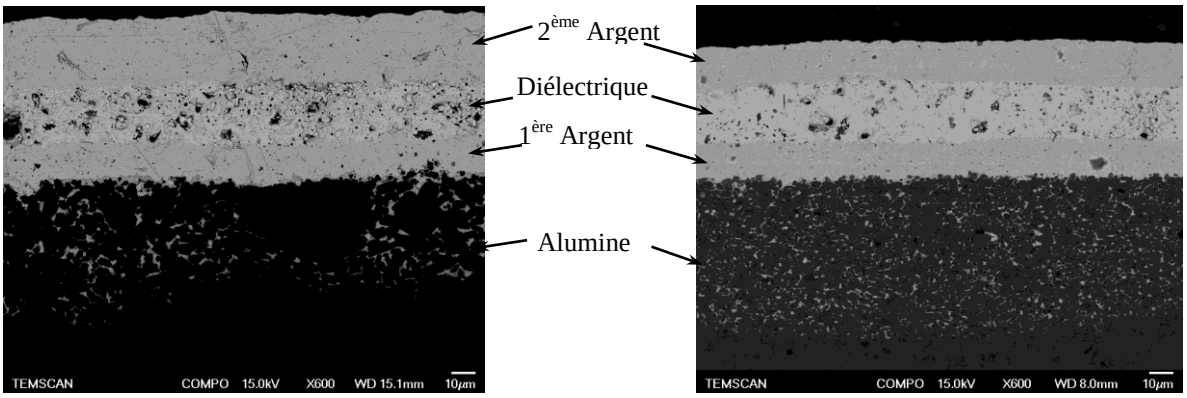
Figure 12: Traitement du pressage isostatique à froid: (a) une couche diélectrique, après séchage, b) la machine à emballer sous vide, c) échantillon emballé dans un sac en plastique scellé sous vide, d) un sac de plastique immergé dans la cuve de pression, e) la couche diélectrique après traitement CIP et frittage.

II. Résultats et discussions

1. Analyse physico-chimique

Microstructure des grains

Cette section se focalise sur la vérification de l'impact du traitement CIP sur la microstructure des grains de la couche ferroélectrique. Certains échantillons (S1P1 sans CIP, et S4P2, S4P3, S4P4 avec la CIP à 3000 bar) ont été découpés en éléments individuels à l'aide d'une machine de découpe de précision (Struers Secotom 10). Ensuite, ils ont été encapsulés dans une résine époxyde et polis en vue de l'observation de leur microstructure par microscope électronique à transmission (MET). La vue en coupe de la morphologie de la figure 13 et les résultats de mesure de l'épaisseur diélectrique donnés dans le tableau 4, montrent une réduction de l'épaisseur de la couche diélectrique ainsi que la variation d'épaisseur de la couche après traitement CIP.



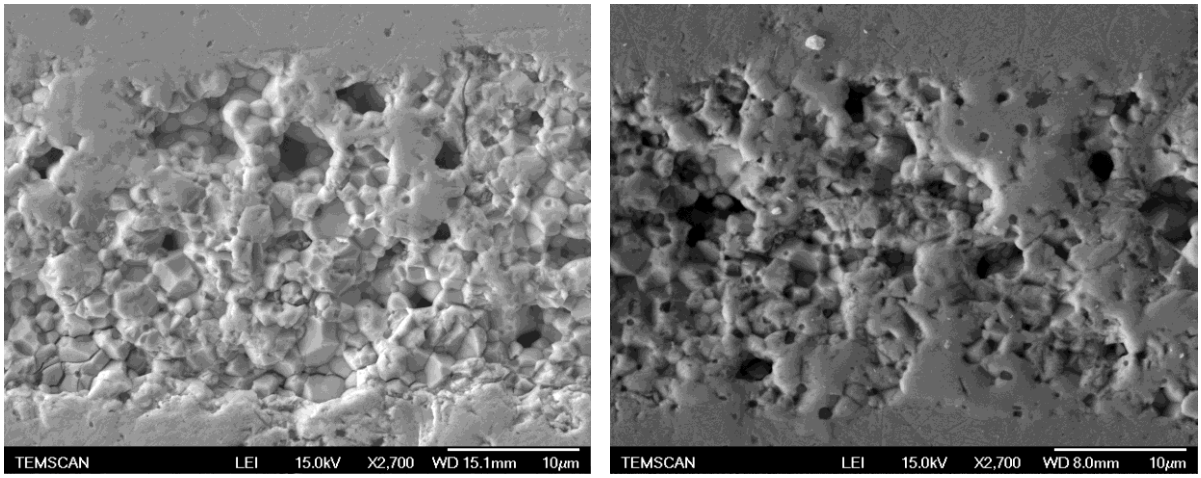
(a) (b)

Figure 13: Vue en coupe de (a) l'échantillon S1P1 sans CIP et (b) l'échantillon S4P4 avec la CIP.

Tableau 4: Epaisseur des échantillons mesurés par TEM.

Nom d'échantillons	Pression (bars)	Point 1 (μm)	Point 2 (μm)	Point 3 (μm)	Epaisseur moyenne, d (μm)
S1P1	0	35	36	35	35
S4P2	3000	21	22	21	20
S4P3	3000	14	15	14	14
S4P4	3000	14	14	15	14

Les images MET de la figure 14 montrent que la morphologie des grains de l'échantillon avec ou sans CIP ne change pas de façon significative bien que les deux couches diélectriques soient fabriquées de manière différente. La structure globale peut être considérée comme uniforme, ce qui diminue les risques de claquage prématuré.



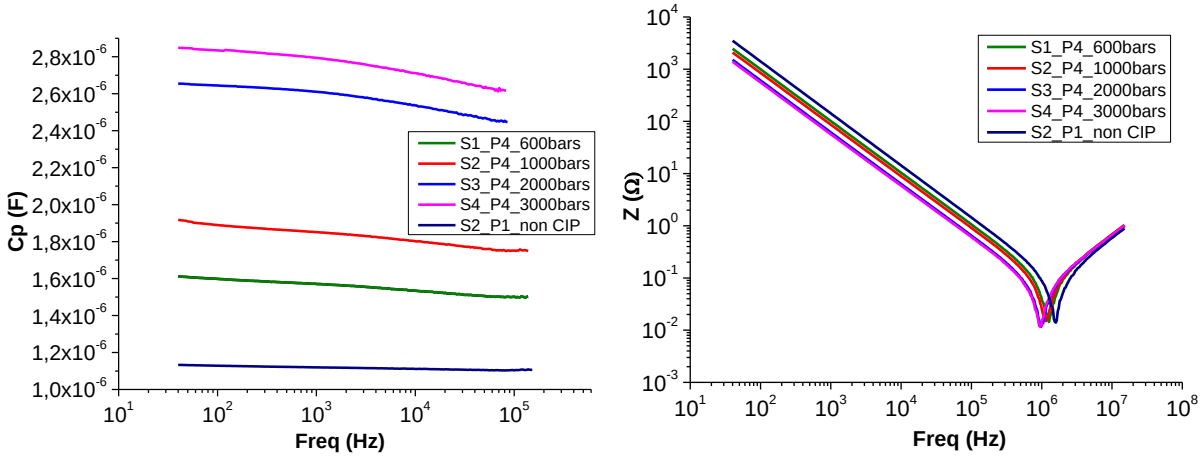
(a) (b)

Figure 14: Images TEM d'échantillons sans CIP (a) et avec CIP (b).

2. Performances électriques

a. Impédance fonction de la fréquence

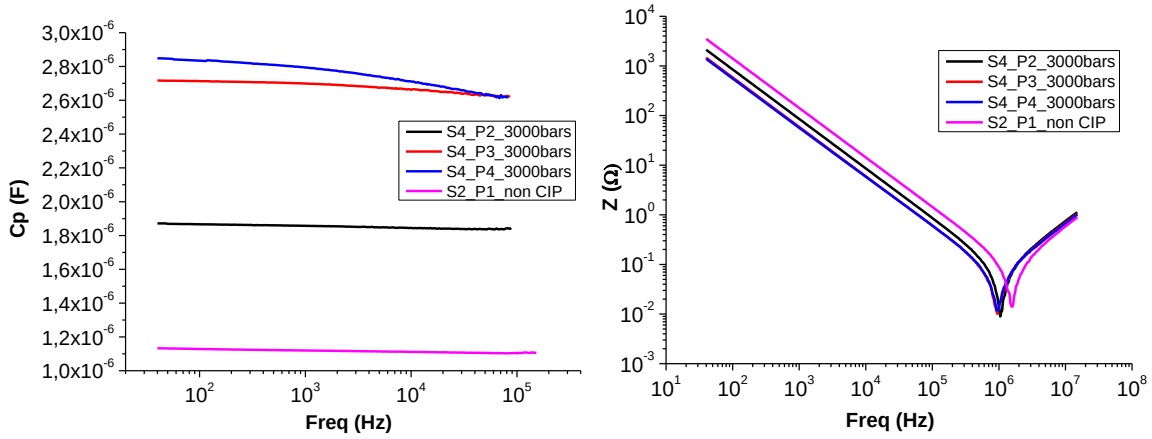
La figure 15 présente les variations relatives de la capacité et de l'impédance en fonction de la fréquence et de l'amplitude de la pression pour des échantillons fabriqués par le même procédé, comparées à celles de l'échantillon sans CIP. La capacité augmente proportionnellement à la pression appliquée à la couche diélectrique. Les échantillons sont capacitifs dans la gamme de fréquences de 100 Hz à 900kHz, une SRF de l'ordre de 1 MHz est déterminée, tandis qu'un comportement inductif domine aux fréquences plus élevées.



(a) (b)

Figure 15: Evolution de la capacité (a) et de l'impédance (b) de l'échantillon sans CIP S2P1 et des échantillons avec des niveaux de pression différents de CIP mais pour un procédé de fabrication identique.

Comme le montre la figure 16, obtenu pour un même niveau de pression, les échantillons élaborés par les différents procédés présentent toujours une densité de capacité plus élevée par rapport à l'échantillon sans CIP. On peut noter clairement que les procédés P3 et P4 permettent d'atteindre des valeurs de capacité plus importantes que le procédé P2 car les deux couches diélectriques des procédés P3 et P4 ont subi des traitements CIP alors que seule la première couche diélectrique du procédé P2 a fait l'objet d'un traitement CIP. Cela souligne une fois de plus l'effet de la réduction de l'épaisseur induit par le prétraitement CIP de la couche épaisse ferroélectrique.



(a) (b)

Figure 16: Comportements de la valeur du condensateur (a) et de l'impédance de l'échantillon sans CIP (b) et des échantillons pour une même pression dans les différents procédés.

b. Influence de la température

La figure 17 montre que les transitions de phase ne varient pas de manière considérable dans les échantillons sans CIP et les échantillons ayant le même niveau CIP mais obtenus suivant différents procédés. La température de Curie semble également proche de la température ambiante. Les pertes diélectriques sont affectées par plusieurs facteurs tels que la fréquence et la température extérieure, la structure interne et les défauts du réseau (joints de grains, vacuoles, et défauts)

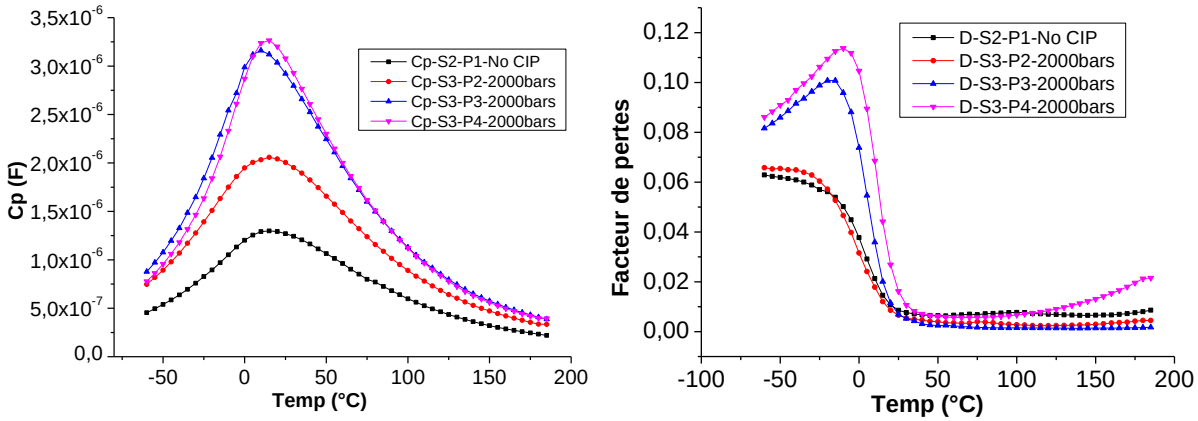


Figure 17: Variation de la capacité et des pertes en fonction de la température pour des condensateurs sans CIP et pour des valeurs de pressions identiques lors du CIP mais obtenus suivant différents procédés.

En résumé, les différentes propriétés du matériau de l'étude répondent aux besoins de l'électronique de puissance. Ces propriétés peuvent être prises en compte lors de la conception des condensateurs pour des applications de puissance. En conséquence, le procédé CIP se révèle être une technologie intéressante pour former des condensateurs intégrés

relativement minces et de plus fortes valeurs de capacité, offrant des options flexibles pour les concepteurs en électronique de puissance.

Chapitre V : Application en électronique de puissance

Ce chapitre propose deux topologies différentes utilisant des condensateurs de découplage intégrés. Les condensateurs intégrés sont directement sérigraphiés sur le substrat en alumine. Le dessin des écrans est conçu pour être adapté à la valeur de la capacité requise. Les substrats planaires capacitifs sont fabriqués en utilisant la technique de sérigraphie, les propriétés électriques sont caractérisées. Les résultats des condensateurs intégrés en fonctionnement sont analysés et discutés.

I. Fonction de découplage classique sur le bus DC

L'objectif de cette approche technologique est d'intégrer des fonctions capacitives très proches des dispositifs semi-conducteurs de puissance. Les masques d'écran spécifiquement développés dans le cadre de ce travail sont présentés sur la figure 17. Les deux condensateurs de filtrage et le condensateur de découplage sont conçus avec des dimensions de 5x7mm^2 - et de 19x19mm^2, respectivement. Tous les condensateurs possèdent la même couche diélectrique avec une surface de 33x22mm^2. Les masques d'écran sont réalisés en acier inoxydable, d'une taille de 40x40cm^2. Les paramètres des écrans pour la pâte diélectrique et le conducteur, présentés dans le tableau 5, ont été établis sur la base des recommandations du fabricant.

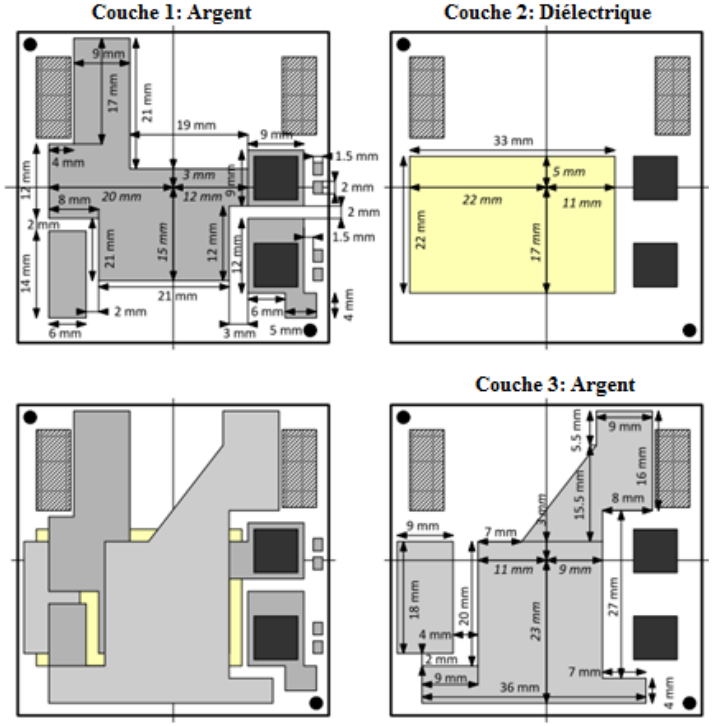


Figure 17: dessins de masques d'écran

Tableau 5: Paramètres des écrans.

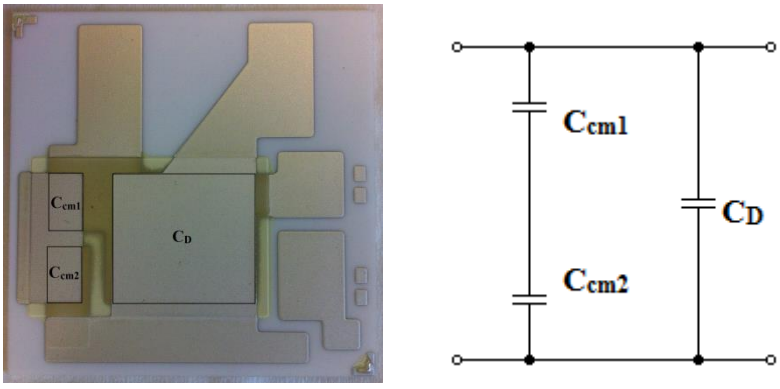
	Masque du diélectrique	Masque du conducteur
Matériau	Inox	inox
Ecran maillé, toile	200	325
Emulsion	37.5µm	25 µm
Vide de maille	90µm	50 µm
Diamètre du fil	40µm	30 µm
Toile	45°	45°

1. Réalisation et caractérisation

Utilisation du procédé P1 décrit dans le chapitre 2 (figure 5), les trois premières couches du condensateur ont été mises en œuvre avec succès.

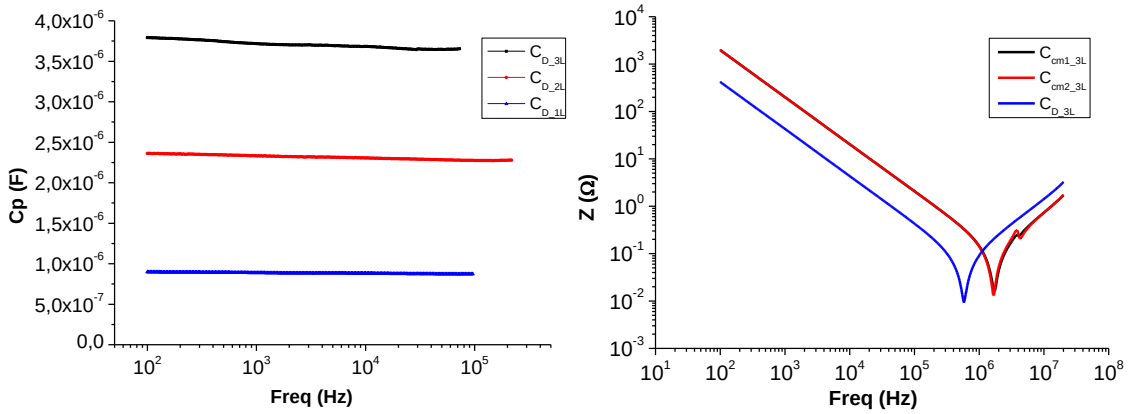
Analyseur d'impédance

Les condensateurs ont été repérés comme le montre la figure 18, avec deux condensateurs C_{cm1} et C_{cm2} de valeur faible pour le filtrage, et un condensateur de plus grande capacité C_D pour le découplage. La figure 19(a) montre l'augmentation de la valeur du condensateur de découplage (mesurée sous faible tension) avec le nombre de couches, à savoir 0,97µF, 2,48µF ; 3,6µF pour une couche, deux couches, trois couches, respectivement. Le comportement de l'impédance capacitive du substrat à 3 couches, représentées sur la figure 19(b), montre que les fréquences de fonctionnement effectif se situent entre 100 Hz et 1 MHz.



(a) (b)

Figure 18: (a) Repérage des condensateurs sur le substrat ; (b) circuit équivalent



(a) (b)

Figure 19: (a) Augmentation de la valeur du condensateur en fonction du nombre de couches, (b) comportement de l'impédance du substrat capacitif à 3-couches.

2. Résultats

Montage expérimental

Les deux dispositifs nécessaires pour réaliser la cellule la plus élémentaire (convertisseur abaisseur, voir montage expérimental figure 20), un MOSFET et une diode, ont été choisis dans la gamme 200V, conformément à l'objectif initial et dans une gamme de courant surdimensionnée afin d'éviter des problèmes expérimentaux supplémentaires.

Ces dispositifs sont les suivants:

- Un MOSFET STD20NF20 (200V ; 0,12Ω ; 20A)
- Une diode Schottky MBRB20200CT (200V ; 20A)

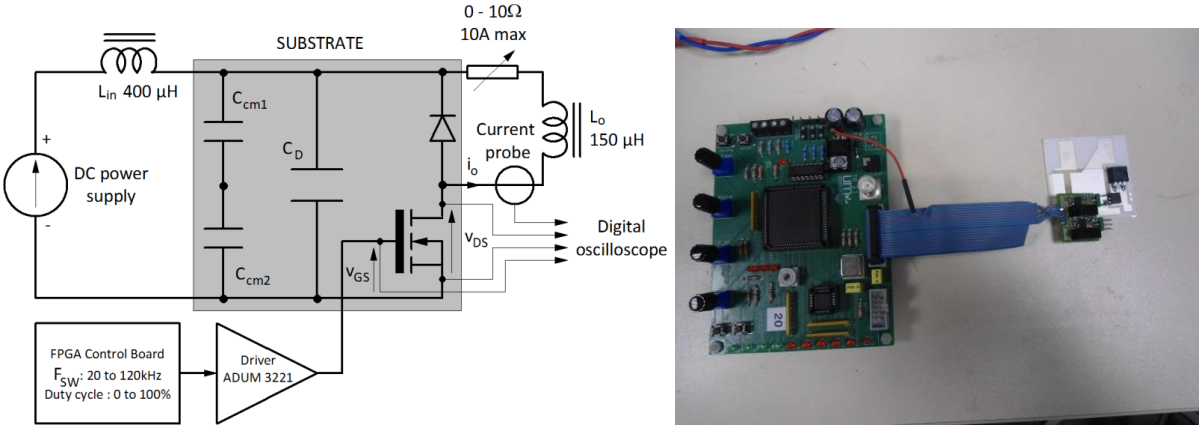


Figure 20: Représentation du dispositif expérimental

Résultats

La figure 21 montre les formes d'ondes électriques obtenues avec un substrat capacitif à trois couches. Ces formes d'onde sont similaires pour tous les échantillons. Celles-ci démontrent la bonne qualité du découplage, l'inductance parasite de la cellule complète est estimée à environ 15 à 20 nH. Cependant, celles-ci mettent également en évidence la diminution de la valeur de la capacité avec la valeur de la tension DC: dans le cas présent, la

valeur du condensateur sous 100 V, mesurée à partir de l'ondulation de tension, est de 650 nF, sa valeur initiale étant 2,94 µF.

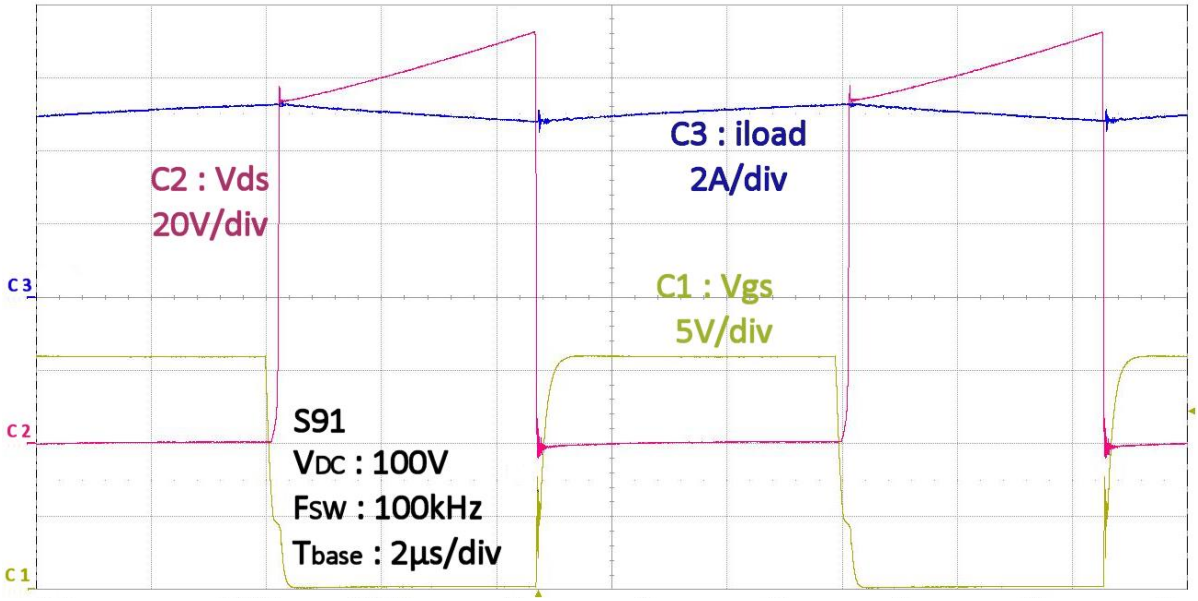


Figure 21: Formes d'ondes obtenues expérimentalement

II. Fonction de découplage dans un convertisseur à condensateur flottant

Les différents éléments constituant le convertisseur sont présentés à la figure 22. La couche active est un circuit imprime deux couches. La première couche accueille les transistors GaN, les drivers ainsi que le filtre de sortie. La seconde couche est un plan de masse qui a pour vocation de réduire les inductances parasites des boucles latérales de puissance, qui engendrent notamment des pertes supplémentaires et des surtensions.

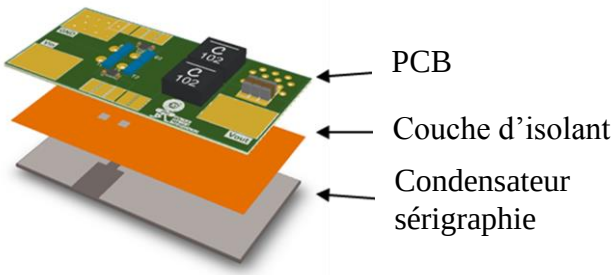


Figure 22 : Constitution de l'assemblage 3D du convertisseur (substrat capacitif, couche isolante, PCB double couche).

1. Réalisation de la couche capacitive

Conception du masque

Les condensateurs intégrés sont réalisés sur un substrat Al_2O_3 d'épaisseur 0,635mm et de dimension 25,4x50,8mm^2. Le substrat présente deux condensateurs distincts. Le plus faible est le condensateur d'entrée (12,57x24,4 mm^2), alors que la plus grande (29,48x 24,4mm^2) est à la fonction flottante du convertisseur. Le dessin du masque utilisé pour la fabrication des

condensateurs multicouches ferroélectrique intégrés est représenté sur la figure 23. Les condensateurs sont fabriqués à partir d'un diélectrique ferroélectrique commercial (ESL 4212C) pris en sandwich entre deux couches d'argent sur un substrat Al_2O_3 selon le procédé P1 (figure 5).

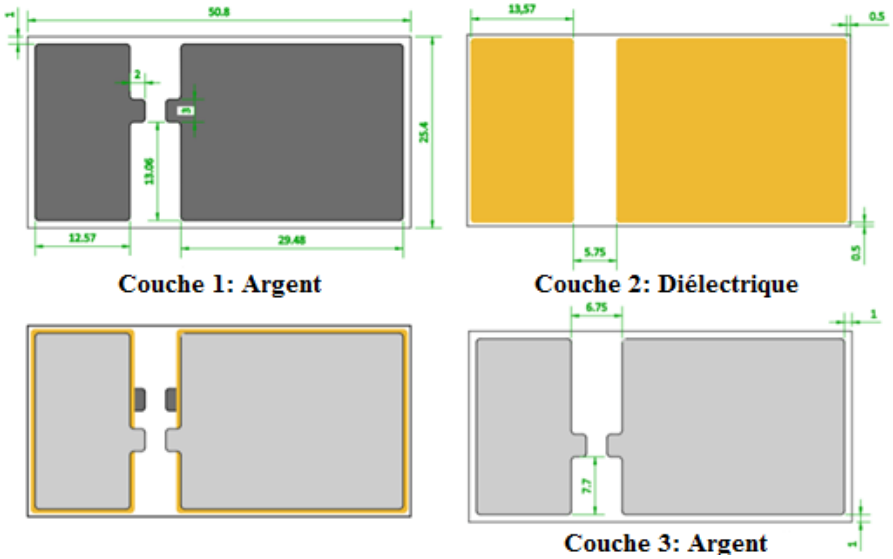
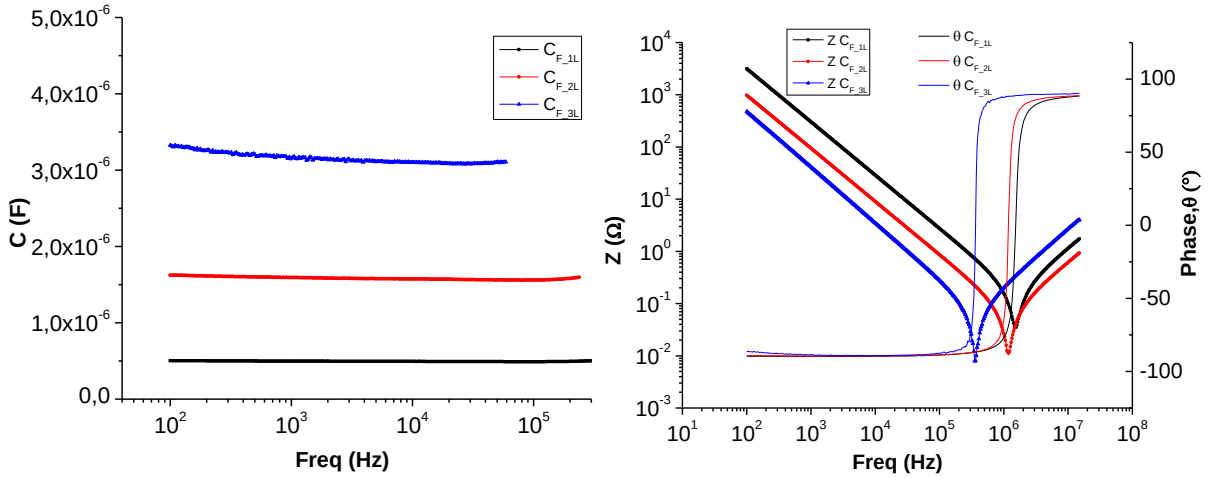


Figure 23: Dessin du masque pour le substrat capacitif flottant.

Caractérisation

Les condensateurs flottant et d'entrée sont caractérisés électriquement. La figure 24 présente les résultats obtenus pour un nombre de couche variable, à faible tension. Il en résulte un lien entre la valeur du condensateur et sa fréquence de résonance propre qui avoisine les 1MHz : plus le condensateur est à surface effective importante, et plus faible est la fréquence de résonance propre.



(a) (b)

Figure 24: Changement de comportement de la capacité (a) et de de l'impédance (b) d'un condensateur flottant en fonction de le nombre de couches.

2. Prototype

La connexion des condensateurs sérigraphiés avec le PCB est faite grâce à des vias. Une couche d'isolant électrique est utilisée pour prévenir du court-circuit entre le plan de masse du PCB et l'électrode du condensateur. Cette isolation est effectuée grâce à un film polymide Pyralux®FR200. L'assemblage consiste en une lamination: l'ensemble est maintenu sous une pression de 20 bars à une température de 200°C pendant deux heures. Cette couche d'isolation de 50,8µm possède une rigidité diélectrique élevée (118kV/mm) et une résistance thermique de 0,2K/W. Sur la figure 25, le condensateur de filtrage est visible. Son rôle est de stabiliser la tension d'entrée. Son rôle est donc tout à fait différent du condensateur sérigraphie C_{IN} qui est un condensateur de découplage, situé au plus proche de la cellule de commutation. Le condensateur de filtrage peut être, quand à lui, éloigné de la cellule de commutation, ne compromettant ainsi pas une perspective de refroidissement double face.

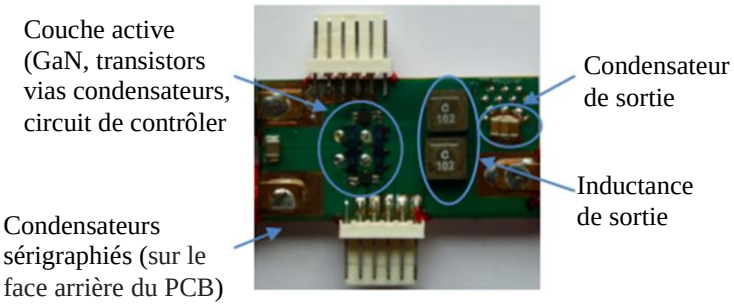


Figure 25 : Ensemble complet du convertisseur

3. Résultats expérimentaux

Le prototype utilise deux condensateurs sérigraphiés double couches ayant pour valeur 0,9µF (entrée) et 2,2µF (flottant). Le convertisseur est composé de quatre transistors 40V en nitrure de gallium GaN (EPC2015) avec 4mΩ de résistance à l'état passant. Le convertisseur est un 48V-5V et a été testé jusqu'à 10A en convection forcée et avec une température maximale de 50°C sur les eGaN FETs (ambiante à 20°C). Le temps mort est de 20ns et les signaux expérimentaux sont présentés à la figure 26 avec un contrôle en boucle ouverte. Sur la figure 26, la tension notée V_F et correspondant à la tension de sortie avant le filtrage, prend pour valeur 0V et 18V ou 30V.

La tension théorique de 0V et 24V est obtenue en prenant en compte le déséquilibre de la tension flottante. Ce déséquilibre fera l'objet de travaux futurs. L'ondulation du courant de sortie est 4,5A. La fréquence de commutation est 310kHz et la fréquence effective du courant de sortie est 620kHz. Les pics visibles sur la tension V_F sont dus aux éléments parasites de la sonde utilisée.

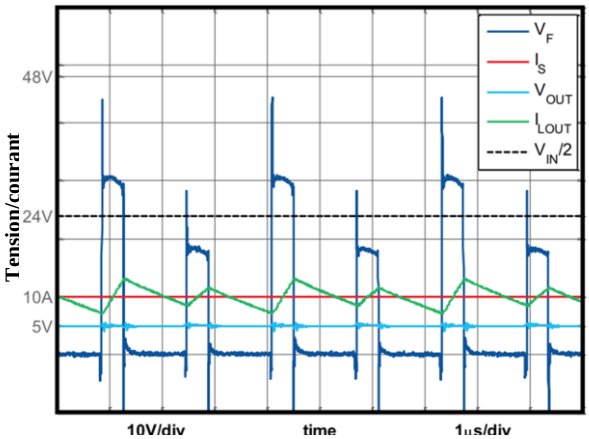


Figure 26: Formes d'onde expérimentales de tension avant filtrage V_F; tension de sortie V_{OUT}; courant sur l'inductance de sortie I_{LOUT} et courant de sortie I_S (48V entrée et 5V/10A sortie).

Conclusion

Notre travail a permis d'évaluer la faisabilité d'une intégration 3D des composants passifs. Un procédé de fabrication a été optimisé pour obtenir des condensateurs multicouches intégrés, planaires, directement sur le substrat. Les résultats obtenus sur les deux démonstrateurs tant pour la fonction de découplage du bus continu que de filtrage ont montrés tout l'intérêt que cette approche présentait. Des travaux complémentaires permettant d'obtenir une meilleure reproductibilité des échantillons et de s'affranchir des comportements observés tant avec la polarisation qu'avec la température doivent maintenant être envisagés.

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General introduction

Power electronics now plays an important role in the efficient conversion of energy for numerous types of applications, ranging from renewable energy resource development (wind power, photovoltaic, and fuel cells) to smart transport systems (electric and hybrid vehicles, navigation systems, dynamic traffic light sequencing, and more), as well as from industrial process control and automation to household appliances and lighting systems.

Power electronics circuits have traditionally been composed of active components, such as discrete semiconductor devices, connected to passive components, such as transformers, inductors, and capacitors to form distinctive functional converters. In recent years, power electronics has been driven relentlessly by progress in active device integration, improvements in circuit topologies, increased switching frequency, and improvements in packaging. The advances in semiconductor devices integration have been drastically faster than those concerning power passive components. Therefore, the latter occupy an increasing part of converter volume. For this reason, a great burden has been placed on the demand to integrated passive components. Furthermore, it is necessary to determine technologies suitable for three-dimensional integration of both active and passive components in a standardized approach.

One of the simplest solutions is to allow one or more capacitance layers to be embedded in the multi-layer printed circuit board, in addition to components placed on the substrate surface, to form a compact 3D system. The integrated passive component technologies that are available at this time consist of thin/thick-film technology, low-temperature co-fired ceramic (LTCC) technology, and technologies based on high-density interconnection (HDI) and other printed circuit board (PCB) technologies. Of the technologies suited for capacitive substrate integration, thick-film technology generally provides the advantage of versatility, component value range, and functional density to achieve more integrated, more shrinkable, lighter, and more cost-effective execution. Among the various thick-film technologies, the screen-printing technique is an attractive choice because of its mass production potential thanks to the use of roll-to-roll (R2R) printing. In addition, the screen-printing technique is simple, economical, and highly feasible in a laboratory environment. It can also be performed under normal conditions (notably atmospheric pressure and room temperature). As a result, screen-printing is emerging as a promising technology that enables a new generation of converters to approach 3D construction, and is notably more competitive in a market with constantly dropping costs.

Planar multilayer integrated ferroelectric capacitive substrates are applied for two main uses. The first objective of this thesis is to develop and validate a plane substrate

technology similar to "busbar", but integrating capacitive layers directly. These capacitive layers may be used to achieve capacitor decoupling required by any switching cells on its DC bus, and/or to develop the capacitors for a common filter placed on the same DC bus. As an additional property, this approach allows matching the shape and the arrangement of the capacitive layers with the building requirements of the full converter. The technological process to achieve this target is the screen- printing technique. The process was optimized to manufacture multilayer ferroelectric ceramic capacitors with high electrical performance. High capacitance value density (2.2 to 2.7nF/mm^2), low parasitic losses, low current leakage, and medium dielectric withstand voltage (100 to 150V) are obtained. These new integrated passive components are then used to create a planar integrated multilayer capacitive substrate in a practical DC-DC converter.

The second objective is to develop an integrated capacitor floating function for a DC-DC flying capacitor multilevel converter. Integrated screen-printed capacitors are used to reduce stray inductance on both the power and the driver loops while allowing the possibility of a double-sided cooling. A 48V to 5V prototype with screen-printed flying capacitors is built to show the feasibility of such a solution.

Further research is performed on dielectric materials, notably regarding the influence of cold isostatic pressure (CIP). Different pressure levels (600 to 3,000 bars) are applied on the printed and dried thick films, before sintering, to increase material density and decrease the thickness of the dielectric layer. The impact of CIP on the characteristics of integrated capacitors are analyzed and evaluated. The main objective of this section of the thesis is to study the characteristics of ferroelectric materials under isostatic pressure, and propose alternative integrated capacitor options for various applications with higher capacitance value.

The final section presents and discusses the first results of DC-DC converters using a planar multilayer integrated capacitive substrate. The decoupling functions of these capacitors in two cases are tested and evaluated. As a result, capacitive layers embedded on substrate show good performance, enhancing the development of embedded passive component technology for lighter, thinner, more advanced, and more cost-effective power electronic converters to remain compatible with continuously increasing requirements in a variety of applications.

Contribution and structure of this dissertation

This work was developed using the technological platform of 3DPHI (3-Dimensional Hybrid Power Integration) ENSEEIHT site for technological operations, and UPS site for characterization. Both sites are located in Toulouse, France. The full converter tests were implemented at the LAPLACE laboratory (Laboratory on PLAsma and Conversion of Energy) and IES (Southern Electronics Institute) in Montpellier, France. This thesis

contributes to studying and validating an enabling planar technology for the concept of 3-dimensional passive and active components integration.

This dissertation is divided into the following seven parts:

General introduction: Overview of the context and objectives of this work.

Chapter 1: Explains the technology trend regarding 3D passive component integration. The status and problems of passive component integration are reviewed. The main objective is to focus on how to make planar integrated multilayer capacitive substrates for DC-DC converter applications where these integrated capacitors are mainly used for decoupling.

Chapter 2: Discusses and compares today's available technologies for passive component integration, such as LTCC, HDI, PCB, and thin/thick film technology. The reasons for choosing the screen-printing technique and the material finally retained are presented. An optimized process to produce integrated capacitors by using this technique is provided at the end of this chapter.

Chapter 3: Presents fundamental methods for characterizing integrated capacitor samples, from simple MIM (metal-insulator-metal) capacitors to complicated multilayer capacitors. This chapter also presents and analyses the advantages and disadvantages of capacitor characteristics when they are taken into account in power electronic design.

Chapter 4: Analyzes and evaluates the impact of cold isostatic pressure (CIP) associated to the screen printing technique on dielectric properties in integrated capacitors, as well as their improved characteristics.

Chapter 5: Implements proposed topologies for DC-DC converters. This includes designing screen masks for a screen-printing machine, and developing and characterizing planar integrated multilayer capacitive substrates. The first results of new integrated capacitive substrates for DC-DC converter applications are tested experimentally and discussed theoretically.

Conclusions and future works: Discusses enabling research for increasing levels of integration to improve the first generation of multilayer integrated capacitors for further applications in the future.

Appendices: Details are provided regarding the derivation of several important formulas.

Chapter 1
State-of-the-art of 3D integrated passive components

1.1 Introduction

Electricity is typically generated in form of alternating current (AC), while most electronic devices use some form of direct current (DC), including computers, mobile phones, motion control devices, and automation equipment. In order to convert electricity to a suitable form for various loads, power electronics uses power semiconductor devices to perform switching actions to achieve certain conversion strategies. Power electronics can play a key role anywhere there are conversions of voltage, current, or frequency. Power electronic converters serve as communication tools between the grid or standalone sources and various types of electrical consumer devices.

In order to meet continually stronger requirements in power electronics applications, converters need to be cost-effective and to present optimized dimensions, while offering high reliability, more features, and greater manufacturability. Besides improving circuit topologies for higher efficiency and lower noise interference, power electronics integration plays an important role in reaching these goals. The trend in integration is towards increased switching frequency, reducing or eliminating structural inductances and capacitances while in integration technologies, it is to provide the best trade-off between three core components of the design: electrical aspects (EMI, control, topology, loss reduction…), constraints issues (spatial design, material technology, system reliability), and thermal considerations (heat transfer, life-time…) within certain boundary conditions (operating temperature) [1]. Over the past several years, progress in active device integration technology has improved the characteristics of power electronics systems (including increasing current, voltage levels, and operational temperature, while enhancing reliability and functionality), as well as reducing size, weight, and cost. However, a large part of volume in converters is occupied by passive components (inductors, capacitors, transformers) and interconnections. Therefore, there are great challenges on passive components, especially on technologies that allow 3D integration of both active and passive components into a small size, standardized module. Parasitic effects of interconnections (losses, parasitic capacitances and inductances) depend on their length. Thus, 3D designs, in which a part of plane interconnections is replaced by vertical vias, have lower parasitic components and lower power consumption than 2D designs [2].

This chapter analyzes key aspects and the overall trend for 3D passive component integration technology. The fundamental definition and construction of integrated passive components is given. The current state, benefits, and weaknesses of integrated passive components are reviewed and discussed. The main application targets are illustrated, focusing on planar multilayer integrated capacitors with different functions for DC-DC converters.

1.2 Technology trend towards 3D integrated passive components

The idea of integrating passive components into the converter's structure had been suggested starting in the early 1990s by a power electronics group (Van Wyk, Ferreira, et al.) from the Rand Laboratory for Energy and University of South Africa [3]. Over the course of many years, various research groups around the world have presented proofs regarding the potential for integrated passive modules. Although passive integration continues to grow, the commercial use of integrated passive components may still be very far in the future. Not only have the optimal material, technology, and proper performance, or cost-effective modeling not yet been identified, but they also represent significant obstacles. The practical applications of integrated passives will be possible only when materials and manufacturing processes for all passive components are established. For magnetic components, recent advances in microelectronics and packaging technologies have enabled a variety of approaches to integrate magnetic components. However, capacitors still have a long way to go, notably because of the difficulty in finding appropriate dielectric materials that are easy to deposit on the different substrates. In addition, there is still the issue of supplying a sufficient specific capacitance value to make component footprint small enough for economical layout without excessive numbers of layers, while still meeting operating voltage level requirements. Finally, these passive components also require compatible fabrication sequences for co-integration in different applications.

1.2.1 Reasons for integrating passive components: general considerations

A power electronics converter is comprised of different active and passive components, often surface-mounted-components, interconnected on a printed circuit board. An approach to build more compact power converters seeks to increase the level of integration for both active and passive components, moving towards high switching frequency with a reduction or mitigation of bulky inductances or capacitances. Reducing the interconnection length between active and passive components increases the performance level and saves package and board space. To meet the continuous incremental requirements of power electronics, passive component integration needs to keep pace with advances achieved in state-of-the-art active power electronics components. The research and development on integrated passive components are therefore driven by the following factors [4], [5]:

- **Reducing mass, volume, and footprint:**
  - Eliminate individual packages
  - Leave more space on the surface
- **Improving electrical performance:**
  - Reduce parasitic components
  - Reduce surface EMI
- **Increasing design flexibility**
  - Design capacitors and magnetic components with any desired characteristics within the technology's range
- **Improving reliability**
  - Reduce the number of solder joints
  - Enable good heat transfer potential
- **Reducing unit cost**
  - Eliminate discrete components and their related costs
  - Reduced board size
  - Increase mass production possibilities
  - Increase manufacturability (modularity and standardization)

1.2.2 Existing issues in integrated passive component integration

While active component integration has led to many innovations in performance improvements and size reduction, the current state-of-the-art in passive component integration still shows drawbacks that delay their diffusion in power electronic systems:

- **Indetermination of materials and technologies**. For example, most of the interesting dielectric or magnetic materials have to be fired, that make incompatible the co-manufacturing with classical substrates as PCBs, this issue concerning the PCB materials as the soldering processes.
- **Lack of design tools for both component sizing and layout**. This is a consequence of the previous issue. Tools cannot be available if the technologies are not clearly identified and characterized.
- **Technical and economical positioning** complicated by the continuous improvement of surface mounted technology. The assembly issue with surface-mounted components is relatively simple. The improvement of multi-layer PCB technologies allows reducing the area occupied by connections, including power windings on which magnetic cores are directly placed to constitute magnetic components and mixing the mounting of signal and power semi-conductor devices. Conversely, the "integrated passive" concept forces to design simultaneously the substrate, the connections and the passive components thus

changing drastically the required knowhow. The overall economic impact of replacing discrete passives with integrated passives is not simple to determine. Understanding the real economic influences obtained from applying integrated passives can be considered once significant experience regarding the designs has been accumulated, that is not the case for now.

Therefore, with existing problems and the present status of integrated passive components, research works on optimal materials and technologies for passive component 3D integration is still essential to achieve further innovations in power electronics.

1.2.3 Some development trends of integrated passive component

1.2.3.1 The inspiring example of 3D integration in microelectronics

Even today, most of passive components used in electronics (even more true in power electronics) are discrete modules mounted on the surface of common substrates (mainly PCBs) with active components. The disadvantages of this discrete construction are the large space occupation on one hand, the reliability issue due to the numerous soldered points on the other hand. To overcome these drawbacks, numerous research works began to focus on concepts such as “integrated” and “embedded” passives, seeking to fabricate the components as a group, in or on a common substrate, instead of as their own individual packages [6]. For now, the first industrial applications of such technologies are limited to signal and digital electronics. The both approaches use the third (and thin) dimension and inspire some developments in power electronics, especially in the low power range.

Integrated passive is a term that refers to multiple passive components sharing a single substrate and single packaging. These components can be placed inside the build-up layers of the primary substrate, using the technique known as “embedded passive components”, or they may be mounted on the surface of a separate substrate that is then placed in an enclosure and surface-mounted on the primary interconnection substrate. This approach offers numerous benefits such as reduced circuit dimensions and improved electrical performance (eliminating board soldering and increasing reliability) (see figure 1.1).

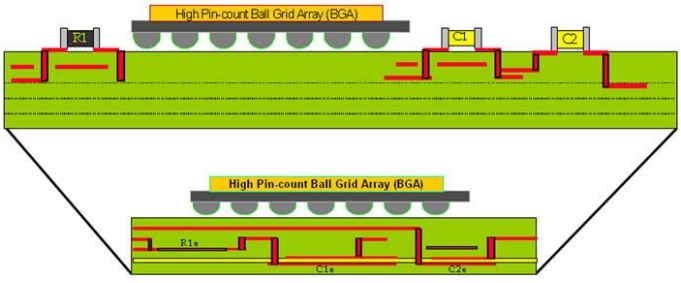


Figure 1.1: Conventional PCB with discrete SMD passive components (*top*) and embedded passives integrated into the laminate substrate (*bottom*) (Source [7]).

Embedded passive technology is one of the most effective methods for integrating passive components in a PCB. The specific chosen materials are formed on top, or otherwise inserted inside the primary interconnection substrate as shown in figure 1.2, aimed at fabricating and burring the passive components such as capacitors, resistors, within layers during the manufacturing process of the raw board or in a subsequent process before the discrete components are mounted. Embedded passive technology enables passive components to be embedded into substrate very close to active devices. The shorter distance between the embedded passives and active devices reduces losses and results in better signal transmission and greater reliability.

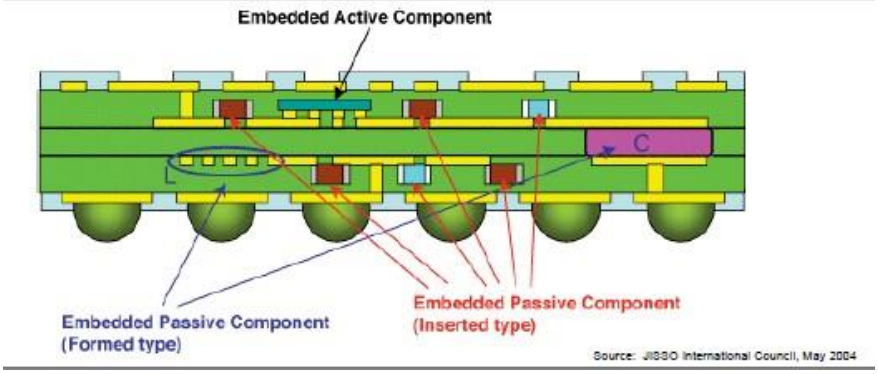


Figure 1.2: Embedding technology inside the PCB (Source:[8])

1.2.3.2 Integrated magnetic components in low power range

Integrated inductors can be considered as one of the key passive components in integrated power electronics circuit. They are widely used in filters, sensors… One of the bottlenecks for the development of their integration is the difficulty to find inductors presenting at the same time a small size, an acceptable inductance (L) and a high quality factor (Q). Lot of efforts have been made to develop new materials and to explore new processes and technologies [9]–[13]. Many approaches have been developed to achieve inductors integration and there are still numerous undergoing researches and optimization projects. Currently, Power System in Packaging (PSiP) and Power System on Chip (PSoC) are the two most widely adopted approaches for power integration.

1. The System-In-a-Package approach uses LTCC or MCM-D (Multi Chip Module – Deposited) techniques to produce off-chip inductors. This approach offers many advantages, such as higher performance, lower loss, and lower cost per unit area, without the difficulties associated to in-chip Si-solutions.
2. The other approach is to increase the performance of on-chip inductors by replacing conventional Al/SiO_2 technology with low-k materials and thick Cu metallization.

The layout of integrated spiral inductors fabricated by one of two previous approaches is driven by the joule and core losses, depending on winding shape/arrangement and magnetic material characteristics respectively. In the following some integrated inductor examples are reviewed.

In 2007, Damien Venturin et al. presented a new ferromagnetic material formed from insulated Fe/Co nanoparticles. A photo of a spiral integrated RF inductor designed with this material is shown in figure 1.3. The realization has been done by Freescale Semiconductors on a 7Ohm.cm Silicon substrate. The characterization showed that the inductance value increases up to 80% until 3 GHz, the quality factor value is enhanced as well until 1 GHz. These results appear compatible with microelectronic miniaturization [14].

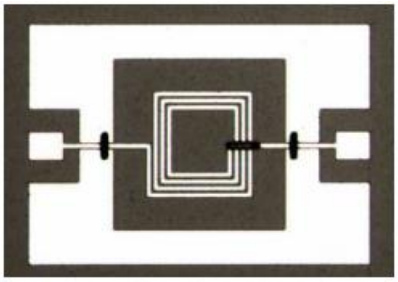


Figure 1.3: Image of the integrated inductor.

In 2011, another research of Elias Haddad et al. [15] introduced planar inductors on a microwave magnetic material (YIG) for monolithic DC-DC converters in System-In-Package of 100 MHz switching frequency (1W, V_{in} =3.6 V, V_{out} =1V). Electroplating of copper was used to fabricate a planar spiral inductor of 3mm^2 surface area as shown in figure 1.4. A high aspect ratio: 75µm in width and 50µm in thickness was achieved at room temperature. The results demonstrated an improvement in the inductance value by a factor of 2 compared to an air core structure, the Merit factor being of 0.6nH/mΩ.mm^2.

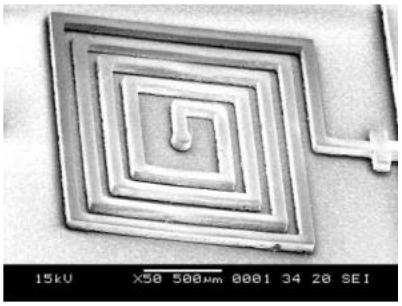


Figure 1.4: SEM images of the micro-fabricated inductor

1.2.3.3 Integration in combination using magnetic components and capacitors

Another major research trend in power electronics is to concentrate on combined integration of passive components, such as LC, or LCT. Many researchers have developed technology for integrating electromagnetic power passives [16]–[18]. These integrated passive modules could replace the functions of discrete capacitors, inductors, and power transformers. The goal is to obtain multifunctional and compact integrated modules using conductive, dielectric, and magnetic materials with different properties, such as high conductivity, high permittivity, and high permeability to build up multilayer, three-dimensional configurations. Integrating a combination of inductors, capacitors, and transformers has opened new opportunities for the technical development of passive electromagnetic modules and EMI filter modules. Extensive research has been conducted over recent years to develop these integrated passive modules.

This approach can be illustrated by the typical examples described figure 1-5 (Fred C. Lee et al. 2002) [19]. By using the parasitic capacitance of windings or by including a real capacitor in these windings (dielectric layers) an electromagnetically integrated LC structure can be obtained (fig 1-5(a)). External connections give different equivalent circuits as parallel, series, or low-pass filter. The construction of these simple bifilar spiral windings can be developed into more complex integrated structures by adding more winding layers as shown Figure 1-5(b), (c) (integrated resonant transformer structure L-L-C-T).

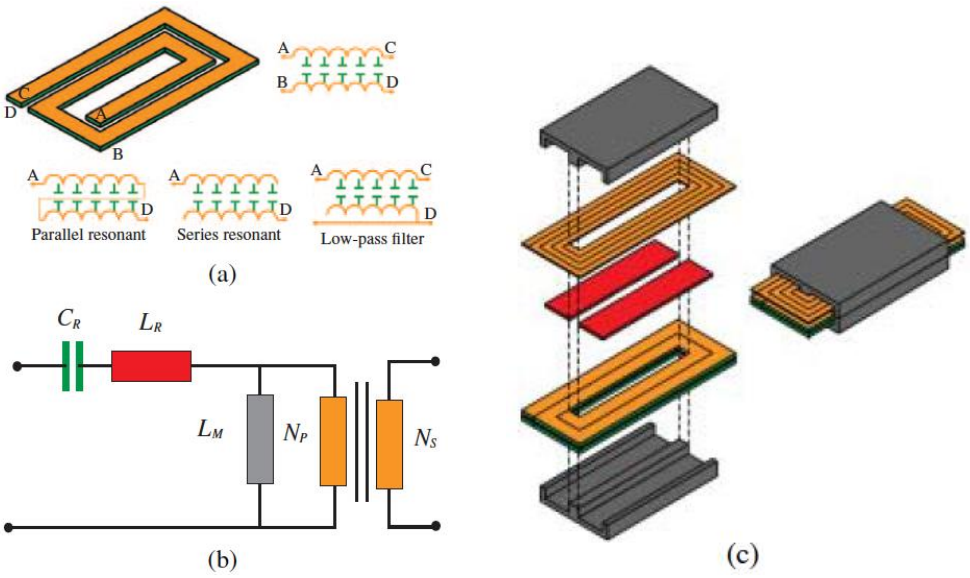
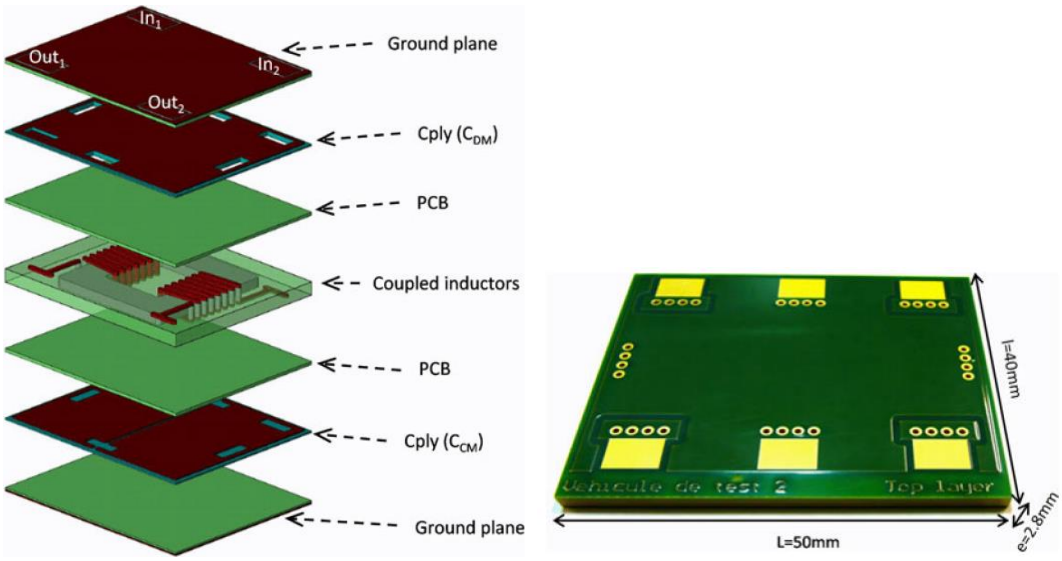


Figure 1.5: (a) Spiral integrated LC structure with distributed capacitance and possible external connection configurations, (b) simplified equivalent circuit, and (c) exploded view.

Results presented in publications show that a power electronics system using this concept could provide several distinct advantages:

- Properly distributed usage of space, increasing power density and reducing converter size.
- Reduced system interconnection, increasing reliability.
- Reduced packaged inductance structure, increasing electrical performance.

Other research works have shown that capacitive layers could be integrated as embedded components on substrate to perform various functions. For example, in 2012, Marwan Ali and al. suggested embedding one or more capacitive layers in the PCB in order to realize a hybrid Integrated EMC filter for a DC-DC power converter for aircraft applications [20]. The technology allowing integrating both capacitive and inductive components inside a printed circuit board structure, as shown in figure 1.6, is proposed. In this structure, two capacitive layers are embedded with, on the top of the PCB, six connections including two central connections to ground on both sides of the filter and four input and output connections. Compare to an EMI filter realized with discrete components, the proposed design reduces its volume by 58% and improves the Common and Differential Mode attenuations at high frequency. The proposed structure optimized for filtering high frequency interferences (beyond 2.5 MHz) must be supplemented by a low-frequency active filter. It is easy to use the PCB board incorporating the passive filter as a support for this new role. This architecture thus ensures maximum efficiency and optimum compactness for the EMC filter.



(a) (b)

Figure 1.6: (a) Realization of the integrated EMI filter; (b) Dimension of EMI filter

In the study of an integrated LC filter on silicon for DC-DC converter application of Philippe Artillan and al. reported the possibility to integrate both passive components (LC) on the same substrate. The micro fabrication of a fully integrated filter contained a spiral inductor on top of a 3-D capacitor as shown in figure 1.7. The feasibility of superposing a 3-D capacitor and a spiral-type inductor with thick conductors while keeping resistive losses to a minimum at high frequencies was demonstrated. Beyond the challenge of technological steps successions, precise impedance measurements in a wide range of frequencies (10 kHz to 4 GHz) proved the interest of realizing a thin magnetic material layer [21].

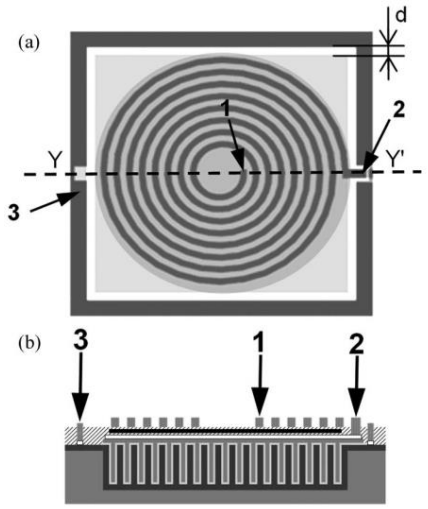


Figure 1.7: Schematic of the integrated LC filter (a) top view; (b) cross-sectional view

The previous approaches seem to be particularly appropriated to filtering functions requiring systematically the association of the different types of passive components and could concern more particularly the low to medium power ranges (few W to few kW).

1.2.3.4 **Integrated capacitors**

Among passive components, discrete capacitors with various functions (filtering, decoupling, resonant circuit…) usually take a significant space in a power converter. A simple way to build a more shrinkable and smaller footprint converter module is to embed one or more capacitive layers directly into substrate. Thanks to simple construction and the absence of leads and interconnections, integrated capacitors tend to have considerably less parasitic inductance than their surface-mounted counterparts. Consequently, integrated capacitors tend to be “purer” components with fewer undesired properties to be taken into account during the design phase. Integrated capacitors with low parasitic inductance have higher self-resonant frequencies and, thus offer larger operating frequency range than is possible with discrete capacitors. This is a particularly important factor in high frequency applications such as decoupling and RF filtering [22].

Over the past many years, significant effort has been devoted mainly in signal electronics to finding appropriate materials and processes for integrated capacitors. The following paragraphs offer an introduction to several relevant research projects in recent years:

In 2002, Chris THOMASON et al. presented high capacitance density thin film with integrated Tantalum Pentoxide decoupling capacitors. A thin film process was given to make multilayer capacitors. Their electrical characteristics were reported for an average capacitance density of 4.40 nF/mm^2 and for capacitance increase with the number of layers [23].

In 2005 Johann HEYEN et al. showed multilayer integrated capacitors fabricated by LTCC technology for an RF blocking application. The LTCC topology comprised 55μm thick dielectric layers (dielectric constant 8) and 10 μm thick silver electrodes. Capacitance reached approximately 15pF in a size of 1mm x 2mm x 0.6mm. Test results showed that the presented multilayer integrated RF-blocking capacitors feature increased frequency self-resonance without impairing the capacitance value [24].

In 2006 N. Kamehara et al. presented low inductance thin film capacitors for decoupling functions. The research group used Barium Strontium Titanate (BST)-based and Pt for dielectrics and electrodes, respectively. BST thin film deposited by RF magnetron sputtering achieved capacitance density of 40 nF/mm^2, leakage current density < 10^{-9} A/cm^2, and ESL lower than 20pH. These thin film capacitors were fabricated on Si wafers, thus relatively easy to integrate into system packaging [25].

In 2009, Aarnoud ROEST et al. were the first to show thin film ferroelectric metal-insulator-metal capacitors on silicon, with capacitance density above 100nF/mm^2 combined with a breakdown voltage of 90V, and lifetime exceeding 10 years at 85^oC and 5V. High capacitance density was obtained by combining high permittivity material (ε =1600) PZT and stacking construction through sol-gel processing. These capacitors are expected to replace discrete components with electrostatic discharge protection [26].

In 2012 J.KULAWK et al. presented multilayer ceramic capacitors with non-ferroelectric high-permittivity $CaCu_3Ti_4O_{12}$ material and silver electrodes fabricated using the LTCC process. The highest capacitances, exceeding $10^3$$nF/mm^2$, were obtained at frequencies under 1kHz and at temperatures above 150^oC. The current voltage characteristic is nonlinear, breakdown voltage is about 10V, and the nonlinearity coefficient is approximately equal to 3 [27].

Almost all of the above-mentioned research concentrated on presenting the possibility of only one type of material and technology for integrated capacitors. Parameters for integrated capacitors were measured but have been not yet been validated for detail-specific power electronics applications.

An overview of recent research on integrated capacitors for power electronics applications confirms the expected demand for finding optimal materials and technologies devoted to building strong integrated capacitors. Moreover, demonstration in specific power electronics applications is indispensable in order to obtain precise evaluations regarding the value of integrated capacitors.

1.3 Positioning of this work

1.3.1 The general objective: integration of capacitors

This thesis is highly driven by a desire to develop research on appropriate materials and technology in order to manufacture embedded, planar, integrated multilayer capacitors directly onto substrate. Another focus is on the semiconductor devices that can be assembled and interconnected on the integrated passive substrate by a wire bonding or flip-chip solder bonding process to minimize interconnection lengths and the amount of surface area required. These embedded capacitive layers not only have shorter leads and lower inductance, resulting in improved electrical performance, but they also have no solder joints, which results in greater reliability.

To develop embedded capacitors, the present work chooses to focus on screen-printing technology because the technique is simple, and offers relatively simple operating conditions. Screen Printing Technique (SPT) is studied using a ferroelectric (FE) ceramic material based ink. Due to their high dielectric permittivity and, in some case, their non-linear behavior with respect to both temperature and voltage, FE materials seem to be a very good choice for integrating passive power components. A process using a combination of FE material and SPT has been optimized to obtain high density, planar multilayer capacitive substrates. This process not only avoids the existence of defects, but it potentially, in some cases, allows self-healing phenomena to appear in dielectric layers. These self-healing capacitors can sustain many dielectric breakdowns during their operating lifetime, thus handling higher operating voltage and therefore, providing larger energy densities. In addition, process flows have been optimized to fabricate planar multilayer capacitive substrates dedicated to DC-DC converter applications.

The results are presented in this thesis and discussed here both from material and PE points of view. The reasons for technological and material selection are analyzed in more detail in Chapter 2.

1.3.2 The application target: decoupling of DC-to-DC power converters

All power electronics converter topologies are based on the association of switching cells using power switches from 2 to 2n (two-levels to n+1 levels). In most cases, the switching cells are connected to a DC-to-DC bus. In all cases, the switching cell requires adding decoupling capacitors on the DC bus, as close as possible to the power switches, in order to minimize parasitic inductance of the physical switching loop and therefore to minimize the turn-off overvoltage. Therefore, decoupling is a very demonstrative function to apply the "capacitor-integrated-in-substrate" concept and to validate corresponding technologies.

1.3.2.1 Two examples requiring planar integrated decoupling capacitor

Two particular examples to emphasize the interest in designing planar integrated capacitors have been selected. On one hand, the proposed approach can be used to integrating the plane's capacitive zones in available areas in existing devices, and, on the other hand, it aims to take advantage of plane configuration to obtain three-dimensional devices by stacking elementary plane switching cells. In both cases, the vicinity between decoupling capacitors and power switches is a critical feature. Figure 1.8 illustrates these two possible application approaches:

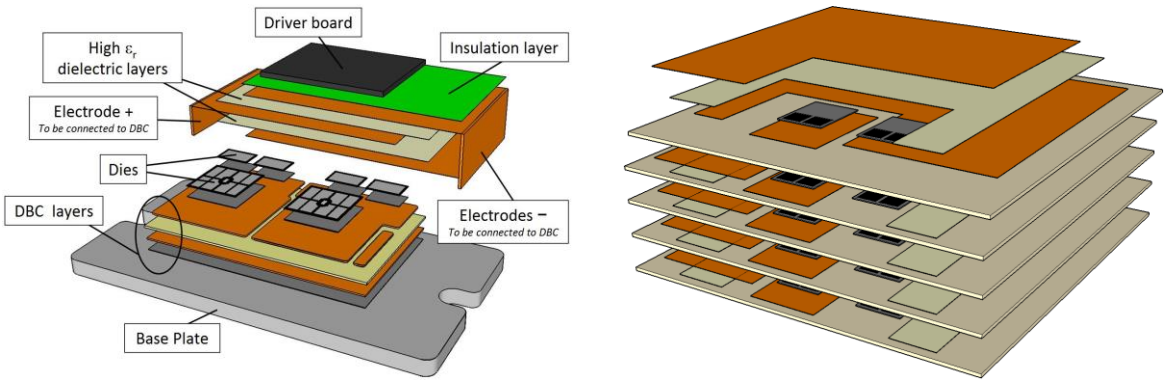


Figure 1.8: Projection of capacitor integration:
(a) Decoupling in the power module, (b) Decoupling in a multi-cell converter.

Figure 1.8(a) presents an example of the first option. The surface available inside a power module could be used to integrate a decoupling capacitor directly in the module, above the semiconductor devices. Gate drivers could be moved to the top face. If the capacitor is thin enough, the height of the module can remain unchanged, thereby creating an improved technological cell that includes the decoupling and the gate drivers. With the expected thickness of the capacitive layers being around few hundred of µm, this target appears to be

reachable. The electrodes shown in the schematic representation of Figure 1.8(b) are not representative, due to the exploded view of the capacitive zone, and connection parts are not represented. To make possible the proposed concept in order to constitute a completely integrated switching cell, many critical issues still have to be solved:

- Interconnection of the upper face of the die.
- Interconnection of the plane capacitor with the previous part.
- Creation of conductive vias through the capacitive zone to connect the gate driver to the dies.

The second option concerns parallel multi-cell converter topologies. The elementary cell should be implemented on a capacitive plane substrate and n samples of this elementary block should be stacked to constitute an n-cell converter. As in the previous case, critical issues must be solved in the same manner, namely: interconnections between the stacked cells and thermal management of the dies.

Therefore, the aim of the present work is to implement capacitive substrates on significant areas (a few cm²) and to obtain high specific capacitance values with a low number of layers by using high-permittivity materials. The issues concerning interconnection and thermal management are not considered here. Nevertheless, it was necessary to validate the proposed technology in a configuration that includes semiconductor power devices

1.3.2.2 First demonstrator: classical decoupling function on DC bus

The first demonstrator is made with the well-known and basic, two-level switching cell that can be achieved with nearly any kind of power device (Figure 1.9, only MOSFET or IGBT+diode options are considered here).

This part of the present work focuses mainly on this decoupling capacitive function. Additional capacitors can be introduced on the DC bus as a part of a common mode filter, if necessary. Both capacitive functions, decoupling and common mode filtering, are considered in the final demonstrator.

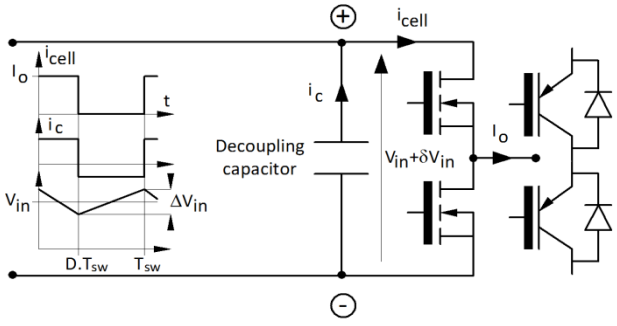


Figure 1.9: Operation of the decoupling capacitor.

The capacitor value needed to achieve the decoupling function correctly in that cell can be estimated by using the following equation (1).

$$C_{in} = \frac{P}{4F_{sw}\frac{\Delta V_{in}}{V_{in}}V_{in}^2} \quad (1)$$

Eq.(1-1) Capacitance value for decoupling.

With:

– $P = V_{in}.I_{on}$ nominal output power of the cell in DC conversion mode

– F_{sw}, switching frequency

– $\Delta V_{in}/V_{in}$ relative voltage ripple across the decoupling capacitor, maximal value obtained for a duty-cycle $D = 0.5$ and $I_o = I_{on}$

For common mode filtering, capacitor's values are approximately five to ten times lower than the decoupling ones.

The substrate designed for this first demonstration and the complete cell are presented in the fourth and fifth sections of this dissertation respectively. The proposed commutation cell is expected to operate with the following characteristics:

$$P = 2000W,\ V_{in} = 200V,\ I_{on} = 10A,\ F_{sw} = 100kHz$$

This choice induces significant values for the decoupling capacitor: around one to two µF for a relative voltage ripple of 10% (see Figure 1.10). The concept limitations have to be evaluated if current dielectric materials are used.

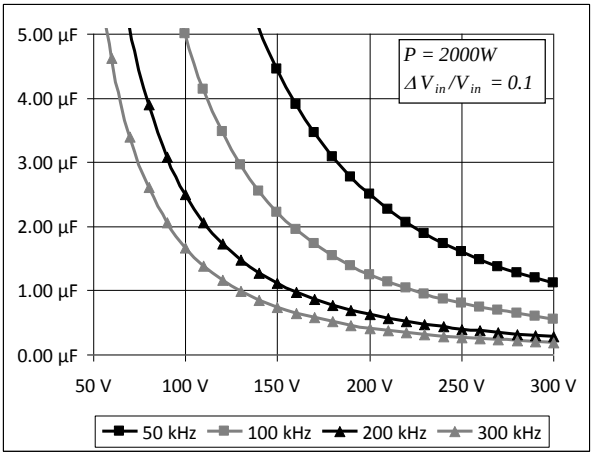


Figure 1.10: Value of decoupling capacitor vs voltage rating.

1.3.2.3 Second demonstrator: decoupling function in flying capacitor converters

The second demonstrator is based on a more specific converter, the multi-level flying capacitor converter, considered for designing Point-of-load (POL) DC-DC converters. POL converters are used in a wide range of applications, from portable devices, electric vehicles, and automotive control to renewable energy applications. These applications continuously demand higher power density, higher conversion efficiency converters with smaller size, lighter weight, and lower cost. Innovative active and passive integration technologies are key factors for obtaining higher efficiency and greater levels of integration. Challenges for obtaining higher power density in POL converter integration include [28]–[30]:

- Minimization of switching losses in order to increase both efficiency and switching frequencies.
- Integration of both active semiconductors and passive components while minimizing parasitic capacitors and inductors.

Therefore, an option to overcome the above issues is the series multilevel topology presented in Figure 1.11. The series association of low-voltage semiconductor devices is very efficient in switching operation and the topology allows reducing output filter size. In that converter, the flying capacitors perform again a decoupling function but the total capacitive energy stored is higher than in a classical two-level cell. Therefore, it is also a good option to demonstrate the interest of integrated capacitors in such a structure.

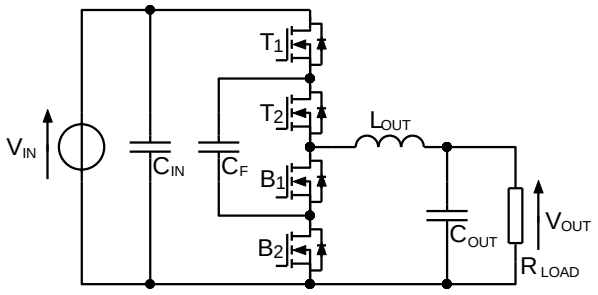


Figure 1.11: Schematic of a three-level flying capacitor converter.

More particularly the objective here is to demonstrate the feasibility of integrated capacitors in a gallium nitride POL converter with double-sided cooling. Concrete advantages can be obtained by using a two-cell converter instead of a classical one-cell converter. The DC-DC step-down converter has an input voltage of 48V and an output voltage of 5V. By using a two-cell flying capacitor (FC) topology, the voltage applied on output inductor is 50% lower than with a classical one-cell buck converter for this same 48V-5V conversion. Thus, constraints on active components are reduced, and the trade-off between inductance and current ripple is improved.

The technological process for producing the capacitive layers and experimental results for the two proposed topologies are presented and discussed in following chapters.

1.4 Conclusions

The purpose of this first chapter was to describe state-of-the-art and challenges of 3D passive component integration for power electronic integration from an electrical point of view. The increasing trend towards system-in-a-module solutions in power electronics requires 3-dimensional integration of both active and passive components into standardized compacts. Passive component integration must be implemented to catch up with the continuous accelerating pace of active component integration. The advantages of integrated passives allow smaller static converter size and better performance, notably due to their shrinkable dimensions and smaller footprints between active and passive devices on the board. The greatest challenges are the indecision on material and process, along with the design tools, standardization, and cost modeling. Numerous recent research projects demonstrated, in part, the feasibility of integrated passives associated with integrated actives. However, in order to apply widely integrated passives to commercial applications in the future, similarly to active components, further investigation on better materials and technologies is still needed. Among the many available passives, capacitors offer an interesting target because they often occupy a significant space. Although integrated capacitors offer a great potential to reduce both the size and cost of converters, capacitors still have a long way to go because of the difficulties in finding appropriate dielectric materials and processing. This situation is a source of motivation for our dissertation research. Our effort seeks to contribute to advancing possibilities for using integrated capacitors in power electronics miniaturization. Not only are the electrical performance and properties of capacitors presented, but we also provide demonstrations of decoupling functions in integrated capacitors obtained in two different proposed DC-DC converter topologies. The next chapter analyzes choices for appropriate materials and technology to achieve integrated capacitors for the above-mentioned purposes.

Chapter 2
Technology and Materials Selection

2.1 Introduction

The main driver for power integration technology is to achieve systems with greater functionality, higher performance, and lower cost in a smaller and lighter module. This demand has been satisfied, in part, by strong development of technologies for semiconductor devices, such as silicon and GaAs, and more recently for semiconductor component integration, such as System-On-Chip (SOC) and System-In-Package (SIP) solutions. SOC is an integration of several heterogeneous analog and digital technologies, whereas SIP is an integration of multiple chips with different functions placed in a single package or module. Both technologies provide greater integration flexibility than was possible before, offering both size reduction and lower product cost [31]. In fact, these technologies are still one of the forces driving improvements in power electronics system development. This chapter reviews today's available technological and materials solutions for fabricating these integrated passive components.

Technologies available today for passive component integration include Low Temperature Co-fired Ceramic (LTCC), thin/thick film technology, High Density Interconnection (HDI), and other printed circuit board (PCB) options. The pros and cons of each technology are reviewed in the following sections, keeping the focus on fabricating planar integrated multilayer capacitive substrate for DC-DC converter applications. Reasons for material selections are given, in addition to technological options. The final section of this chapter introduces the technique that enables the development of the appropriate process for manufacturing planar integrated capacitors.

The choice of one technology over another depends on a large number of characteristics and performance factors. First, a theoretical overview is given to determine the required performance and configuration of the integrated capacitor for the purpose of this thesis. Then, the most suitable technology and material are chosen based on these specifications.

Capacitance values for decoupling (a few µF) and filtering (a few hundred nF) are targeted. Change in capacitor parameters definitely depends on the materials and technology used to fabricate them. In theory, for uniform homogeneous field, the capacitance of a plane capacitor can be calculated by the following simple formula:

$$C = \frac{\varepsilon_r . \varepsilon_0 . A}{d}$$

Where:

C is capacitance of capacitor, F

$\varepsilon_0 = 8.84 \cdot 10^{-12}$ F/m is the vacuum permittivity

ε_r is the relative permittivity of the dielectric

d is the thickness of the dielectric, m

A is the surface area of capacitor, m^2

Here the capacitance is directly proportional to the dielectric permittivity and to the surface area of the capacitor, and inversely proportional to the distance between the two electrodes. Electrical parameters and features must be considered when designing planar integrated capacitors, namely:

- Capacitance value and tolerance
- Dissipation factor
- Surge voltage, rated voltage
- Temperature coefficient of the capacitance
- Equivalent serial resistance (ESR), equivalent serial inductance (ESL), and self-resonant frequency (SFR)
- Leakage current
- Maximum current
- Ripple control
- Quality factor (Q-factor)

The capacitance density can be given by (C/A). When capacitors have the same surface areas, the capacitance density depends on the permittivity value and dielectric thickness d of the material. It is possible to increase the capacitance density by using high dielectric constant material and reducing dielectric thickness.

Lastly, the greatest challenges for achieving high capacitance embedded multilayer capacitors for DC-DC converter applications are:

- *Flexible design and appropriate performance:* high capacitance density ensures required capacitance from a *few hundred nanofarads* for filtering, to a *few microfarads* for decoupling functions, low leakage current, high Q, low ESR and ESL, operating voltage larger than 100V, operating frequency in the range of a few hundred kHz.
- *Thin, light weight, and low cost.*
- *Testing and mass production capabilities:* bare board electrical testing is needed to verify embedded capacitance, inductance and resistance, and frequency responses.
- *Minimize defects during the manufacturing process:* increase overall board yield.

- *Planar construction and surface:* thinner layers are required for the desired capacitance. Minimized internal connection leads to less parasitic ESL, ESR, increase SRF.

The above issues must be evaluated as part of technological and dielectric material selection.

2.2 Technological selection

2.2.1 LTCC

What is the LTCC technology?

LTCC stands for "Low Temperature Co-fired Ceramic", a technology that emerged in the late 1950's and early 1960's to make capacitors more robust. Over time, the use of LTCC was expanded to build stacked structure circuits for a variety of applications such as automotive, industrial, medical, and aerospace. LTCC is used to deposit conductive, dielectric and/or resistive paste on a glass/ceramic dielectric tape to produce multilayer circuits [32]. These tapes must be stacked, laminated together, and co-fired in parallel in a temperature range of 800-900°C. This is the main difference with thick film technology, where each layer is printed, dried, and fired sequentially. LTCC enables high output, saves time, and reduces cost, while shrinking circuit dimensions. Each single layer can be checked individually and, in case of inaccuracy or failure, they may be replaced before sintering. Figure 2.1 presents the traditional LTCC technology process. LTCC can be used to create complex circuits with high density and fully integrated substrate, such as that presented in Figure 2.2. Passive components can be integrated into substrates, and semiconductor devices are placed to fill in the holes.

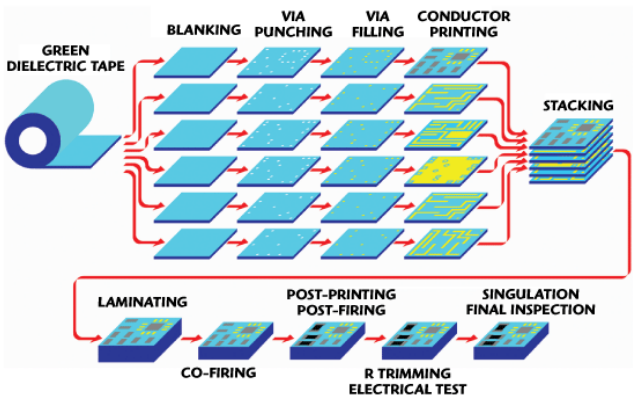


Figure 2.1: Process for fabricating LTCC (source [33]).

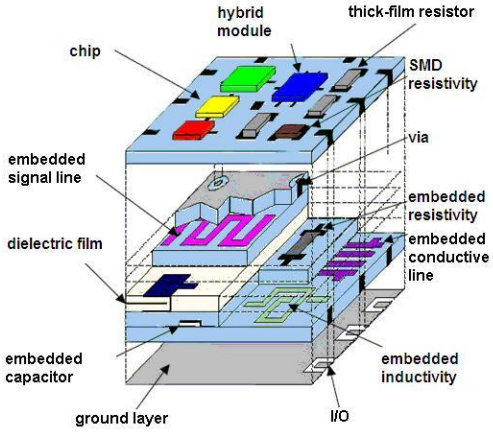


Figure 2.2: Complex LTCC circuit structure (source [34]).

Advantages:

LTCC provides the following advantages over other technologies:

- Processes are relatively flexible and cost-effective.
- High manufacturability (mass production possible thanks to the automation of several steps).
- Multiple layers can be built up (with a large number of layers: 40-50 layers).
- Possibility for passive components integration and smaller size 3-dimension circuit manufacturability.
- Good connection to active devices.

Disadvantages:

Although LTCC is a good technology for integrating 2D and 3D passive components, LTCC still has a major disadvantage: chemical and physical problems may occur between various tape materials during co-firing. The interaction of glass phases in the different tapes and the thick film involves chemical issues; the shrinkage mismatches of tapes and screen-printed inks involve physical issues. Ferrite tapes, capacitor tapes, and ceramic tapes often have different CTE and their co-firing may cause cracks [35].

Materials:

The choice of materials for LTCC technology concerns not only their dielectric properties, but also their firing behaviors and chemical compatibility, notably because they are co-fired at the same time, in one step. Therefore, materials chosen for LTCC generally have good thermal conductivity, good mechanical properties, and must not react chemically with the conductive material used. A wide range of conductive, resistive and dielectric materials use LTCC technology.

2.2.2 HDI

What is HDI technology?

High Density Interconnect (HDI) technology is a method to compress integrated circuit packaging by placing bare chips into cavities on a substrate and fabricating the thin-film interconnect structure on top of the components. Interconnections to the chip pads are formed as a part of the thin-film fabrication process, thus eliminating the need for wire bonds, tape-automated bonds, or solder bumps. HDI packaging can therefore minimize size and weight, and increase performance of the electronic circuit.

HDI is one of the technologies that allow integrating three-dimensional passive components. Figure 2.3 shows an example of an integrated passive component circuit built sequentially by a number of thin interleaving layers of metal and dielectric material on a substrate. Integrated resistors are made using thick polymer film materials, while the local deposition of high permittivity material creates integrated capacitors.

Flexible High Density Interconnect (HDI) circuits offer increased design, layout and construction options over typical flexible circuits. Each High Density Interconnect incorporates microvias. Processes include microvias such as photo-via, laser-via, plasma-via, and Any Layer Inner Via Hole (ALIW).

There are six different types of HDI boards: through vias from surface to surface; with buried vias through vias; two or more HDI layers with through vias; passive substrate with no electrical connection; coreless construction using layer pairs and alternate constructions of coreless constructions using layer pairs. By using HDI technology, designers now have the option to place more components on both sides of the raw PCB. Multiple via processes, including *via-in-pad* and *blind via* technology, leave designers with more PCB real estate to place smaller components even closer together. Decreasing component size and pitch allows for more I/O in smaller geometries. This means faster transmission of signals and a significant reduction in signal loss and crossing delays.

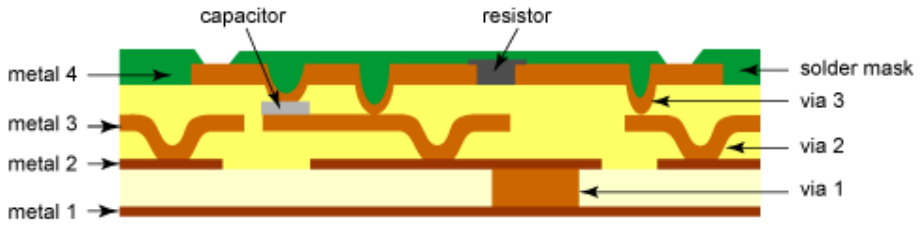


Figure 2.3: An example of passive components in HDI technology (source: [36]).

Advantages:

This technology offers:

- Better electrical performance and signal integrity
- Cost and size reduction
- More design options and flexibility
- Improved thermal performance and reliability [37]

Disadvantages:

There are limitations on resistor stability and accuracy, although parts can be laser-trimmed to specific values before the solder mask is applied. Similarly, there are limitations regarding the value and tolerance of capacitors.

2.2.3 Other PCBs

Conventional PCB technology is used to etch the desired patterns on the copper-laminated plastic board. The most common processes used in PCB fabrication are plating, bonding, etching, and drilling as presented in Figure 2.4. Processes range from a simple single-sided board to complex multi-layer boards, and double-sided surface-mount designs. The conventional printed circuit board manufacturing process is summarized below, including, drill, plating, and final fabrication.

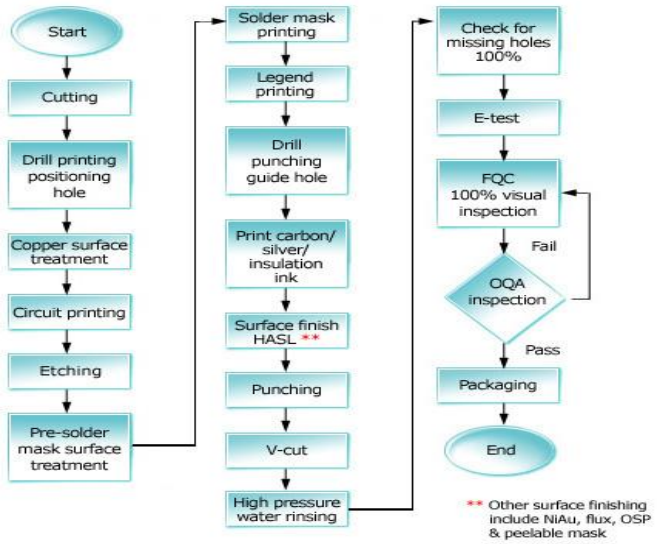


Figure 2.4: PCB manufacturing process (source: [38]).

In addition, other PCB technologies available today provide more options for customers, notably: thermal clad, heavy copper, extreme copper, and power link PCBs [39].

2.2.3.1 **Thermal Clad PCBs**

This technology offers thermal clad PCBs made from a dielectric metal base and a bonded copper circuit layer that uses high performance and low cost materials. This construction provides effective heat transfer to cool components and avoids the problem of brittle ceramic substrates.

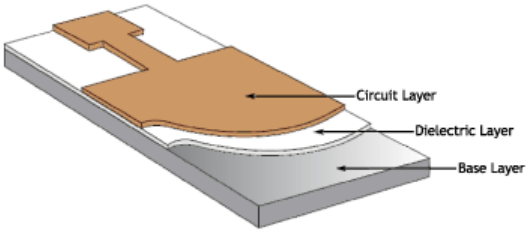


Figure 2.5: Thermal clad PCB construction.

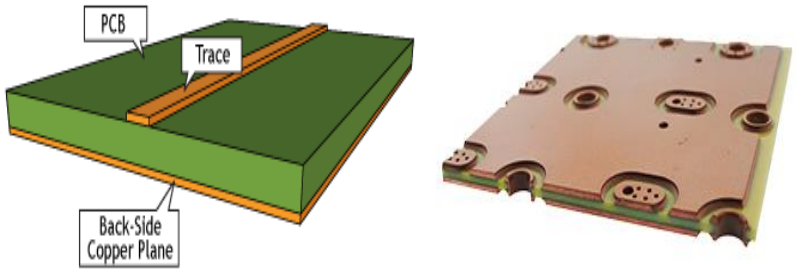
Thermal clad PCB construction is shown in Figure 2.5. The circuit layer is a bonded copper foil, with thickness of 35µm to 180 µm. The dielectric layer is made from a selection of many insulating materials to achieve minimum thermal resistance. Most of the base layer is made of aluminum or copper, with thickness of about 1mm. The benefits to Thermal Clad PCBs include:

- Lower operating temperatures
- Improved product durability
- Increased power density
- Increased thermal efficiency
- Reduced number of interconnections
- Lower junction temperatures
- Reduced PCB size
- Minimized labor for assembly
- Wide variety of form factors
- Minimized thermal impedance.

2.2.3.2 **Heavy copper, extreme copper, and Powerlink PCBs**

Heavy copper, extreme copper, and Powerlink PCB technologies build heavy copper circuit boards with traces and copper planes. Heavy copper is defined as any circuit with copper conductors of 0.0079kg/m^2 – 0.026kg/m^2 contained in inner and/or outer layers on a printed wiring board (Figure 2.6.a). Copper weights above 0.0527 kg/m^2 and up to 0.527

kg/m^2 are also possible, referred to as "extreme copper" PCBs (Figure 2.6.b). Powerlink is defined as the use of two or more copper weights on the same external layer of the printed wiring board (Figure 2.7). These PCBs are used in a variety of product applications, such as: high power distribution, heat dissipation, planar transformers, power convertors, and more.



a: Heavy copper PCB b: Extreme copper PCB

Figure 2.6: Examples of heavy and extreme copper PCBs

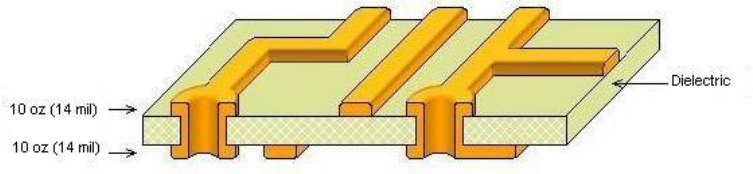


Figure 2.7: Powerlink PCB (source [40]).

Advantages of copper PCBs include: [41]

- Increased endurance to thermal stresses
- Increased current carrying capacity
- Increased mechanical strength at connector sites and in PTH holes
- Increased conductor cross-sectional area without increasing trace width or decreasing trace/trace spacing
- Reduced product size by incorporating multiple copper weights on the same circuitry layer
- Heavy copper plated vias carry higher current through the board and help to transfer heat to an external heat sink
- On-board heat sinks, directly plated onto the board surface using up to 4mm copper planes

PCB disadvantages:

- High cost
- Requires redesign for new types of circuit operation
- Requires larger footprints, less reliability
- Difficult to repair if damaged
- Complicated process, hard to update PCB once printed
- Not good for multiple reflow/assembly processes
- Not environmentally friendly

2.2.4 Thin/thick film technique

Thin-film and thick-film technologies are currently contributing significantly to efforts to downsize passive components in power electronics devices using monolithic or hybrid integration processes. These technologies are used to provide high-density interconnections in electronics applications ranging from industrial control equipment and hybrid vehicles to lighting and solar panels. They can be applied to electronic products requiring high design flexibility, functional density, and customization. The fundamental differences between thick film and thin film are the methods and materials involved, as well as the relative deposition thickness. Thin film technology involves depositing individual molecules or atoms, whereas thick film technology deposits particles. The differences are compared in section 2.3, following a general review of these two technologies.

2.2.4.1 **Thin film technology**

Thin film technology is often used to integrate passive devices in which conductive, resistive, capacitive, and/or insulating films are sputtered or evaporated onto a ceramic substrate or other type of insulating substrate. Chemical processes such as sol-gel, plating, and chemical vapor deposition are used, and laser cutting technique makes it easy to build custom shapes. Thin film processes are typically implemented under vacuum. The film can be deposited according to a designed pattern, or film layer photolithography, and etching is then applied to form circuit pattern features by cutting away unnecessary material. Figure 2.8 presents a traditional process of thin film technology for fabricating an integrated capacitor. Thin-film is most applicable when high volume, high density, or high performance is required. Applications that take advantage of this type of high performance include sensors, flat-panel displays, micro electro-mechanical systems (MEMS), biomedical devices and coatings, optical instruments, sensors, microwave and other integrated circuits, and thin film integrated passive devices (IPDs).

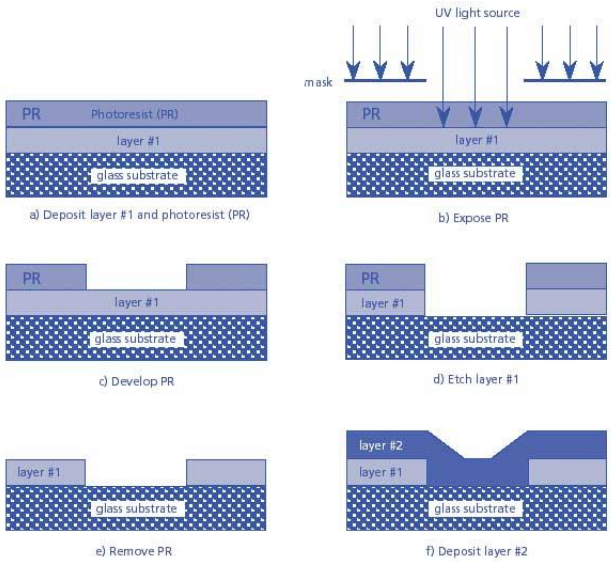


Figure 2.8: An example of thin film processing (source:[42]).

The materials used for thin film technology generally include:

- Conductors, including pure metals such as gold, aluminum, and copper. Gold and aluminum provide compatibility with wire bonding used in electronics packaging. Conductive films for optical transparency applications are based on tin oxides (indium-tin-oxide and antimony-tin-oxide). Thin film resistor materials are usually made of nickel chromium alloys or tantalum nitride.
- Dielectrics, such as polyimide, SiO_2 and Si_3N_4, provide electrical insulation or allow multiple layers to be formed on a single substrate.
- Substrate, which can include glass, silicon, sapphire, alumina, and aluminum nitride.

Advantages:

- Provides environmentally stable passive components with high ratio tolerances.
- High precision and very high-resolution processes involved in thin film technology can result in highly competitive products in terms of cost-per-function.

Disadvantages:

- Capital equipment costs are high for vacuum deposition, photolithography, etching, pattern transfer, and mask design.
- Complicated process with strict implementation conditions.

2.2.4.2 **Thick-film technology**

Thick-film technology is one of today's very promising methods for integrated passive component development, notably thanks to its highly flexible process and wide range of conductive, resistive, and capacitive inks. Pastes are printed as a screen mask pattern on an insulating substrate, then dried and sintered (Figure 2.9). Once each layer is dried at about 120°C, and then fired at about 900°C, the next layer is printed. Application examples include photovoltaic solar cells, chip resistors, gas analysis sensors, heaters, transducers, and more.

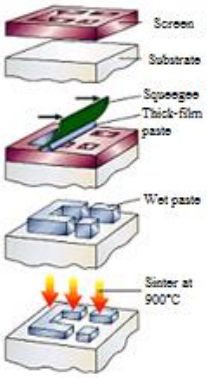


Figure 2.9: Thick film process flow.

The main materials used for thick film technology are:

- Conductors: A wide variety of conductor pastes exist to satisfy the circuit's bondability, solderablity, and electrical performance requirements. Gold, platinum-gold, copper, silver, palladium-silver, and platinum-silver are the most common.
- Dielectrics: Thick-film dielectrics are used to provide electrical insulation and protection, and to build multiple circuit layers. Alumina, glass, and barium-titanate oxide are common dielectric materials.
- Resistors are formulated in a glass matrix using metal oxides, typically ruthenium dioxides.
- Substrate: materials such as alumina, aluminum nitride, and beryllia provide the mechanical support and electrical insulation necessary for the circuit.

Advantages:

- High manufacturability thanks to roll-to-roll printing.
- Good possibilities for passive components integration and 3-dimensional electronic circuit manufacturability with much smaller size.
- Based on simplicity in processing, thick-film circuits can be produced with low initial investment and low running costs.

- As such, they are often utilized for low-volume, fast-turn applications.
- The relatively high printed volume of the films makes them useful in high power circuits where low resistivity is required.

Disadvantages:

- Screen mask may fail easily after many repetitions.
- Print designs with small, intricate details can sometimes result in technical problems, bleeding, and poor quality results.
- Long preparation may be required due to dependence on numerous initial machine parameters. Such problems definitely impose quality limitations on dielectric layers, which may be less uniform and contain more defects.

2.2.5 Final selection

Each of the technologies presented here has different pros and cons, and there is no way to cover all possible interrelationships of technologies, cost, and manufacturability. However, our best effort is applied here to provide a qualitative comparison between different integrated passive component technologies, based on optimization of capacitor characteristics regarding other important factors, such as process conditions and production cost.

A side-by-side performance comparison for the different technologies is given in Table 2.1. HDI, PCB, and thin film technology provide high-integrated density. However, like LTCC, their process is complicated and requires special production conditions, including as lighting, atmosphere, and other parameters. This results in higher production cost. LTCC technology seems to be a good choice because of its cost-effective process, but one of the great disadvantages of LTCC is its poor reliability during the co-firing of different material tapes. Thick film technology has the advantage of offering the lowest cost (including both new design costs and production costs), while being able to be implemented easily under normal conditions without requiring highly-skilled labor, and supporting mass production. In addition, thick film technology (more accurately referred to as screen printing technique - SPT) is able to run using a wide range of material inks with high dielectric permittivity. It is relatively easy to change screen mask patterns to make passive component designs more flexible with smaller size. This allows a higher integrated density capacitance value.

Table 2.1: Comparison of different technologies

	LTCC	HDI	PCB	Thin film	Thick film (*screen-printing*)
Cost	Low	High	High	High	Lowest
Size reduction	Good	Medium	Medium	Better	Better
Process	Complex	Complex	Complex	Complex	Easy control and manage
Tolerance	10%-20%	10%-20%	10%-20%	5-10%	10-20%
Functional density	High	Low	Low	High	Highest
Reliability	Medium	Lower	Lower	Low	High
Design methodology	Complex	Complex	Complex	Complex	Easy and flexible

The advantage of screen-printing over other printing processes is that it can work on substrates of any shape, thickness, and size. A significant characteristic of screen-printing is that a larger thickness of ink can be applied to the substrate than is possible with other printing techniques. Thanks to the simplicity of the application process, a wider range of conductive and dielectric inks is available for use in screen-printing than for any other printing process. With SPT, paste may be deposited with precision, while maintaining extremely good volume control and line definition.

In the end, thick film technology was found to be highly suitable for the purposes of this thesis. This technology offers a viable alternative option for providing a lower cost solution in the future. SPT and an optimized process are presented in section 2.4.

2.3 Material selection

2.3.1 Dielectric materials

The capacitance value required to ensure more effective filtering and decoupling functions, ranging from a few hundred nanofarads to a few microfarads, can be obtained by using high permittivity materials, larger electrodes, and a thinner dielectric layer. The dielectric selection here depends not only on a tradeoff between price and performance, but also on compatibility with screen-printed technology.

There are two groups (or classes) of dielectric ink materials: “Class1” is comprised of paraelectrics such as SiO_2, Ta_2O_5, Al_2O_5, and BCB. “Class 2” is comprised of ferroelectrics such as $BaTiO_3$, $Pb_xZr_{l-x}TiO_3$, and $Ba_xSr_{l-1}TiO3$. The dielectric permittivity of ferroelectric materials is usually much higher than the permittivity of paraelectric materials. Moreover,

paraelectric materials are more suitable for high tolerance applications, such as timing, RF wireless, and A/D for which constant, predicable capacitance is required. Ferroelectric materials would be better for high capacitance applications, such as decoupling and energy storage, in which high tolerance and stability are not extremely important, as long as a minimum amount of capacitance is provided [43]. Table 2.2 shows a comparison of commercially-available high permittivity ferroelectric inks from various manufactures.

Table 2.2: Comparison of commercial dielectric pastes.

	Dielectric materials	Permittivity	Dissipation factor (≤)	Insulating resistance ≥(Ω)	Fired thickness (μm)	Dielectric strength (VDC)	Shelf life (months)
Koartant	5350	50	1.0	10^{12}	34-35	600	6
	5351	100	1.2			600	
	5352	250	1.5			600	
	5355	500	2.0			600	
	5483	>8000	2.0	10^{9}	45-85	300	
Dupont	EP312	>2000	8		10-14	300	3
Heraeus	IP6075	20	0.5		22-27	1000	6
	IP 9217	8.5-11.5	0.5	10^{11}	21		
Electro science	ESL 4202	2000	3	10^{9}	40-55	100(air) 200(G481)	
	ESL 4212	12000	3		35-50		

From this table, it can be seen that ESL 4212 is the most suitable paste for our purposes because it can reach the highest dielectric values, up to 12000. ESL 4212 is a low-temperature firing, screen-printable, high capacitance density ink. This material is compatible with a wide range of ESL conductors, but best results are obtained when the dielectrics are terminated with specially developed silver- or gold-based conductors. Optimum properties are achieved when the capacitors are overglazed to provide hermeticity and prevent flashover.

2.3.2 Conductive materials

The most important properties of conductive thick films can be summarized as follows:

- High electrical conductivity
- Good adhesion to substrate
- Good solderability

- Good bondability
- Low price

The choice of conductive material here is based mainly on the low resistivity value. Silver, copper, gold, and their alloys are all conductive materials with high electrical conductivity. Among these conductive materials, silver is the most appropriate choice because it offers the highest level of conductivity (Table 2.3) and chemical stability. Moreover, silver's melting point (961°C) is suitable for the low firing (<900°C) step in the thick film process.

Table 2.3: Comparison of conductive materials.

	Material	Conductivity S/m
1	Silver	6.3×10^7
2	Copper	5.85×10^7
3	Gold	4.25×10^7

Therefore, to benefit from the higher performance of the dielectric material (ESL 4212), ESL 9916 was chosen as the conductive material to produce electrode layers. ESL 9916 is a silver-based conductor, specially developed for use as an electrode with the 4200-C series of dielectrics. Typical properties of these conductors were derived from printing and firing directly on alumina.

Table A.1-1 and table A.1-2 in the Appendix A provides dielectric and silver paste parameters (ESL 4212 and ESL 9916) from Electro Science Laboratories, Inc manufacturer.

Before use, it is necessary to measure ink viscosity. Material viscosity has an influence on the properties of the final thick film. Controlling the viscosity of deposited inks during the screen-printing process is therefore very important. An ink whose viscosity is too high does not yield a uniform and smooth surface for the deposited layer after through-screen printing [44]. Conversely, an ink with low viscosity spurts around the area defined by the screen. With appropriate modification of material viscosity (heating before screen-printing, adding solvent, etc.), it is possible to avoid failure in the technological process and enhance production quality. All inks were measured using a Brookfield RVT viscometer, ABZ spindle, 10rpm speed at 25.5°C ± 0.5°C (Figure 2.10).

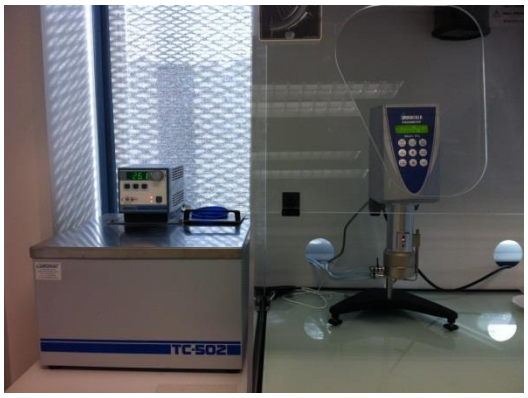


Figure 2.10: Thermal bath and viscosity meter (*viscometer*).

2.3.3 Substrate

The most widely used substrates in screen-printing technology are ceramics. These substrates provide the base onto which all thick film elements are screen-printed and fired. They therefore have an influence on the electrical and thermal performance of the circuits. The most important substrate properties can be summarized as follows:

- Dimensional stability
- Uniform surface
- High electrical resistivity
- High thermal conductivity
- Good layer adhesion
- Thermal compatibility with components
- Low dielectric permittivity
- Low dielectric loss tangent
- Low cost

Table 2.4 provides a comparison of various ceramic substrates. As previously mentioned, the substrate's thermal conductivity is one of the most important design parameters, due to the frequent requirement for maximum heat extraction from thick film circuits. Beryllia (BeO) or AlN substrates are used for circuits with very high dissipation, due to their thermal conductivity, which is about 12 times higher than that of alumina. The disadvantages of BeO are its cost and its high toxicity in both vapor and powder form in processing. The properties of AlN are well-suited for electronic packaging, but AlN is much more expensive than alumina and the adhesion of inks designed for alumina is low on AlN.

Alumina (96% Al_2O_3, with 4% glassing containing MgO, CaO, and SiO_2) is the most appropriate option because it meets all of above requirements to an acceptable degree. Alumina is quite uniform and has very good ability for facing high temperature during the

sintering process, while providing very good adhesion to fired layers [45]. For our research, we chose a substrate of 96% pure Alumina, 2 sq. inches, and 635µm thickness.

Table 2.4: Comparison of alternative ceramic substrates.

Substrate materials	Relative permittivity	Dielectric loss	Dielectric strength (kV/mm)	Linear thermal expansion coefficient 25°C [10^{-6}/K]	Thermal conductivity ($Wm^{-1}K^{-1}$)	Young's module (GPa)
Alumina ceramic (96% pure)	9.4	0.001	15	6.4	15-20	330
Beryllium oxide ceramic BeO	6.7	0.003	10	6.1	230-260	345
Aluminum nitride (AlN)	8.6	0.002	15	6	120-210	320

Before the screen-printing process, Alumina substrates are cleaned with an RBS 25MD solution according to the cleaning chart provided in Appendix A.2.

2.4 Introduction of the screen-printing technique (SPT)

Screen-printing is a relatively simple method. This thick film technology has already contributed progress in 3D passive integration for power electronics applications. SPT makes it possible to obtain multi-layer conductive, resistive and capacitive, inductive films in arbitrary shapes on the same substrate. Then, active devices and their associated control circuitry may be placed on the top of the passive layer to implement 3D construction while minimizing internal connections. It is necessary to adjust operating parameters of the screen-printing machine. Parameters for materials and process characteristic can improve the quality of the result. Nonetheless, thick prints are also challenging: the printing process must be strictly controlled in order to obtain high-quality, high-resolution figures. This section focuses on describing the screen-printing machine used in our research works and on selecting the optimized parameters to achieve the desired print strategy.

2.4.1 Configuration of the screen-printing (SP) machine

The screen-printing machine is presented in figure 2.11. This machine is comprised of three main parts: the controller, operating aspects, and observation tools. The controller part includes a computer with control software, a monitor, a keyboard, and a pedal for manual prints. To handle operations, the second part includes an actuator block, squeegees, a screen,

and a stencil. For observation, the machine includes two cameras operating in parallel to adjust the exact position of print patterns on the substrate.

Operational screen printing parameters, such as squeegee speed and position, printing mode, aspiration, cameras, etc, are controlled by software. The basic operating principle of the screen-printing machine is shown in Figure 2.12. The squeegee, applying specific pressure, pushes the ink flow through the screen to place a mesh pattern on the substrate. The opposite squeegee draws residual ink to the beginning position for continuous prints.

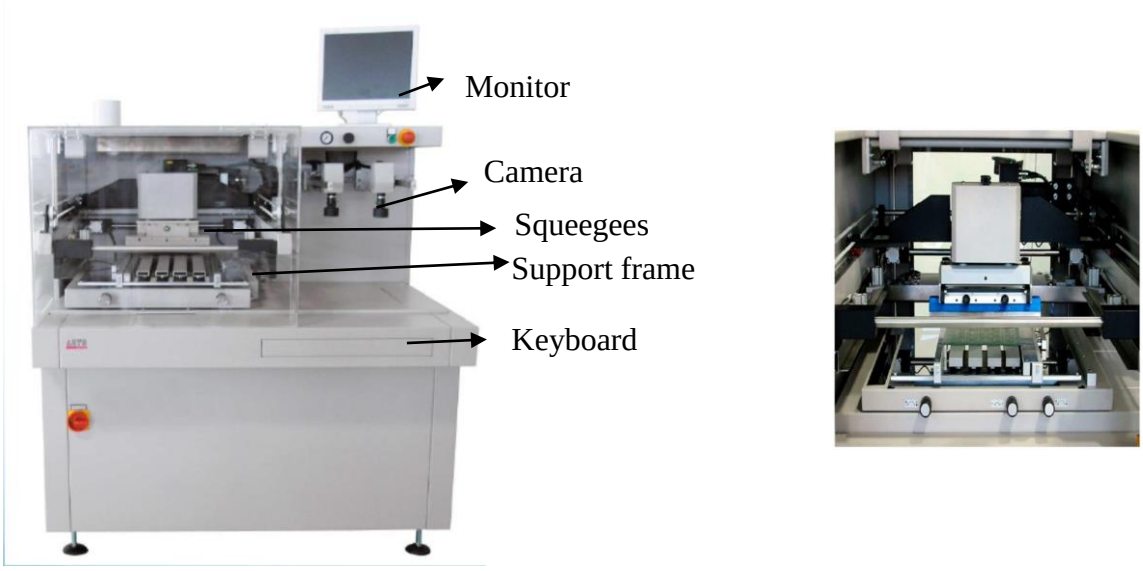


Figure 2.11: Photo of screen printing machine.

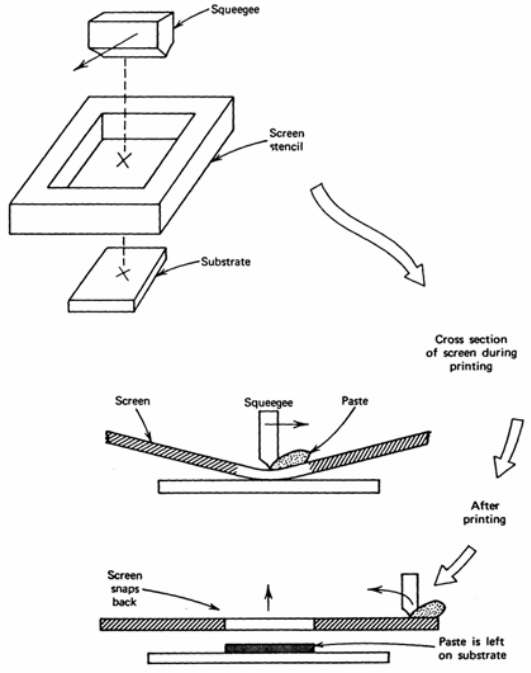


Figure 2.12: Operating schematic of screen-printing process [46].

In order to get high-quality and "perfect" thick films, it is necessary to establish a set of parameters for the screen-printing machine and materials, personnel and environment, and operation and metrics. Such a diagram is given in the following figure 2.13.

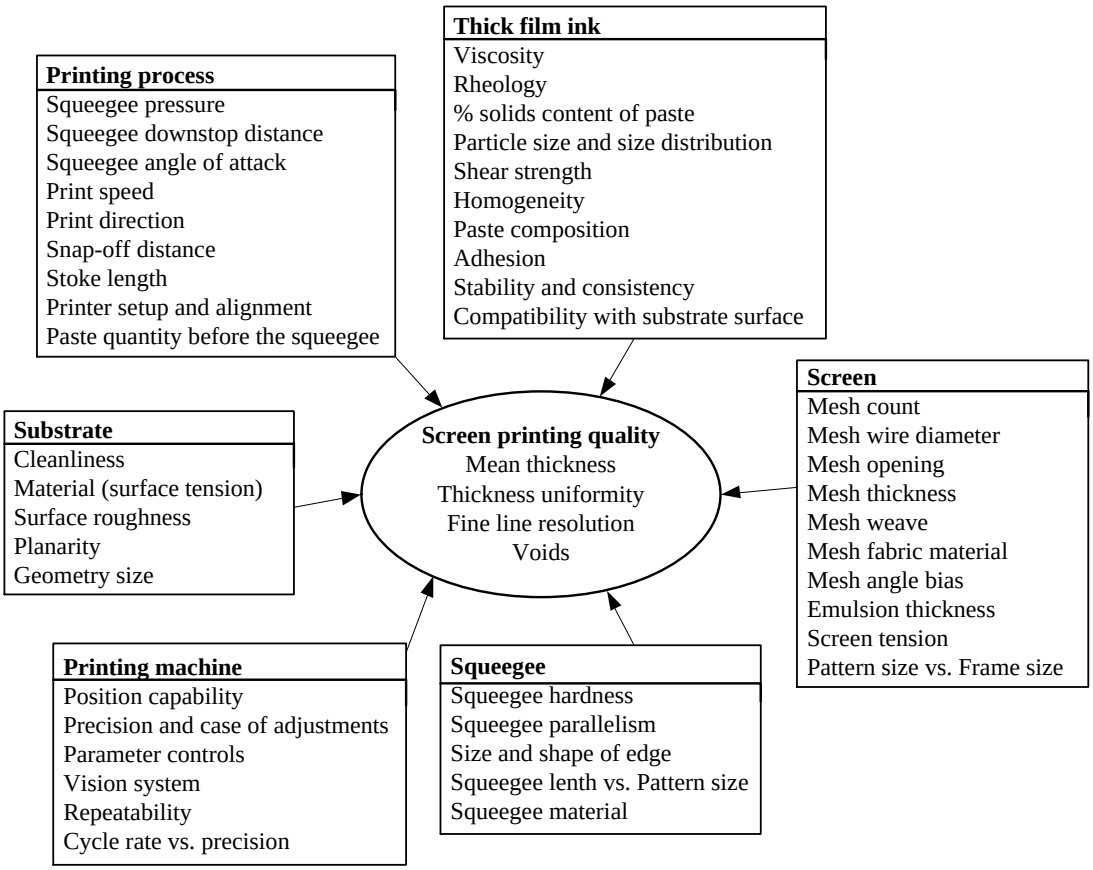


Figure 2.13: Factors leading to a good print (source [47]).

It is very important to design the right mesh screen and choose the right squeegee for each high quality print. Screen configuration and squeegee types are described in more detail in Appendix A.3 and Appendix A.4.

2.4.2 Drying and Sintering ovens

After material layers are deposited on the substrate, they are dried in a muffle oven (Figure 2.14(a)) to remove traces of the mesh from the surface of the thick film, as well as any amount of solvent residue in the ink.

Dried samples are then sintered in a Carbolite furnace (Figure 2.14(b)) according to a thermal cycle in figure 2.15 that includes peak firing temperature, dwell time at peak, and the rate of temperature ascent/descent. Sintering completely removes solvent from starting materials, and increases material quality with respect to levels of purity, uniformity, etc..

(a) (b)

Figure 2.14: (a) Drying oven, (b), Sintering oven.

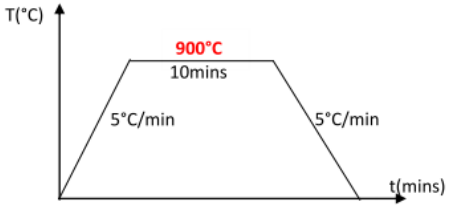


Figure 2.15: Sintering cycle.

2.4.3 Optimized SP machine operating parameters

Many variables affect print quality, such as the printer, nature of thick film inks, substrate, screen and squeegee parameters (print speed, hardness, squeegee pressure and snap-off distance). Dielectric ESL 4212 ink, conductive ESL 9916 ink, and 96% Alumina substrate are chosen in section 2.3. According to ink manufacturers, the screen mesh configurations suitable for these inks are 200/37.5μm for dielectrics and 325/25μm for electrodes. Squeegee choice is based on statistical results from design experiments (Table 2.5). After many experiments, the appropriate choice of squeegee parameters yielded dielectric films with smooth surface, low defects, and high quality electrodes with high resolution and good interconnections.

Table 2.5: Optimized squeegee parameters.

Squeegee	Color	Hardness (shores)	Angle (degree)	Pressure (bars)	Length (mm)	Snap-off (mm)
	White	30-35	45	200	250	0.3

2.5 Proposed process flow for passive integration

For fabricating multi-layer ceramic capacitors (MLCC), barium titanate-based ferroelectrics are usually used as dielectric layers because of their high and stable dielectric properties. Due to the high dielectric permittivity, organic insulating substrate could be used to manufacture embedded capacitors between conductive layers, and can be designed to form a sandwich structure between two silver layers. Nevertheless, it is also important to note that screen-printing also has some disadvantages, such as, because screen frames are durable, they can eventually become warped and uneven after being reused many times in a roll-to-roll process. Such problems have influences on the quality of dielectric layers, which become less uniform and show more defects. The optimized process, presented in Figure 2.16, mainly focused on removing defects in the dielectric to increase its breakdown strength while reducing the dielectric loss of the capacitor.

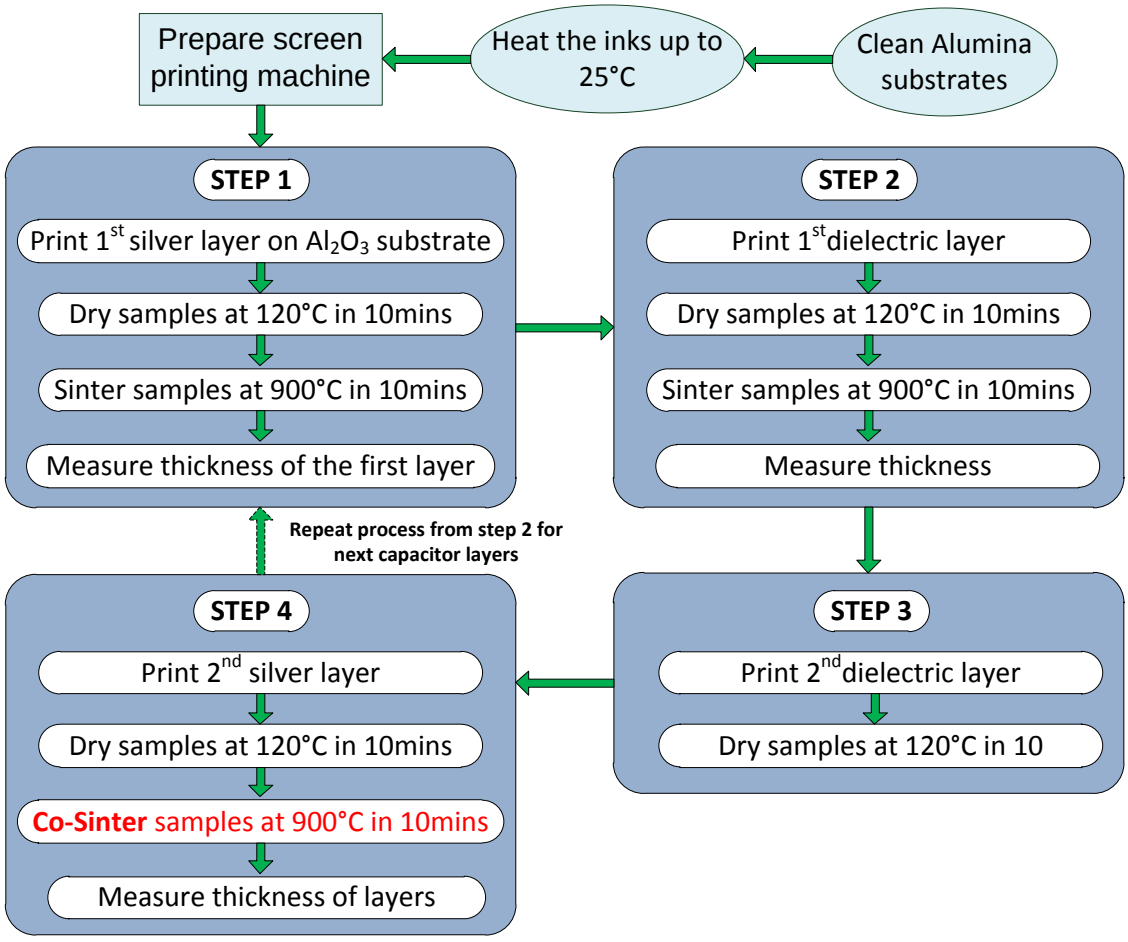


Figure 2.16: Summary of the process flow used to fabricate the different layers of the integrated capacitors.

2.6 Conclusions

In order to meet the requirements of practical DC-DC converters for a wide range of applications such as computers, mobile phones, and much more, their integration is a key issue covered in this study. In the context of integrated passive components, there are many opportunities for finding techniques and materials that offer a competitive price. The technologies reviewed in this chapter included LTCC, HDI, other PCBs and thin/thick film technology. All of these options have benefits as well as some drawbacks. Thick film technology based on the screen-printing technique (SPT) is the most appropriate selection for our work. SPT's process is relatively simple and does not require highly skilled labor. Lastly, it is very easy to print dielectric, conductive, or resistive thick film under normal conditions, whereas other technologies require precise conditions, such as lighting, operating under vacuum,…

In order to fabricate high capacitance values adapted to the screen-printing technique, the commercial ESL 4212 C ink was chosen. This ink offers high permittivity ranging from 2000 to 12000, high dielectric strength, and a low-sintering temperature (900^{o}C). A silver paste (ELS 9160), with high conductivity and chemical stability, is used for electrodes to avoid mechanical problems with dielectric layers during the co-firing process. Alumina (96%) substrates are used because of their high thermal stability and their smooth surface, allowing appropriate connections between layers.

To limit defects in dielectric layers, while increasing withstand voltage and reducing loss factor, an optimized process in which two dielectric layers are printed for each capacitive layer, is proposed. The first dielectric layer is printed, dried, and fired while the second dielectric layer is printed, fired, and then co-fired with the second electrode. This avoids short-circuit problems and increases the capacitor success level. The author used this process to fabricate many successful samples with a large number of different layers.

It is very important to have a precise idea of the parameters for the integrated capacitors in order to consider their compatibility for the purposes of a DC-DC converter. The characterization methods and measurement results of capacitance versus temperature and frequency, as well as leakage current and withstand, breakdown voltage are presented and discussed in the next chapter.

Chapter 3
Analysis and characterization of integrated capacitors

3.1 Introduction

Physico-chemical analysis and electrical characterization are tasks for understanding and developing the properties of the materials to use for capacitive integration. The goal of this step is to determine the appropriate application range for integrated ferroelectric capacitors that were fabricated successfully based on the process flow given at the end of Chapter 2 (Figure 2.16).

Integrated capacitors, from simple MIM (Metal-Insulator-Metal) capacitors to multilayer interdigitated capacitors, were characterized in order to evaluate their applied capabilities for different functions precisely, such as filtering, decoupling, and floating functions in DC-DC converters. At the beginning of this chapter, the methods for physico-chemical analysis and electrical characterization are described. The cross-section, microstructure, and chemical compositions of conductive and dielectric materials are observed and analyzed using a scanning electron microscope (SEM) or transmission electron microscope (TEM). The HP4191A impedance/gain-phase analyzer (40Hz-110MHz) was used to characterize main capacitor parameters, such as capacitance, impedance, ESL, ESR, SRF, while a probe station (Signatone) connected to a Keithley 2410 unit was dedicated to measuring leakage current and withstand/breakdown voltage. Capacitor temperature dependence is measured thanks to a temperature test chamber (Heraeus HT 7010) hosting the characterization cell connected directly to an HP 4284A impedance analyzer (20Hz-1MHz). Lastly, the measured results of integrated capacitors made from high permittivity dielectrics using the screen-printing process are presented and discussed.

3.2 Measurement methods

3.2.1 Physico-Chemical methods

The quality of the dielectric and conductive thick film determines the success of the capacitor. Integrated capacitors can reach higher breakdown voltage, lower parasite levels, and offer a longer lifetime during operating process in the circuit if there are fewer defects in dielectric layers and good interconnection conductive layers. Each material layer is screen - printed, dried, fired, and then observed and analyzed both physically and chemically using transmission electron microscopy (TEM) or scanning electron microscopy (SEM).

SEM is a type of electron imaging that only scans the surface of the sample (Figure 3.1(a)). SEM imaging captures secondary electrons and backscattered electrons in order to map an image. SEM is used to characterize surface morphology and particle size, and is used for elemental analysis in composition, as well as detection of composition contamination. In

our work, SEM is used to view cross-sections of deposition layers, microstructures, and thickness.

TEM is also a type of electron imaging, but a TEM scan transits through a sample (Figure 3.1.b). This makes it possible to see beyond the surface in particulate material samples. TEM provides details about internal composition. Therefore, TEM can show many characteristics of the sample, such as morphology, crystallization, stress, and even magnetic aspects. TEM is a high-resolution tool, able to provide high resolution analysis at the nano level. TEM used to measure nano particle size, grain size, crystallite size, atomic arrangement in material, and perform chemical and energy-dispersive X-ray (EDX) analysis [48].

a) Photo of SEM b) Photo of TEM

Figure 3.1: Photos of SEM and TEM.

The different MIM capacitor and interdigitated capacitor samples were prepared for observation and physico-chemical analysis following the process in Figure 3.2.

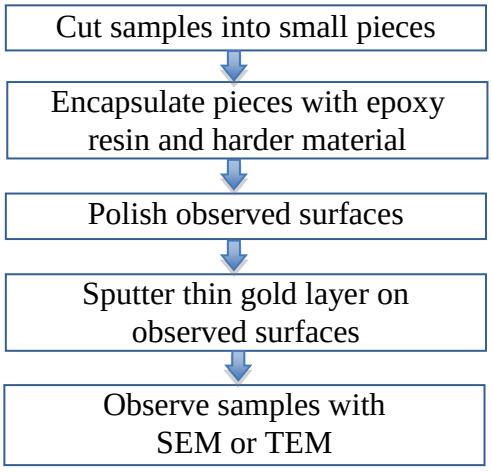


Figure 3.2: Flowchart for preparing samples for physico-chemical analysis with SEM/TEM

First, a cutting machine (Struers SECOTOM 10) cuts the various samples into small pieces, and then encapsulates these pieces into different packs, as shown in Figure 3.3 and Figure 3.4. The main observations and chemical analysis focus on the MIM capacitor sample

to evaluate dielectric properties, whereas physical analysis on interdigitated samples demonstrate the ability to build up multilayer configurations on integrated capacitors.

Figure 3.3: Photos and 3D configuration of integrated MIM capacitor.

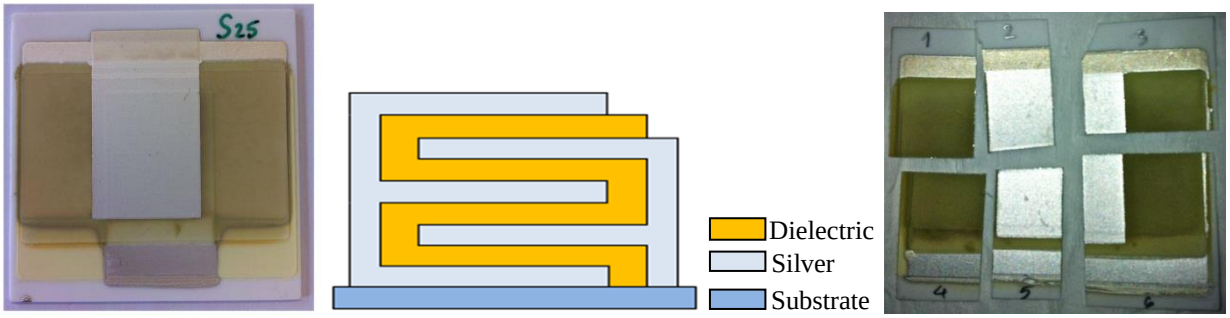


Figure 3.4: Preparation of interdigitated capacitor for SEM observation.

EDX analysis: Energy Dispersive X-ray Spectroscopy (EDS, EDX or XEDS) is a qualitative and quantitative X-ray micro analytical technique that can provide information on the chemical composition of a sample for elements with atomic number (Z) >3.

EDX uses of the X-ray spectrum emitted by a solid specimen bombarded with a focused beam of electrons to obtain a localized chemical analysis. Qualitative analysis involves the identification of the lines in the spectrum and is fairly straightforward owing to the simplicity of X-ray spectra. Quantitative analysis (determination of the concentrations of the elements present) entails measuring line intensities for each element in the sample and for the same elements in calibration Standards of known composition. By scanning the beam in a raster and displaying the intensity of a selected X-ray line, element distribution images or 'maps' can be produced. Also, images produced by electrons collected from the sample reveal surface topography or mean atomic number differences according to the mode selected [49], [50]. There are two main outputs of EDX analysis:

- ✓ *Spectrum*: displays a plot of the number of X-rays detected versus their energies. Characteristic X-rays form peaks superimposed on Bremsstrahlung X-rays. The Characteristic X-rays allow the elements present in the sample to be identified as illustrated in figure 3.5.

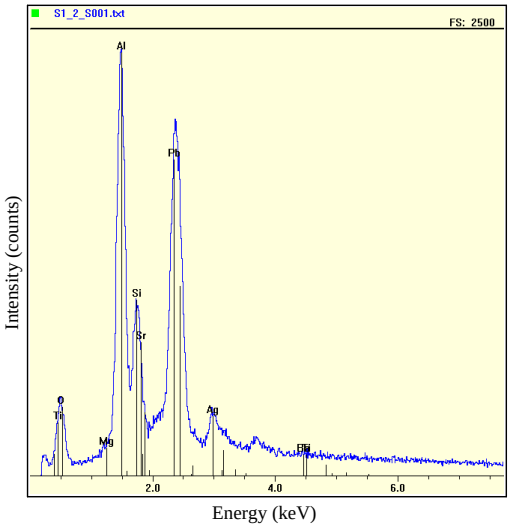


Figure 3.5: Line markers for Al, Si, Pb and Ag… lines in the ED spectrum.

✓ *Map*: an image showing how the concentration of one element varies over an area of a sample. An example in figure 3.6 presents EDX analysis of sample S: dark blue indicates concentration of Pb while green colors indicate concentrations of Ag and light blue colors reflect concentrations of Al.

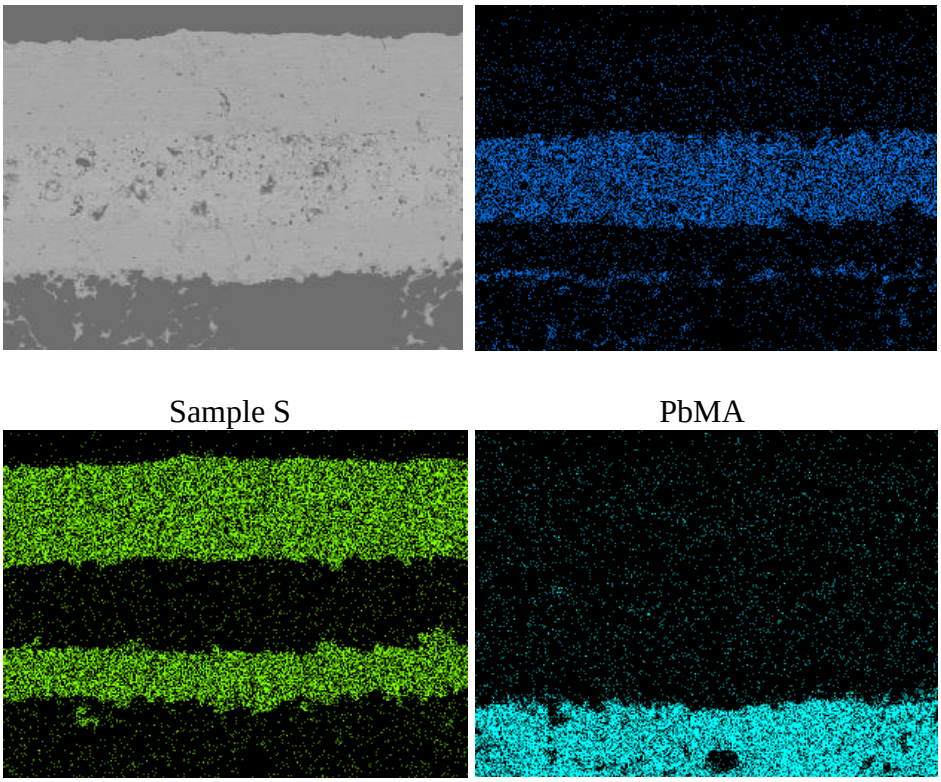


Figure 3.6: An example of map output of EDX analysis

3.2.2 Electrical characterization methods

This section presents some methods to measure a handful of the main parameters for different integrated capacitor samples, including capacitance value, dissipation factor, voltage rating, ESR, leakage current, DC bias and temperature dependence.

3.2.2.1 **Impedance measurements**

Frequency response of a typical capacitor

Figure 3.7 shows a typical equivalent circuit of a real capacitor in which C denotes the main capacitor element; Rs and L are the residual resistance and inductance existing in the lead wires and electrodes; Rp represents the dielectric loss of the dielectric material. The total equivalent circuit impedance presents the real and imaginary (resistive and reactive) parts in formula Eq.(3-1).

Parasitic inductance can be ignored in low frequency regions (<SRF). When the capacitor exhibits high impedance value, parallel resistance (Rp) is more significant than series resistance (Rs), thus a simpler parallel equivalent circuit including C and Rp can essentially replace the complex circuit model. Likewise, when the impedance is low, Rs is more significant than Rp, resulting in an approximate series equivalent circuit as in Figure 3.8. However, as the impact of inductance in the higher frequency region cannot be ignored, most capacitors are thus presented by using a series C-R-L circuit model as shown in Figure 3.9. Typical impedance (Z,θ versus f) behaviors in Figure 3.10 show the existence of L from the resonance point in the higher frequency region [51].

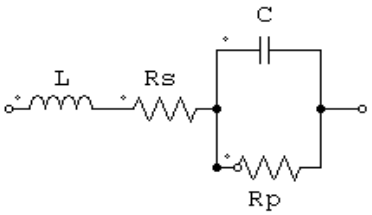


Figure 3.7: Equivalent circuit of real capacitor.

$$Z = R_s + \frac{R_p}{1+\omega^2 R_p^2 C^2} + j\frac{\omega L - \omega R_p^2 C + \omega^3 R_p^2 L C^2}{1+\omega^2 R_p^2 C^2}$$

Eq.(3-1): Impedance of a real capacitor.

$$C_s = \frac{-1}{\omega X} = \frac{-1-\omega^2 R_p^2 C^2}{\omega^2 L - \omega^2 R_p^2 C + \omega^4 R_p^2 L + \omega^4 R_p^2 L C^2} = \frac{C + \frac{1}{\omega^2 C R_p^2}}{1 - \frac{L}{R_p^2 C} - \omega^2 L C}$$

Eq.(3-2): Capacitance value in the series C-R-L mode.

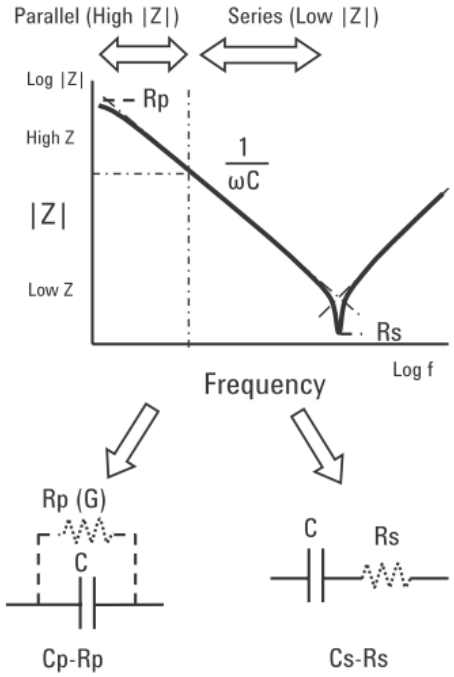


Figure 3.8: Simple equivalent circuit model of a real capacitor (source: Agilent technologies).

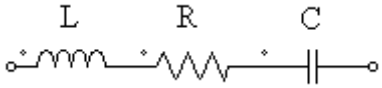


Figure 3.9: Simple series equivalent circuit of a typical capacitor.

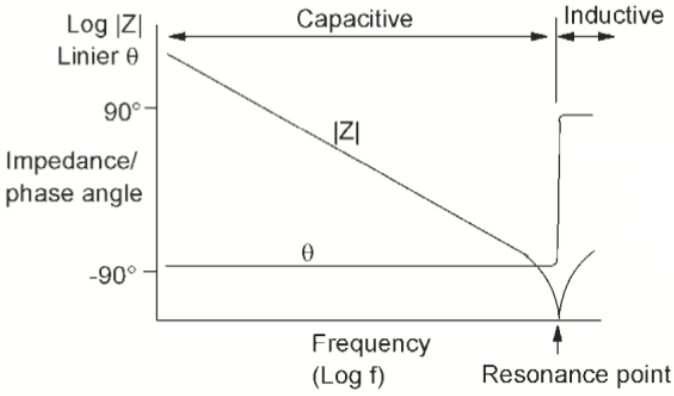


Figure 3.10: Frequency responses of typical capacitor (source: Agilent technologies).

Measurement method

Based on an auto-balancing bridge principle, the **HP4191A impedance/gain-phase analyzer** is an appropriate device for characterizing electrical properties of all the samples,

notably because this instrument provides wide frequency coverage from LF to HF (100Hz-40MHz) as well as high accuracy over a wide range of impedance values. As shown in Figure 3.11, samples are connected directly to the HP4191 to eliminate undesired inductance parasites when connecting with a long cable. This instrument is composed of three main section blocks: signal source, vector ratio detector, and auto-balancing bridge. The operating principle of each block provided by the manufacturer, Agilent, is illustrated in Appendix B.

Figure 3.11: Photos of an Agilent-HP4191 gain/phase impedance analyzer.

3.2.2.2 **Leakage current**

The causes of leakage current

When applying DC voltage to a capacitor, the current increases suddenly. As the capacitor is charged gradually, the current decreases exponentially as shown in Figure 3.12.

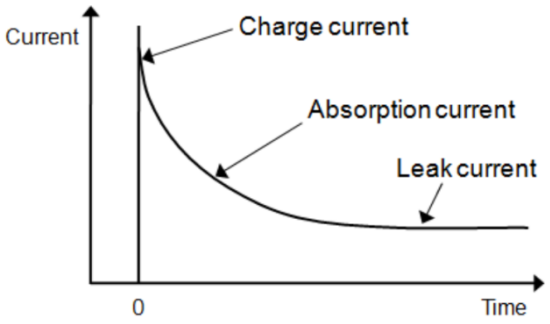


Figure 3.12: The current over time when applying DC voltage to a capacitor.

Current I(t) flowing after time t is divided into three types: charge current $I_c(t)$, absorption current $I_a(t)$, and leakage current I_r.

$$I(t)=I_c(t)+I_a(t)+I_r$$

Charge current indicates the current flowing through an ideal capacitor. Absorption current flow is delayed with respect to the charge current and corresponds to the displacement current associated to all the polarization mechanisms able to exist in the material (from electron polarization to interfacial mechanisms like those due to the Schottky barrier that occurs at the interface between the ceramics and the metal electrodes. Leakage current is a small constant current, in the region of nano-amps (nA) and below, flowing through the dielectric after a certain period of time when the influence of absorption current diminishes. The appearance of this current is due to the effects of the electric field developed by the charge on the plates and defects in the dielectric material. The leakage current is generally associated to as "insulation resistance" (R= U/I). The value of the flowing current varies depending on the amount of time that voltage is applied to the capacitor. This means that the capacitor's insulation resistance value cannot be determined unless the timing of the measurement after applying voltage is specified.

Measurement method

The value of the leakage current is measured versus the applied DC voltage, at room temperature (25°C), using a Keithley 2410 Electrometer of the connections being realized thanks to the Signatone probe station. The capacitor connects in series to the instrument as shown in Figure 3.13, and constant voltage is applied. The resulting current is then measured. The leakage current decays exponentially over time, so it is necessary to apply the voltage for a known period of time (the polarization time) before measuring the current. For this test, leakage current behavior is determined for a time of 120 seconds, with each fixed voltage level from 10V to 130V.

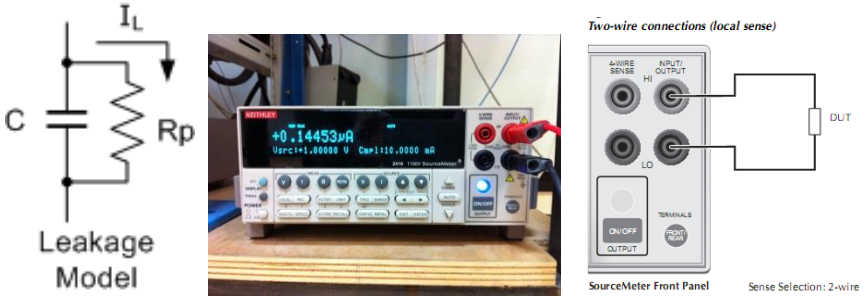


Figure 3.13: Keithley 2410 SourceMeter front panel.

3.2.2.3 **Withstand and breakdown voltage**

The causes of breakdown voltage

All capacitors have a maximum operating voltage that depends on the type of dielectric material used and its thickness. Rating voltage is the voltage that can be applied to the capacitor without damaging its dielectric material. If the voltage is beyond the dielectric strength, failure may result and a short circuit occurs. The origins of breakdown are due to different kinds of mechanisms occurring in the dielectric like:

- Intrinsic breakdown of the material occurs when the electric field is sufficiently high to ionize an atom in the dielectric (or accelerate a stray electron sufficiently to do the same), with the resulting new free electrons then being accelerated by the field to repeat the process with another atom. If more free electrons are produced than reattached, the process grows exponentially and results in breakdown.
- If there are voids, porosities, cavities or defects in the dielectric material, the residual gas in the voids breakdown at a lower electric field value (again an electron avalanche), and the freed electrons strike the sides of the void, heating the dielectric and eroding it. This type of discharge is small and perhaps unnoticeable, but with enough time, the void would grow and eventually destroy the dielectric [52].

Withstand voltage tests can be performed to avoid destroying the capacitor and is considered as the rating voltage whereas **breakdown voltage** is the voltage at which the failure occurs. The former test is *non-destructive*, the latter is *destructive*.

Measurement method

Breakdown and withstand voltage for a large number of samples were measured using the same experimental setup composed of a Keithley 2410 SourceMeter instrument (1100V, 1A, 20W) connected to a Signatone probe station support, as presented in figure 3.14.

(a) (b) (c)

Figure 3.14: Experimental setup for withstand and breakdown voltage test: (a),(b) connection of the SourceMeter Keithley 2410 to the Signatone probe station support ; (c) connection of the sample to Signatone probe station support.

NON-DESTRUCTIVE TEST (withstand voltage test)

In this study and arbitrarily, the withstand voltage is determined by applying a step DC voltage during 120s and if no failure is observed, by increasing its value of 10 V, until first flashover occurs (see figure 3.15). The value immediately before the failure is considered as the withstand voltage.

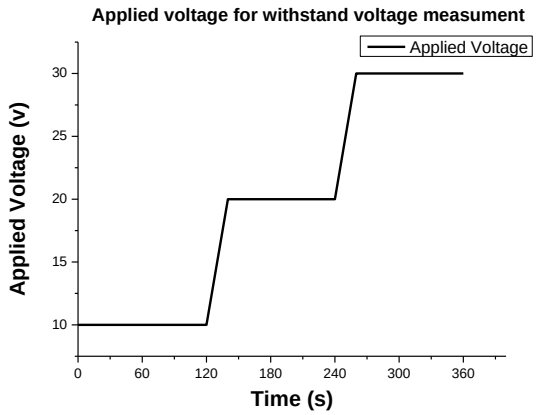


Figure 3.15: Applied voltage ramp used to determine the withstand voltage

DESTRUCTIVE TESTS (breakdown voltage tests)

In a breakdown test, DC voltage is applied at a controlled ramp rate of 10 Volts per second until failure occurs as shown in figure 3.16. It is important to note that the realized capacitors may present a self-healing mechanism allowing the voltage to be re-applied once the weakest part of the sample has been destroyed. For this reason, when such an event occurs the capacitance value is measured.

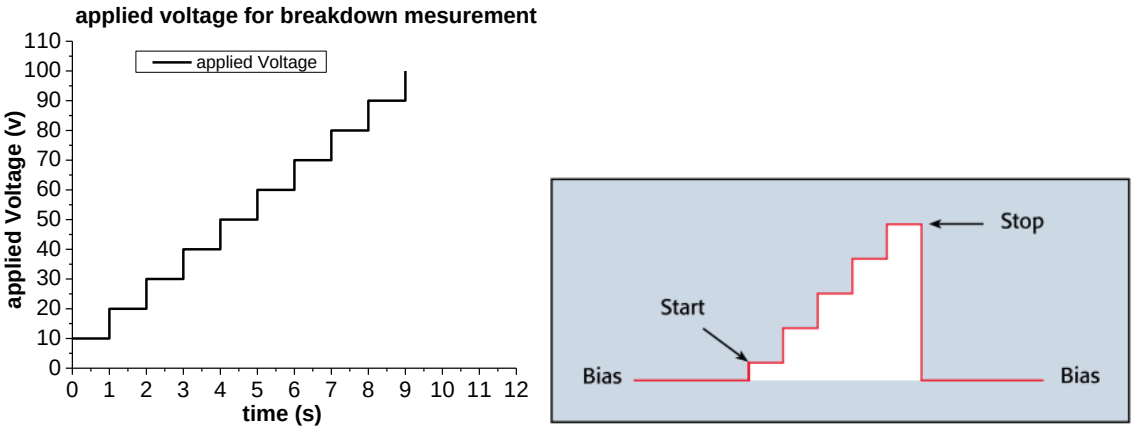
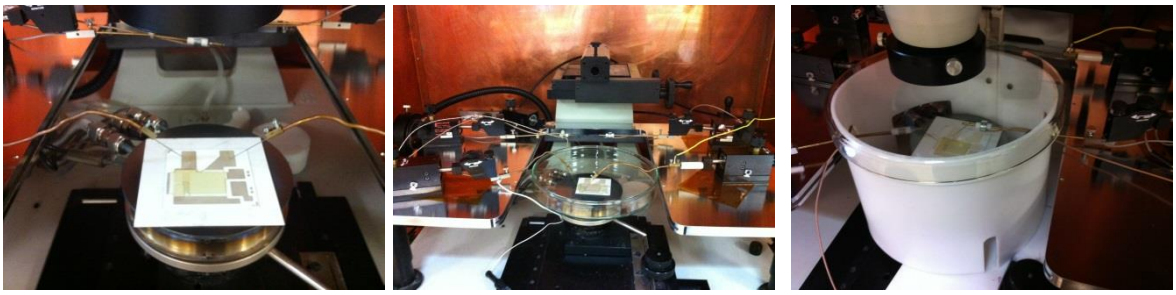


Figure 3.16: Controlled ramp rate of voltage increase during breakdown test

Breakdown voltage first tested in an open-air environment, as shown in Figure 3.17 (a). Then, to avoid flashover, capacitors were tested in FC-72 insulating liquid as shown in Figure 3.17 (b). Lastly, the influence of temperature on the dielectric strength was evaluated on several capacitors at temperatures varying from 25°C to 100°C, as in Figure 3.17 (c).



(a) In the air. (b) In FC-72 liquid (c) When temperature changes

Figure 3.17: Experimental set-up for breakdown voltage test.

3.2.2.4 **Temperature and DC voltage dependency**

For the ferroelectric ceramic materials like the one studied here, changes of the temperature or of the polarization voltage (DC Voltage as long as it is lower than the breakdown voltage) produce, a significant variation of the capacitance value because of the related changes in the dielectric permittivity.

The temperature dependence is related to the crystallographic phase of the material. For temperature lower than the Curie-Temperature (Tc), the material is in ferroelectric phase and the permittivity increases with the temperature. For temperature larger than Tc, the material is in its paraelectric phase and the permittivity decreases when the temperature increases [53].

The voltage dependence is related to the hysteresis and non-linearity in the relation between the polarization P and the applied electric field in ferroelectric materials. It appears in a "butterfly" phenomenon when plotting the changes in the capacitance versus voltage (figure 3.18). Such an effect may be interesting for resonant inverters or snubber circuits but is detrimental when a constant behavior is desired.

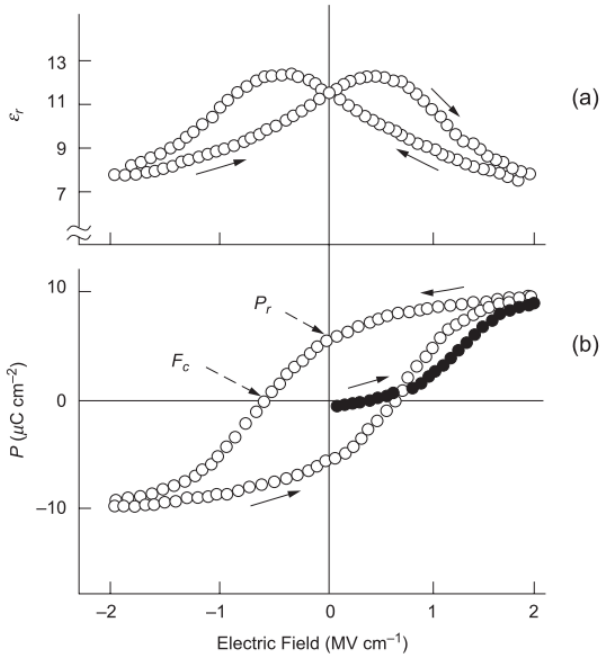


Figure 3.18: The variation of (a) dielectric constant and (b) polarization of b-phase ferroelectric films with applied electric field. ● Initial poling, ○ subsequent poling cycles

Measurement method

An HP 4284A impedance analyzer (20Hz-1MHz, DC voltage ± 30 V) connected to a temperature test chamber/Heraeus HT 7010 oven and a computer, as shown in Figure 3.19, was used to characterize the temperature responses of integrated capacitors.

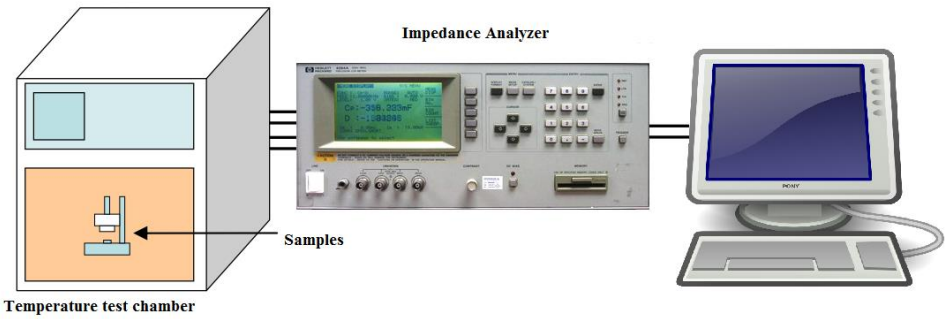


Figure 3.19: Temperature dependence measurement.

The samples are placed inside the oven and are connected to the impedance analyzer via a 1m long cable. Using computer software to control temperature changes inside the oven gradually increased from -50°C to 200°C. The impedance analyzer can automatically measure

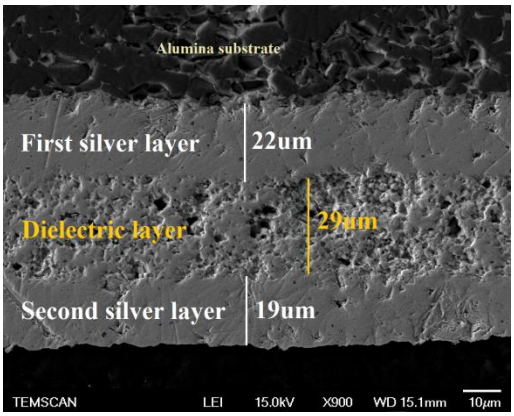
capacitance and losses behaviors as a function of both frequency and temperature at each different temperature level. DC behavior is only determined at room temperature, the DC voltage varying linearly from 0 to 30V and then from 30 V to -30 V.

3.3 Results and discussions

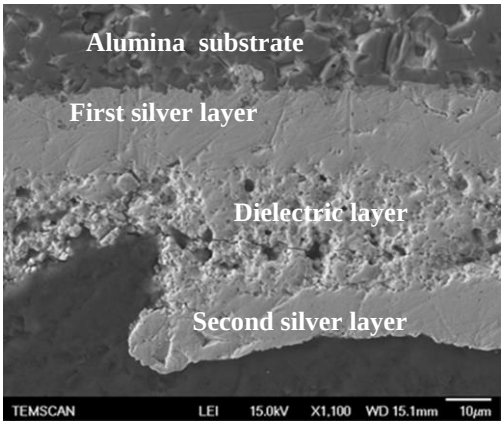
3.3.1 Physico-chemical analysis

3.3.1.1 MIM capacitors

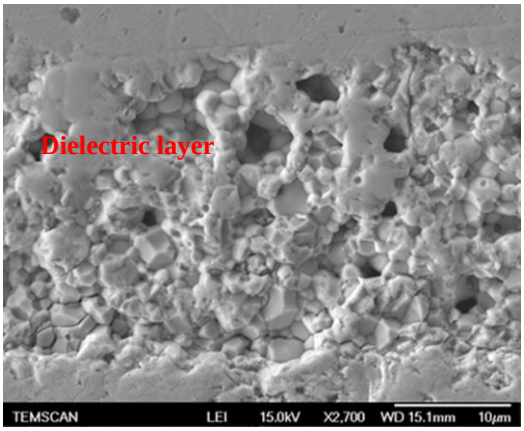
The MIM capacitor's microstructure is shown in Figure 3.20(a) and (b). The thicknesses ranges from 15-25µm and 25-35µm for silver electrodes and the dielectric layer, respectively. Grain morphology of the dielectric layer in Figure 3.20(c) demonstrates the uniformity of two dielectric layers without distinctive delamination, although they are fabricated in different ways. It also can be seen that there is no diffusion between the second dielectric layer and second silver layer, although they are co-fired. This can eliminate the risk of premature failure during capacitor operation.



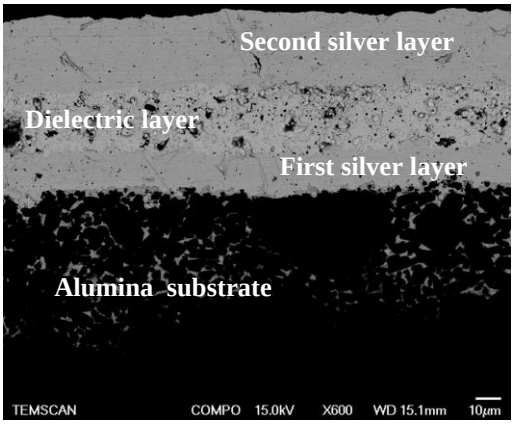
a) MIM capacitor microstructure.



b) The edge of second silver electrode.



c) Particle morphology of dielectric layer.



d) Diffusion in the alumina substrate.

Figure 3.20: TEM observation of MIM capacitor.

A COMPO scan mode for TEM in Figure 3.20 (d) shows a low amount of material diffusion into the alumina substrate. Energy-dispersive X-ray (EDX) inspection was implemented at six different points (see Figure 3.21) on the sample to determine the main chemical composition and the kind of the material diffused into the alumina substrate. EDX examination in Figure 3.22, from point 1 to point 6, shows the main chemical composition matched to data provided by manufacturers. A small amount of lead in the dielectric layer is seen diffusing into the alumina substrate in Figure 3.22(f). This diffusion is also confirmed in the image set report for the EDX mapping analysis shown in Figure 3.23(j). The consequences of such diffusion on the assembly's breakdown voltage would have to be studied further if the values obtained, or the location of the breakdown, appear unrealistic (failure of the substrate instead of failure of the dielectric material).

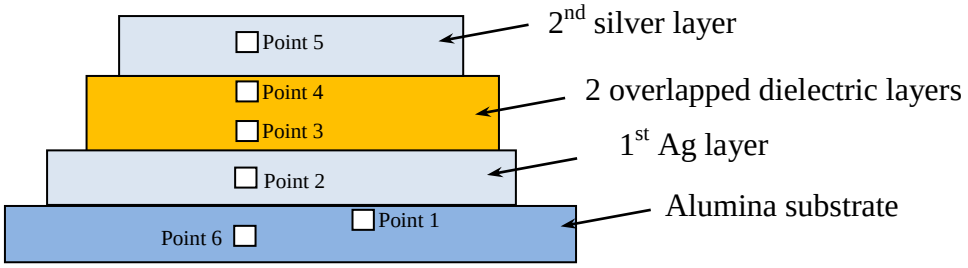
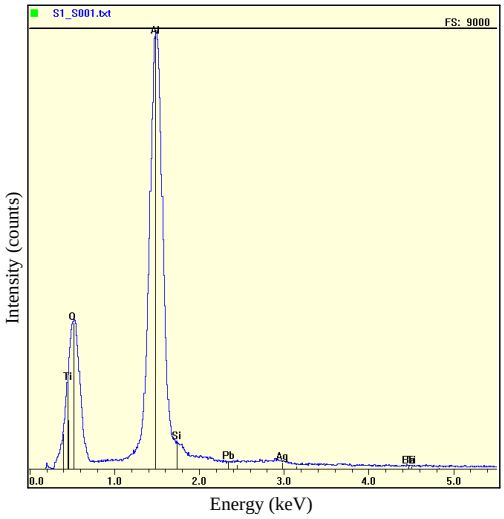
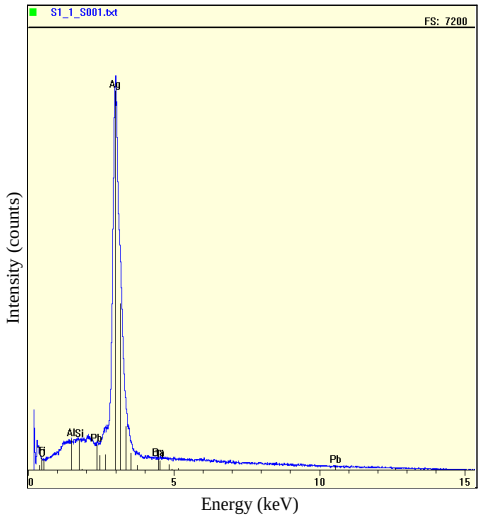


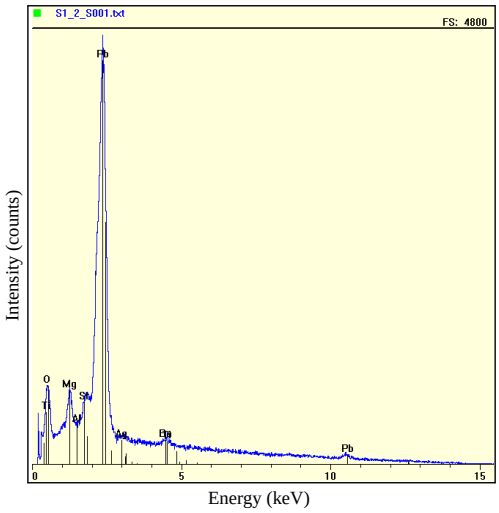
Figure 3.21: Six points location for EDX analysis of the MIM capacitor.



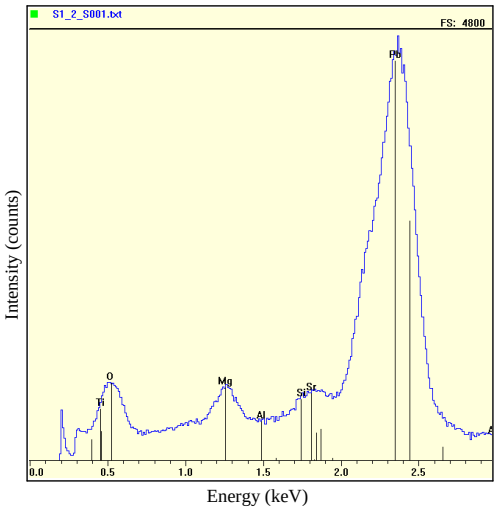
a) Point 1 (Alumina substrate).



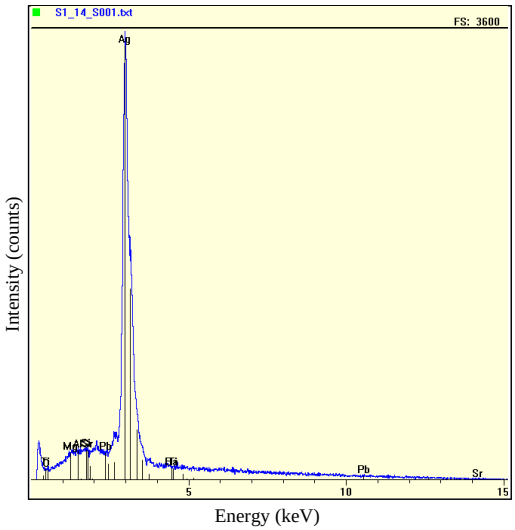
b) Point 2 (first silver layer).



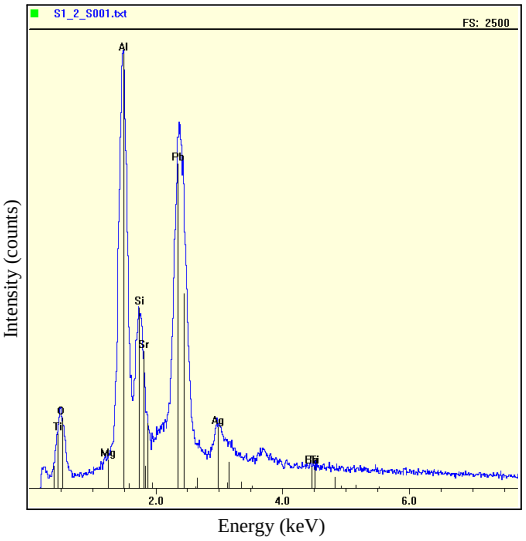
c) Point 3 (first dielectric layer).



d) Point 4 (second dielectric layer).



e) Point 5 (second silver layer).



f) Point 6 (lead diffusion)

Figure 3.22: The main chemical composition of six different points in the capacitor.

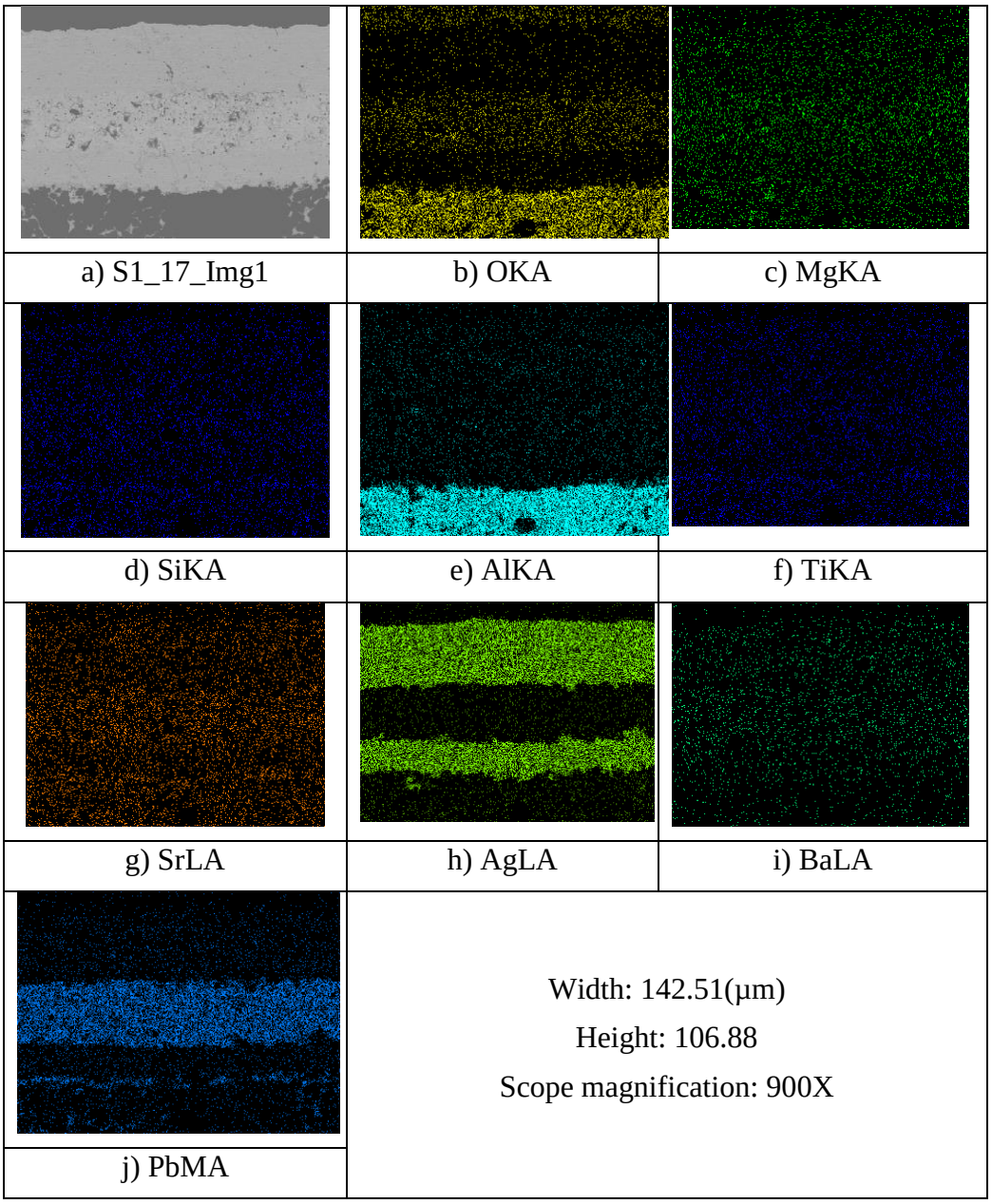
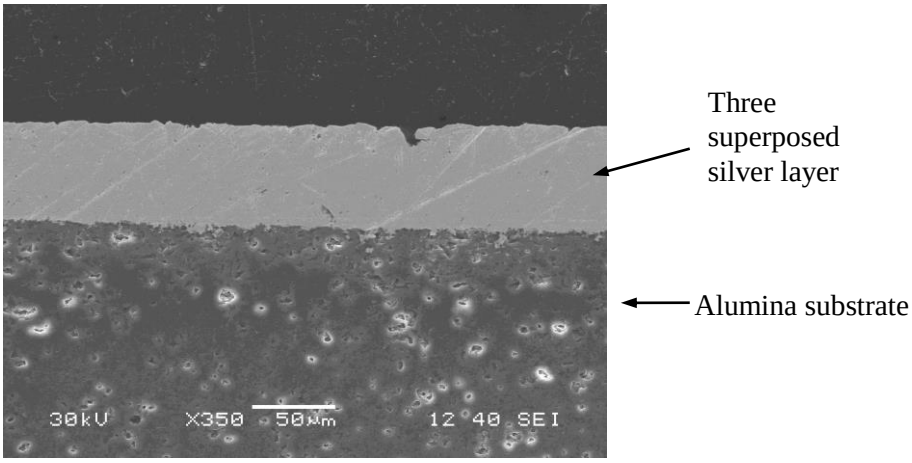


Figure 3.23: Image set report of capacitor mapping by TEM.

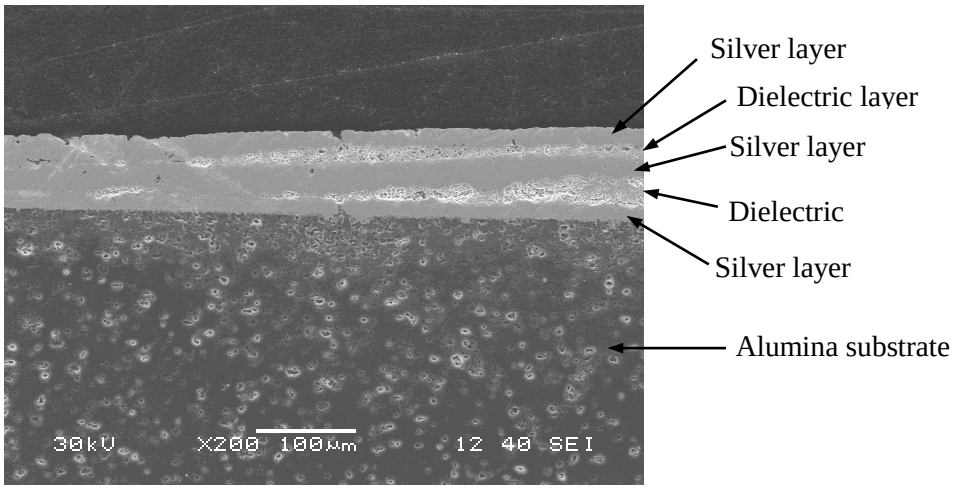
3.3.1.2 **Interdigitated capacitors**

The interdigitated capacitor (figure 3.4) was developed from a MIM capacitor to determine the potential for establishing multilayer capacitors. Figure 3.24 (a) shows very good interconnection between the different silver electrodes, while Figure 3.24(b) illustrates enabling stack configuration in interdigitated capacitors. The grain morphology image in

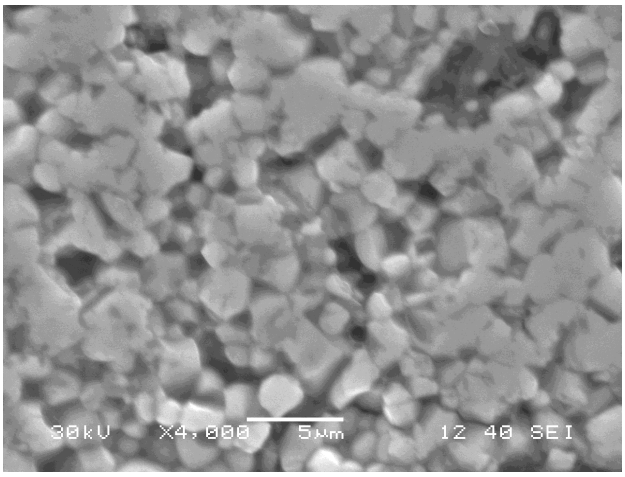
Figure 3.24(c) presents unchanged microstructure of the dielectric layer with respect to MIM capacitors. Thus, the interdigitated capacitor can be realized entirely by the screen-printing technique and thick-film material pastes.



a) Interconnection of silver layers.



b) Construction of the 2-layers capacitor.



c) Particle morphology of dielectric

Figure 3.24: SEM photos of 2-layer interdigitated capacitor.

3.3.2 Electrical characterizations

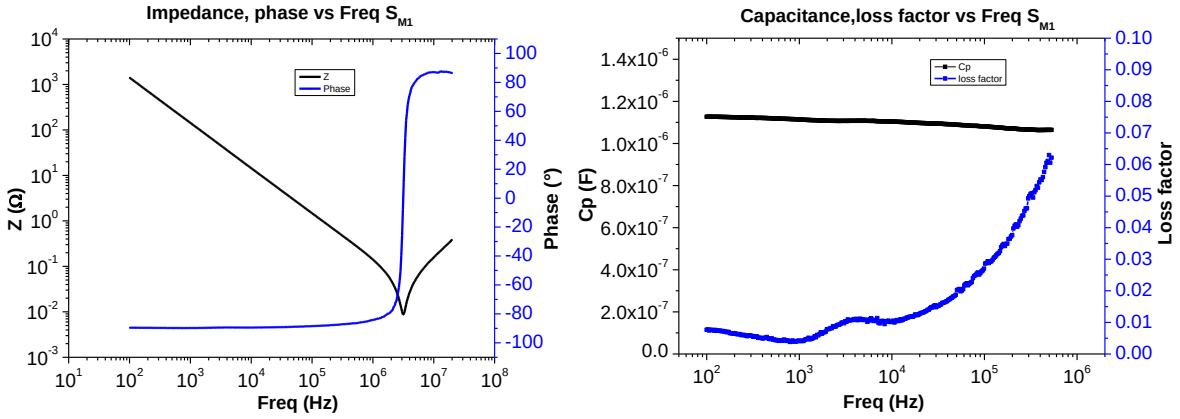
3.3.2.1 Frequency dependence

MIM capacitors (Sign S_{Mn}; M mean MIM; n is the sequence number of sample)

In the first stage, electrical characterization focused on the MIM capacitors to evaluate all the behaviors of dielectric material over a wide range of frequencies.

Frequency responses of MIM capacitors S_{M1} in Figure 3.25 (a) show that impedance in regions from low frequency to self-resonant frequency (SRF), around 1MHz, decreases inversely with frequency. At the SRF point, ESR may be determined. As frequency rises above SRF, the element characteristic changes from the capacitive behavior to the inductive behavior.

The MIM capacitor, with effective area of 33mm x 19mm, presents a high capacitance density (1.9nF/mm^2 for a dielectric thickness of 30µm) and a low dissipation factor, as plotted in Figure 3.25 (b). The capacitance density allows calculating the dimensions of the filtering and decoupling capacitors based on required capacitance when designing capacitive substrate later in Chapter 5.



a) Impedance and phase behaviors. b) Capacitance and dielectric loss factor behaviors.

Figure 3.25: Frequency responses of MIM capacitor.

The permittivity of four MIM capacitors, plotted in Figure 3.26(a), remains nearly constant in the low frequency region and it declines quickly with increasing frequency. The chosen dielectric material can reach a high permittivity value (nearly 10,000) and enables the implementation of high capacitance density components for different applications in power electronics. Thus, it can be seen that the process and co-sintering treatment have a positive impact on the dielectric properties.

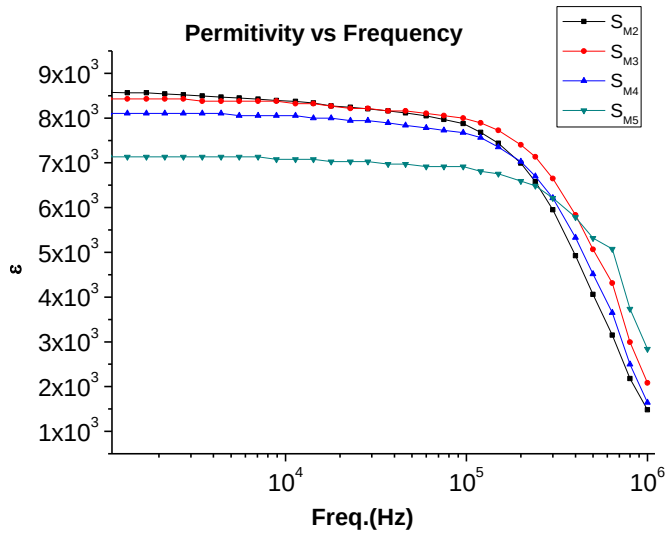


Figure 3.26: Permittivity behaviors of four MIM capacitors as a function of frequency

MIM capacitors in series (S_{MSn})

In the next stage, the MIM capacitors were developed into multilayer capacitors in series S_{MS11} and S_{MS12}, as shown here:

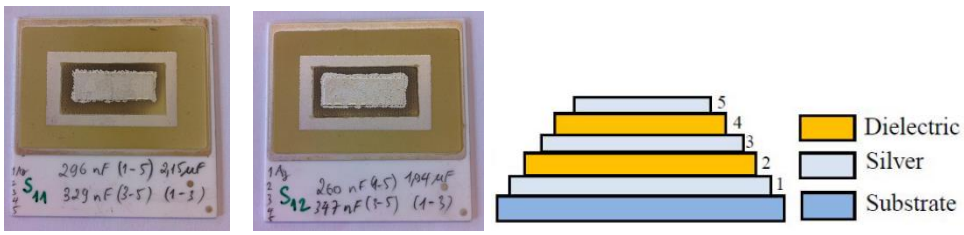
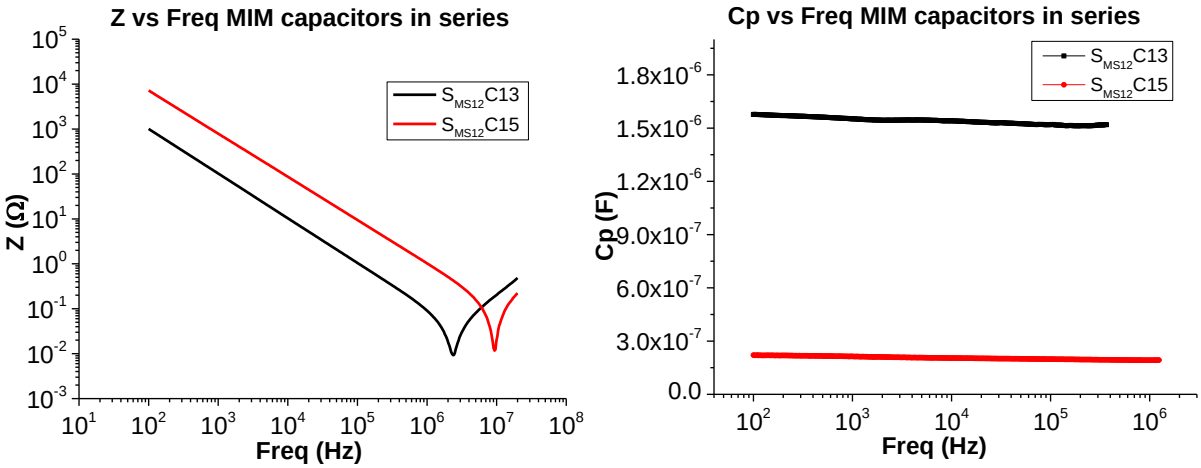


Figure 3.27: Photos and configuration of MIM capacitors in series.

The sample presented in Figure 3.27 includes capacitor C_{13} and C_{35} in series. The equivalent multilayer capacitor is thus $C_{15}=C_{13}C_{35}/(C_{13}+C_{35})$. The parameters of the capacitor C_{13} and C_{15} are compared in Figure 3.28. It is clear that there is a decrease in the capacitance value with a shift in the resonant frequency (the ESR being nearly the same) from 3MHz to 5MHz. However, such a design is limited in shape and configuration for building up multilayer capacitive substrate.



a) Impedance behaviors. b) Capacitance behaviors.

Figure 3.28: Frequency responses of MIM capacitors in series.

Interdigitated capacitors (S_{MIn})

In a third stage, stacked capacitive layers are intended to create the multilayer structure and increase the capacitance value of MIM capacitors (see Figure 3.3). Comparing impedances of a simple MIM capacitor S_{M6} and a multilayer intedigitated capacitor S_{MI1} (Figure 3.29) proves that the quality of the interconnections between electrodes makes it possible to establish a multilayer capacitor, and demonstrates the role of interdigitated layers on the capacitance value. Increasing the number of capacitive layers produces an increase in capacitance.

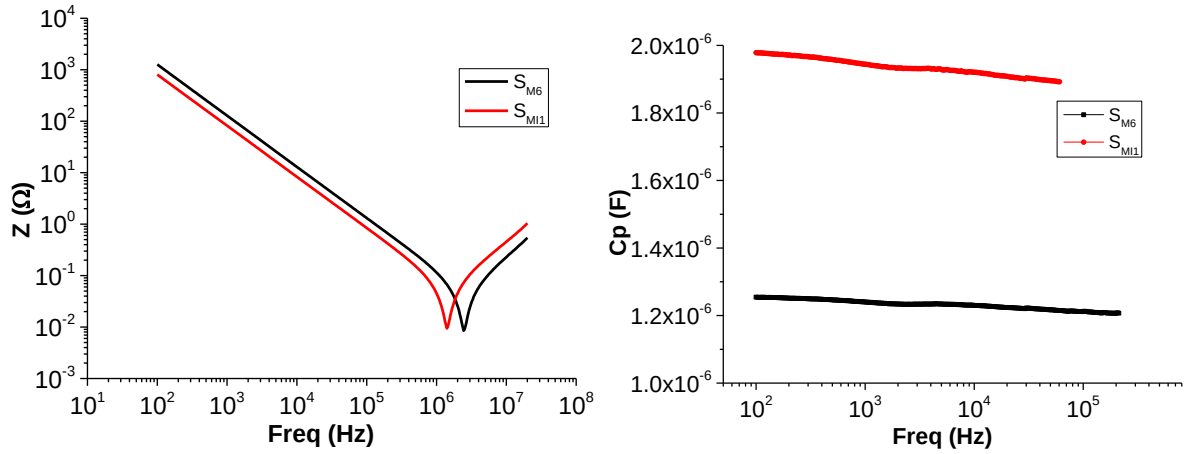


Figure 3.29: Frequency response comparison between MIM capacitor (S_{M14}) and interdigitated capacitor (S_{MI25}).

The electrical characteristics of MIM and interdigitated capacitors were collected in Table 3.1, in which SRF, C, D, ESR are determined from impedance and capacitance

measurements as a function of frequency. ESL that is considered as inductance at SRF is estimated by the following formula:

$$L = \frac{1}{(2\mu . F_0)^2 C_0}$$

Where:
- L is the estimated ESL (H)
- F_0 is the self-resonant frequency (Hz)
- C_0 is the capacitance value at the self-resonant frequency (F)

According to the data in Table 3.1, integrated capacitors present a very low value of equivalent series resistance (ESR) and equivalent series inductance (ESL). These factors are particularly important in electronic designs: a capacitor's ESR is responsible for dissipated energy. ESR may not be a problem when dealing with low current values. However in high-power structures where current levels are high, the power dissipated due to ESR may result in a significant increase in temperature. This parameter must be taken into account when designing the capacitor to avoid undesired problems and to increase reliability. Moreover, it is generally found that when the temperature of a capacitor increases, ESR increases, although non-linearly. Increasing frequency also has a similar effect. The ESL of any given capacitor is more related to its physical size and geometry than to anything else. A capacitor with a larger capacitance almost always has a larger inductance than a smaller version of the same type of capacitor. The lead length is usually, by far, of greater importance for high frequency operation. It is noticeable that the equivalent series inductance (ESL) of capacitors is detrimental to their high frequency (HF) performance. Minimizing ESL to significantly improve a capacitor's HF filtering performance is very important for noise suppression and current ripple reduction in power electronics applications.

Table 3.1: Parameters at SRF of integrated capacitors.

Capacitor name	**SRF (MHz)**	**C (F)**	**D**	**ESL (nH)**
S_{M1}	3.02	1.13	1.93	**2.46**
S_{MS12} C13	2.29	1.58	3.13	**3.06**
S_{MS12} C15	6.91	0.221	1.41	**2.40**
S_{M6}	2.36	1.25	1.7	**3.64**
S_{MI1}	1.36	1.98	2.22	**6.92**

3.3.2.2 **Leakage current**

The next consideration focuses, in particular, on the leakage current I_L of these integrated capacitors. Good insulation resistance (derived from leakage current and applied voltage ($R_{Is}=V/I_L$)) is necessary for capacitors used for blocking off DC voltage and/or for storing electromagnetic energy where a particular voltage rate must remain unchanged for a long period of time. In the simple case, the leakage current I_L of a ferroelectric MIM capacitor S_{M2} depends on the applied voltage. The curve presented in figure 3.30 shows the changes in the polarization current during the first 200 seconds following voltage application. Its magnitude is in the nano Ampere range and tends rapidly to a constant. The leakage current versus the applied voltage $I_L(V)$ extracted from the previous I(t) graph in Figure 3.31 shows a high insulation resistance value (in the Giga Ohms range).

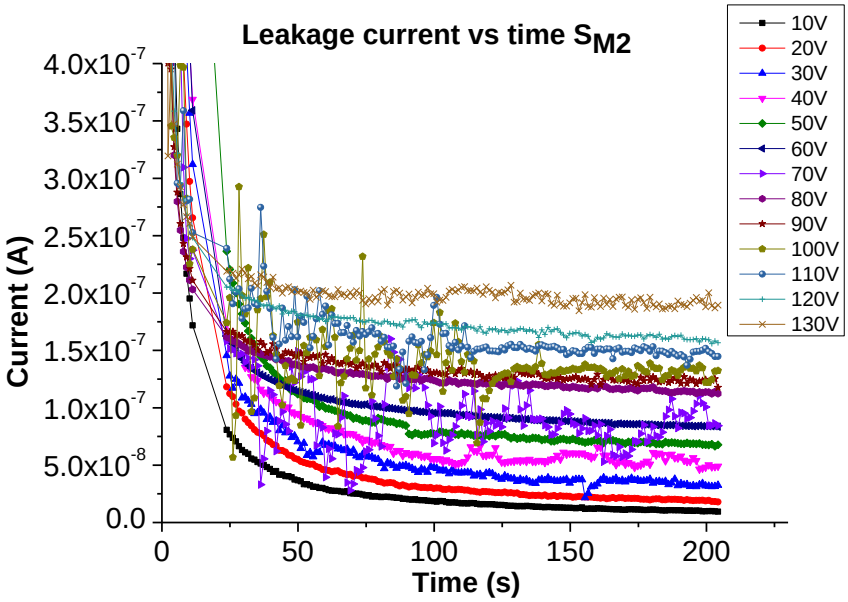


Figure 3.30: Leakage current of MIM capacitor S_{M2}

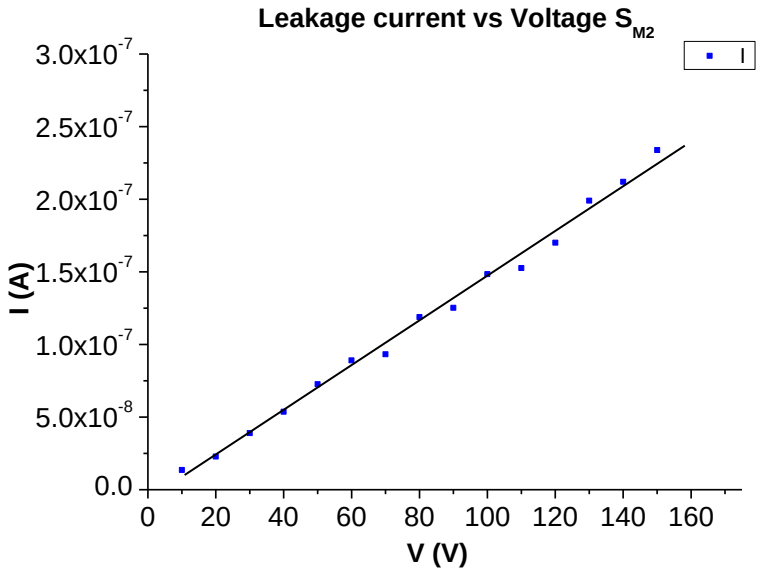


Figure 3.31: Leakage current and I-V characterization.

3.3.2.3 **Withstand voltage and breakdown voltage measurements**

The consideration examined here concentrates on the capacitor's withstand and breakdown voltage. Withstand voltage testing was performed on two MIM capacitors S_{M7} and S_{M8} in FC-72 at room temperature. The results given in Table 3.2 show that the threshold of integrated capacitors can reach over 300 Volts under DC stress. Limit current is set for Keithley 2410 SourceMeter is 1mA.

Table 3.2: Withstand voltage test of MIM capacitors.

Name	U (V)	I (µA)	Result	C(µF)
S_{M7}	200		Ok	
	300		Flashover	
	400	$>I_{Limit}$	Flashover	1.9
S_{M8}	200	Low	Ok	
	300	0.7	Ok	
	400	$>I_{Limit}$	Flashover	1.26

Breakdown voltage test

Destructive tests are performed on samples composed of the first silver electrode and a dielectric layer implemented according to the same process described earlier in Chapter 2. Seven small diameters of "second electrodes" are created by silver evaporation on top of the dielectric surface. They are illustrated in figure 3-32

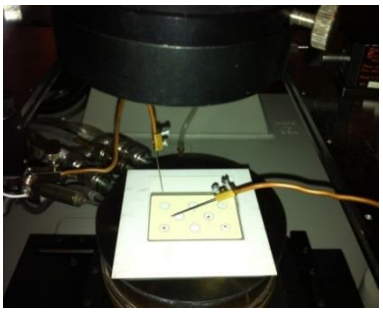


Figure 3.32: Samples for the breakdown voltage tests

The results given in Table 3.3 show that the dielectric layer's ability to withstand voltage is better in the liquid insulator (FC-72) than in open air. This is mainly due to the fact that the geometry used favors flashover. Therefore, in order to improve the withstand voltage without the help of a liquid, a specific dielectric layer (passivation) must be screen-printed. This capacitor behavior in FC-72 is noted when implementing the multilayer capacitive substrates in Chapter 5. Measured results also illustrate that the breakdown voltage declines remarkably when the temperature rises higher than room temperature. Thus, it should be noted that a proper cooling strategy is required for capacitors in electronic designs seeking to extend their useful life.

Table 3.3: Breakdown voltage test results.

Sample	Point	Temp	V_{BD} (V)	Note
S_{M9}	1	22	545	Air
S_{M9}	2	22	>600	Air
S_{M10}	1	22	472	Air
S_{M10}	2	22	558	Air
S_{M10}	3	22	388	Air
S_{M10}	4	22	>600	FC-72
S_{M10}	5	22	>650	FC-72
S_{M10}	6	22	304	FC-72
S_{M11}	1	22	521	FC-72
S_{M11}	2	22	>700	FC-72
S_{M11}	3	22	587	FC-72
S_{M9}	3	50	558	Air
S_{M9}	4	50	582	Air
S_{M11}	4	50	424	Air
S_{M11}	5	50	406	Air
S_{M11}	6	50	358	Air
S_{M11}	7	50	436	Air
S_{M9}	5	100	578	Air
S_{M9}	6	100	396	Air

3.3.2.4 **Temperature dependence**

Thermal stability is one of the major limiting factors for capacitor applications. The dielectric properties of MIM capacitors were therefore also measured as a function of temperature, as shown in Figure 3.33. Due to the nature of the dielectric used, and not surprisingly, capacitance tends to increase with the temperature until the Curie temperature is reached – the point at which capacitance is its maximum due to a phase transition. Its value approaches room temperature, approximately 23°C. These changes with temperature imply that this material composition is probably not a good candidate for applications in harsh environments. Losses are very low in both the frequency and the temperature range studied here.

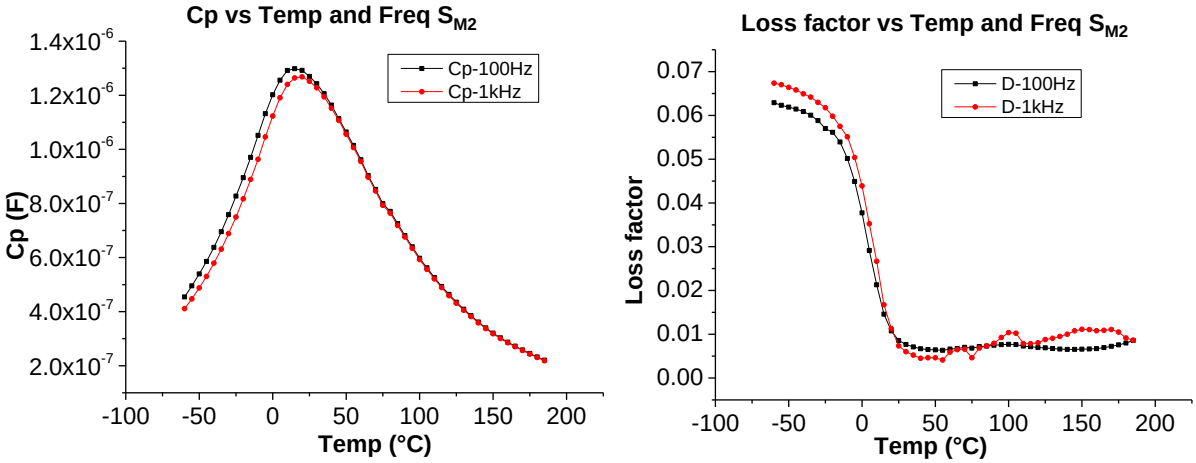
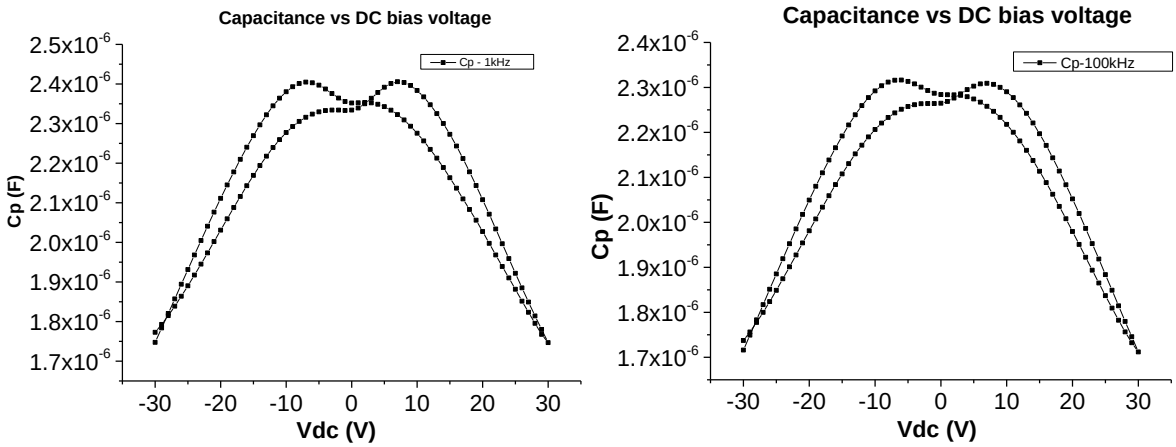


Figure 3.33: Temperature dependence of MIM capacitors at 100Hz and 1kHz.

3.3.2.5 **DC bias dependence:**

The results given in figure 3.34 show the changes in the capacitance measured at 1kHz and 100 kHz when a DC voltage is applied (V_{DC} from -30 to +30 V). The capacitance significantly decreased with increasing DC bias at room temperature.



(a) (b)

Figure 3.34: DC bias dependence of integrated capacitors at (a) 1 kHz and (b) 100 kHz

Such a behavior is detrimental when a constant behavior is expected. It will be necessary to take it into account when achieving the dimensioning of the capacitors for the targeted applications.

3.4 Conclusions

This chapter presents and analyzes important characteristics of integrated capacitors, namely dimension, microstructure, chemical composition, and electrical properties.

Physico-chemical analysis illustrates the microstructure of the MIM capacitor and particle morphology of dielectric material. The uniform construction of two dielectric layers of different capacitors has a positive impact in the capacitor quality process. The physical observations of MIM capacitors and interdigitated capacitors also confirm the ability to create planar multilayer configurations for specific applications in power electronics.

The electrical characterization of capacitors made from ferroelectric ceramics, obtained using the screen-printing technique, offers good values for their main characteristics, together with a reduction in their volume. Compared to commercial ceramic capacitors, these integrated capacitors are much thinner and offer higher electrical performance, as well as large capacitance density from 1.9 to 2.7µF/mm^2, low leakage current, low ESR, low ESL, and high withstand voltage (>300V). Nevertheless, their dependence in both the temperature and the voltage due to their ferroelectric nature could limit their application or at least, could necessitate new design rules to be established. As a result, they can be considered as applicable for filtering, decoupling, or floating functions in passive power integration. The screen mask pattern can be designed flexibly to print the various capacitive function areas on the same substrate.

In summary, the different properties of the material under study, and of the manufacturing process used to produce the capacitors, offer a complementary match for satisfying the demands of power electronics. These properties may be taken into account when designing capacitors for power electronics applications. In fact, designers tend to use high capacitance values for different functions, especially for decoupling. The next chapter thus introduces a method to increase capacitance value without changing the integrated capacitor configuration.

Chapter 4 Influence of cold isostatic pressing on ferroelectric thick film

4.1 Introduction

In DC-DC converters, the multilayer integrated capacitors characterized in Chapter 3 can be used as embedded capacitive layers on alumina to implement many functions, such as filtering, decoupling, and floating capacitors. Proper design enables them to replace discrete surface-mount capacitors with the goal of reducing converter dimensions and increasing performance. This replacement not only narrows component spacing and reduces board size, but it also increases electrical performance and reliability due to a miniaturization in interconnection length as well as the number of solder joints and vias. Designers actually tend to use larger value capacitors for more efficient decoupling and filtering purposes. Therefore, in order to increase the capacitance of an embedded capacitor, higher dielectric constant material can be used, while keeping the electrodes as large as possible.

This chapter introduces another simple method to obtain high capacitance by reducing the thickness of the dielectric layer thanks to cold isostatic pressure (CIP) [54]–[56]. The impact of CIP treatments on the ferroelectric thick film of the screen-printed capacitors was investigated.

CIP is an effective pretreatment technique to compact ceramic thick film or powders for high quality production. It makes use of the following principle: "*A change in the pressure of an enclosed incompressible fluid is conveyed undiminished to every part of the fluid and to the surface of its container,*" proposed by the renowned French scientist Blaise Pascal. CIP applies pressure uniformly from multiple directions to compact ceramic films or powders encapsulated in a flexible sealed container and immersed in a pressure vessel filled with an aqueous suspension at ambient temperature. The process has many advantages over other more conventional pressing techniques: the obtention of greater uniformity of structure and isometric shrinkage, higher densification for a given pressure , and generally the overall flexibility of equipment for producing different shapes. Samples compressed with CIP have higher relative density [55] as compared with uniaxial pressing.

Several processes are presented to fabricate a planar ferroelectric capacitor on alumina substrate, with high pressure applied to study the impact on the properties of screen-printed ferroelectric thick film. Ferroelectric thick-film is printed on Ag/Al_2O_3 substrates and dried at 120^0C for 10 minutes. A novel pretreatment of cold isostatic pressing (CIP) is then applied with different levels from 600bar to 3000 bars for 5 minutes to improve densification and enhance the quality of the ferroelectric thick-film. Comparisons between samples with and without CIP have been made for both physico-chemical analysis and electrical performance. Possible reasons for reducing dielectric thickness are also discussed in terms of reducing porosity and joints formed among nanoparticles in the CIP process. Results show that the

microstructure of thick films with compression is compacted and exhibits better dielectric properties. Impedance measurements also presented, demonstrating that the CIP process is an effective way to increase capacitance value thanks not only to a significant reduction in thickness of dielectric layers but also due to the impact it may have on the permittivity value. These embedded capacitors with CIP present higher capacitance, low parasitic ESL, ESR, emerging as a very promising option for applications that require higher capacitance with more shrinkable size and lower cost.

4.2 Proposed CIP processes

In the new proposed processes, alumina substrates are still used due to their low price, good thermal conductivity, relatively light weight, and environmentally friendly position. To observe the effects of CIP on the physico-chemical properties of ferroelectric thick films, ESL 4212C and ESL 9916 are still used for the dielectric layers and electrodes, respectively. In order to compare the capacitance value change of capacitor samples with CIP and without CIP, their configuration and dimensions remain the same. This section presents process flows to make integrated capacitors with higher capacitance.

4.2.1 Sample packaging selection for CIP treatment

The research was performed on MIM capacitors as described in Figure 3.3. After the dielectric layer was screen-printed and dried, one sample was immersed directly into the cold isostatic machine pressure tank, while another sample was packaged into a plastic bag with good tenacity. The bag was vacuum-sealed and hermetically packaged using a vacuum machine, as shown in Figure 4.1(b),(c). The plastic bag was then immersed completely in a liquid medium in the cold isostatic pressure machine's chamber. To form a densified layer with reduced porosity and surface roughness on the dielectric layer, pressure was applied in all directions at 600 bars and held for 5 minutes on both samples, as demonstrated in Figure 4.1(d). After CIP pretreatment, the plastic bag was removed and the samples were fired following the cycle indicated in figure 2-16 chapter 2.

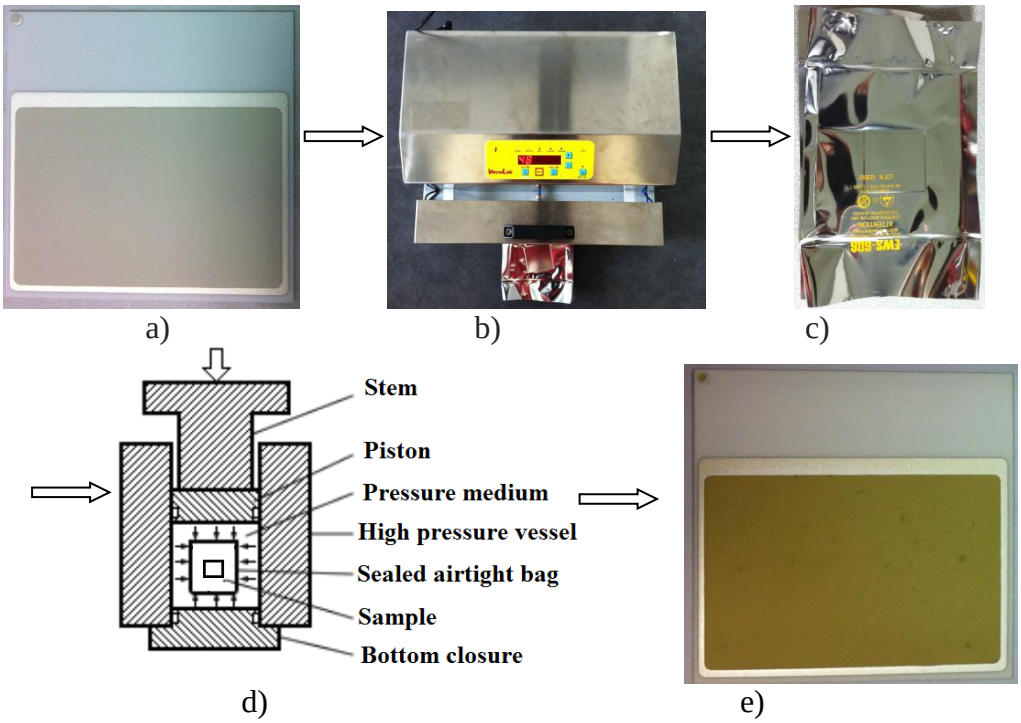
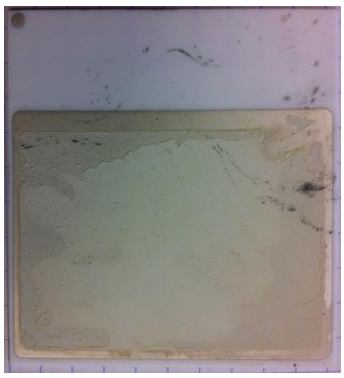


Figure 4.1: Cold isostatic pressing treatment: (a) dielectric layer after drying, b) vacuum-packing machine, c) sample packed inside a vacuum-sealed plastic bag, d) plastic bag immersed in pressure vessel, e) dielectric layer after CIP and sintering.

Figure 4.2(a), (b) show that the quality of the sample in the sealed airtight plastic bag is much better than the sample without packaging. In fact, the dried sensitive dielectric layer of the sample without packaging was partly destroyed by high pressure in the aqueous suspension.

In

Figure 4.2(c), (d), it can be seen clearly that, after sintering, there are many cracks in the dielectric layer of the sample without packaging, while the sample in the sealed plastic bag presents a highly uniform dielectric layer. Its thickness, measured by an Alpha Step-IQ Surface Profiler, reduces noticeably from 55µm to 25µm compared to the sample without such a treatment. As a result, the vacuum-sealed plastic bag is subsequently used to package all samples before immersion into the CIP machine's pressure vessel following the process shown in Figure 4.1.



(a) Sample without packaging, after CIP.

(b) Sample packed in plastic bag, after CIP.

(c) Sample without packaging, after sintering.

(d) Sample packed in plastic bag, after sintering.

Figure 4.2: Sample comparison with and without packaging in the CIP process: (a) Sample without packaging after CIP; (c) after sintering, (b) Sample packed in plastic bag, after CIP; (d) after sintering.

4.2.2 Process flows under study

The process flow without CIP pretreatment in Chapter 2 (figure 2.16) was referred to as P1. Figure 4.3 describes a process, P2, in order to study the differences between dielectric layers with and without pressing. Only one first dielectric layer is subject to CIP, and the second dielectric layer is still printed, dried and co-sintered with second silver layer. The pressure level applied for the thick films is from 600 to 3000 bars. The second dielectric layer is printed to fill porosity and to compensate for defects in the first dielectric layer.

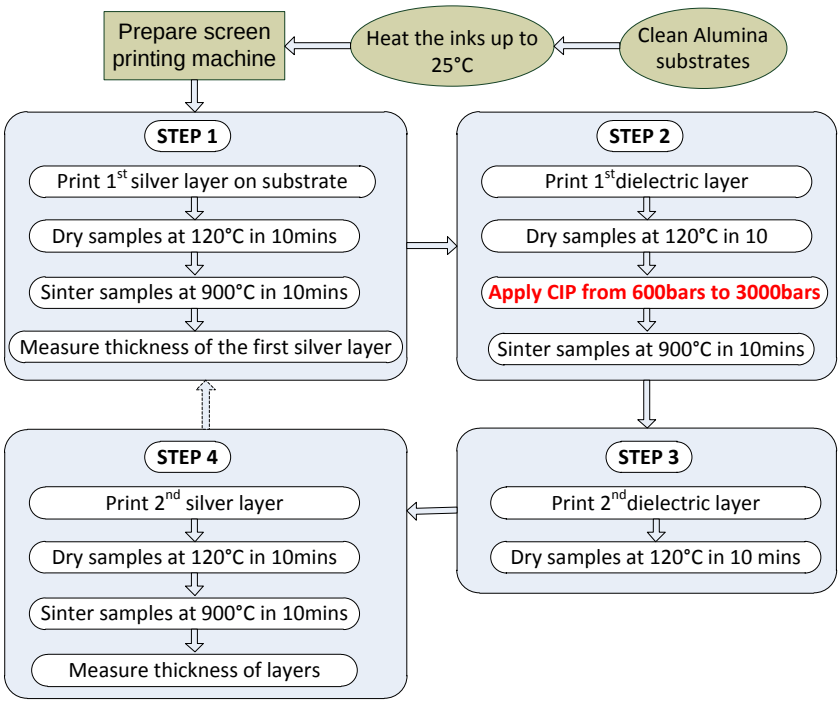


Figure 4.3: Process flow P2.

Process P3, shown in Figure 4.4, was adapted to study the influence of CIP on both metal and dielectric films. CIP was applied for the first dielectric layer, which was next sintered, and then CIP continued to be applied for both the second dielectric layer and the silver with the same pressure value. Lastly, the samples were co-sintered.

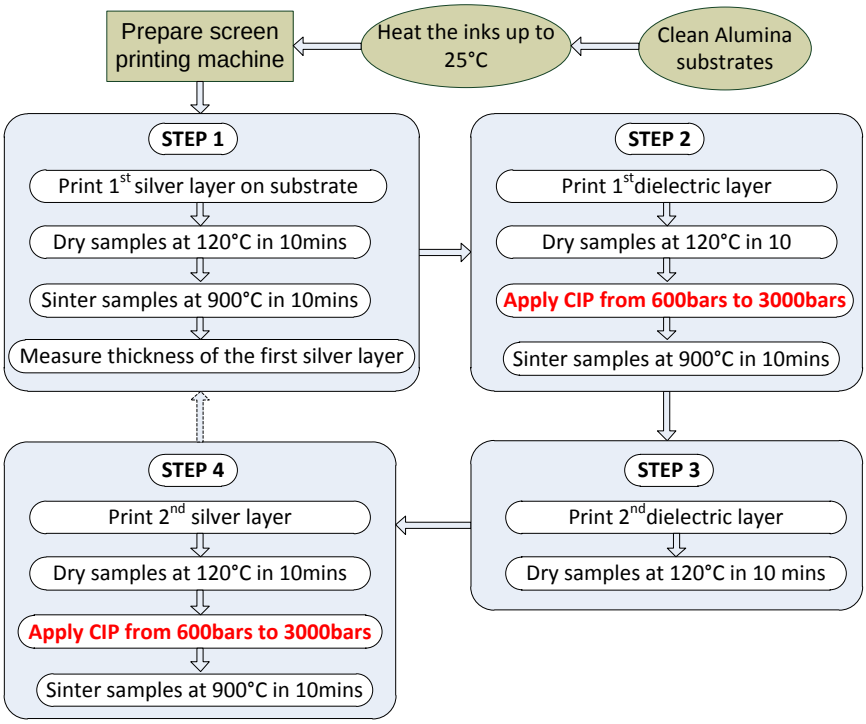


Figure 4.4: Process flow P3

On the other hand, process P4 (see Figure 4.5) seeks to study the influences of CIP on both dielectric layers. The first (dried) dielectric layer undergoes CIP and sintered; then the second dielectric layer is printed, dried, undergoes CIP with the same value, and then sintered. Lastly, the second silver layer is screen-printed, dried, and sintered.

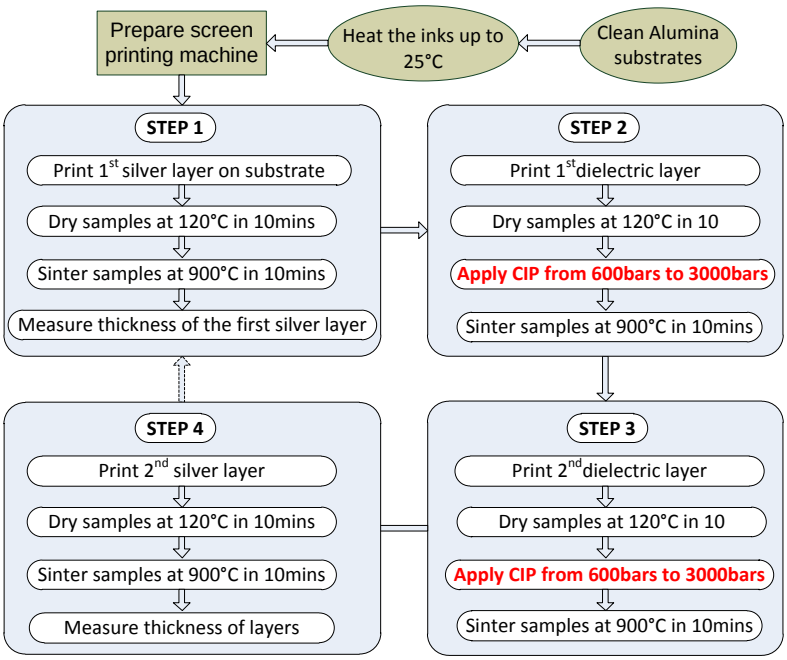


Figure 4.5: Process flow P4

Process P5 (Figure 4.6) is similar to process P4, but the second electrode is printed after the second dielectric layer underwent CIP without sintering. The sample is then annealed following the sintering scheme in figure 2-15.

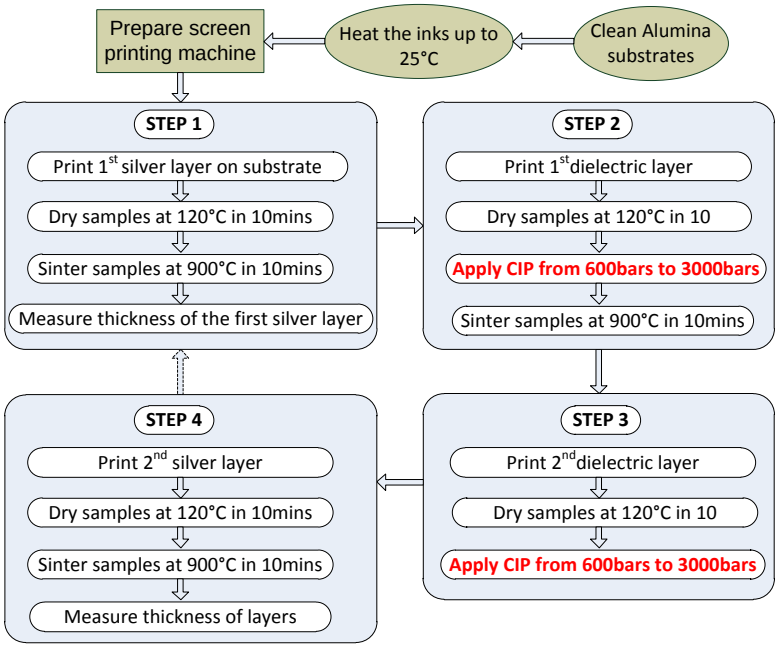
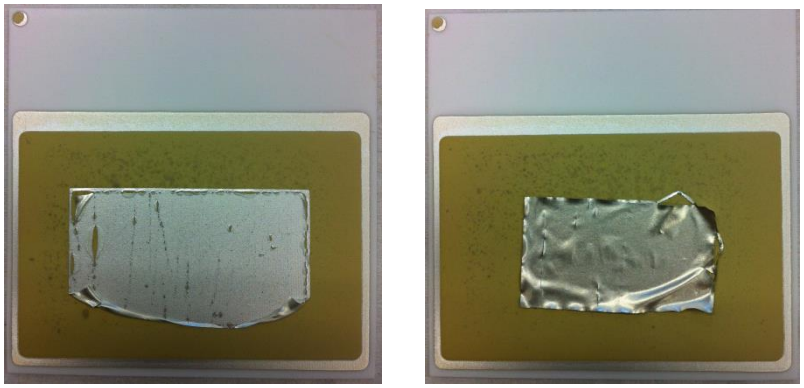


Figure 4.6: Process flow P5

This process P5 was not successful, as the second silver layer did not adhere to the dielectric layer, as shown in Figure 4.7. The reason for this non-adhesion phenomenon can be explained by the fact that the shrinkable capability of the dried dielectric layer after CIP treatment is different than that of the dried second silver layer without the CIP process. Thus, the four processes P1 to P4 listed in Table 4.1 were chosen to fabricate MIM capacitors for the purposes being studied in this chapter. Total dwell time mentioned for all four successful process flows reveals that process P4 requires the longest time to produce one sample (4 days), while the other processes only require 3 days. In each CIP process, physico-chemical analysis and electrical characterization were performed on four typical samples with four CIP levels at 600, 1000, 2000, and 3000 bars, and compared to a sample without CIP in the next section.



a) 700 bars CIP. b) 1500 bars CIP.

Figure 4.7: Two samples had CIP applied at 700bars and 1500bars for 5 minutes according to process P5.

Table 4.1: Sample preparation steps for fabricating MIM capacitors.
(DL = Dielectric; De/D/S = Deposit/Drying/Sintering; CS = Co-sintering, CIP = Cold isostatic pressing)

Process	Layer	Flow	Duration (day)	Note
P1	1st Ag	De/D/S	1	No CIP applied
	1st DL	De/D/S	1	
	2nd DL	De/D	1	
	2nd Ag	De/D/CS		
P2	1st Ag	De/D/S	1	CIP applied only on the 1st DL
	1st DL	De/D/CIP/S	1	
	2nd DL	De/D	1	
	2nd Ag	De/D/S		
P3	1st Ag	De/D/S	1	CIP applied on the 1st DL and then CIP applied for both 2nd DL and 2nd Ag
	1st DL	De/D/CIP/S	1	
	2nd DL	De/D	1	
	2nd Ag	De/D/C-CIP/CS		
P4	1st Ag	De/D/S	1	CIP applied for the 1st DL and 2nd DL separately
	1st DL	De/D/ CIP/S	1	
	2nd DL	De/D/CIP/S	1	
	2nd Ag	De/D/S	1	

4.3 Results and discussions

4.3.1 Physico-chemical analysis

4.3.1.1 **Permittivity comparison**

The pretreatment with cold isostatic pressing makes thick films denser, causing variations in their dielectric properties. In order to compare the permittivity of the samples which had CIP applied, to others to which CIP was not applied, the thickness of the dielectric layer is measured by an Alpha Step-IQ Surface Profiler, and the capacitance of different capacitors are measured by an HP 4191 gain-phase analyzer. The name of sample is SnPi (n is sequence of sample, i is process from 1 to 4). The results in Table 4.2 show that the thickness of the dielectric layer is reduced significantly when they are subjected to CIP. The comparison of relative permittivity between the sample with CIP and that without CIP can be calculated using this formula:

$$n = \frac{\varepsilon_{CIP}}{\varepsilon_{no\_CIP}} = \frac{C_{CIP} d_{CIP}}{C_{no\_CIP} d_{no\_CIP}}$$

Where n is the permittivity change of the sample with CIP compared to the sample without CIP in process P1, C is capacitance, ε is the dielectric material's permittivity. It can be seen clearly that in most cases, the capacitance increases for the samples with CIP (n>1) for the two following reasons:

- The thickness of the dielectric layer is reduced thanks to CIP pretreatment. In Table 4.2, the thickness of each sample was calculated from the average of three measured points by an Alpha Step-IQ Surface Profiler. The thickness of most of the samples with the CIP process is around 20µm, while this value for sample without CIP is much greater (about 35µm). Thus, the CIP process has an obvious influence on the shrinkage of the screen-printed thick films.
- The permittivity of dielectric material increases due to the improvement of thick film's dielectric properties when the layers were compressed. The variation of the dielectric constant with frequency and compressive pressure for different samples is plotted in Figure 4.8. It is clear that the permittivity of the dielectric material after CIP treatment can reach a much higher value (nearly 18000) compared to the material without CIP (around 10000). The increased dielectric constant reflects a more densified microstructure of dielectric films. The dielectric properties of thick film are closely related to the microstructure of the dielectric layer and the grain size effect [57]. Denser microstructure with less external porosity is also beneficial for lower dielectric loss. The porous microstructure and rough surface of the unpressed thick film degrade dielectric properties.

Table 4.2: Comparison of dielectric layer thickness and relative permittivity change for sample (n) with and without CIP application.

Name	Pressure (bar)	Point 1 (µm)	Point 2 (µm)	Point 3 (µm)	Average thickness d (µm)	Cp at 1kHz, room temp	n
S2 P1	0	35	35	36	35	1.12	1
S1 P2	600	33	32	33	32	1.18	1.2
S2 P2	1000	20	20	22	19	1.94	1.2
S3 P2	2000	21	21	22	21	1.79	1.18
S4 P2	3000	21	22	21	20	1.86	1.38
S1 P3	600	30	30	31	30	1.28	0.82
S2 P3	1000	20	20	19	20	1.93	1.16
S3 P3	2000	15	15	16	15	2.53	1.32
S4 P3	3000	14	14	14	15	2.70	1.57
S1 P4	600	24	25	26	24	1.57	1.005
S2 P4	1000	21	22	21	21	1.85	1.22
S3 P4	2000	15	16	14	15	2.61	1.57
S4 P4	3000	14	15	14	13	2.79	1.67

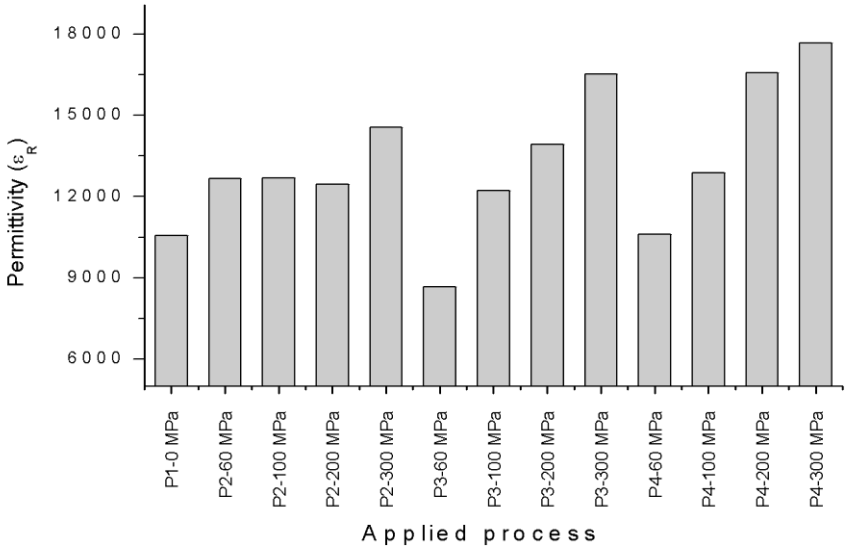
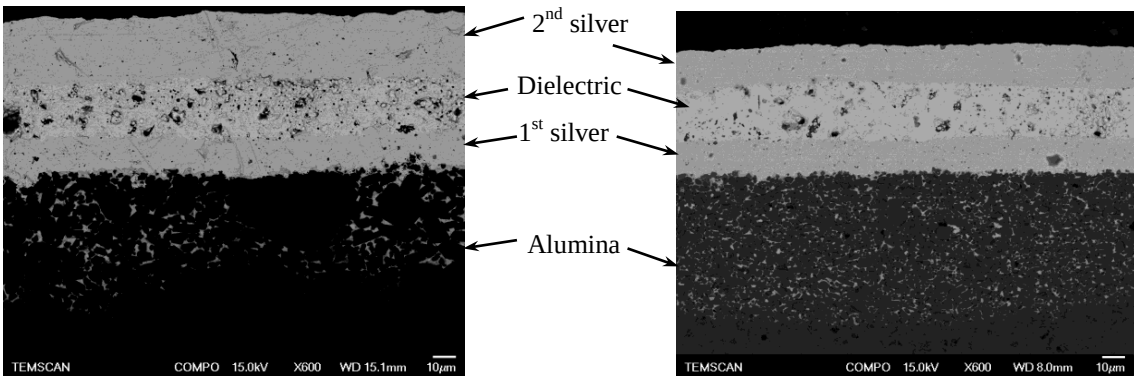


Figure 4.8: Changes of permittivity versus pressure level.

4.3.1.2 **Grain microstructure**

One of the properties that affects the permittivity variation of dielectric materials is the change in grain microstructure, which has been reported in a good number of research reports [57]–[59]. This section is therefore focused on verifying the impact of CIP treatment on the grain microstructures and chemical composition of ferroelectric thick film.

Some samples (S1P1 without CIP, and S4P2, S4P3, S4P4 with CIP at 3000 bars) were cut into individual elements using a Struers SECOTOM 10 precision cut-off machine. Then, they were encapsulated in epoxy and polished to observe microstructure and chemical properties through a transmission electron microscope (TEM). The cross-section morphology in Figure 4.9, and dielectric thickness measurements in Table 4.3, demonstrate a clear reduction of the dielectric layer's thickness as well as shrinkage of thick film after applying CIP.



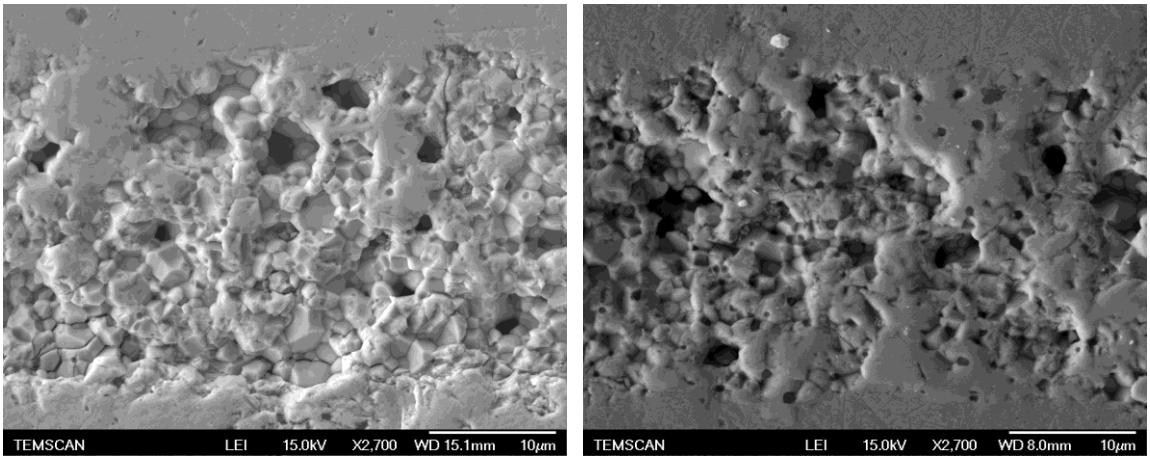
(a) (b)

Figure 4.9: Cross-section of (a) sample S1P1without CIP and (b) sample S4P4 with CIP.

Table 4.3: Thickness of samples measured by TEM.

Name	Pressure (bars)	Point 1 (μm)	Point 2 (μm)	Point 3 (μm)	Average thickness d (μm)
S1P1	0	35	36	35	35
S4P2	3000	21	22	21	20
S4P3	3000	14	15	14	14
S4P4	3000	14	14	15	14

TEM scan photos in Figure 4.10 show that, although the two dielectric layers are fabricated in different ways, the grain morphology of the sample with or without CIP does not change significantly and the global structure can be considered as uniform, thus decreasing the risks of premature failure. Due to isostatic pressing pretreatment, the dielectric properties of the thick films improved, notably because the pores with low relative permittivity are eliminated progressively [60]. The room temperature permittivity of ferroelectric material clearly reaches its maximum at a grain size of about 1μm. The increase in permittivity may also be caused by an aggregation of domain size and stress effects [58].



(a) (b)

Figure 4.10: The TEM scan photos of samples without CIP (a) and with CIP (b).

The main problem remains the lead diffusing out of the dielectric film onto the alumina substrate. Chemical analysis of both samples with and without compression in Figure 4.11 and figure 4.12, shows that the contaminant in the alumina substrate is a small amount of lead. It is also seen in Figure 4.9 that, for the sample with CIP, the density of lead diffusion distributed in the alumina substrate is more uniform than for the sample without CIP, due to stress from multiple directions. Lead diffusion may cause the location of the breakdown of the substrate. An intermediate barrier layer of IP211 was suggested by R. Maas et al. from University of Southampton in [61] to prevent the diffusion of lead onto the substrate. In their

work, the insulating IP211 ink was screen-printed onto the substrate as a barrier layer between other thick-films and substrate. This ink contains a devitrifying glass component that crystallizes upon initial sintering. Subsequent firings do not cause the film to soften, thus providing a stable foundation layer for additional films. After sintering, no visible contamination could be seen in the area covered with the insulator.

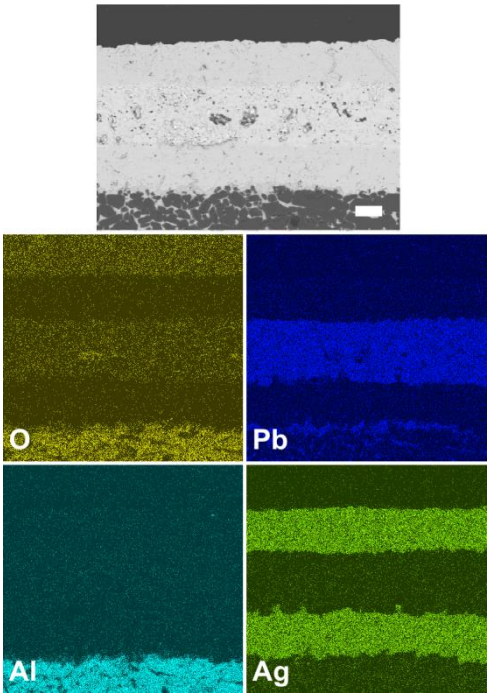


Figure 4.11: Chemical analysis of sample without CIP.

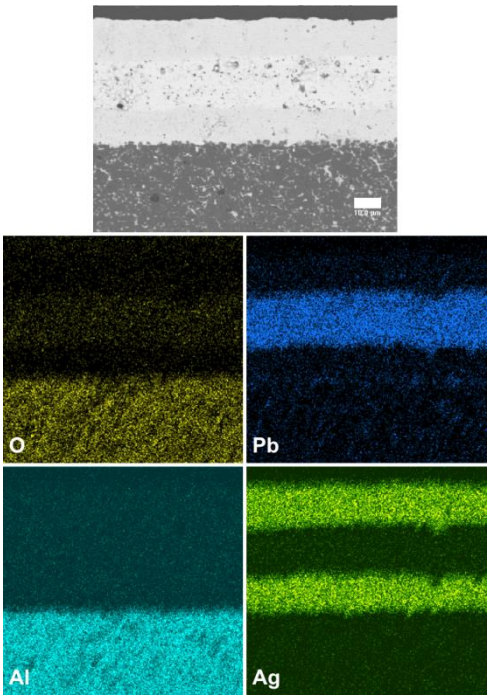
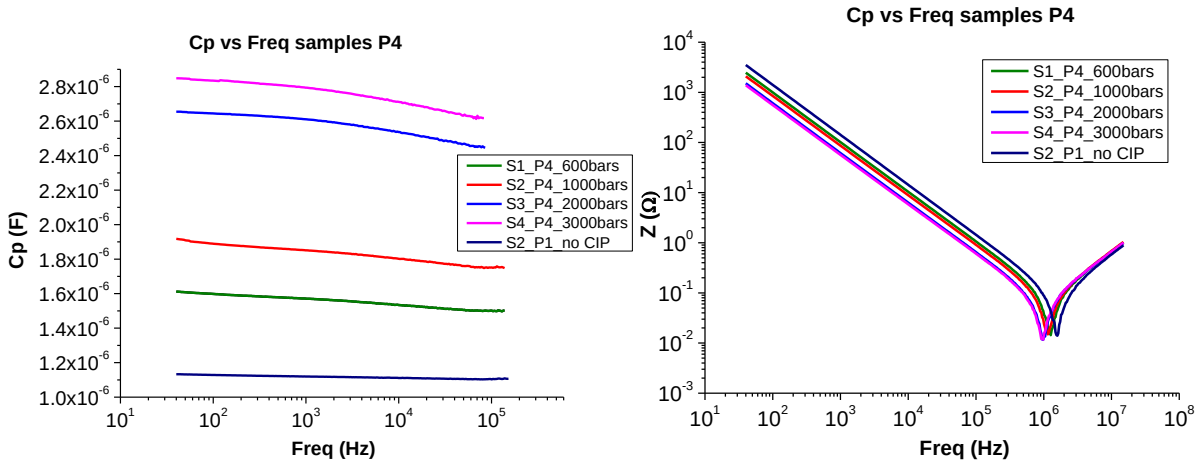


Figure 4.12: Chemical analysis of sample with CIP

4.3.2 Electrical performance

4.3.2.1 Impedance and capacitance versus frequency

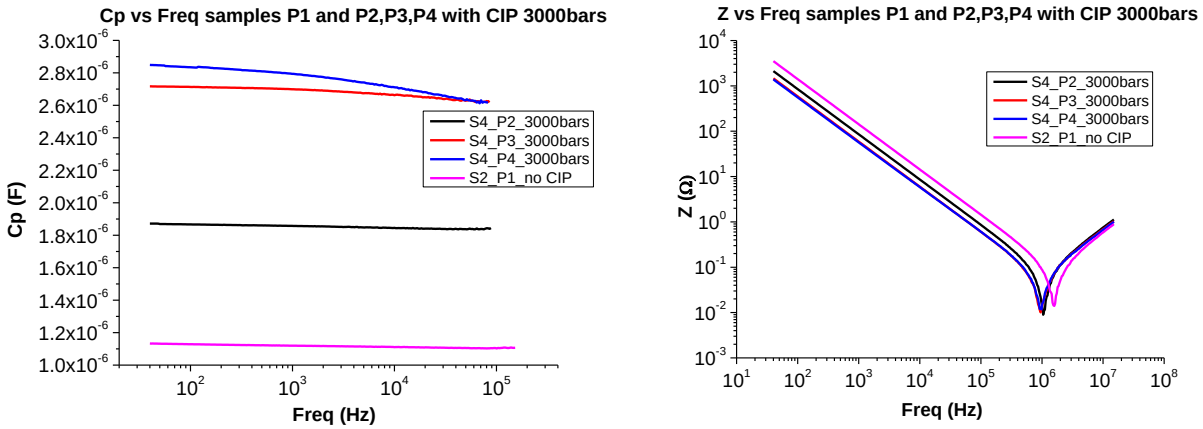
Figure 4-13 presents the relative change of capacitance and impedance with frequency and pressure level for the samples in the same process, compared to sample without CIP. Capacitance density increases proportionally with pressure levels applied to the dielectric layer. The samples are capacitive in the frequency range from 100Hz to 900 kHz, the equivalent series resistor (ESR) may be measured at about 1MHz, whereas inductive behavior dominates in higher frequencies.



(a) (b)

Figure 4.13: Capacitance and impedance behaviors of sample without CIP S2P1 (a) and samples with CIP levels (b) in the same process.

As shown in Figure 4-14, even with the same pressure level, samples based on different processes still present higher capacitance density compared to the sample without CIP. It can be noted clearly that processes P3 and P4 can achieve higher capacitance than process P2 because they had CIP applied for both dielectric layers while only the first dielectric layer in process P2 was subjected to CIP. This once again highlights the impact of CIP pretreatment on ferroelectric thick film properties.



(a) (b)

Figure 4.14: Capacitance and impedance behaviors of sample without CIP S2P1 (a) and samples with same CIP level (b) in the different processes.

4.3.2.2 **Temperature dependence**

The capacitance value and dielectric losses of MIM capacitors were therefore also measured as a function of temperature.

Figure 4.15 compares the capacitance behavior of the sample with CIP and without CIP in the same process. The capacitance value decreases when temperature increases, which is not beneficial for power electronics applications. It is clear that neither the Curie temperature nor the ferroelectric behaviors are modified by the CIP process.

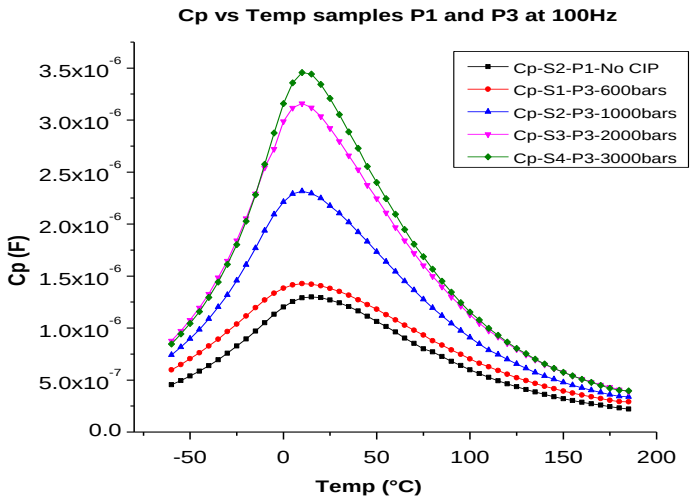


Figure 4.15: Temperature dependence of the capacitance for samples without CIP and with different CIP levels in the same process.

Similarly, Figure 4.16 shows that phase transitions for dielectric composition do not vary widely in samples without CIP and with the same CIP level in the different processes. The Curie temperature also appears to be approximately room temperature. The losses in the ferroelectric phase are relatively high as a function of both frequency and temperature range.

At temperatures ranging from room temperature to 200°C, the dielectric properties are within the same lower scale for both un-treated and pressed samples. At room temperature, the dielectric losses at 1kHz in the film after pressing is 0.0028, compared to 0.0037 without pressing. Dielectric losses in the sample with cold isostatic pressing treatment are generally lower than those in the un-treated sample. The isostatic-pressure-treated screen-printed thick films show a prominent modification on the dielectric permittivity while maintaining low dielectric losses.

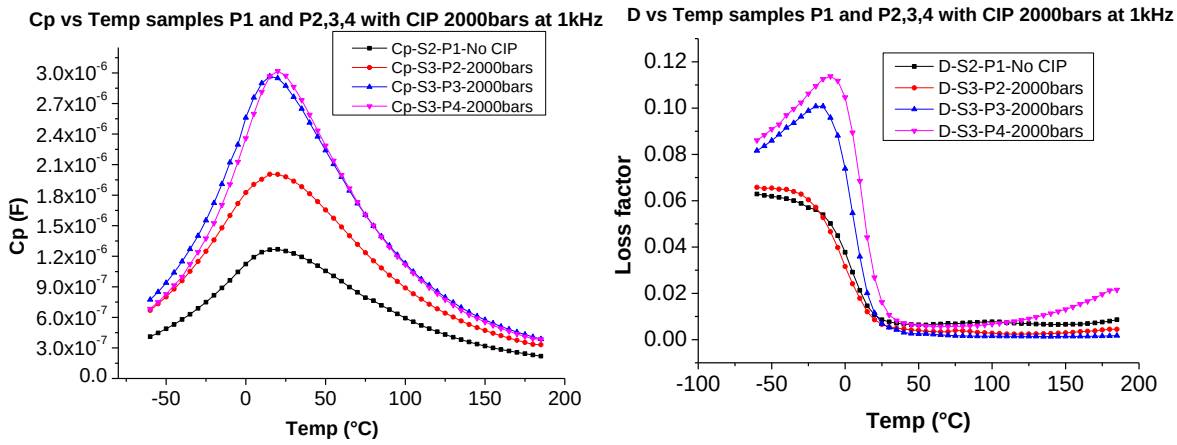


Figure 4.16: Loss factor as a function of temperature for samples without CIP and with the same CIP level in the different processes.

4.3.2.3 **Withstand voltage test**

Besides temperature and humidity, pressure also has a critical effect on capacitor breakdown voltage. The samples with CIP and without CIP were tested to find the threshold voltage that they can withstand before being destroyed. The results in Table 4.4 show that the withstand voltage of the capacitors after the CIP process seems to be increased for the largest capacitance values whereas it is decreased for the lowest ones when compared to the sample without CIP treatment.

Table 4.4: DC voltage that can be applied to the MIM capacitors.

Name	Pressure (bars)	Average thickness d (μm)	Cp at 1kHz, room temp (μF)	$V_{withstand}$	$I_{leakage}$
S2 P1	0	35	1.12	300*	small
S1 P2	600	33	1.18	190	small
S2 P2	1000	20	1.94	300*	small
S3 P2	2000	21	1.79	140	small
S4 P2	3000	21	1.86	300*	small
S1 P3	600	30	1.28	220	small
S2 P3	1000	20	1.93	300*	small
S3 P3	2000	15	2.53	190	small
S4 P3	3000	14	2.70	60	small
S1 P4	600	24	1.57	110	small
S2 P4	1000	21	1.85	130	small
S3 P4	2000	15	2.61	140	small
S4 P4	3000	14	2.79	300*	small

* There is no flashover up to this voltage level.

Although the mechanical pressure improves dielectric properties, the reduction of dielectric thickness is also a reason for the lower withstand voltage of the compressed capacitors. The electrical strength of ferroelectric ceramics also depends on the composition, grain size, microstructure specifics, and metal electrode material [62].

After the first breakdown, compressed capacitors still exhibit a self-healing phenomenon like the uncompressed capacitor. The voltage level of the first breakdown clearly shows that the ferroelectric capacitors present a short-circuit after a few self-healing processes have occurred. These self-healing capacitors can sustain many dielectric breakdowns during their operating lifetime, thus allowing higher operating voltage, a much greater designed electric field, and therefore larger energy densities.

4.3.2.4 **Leakage current**

Leakage current in pressed and un-pressed capacitors was monitored using a Keithley 2410 High-Voltage SourceMeter after applying different voltages for the first 200 seconds. Measured results showing leakage current variations over time at rated voltages are presented in Figure 3.31 (un-treated sample) and Figure 4.17 (treated sample). The leakage current for a capacitor with CIP processing is similar to that observed for a capacitor without CIP processing, and indicates that the leakage current value is in the range of nanoamperes. Typical I-V characteristics of integrated capacitors can be approximated with straight lines as shown in Figure 4.18. The insulation resistance that is derived from I-V characteristics is

around GΩ. This reveals a good isolation level suitable for the storage or decoupling function in power electronics.

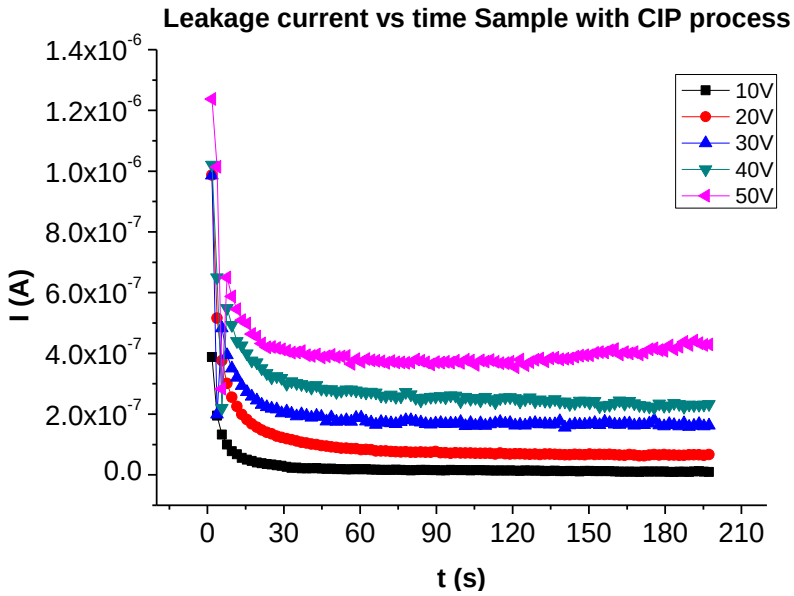


Figure 4.17: Leakage current over time of sample with CIP process.

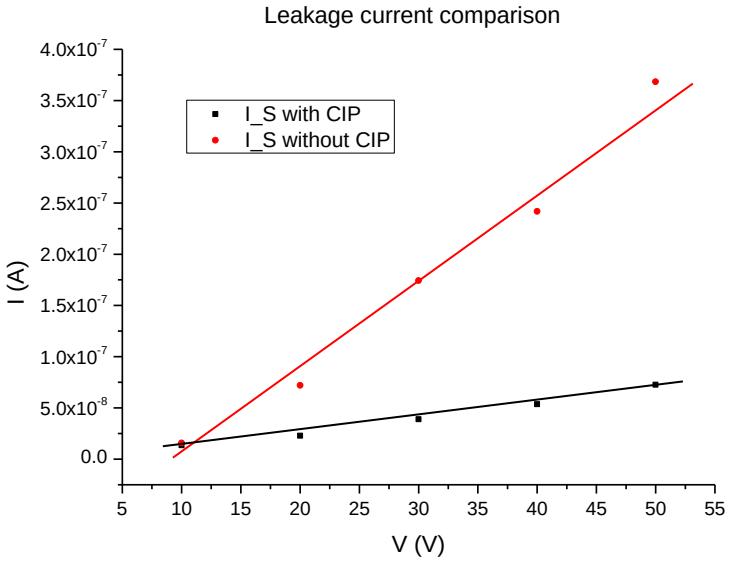


Figure 4.18: Leakage current comparison.

4.4 Conclusions

High-capacitance integrated capacitors were fabricated successfully with four different processes. Cold isostatic pressing was investigated to improve dielectric properties of screen-printed thick films. Higher capacitance densification was reached due to different CIP application modes.

In almost all cases, the higher the pressure applied to thick-films, the greater the permittivity changes. The dielectric permittivity of samples with CIP reached 18000, a much higher level when compared to 10000 for the sample without CIP. The permittivity change is based on two factors. The first factor is the reduced thickness of the dielectric layer thanks to the application of CIP in multiple directions. It is well known that in Ferroelectric materials the permittivity increases when the size of the grain decreases until a value- generally corresponding to the elementary domain size is reached. Then, the permittivity still decreases. It is therefore possible that CIP may induce such an effect. Nevertheless, physico-chemical analysis shows that the grain size of a sample with and without compression is not significantly different. Therefore, the second factor leading to the permittivity increase is possibly caused by a combination of domain size and stress effects.

The electrical characterizations of the samples with CIP processing also show a capacitance value that increases with the applied pressure level. With a same effective surface area (19mm x 33mm), the capacitance of samples with CIP treatment can reach 3µF, leading to an effective capacitance density of 4.7nF/mm² for a dielectric thickness of 22µm. On the other hand, the one sample without CIP processing is only around 1.2µF, resulting in a capacitance density of 1.9nF/mm². It is clear that capacitance density increases when using the CIP process, and the dielectric properties are improved. The other characteristics of capacitors with CIP processing also appear to be compatible with various functions, such as filtering, decoupling, or flying in power electronics applications. Impedance measurements show that the capacitors with CIP treatment can be operated in the range of a few hundred kHz because the CIP samples are capacitive in the frequency range from 100Hz up to about 1MHz. Temperature dependency measurements show that the Curie temperature is not modified by CIP treatment. Losses in the ferroelectric phase are very low over both the frequency and the temperature range. It is not surprising to note that, in some cases, the withstand voltage of capacitors with CIP processing is lower due to the reduced thickness of the dielectric layer. The leakage current of samples with and without CIP processing is in the nanoampere range and revealed good insulation properties for dielectric materials.

In summary, the different properties of the material under study, and of the manufacturing processes used to produce the capacitors, are a good match for power electronics demands. These properties may be taken into account when designing capacitors for power electronics applications. As a result, CIP is shown to be a useful technology for forming much thinner and higher capacitive integrated capacitors, providing flexible options for power electronics designers.

For future works, we propose further investigations into building multilayer capacitor constructions to reach much higher capacitance. These capacitors can be integrated into planar

capacitive substrate with semiconductor dies placed on their surface. With significant potential in terms of reducing size such capacitors would be strong candidates to replace traditional, bulky printed circuit boards (PCB).

Chapter 5
Integrated capacitors applied to power electronics

5.1 Introduction

DC-DC converters are widely used in a wide variety of power electronics applications, including power supplies for renewable energy, smart grids, spacecraft power systems, telecommunications equipment, and even DC motor drives. In these converters, capacitors are given different functions, mainly filtering and decoupling. The integrated capacitors described in this work can be used to replace surface-mount decoupling capacitors in the different topologies.

This chapter suggests two topologies using integrated decoupling capacitors. The integrated capacitors are screen-printed directly on the alumina substrate. The screen mask drawing is designed to be suitable for the required capacitance value. The planar capacitive substrates are fabricated using the screen-printing technique according to process P1 described in Chapter 2. The electrical properties are characterized following the methods presented in the Chapter 3. The operating results of integrated capacitor applications are analyzed and discussed.

5.2 Classical decoupling function on DC bus

Decoupling is one of the most important functions in any power electronics circuit, especially for power distribution. The switching cells must be supplied by voltage sources but they do not exist in the real world because of parasitic inductors inside generators, lines and connections. Decoupling capacitors are required to deal with this problem. However, using discrete capacitors in decoupling can become less effective due to their own parasitic inductor but also due to the parasitic inductor of the connections with the substrate. In addition, they occupy a significant area on the board. This situation creates an excellent opportunity to use integrated capacitors, taking advantage of the substrate volume and with reduced parasitic inductors.

A classical way to reduce the impact of parasitic ESL and ESR is to place multiple capacitors in parallel. Altogether, these discrete capacitors can occupy a large amount of space, increase product cost, and reduce reliability due to the high number of solder joints. In order to overcome this problem, integrated capacitors that have far less parasitic ESL than surface-mount discrete capacitors are an attractive choice for several reasons. The first reason is that with the configuration of two plates in parallel, the current flows in opposite plates, resulting in electromagnetic fields that tend to cancel each other out, therefore lowering the inductance. The second reason is that the plane configuration also decreases the current loop size relative to coiled folded capacitors in a surface-mount case. The third reason is that the integrated capacitors are in a plane with interconnections, further reducing the current-loop

area and eliminating vias that increase parasitic inductance. As a result, the total inductance of an integrated capacitor, including lead and spreading inductance, can be less than that of surface-mount capacitors.

In order to determine the effectiveness of integrated capacitors for decoupling, this section presents the steps for creating an integrated capacitive substrate applied to a specific topology.

5.2.1 Proposed topology and screen mask design

The aim of this technological approach is to integrate capacitive functions very close to semiconductor power devices, as described in the *First demonstrator* section of Chapter 1. This proximity is mainly required to minimize the parasitic inductance of the switching cell. To emphasize the interest of the process regarding integration possibilities, a common-mode capacitor for the filtering part, directly connected to this switching cell, is added on the proposed capacitive substrate (Figure 5.1).

Actually, at the beginning of this work, this substrate was supposed to constitute the base of a 200V-10A switching cell that should be able to operate in a frequency range from a few tens of kHz to a few hundred kHz. According to these objectives, the target was to reach values of the decoupling capacitor close to a few µF, while the appropriate values of both common mode capacitors, using the same dielectric layers, were estimated to a few tens of nF. This common mode filtering function directly associated with the switching cell can be very efficient due to their close vicinity and this is typically the kind of improvement offered by integration. To obtain the complete filtering function, a common-mode choke must be added, that will be covered in a subsequent step of this work, as the final goal here is to test a complete cell that includes semiconductor power devices.

Unfortunately, the design of this substrate has been made from the start of the work, to anticipate technological processes highly time consuming, with the consequence of an insufficient experience to obtain optimal results. For example, concerning the dielectric ink, the impact of the ferroelectric behavior, observed later during the characterizations (decrease of ε with the polarization), has been underestimated. Consequently, the combination of voltage rating and capacitor values mentioned above is not reachable with the developed substrate. Nevertheless, the results presented in this section are considered as proofs of concept, this preliminary warning being necessary to explain the limitations of the substrate design in regards with the objectives.

According to the addition of common mode capacitors, the substrate is divided into three capacitive zones: two smaller zones for two filtering capacitors and one larger zone for the decoupling capacitor.

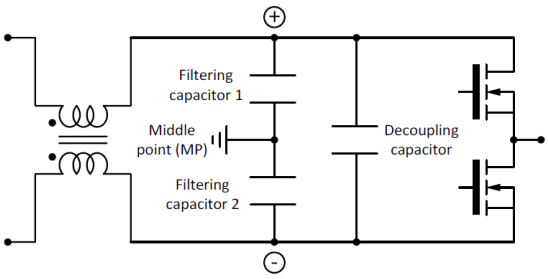


Figure 5.1: Operation of a decoupling capacitor.

Specific screen masks developed for this work are shown in Figure 5.2. Based on capacitance density value and required decoupling capacitance, it is straightforward to calculate the dimensions of integrated capacitors (capacitor surface area: $A = Cd/\varepsilon_o\varepsilon$). Two filtering capacitors are designed with 5x7 mm^2 size to obtain the capacitance range in a few hundred nF, while the decoupling capacitor with dimensions of 19x19 mm^2 is expected to reach the range of a few µF. All capacitors have the same dielectric layer with an area of 33x22 mm^2. The screen masks are made from stainless steel, from a size of 40x40 cm^2. Screen mask parameters for dielectric and conductive paste, shown in Table 5.1, are established based on ink manufacturer recommendations.

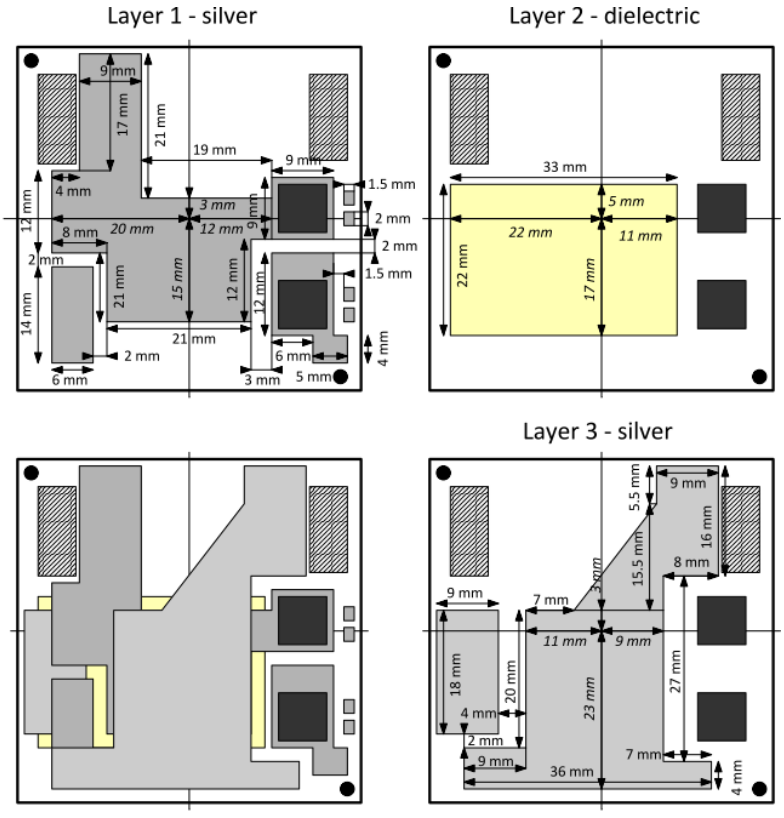


Figure 5.2: Screen mask drawings.

Table 5.1: Screen mask parameters.

	Dielectric mask	Conductive mask
Material	Stainless Steel	Stainless Steel
Screen mesh	200	325
Emulsion	37.5µm	25µm
Width of mesh	90µm	50µm
Diameter of wire	40µm	30µm
Gauze (mesh)	45°	45°

5.2.2 Realization and characterization

5.2.2.1 **Realization**

Using process P1 described in Chapter 2 (Figure 2.16), the three first capacitor layers were fabricated successfully, with their capacitance values increasing gradually with the number of layers. The complete process presented in figure 5.3.

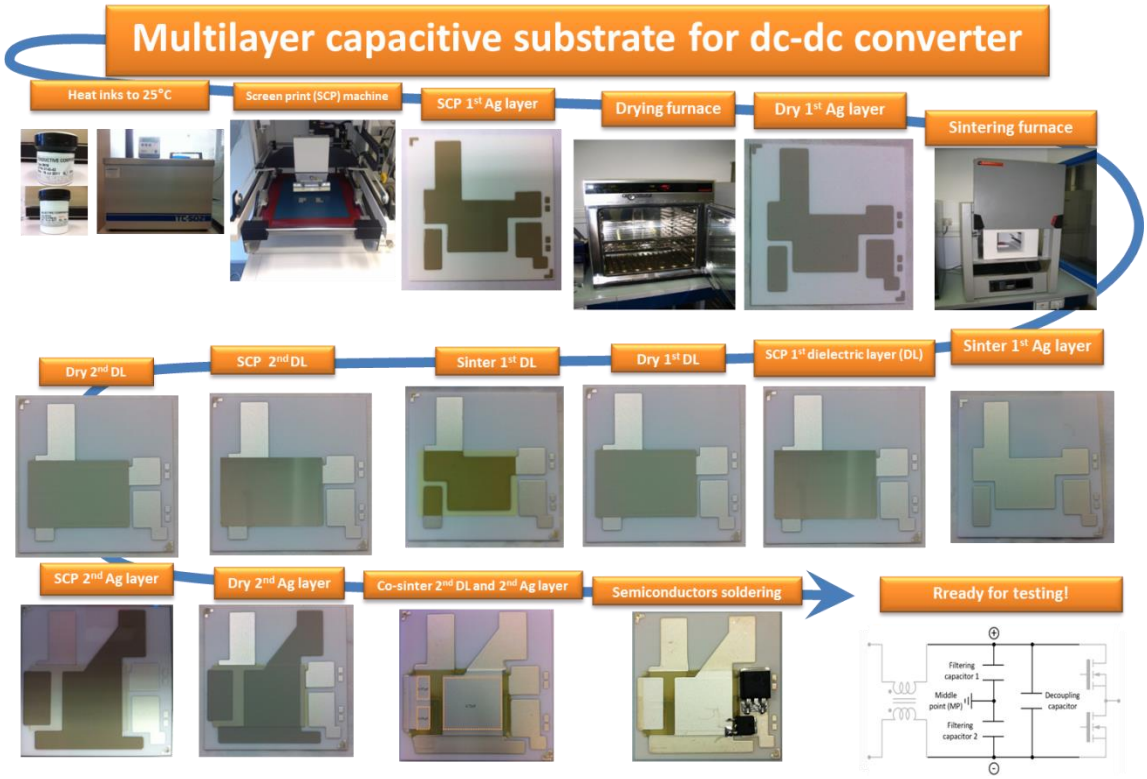


Figure 5.3: Process for fabricating planar multilayer integrated capacitive substrate.

5.2.2.2 Electrical characterizations

The capacitors were signed as shown in figure 5.4, with two smaller capacitors C_{cm1} and C_{cm2} for filtering (surface area of 5x7mm^2), and a larger capacitor C_D for decoupling (19x19mm^2). The name of capacitive substrate samples are Sn, n is sequence number. Their electrical performance and physical analysis were performed according to the methods described in Chapter 3. Figure 5.5(a) shows the increase of the decoupling capacitor value with the number of layers (Vdc = 0V), namely 0.97µF, 2.48µF, 3.6µF for 1, 2, 3 layers respectively. The impedance behavior of the 3-layers capacitive substrate shown in Figure 5.5(b) shows that the effective operating frequencies range from 100Hz up to nearly 1MHz. The measured results are compatible with the required value for decoupling purposes.

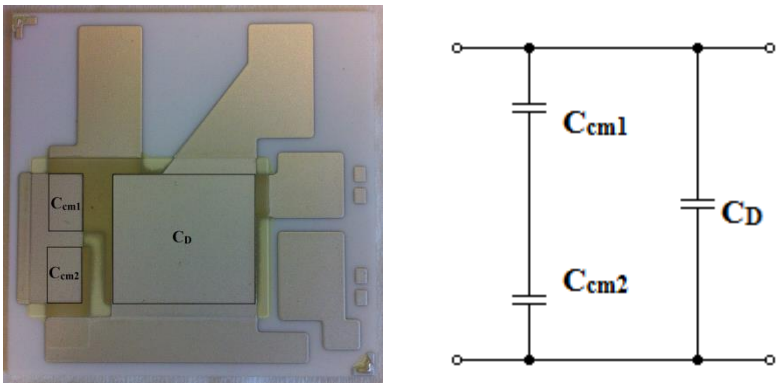
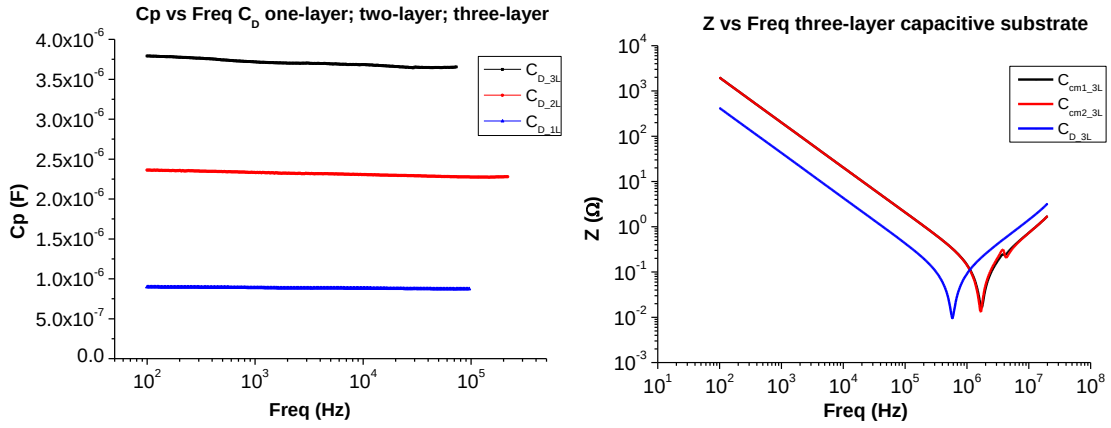


Figure 5.4: Identification of the capacitors on the substrate.



(a) (b)

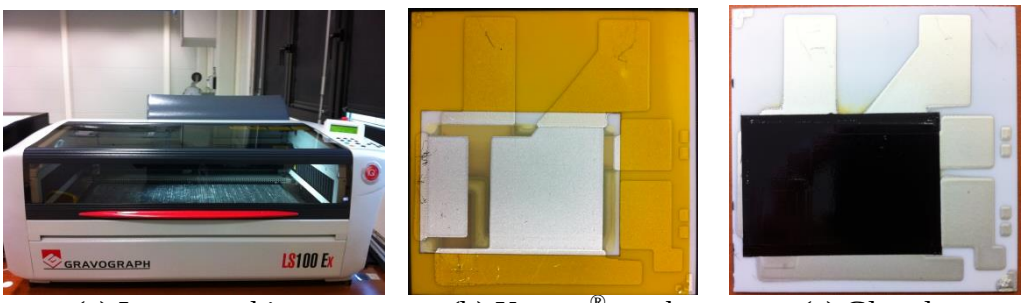
Figure 5.5: (a) Capacitance increase with the numbers of layers, (b) Impedance behavior of 3-layer capacitive substrate.

5.2.3 Sample passivation

As analyzed in section 3.3.2.3, the ability of the dielectric layer to withstand voltage seems to be better in a liquid insulator (FC72) than in open air. This is mainly due to the fact that the used geometry favors flashover. Therefore, in the expectation to improve the withstand voltage; some samples have been passivated by mean of glass layer or parylene layer.

5.2.3.1 **Glass layer**

A glass layer was screen-printed, dried, and sintered on top of the sample surface. Using a Gravograph laser cutting machine to open a required Kapton® area to cover the glass layer, then glass layer was then printed directly, dried at 120°C, and fired at 600°C with dwell time of 10 minutes. Figure 5.6 presents the process for making the capacitor's glass layer.



(a) Laser machine (b) Kapton® mask (c) Glass layer

Figure 5.6: Direct screen-printing process of glass layer on top of the capacitive substrate.

5.2.3.2 **Parylene layer**

Some 1-layer samples were given a 10µm coated of parylene using a PPS (Plasma Parylene System) machine, as shown in Figure 5.7.

Figure 5.7: Parylene coating machine.

5.2.4 Implementation of semiconductor devices

5.2.4.1 Choice of semiconductor devices

At the beginning of the work, the aim was to use bare dies directly soldered on the substrate, the gate and source connections being performed by wire bonds as illustrated in the figure 5.8. Unfortunately, the sourcing of semiconductor dies is difficult in a research context and we have not found appropriated dies for our application. The solution finally retained is the implementation of devices packaged for surface mounting as those presented figure 5.9. It has no impact regarding the integrated capacitor evaluation and, has great benefit since many devices are available in such packages.

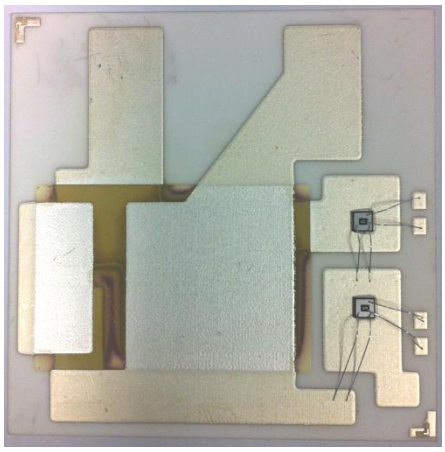


Figure 5.8: Bare dies directly soldered on the substrate

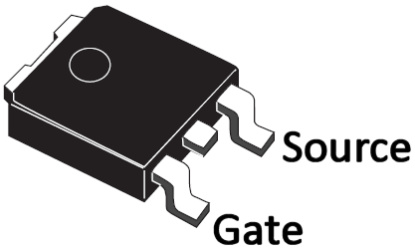


Figure 5.9: MOSFET STD20NF20 (200V, 0.12Ω, 20A)

The two devices required to realize the most basic cell (buck converter, see experimental setup), one MOSFET and one diode, have been chosen in the 200V range, according to the initial objective and in an oversized current range to avoid additional experimental problems.

These devices are :

- A MOSFET STD20NF20 (200V, 0.12Ω, 20A)
- A shottky Diode MBRB20200CT (200V, 20A)

5.2.4.2 Soldering

The semiconductor devices are soldered using a Zevac machine. The soldering process is shown in figure 5.10.

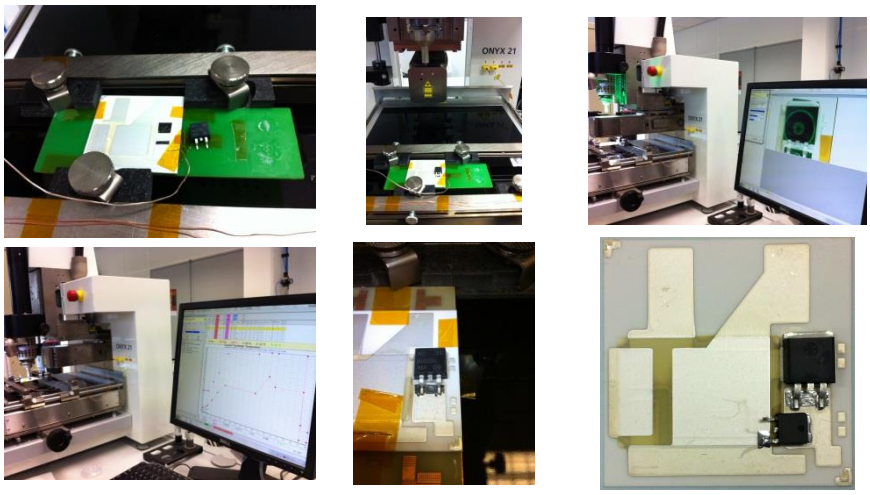


Figure 5.10: Semiconductor die soldering process.

5.2.5 Results

5.2.5.1 Experimental setup

The experimental setup is given in figure 5.11. A gate driver developed for another application and compatible with the chosen MOSFET is connected to the previous power board. This driver uses an integrated circuit that includes high frequency isolation. A FPGA control board provides to the driver a basic PWM signal where switching frequency and duty cycle may be varied. The substrate rests on a heatsink with low pressure to simplify the test preparation. Some views of the setup are shown in Figure 5.12.

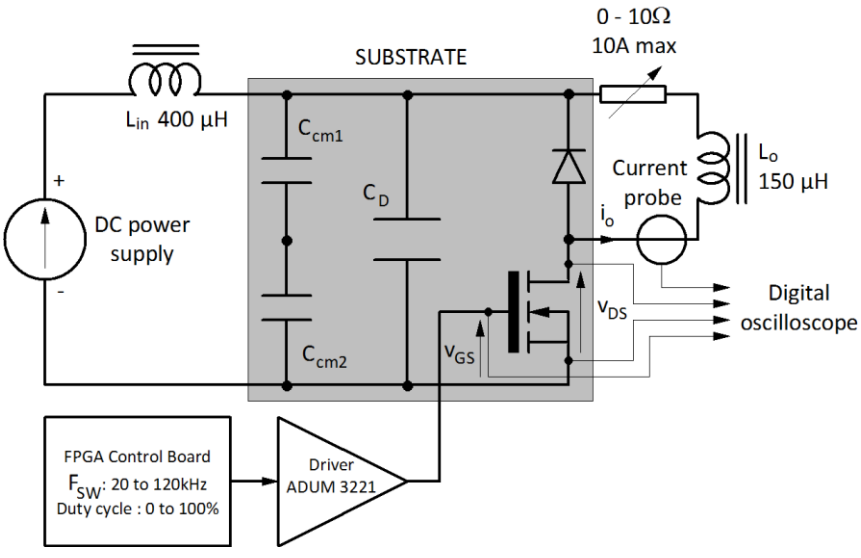
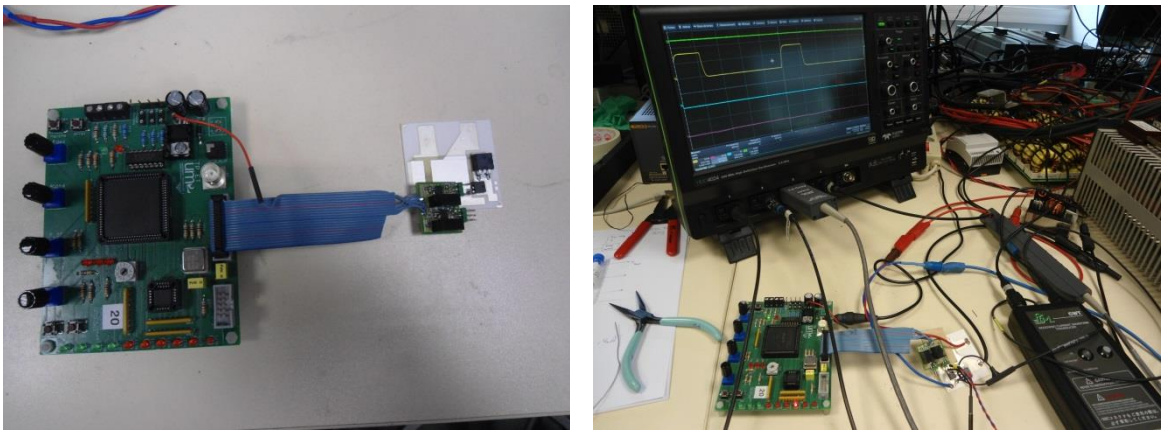


Figure 5.11: Experimental setup



(a) (b)

Figure 5.12: DC-DC converter test: (a) connection of the DC-DC converter to its driver, (b) connection of the DC-DC converter to instruments

5.2.5.2 **Test conditions and results**

14 substrates, passivated or not, have been tested in this part of the work. Unfortunately, the first three samples have been destroyed (vaporization of Ag top layer) due to an over current due to oscillations between the decoupling capacitor and the line inductor (few µH). Therefore, the inductor L_{in} has been added to overcome this problem. In the following results, only samples properly tested are taken into account.

Some trials and errors have been necessary to define a satisfying protocol. For example, we have tried directly to test the first samples under significant voltage, too confident in the voltage ability, or we have increased the load current over the thermal ability of the MOSFET, by forgotten the limitation of the basic cooling system. Finally, the retained test protocol is the following:

- An "expected operating voltage" has been previously defined, namely 100V for all the substrates.
- Each substrate is first tested in switching conditions (100 kHz) with the setup described above, by increasing step-by-step the DC voltage (5V). The starting of each step is made with an output current equal to zero. The output current is then increased step-by-step up to 5A by adjusting the duty cycle and/or the load: *Indeed, the decrease of capacitance with the DC voltage made the voltage ripple non-negligible when the current and the DC voltage increase and the dielectric losses increase in the same time, creating an additional risk of failure. The 5A limit has been defined to avoid any problem on the MOSFET*. If the sample does not fail, the next step is started. If the sample fails before the final step (expected operating voltage 100V and 5A), the failure voltage is marked as the "switching breakdown voltage" of the sample.

- In case of proper operation at the final step, the switching test is stopped. A destructive test of the sample is then carried out to determine the static breakdown voltage. During these tests, the MOSFET is disconnected of the substrate that is now directly connected to the DC power supply. Once again, the DC voltage is increased step-by-step up to obtain the failure. The failure voltage is marked as the "DC breakdown voltage".

The justification of this protocol comes from the uncertainty on the substrate voltage ability. For now, due to the dispersion of the substrates characteristics and to the small number of samples in regards with statistic analysis, we are not able to give an exact figure of the DC breakdown voltage of each sample family (one layer, two layers…). In addition, we are not sure that the breakdown mechanism observed during switching has the same physical origin that the one obtained under DC. The previous protocol allows testing all samples in switching mode and in addition, allows estimating the DC breakdown voltage in the more favorable cases (no breakdown up to the expected operating voltage). The results are summarized in table 5.2 and 5.3.

Table 5.2: Test results 1 (STD: Standard, PC: Parylene Coating, CIP: Cold Isostatic Pressing)

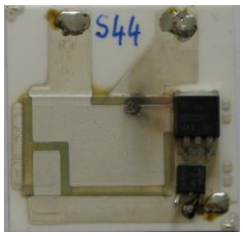
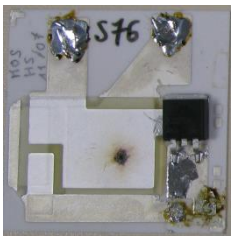
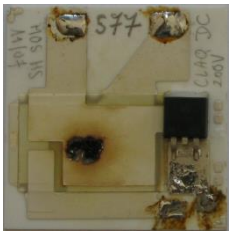
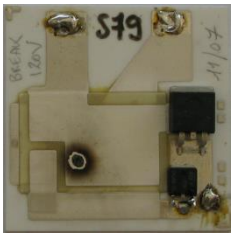
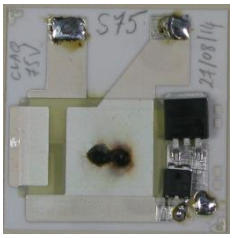
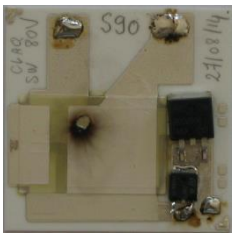
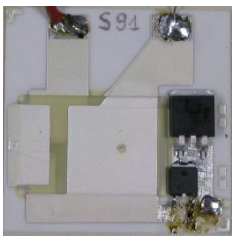
	Sample	**Layers**	**Process**	**V_{Break} SW**	**V_{Break} DC**	**Best operation**	**Degradation view**
1	S81	1	CIP	70V (Still functional)		70V-2A 100kHz	
2	S82	1	CIP		150V (7mA)	100V-5A 100kHz	
3	S44	2	STD	100V		100V-4A 100kHz	
4	S76	2	STD		188V (100mA)	100V-8A 100kHz	
5	S77	2	PC		200V (500mA)	100V-9A 100kHz	
6	S79	2	PC	120V		120V-1A 50kHz	

Table 5.3: Test results 2. (STD: Standard, PC: Parylene Coating, CIP: Cold Isostatic Pressing)

	Sample	**Layers**	**Process**	**V_{Break} SW**	**V_{Break} DC**	**Best operation**	**Degradation view**
7	S48 *(previously damaged in voltage DC test)*	3	STD	60V		60V-2A 100kHz	
8	S75	3	PC	75V		70V-5A 100kHz	
9	S80	3	STD		175V (8mA)	100V-5A 100kHz	
10	S90	3	STD	80V		75V-5A 100kHz	
11	S91	3	PC		140V (7mA)	100V-5A 100kHz	

The three first samples correspond to the "trial and error" phase. For S79, a voltage of too high magnitude has been directly applied. Nevertheless, a low load operating point has been obtained. In case of samples S76 and S77, a load current value too high has been imposed and the MOSFETs have failed. Nevertheless, the substrates were no damaged and the DC breakdown tests may be performed.

The figure 5.13 shows the electrical waveforms obtained with S91. These waveforms are similar whatever the samples. They demonstrate the good quality of the decoupling, the estimated parasitic inductance of the complete cell being around 15 to 20nH. Unfortunately, they also emphasize the decrease of the permittivity value with the DC voltage: in the case under study, the capacitor value at 100V, measured from the voltage ripple, is 650nF, whereas its initial value was 2.94µF. The same trend is observed on all the samples under study.

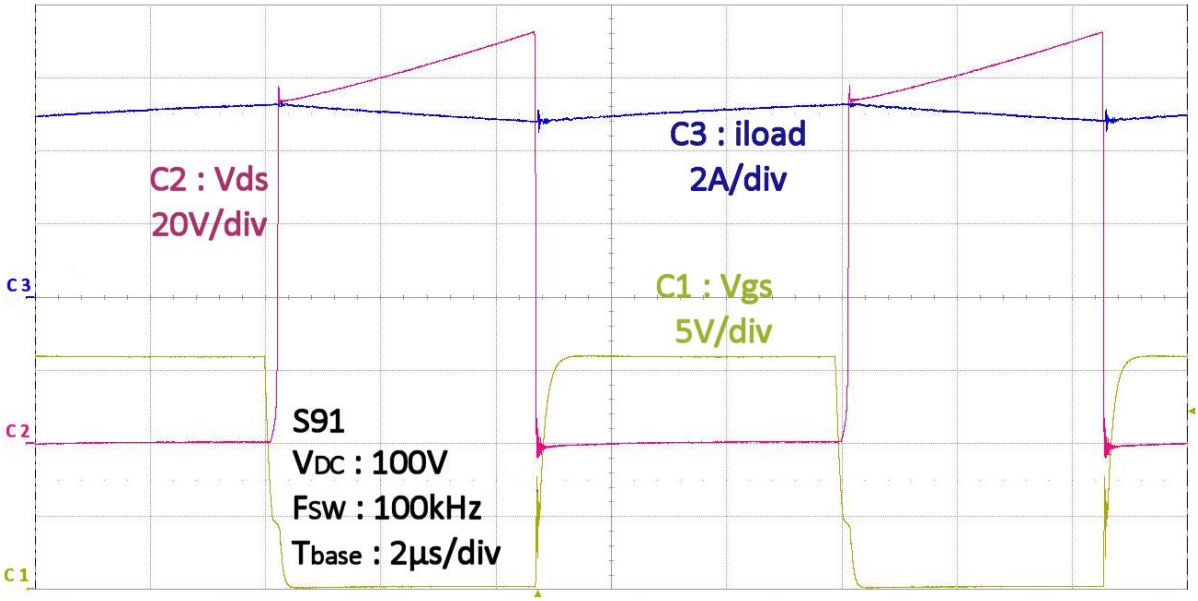


Figure 5.13: Experimental waveforms

The analysis of results given in table 5.2 and 5.3 leads to the following observations/conclusions:

– The dispersion on the withstand voltages is very significant. Conversely to the trend of previous measurements (chapter 3), the number of layers is not really a limiting factor for the withstand voltage. For any family type (in regard with the number of layers), large and low values have been measured .

– The breakdown voltage zones are not localized on the electrodes'edges. This is a very positive result because it demonstrates the relevance of the screen-printing technique to make high voltage devices. Nevertheless, the quality and the reproducibility of dielectric layers have still to be improved.

– As a consequence of the previous observation, the passivation layers, of which the expected function was to limit edge effects, are useless which is confirmed by our (some "standard" samples present a better behavior than the passivated ones)

– The particularly good performances of some samples (S76, S77, S80, S91) demonstrate the validity of the concept.

5.3 Decoupling function in flying capacitor converters

5.3.1 Proposed topology

The demand for high efficient and more compact converters is increasing with the rapidly development of electronic devices in everyday life such as computers, smart phone and automotive electronics. In close proximity to the load, DC to DC converters power the load with regulated low voltage. Typically, the Point Of Load (POL) converters are widely used in the range of a two-stage architecture (Figure 5.14) with an 8-to-12V distribution bus and have voltage outputs from 0.8V to 5V. The emergence of gallium nitride (GaN) transistors offers new perspectives and makes it possible to suppress the intermediate converter commonly used and distribute the 48V throughout the system [63]. This is possible because very short pulses can be achieved by GaN power devices without compromising the efficiency; the high switching speed capability and low on-state resistance of these power components allows reaching better tradeoffs between power density and efficiency than Silicon (Si) transistors.

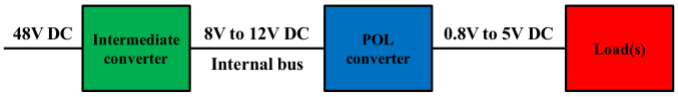


Figure 5.14: Conventional power supply architecture

In order to improve the power density and reduce the converter size, a conventional solution is to increase the transistors commutation frequency. Thus, the values of passive components are reduced and so are the volume and weight. A typical strategy commonly used is to increase the transistors commutation frequency from 100 kHZ to 1 MHz, leading to a significant reduction of the size of passive components but reduces converter efficiency due to the increase of switching losses. To compensate this drawback, series multicell topology is an option to be considered [64]. Interleaving the control signals of the different cells creates an apparent switching frequency that is higher than the effective switching frequency, and the size of the inductor on the low voltage side can be reduced without increasing semi-conductor losses. Moreover, the combination of reduced constraints on switches and reduced current rating and/or breakdown voltage can lead to decrease the total converter losses. Finally, the filter cutoff frequency can be increased leading to a reduction of filters' volume and mass [65]. To achieve both a high density and a

high efficiency, the design of the power board is critical. First, very fast turn-on and turn-off transitions require minimized stray inductances in order to reduce switching losses and overvoltage for safe operation [66]. Second, improved thermal management, such as double side cooling techniques, may be required to extract the heat of the very small GaN devices. However, double side cooling with Thermal Interface Material is not compatible with the use of bulky decoupling capacitors that need to be located very close to the GaN devices to limit voltage overshoots. We propose a solution addressing this question by allowing both a reduction of parasitic inductances and the use of a common heatsink. This result is possible thanks to the integration of capacitors in the substrate using screen-printed capacitors. Without bulky capacitors on the top of the PCB, a common heatsink can be attached to the top of each GaN transistors. The main objective of this part is to demonstrate the feasibility of integrated screen-printed capacitors in a gallium nitride POL converter allowing double side cooling. The DC to DC step-down converter has an input voltage of 48V and an output voltage of 5V and the benefits of integrated capacitors were described in section 1.3.5.3. The next section will present how to realize and characterize the integrated capacitive substrate.

5.3.2 Screen mask design

Integrated capacitors are designed on a 25.4 x 50.8 mm^2 area with a 0.635 mm thick AlN/Al_2O_3 substrate. The substrate presents two distinct capacitors: the smaller is the input capacitor (12.57 mm x 24.4 mm), whereas the larger (29.48 mm x 24.4 mm) is dedicated to the converter's floating function. Electrode positioning was designed to connect with the PCB through 4 holes using assembly technologies such as using Kapton polyimide film; 370HR laminate, and Prepreg or Pyralux FR sheet adhesive. The screen mask drawing for fabricating multilayer, integrated ferroelectric flying capacitors is shown in Figure 5.15. Capacitors are still fabricated from a commercial ferroelectric dielectric (ESL 4212C) sandwiched between two silver layers on an AlN/Al_2O_3 substrate according to process P1 (Figure 2-16). Figure 5.16 shows the 3D construction of the 2-layers capacitive substrate.

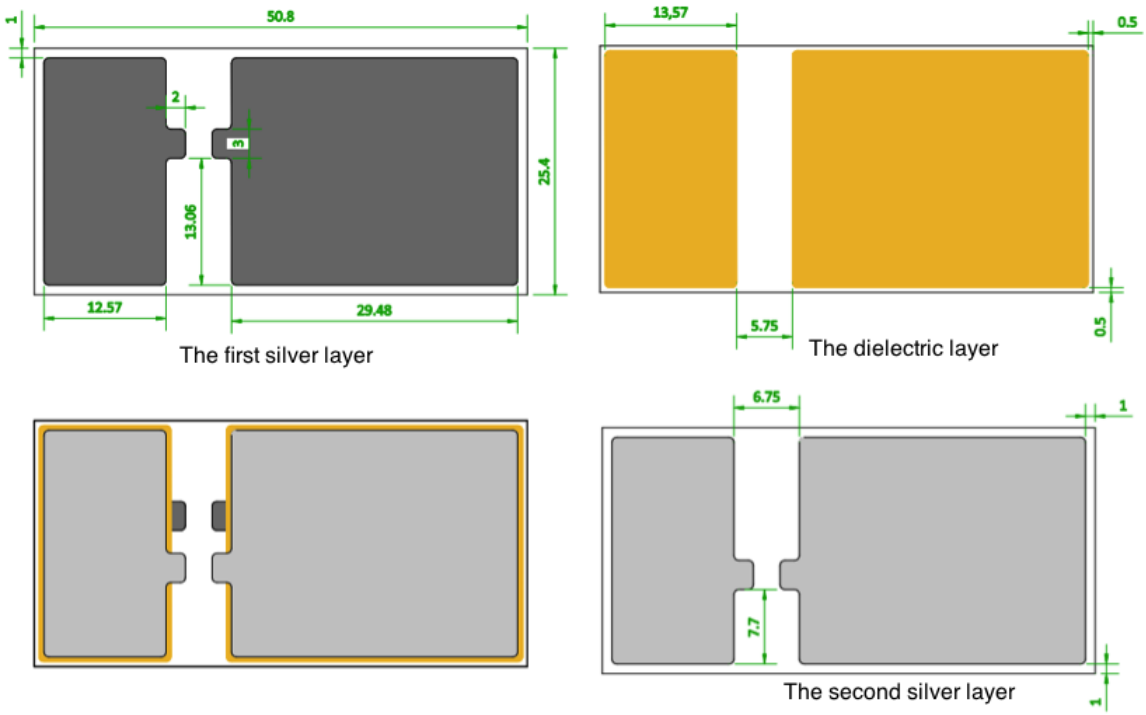


Figure 5.15: Screen mask drawing for flying capacitive substrate.

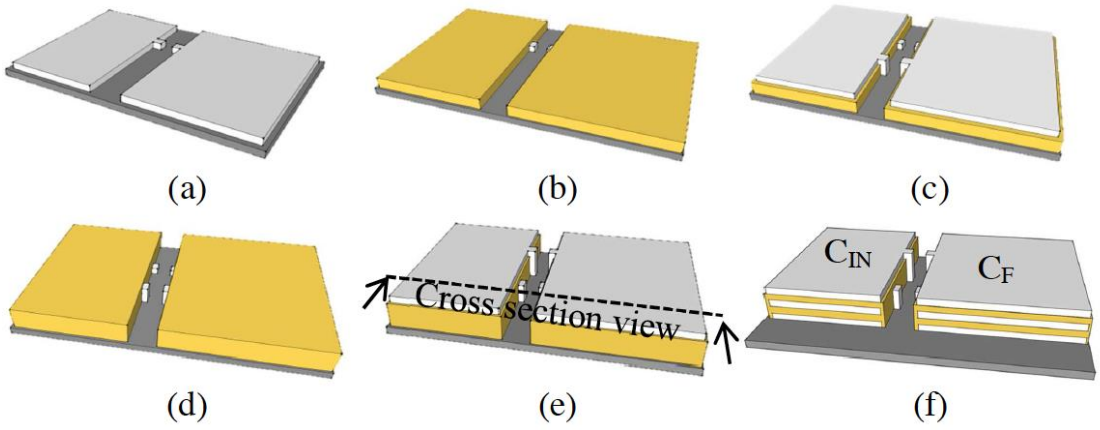


Figure 5.16: 3D construction of the 2 layers capacitive substrate: (a) 1st silver layer on AlN substrate, (b) 1st dielectric layer of 1st capacitor layer, (c) 2nd silver layer of 1st capacitor layer, (d) 2nd dielectric layer of 2nd capacitor layer, (e) 2nd silver layer of 2nd capacitor layer, (f) cross-sectional photo of 2-layers capacitive substrate.

5.3.3 Production

In this first step, we tried to screen-print on the AlN substrate according to the process shown in Figure 5.17. With an extremely interesting combination of very high thermal conductivity (180W/m.K) and excellent electrical insulation properties (>$1.10^{12}\Omega$ /cm), AlN can be a good choice for more efficient cooling on both converter sides. However, the

adhesion on AlN is not as good as on alumina, as shown in Figure 5.18 and Figure 5.19. In the end, we selected alumina as the substrate of the flying capacitor converter.

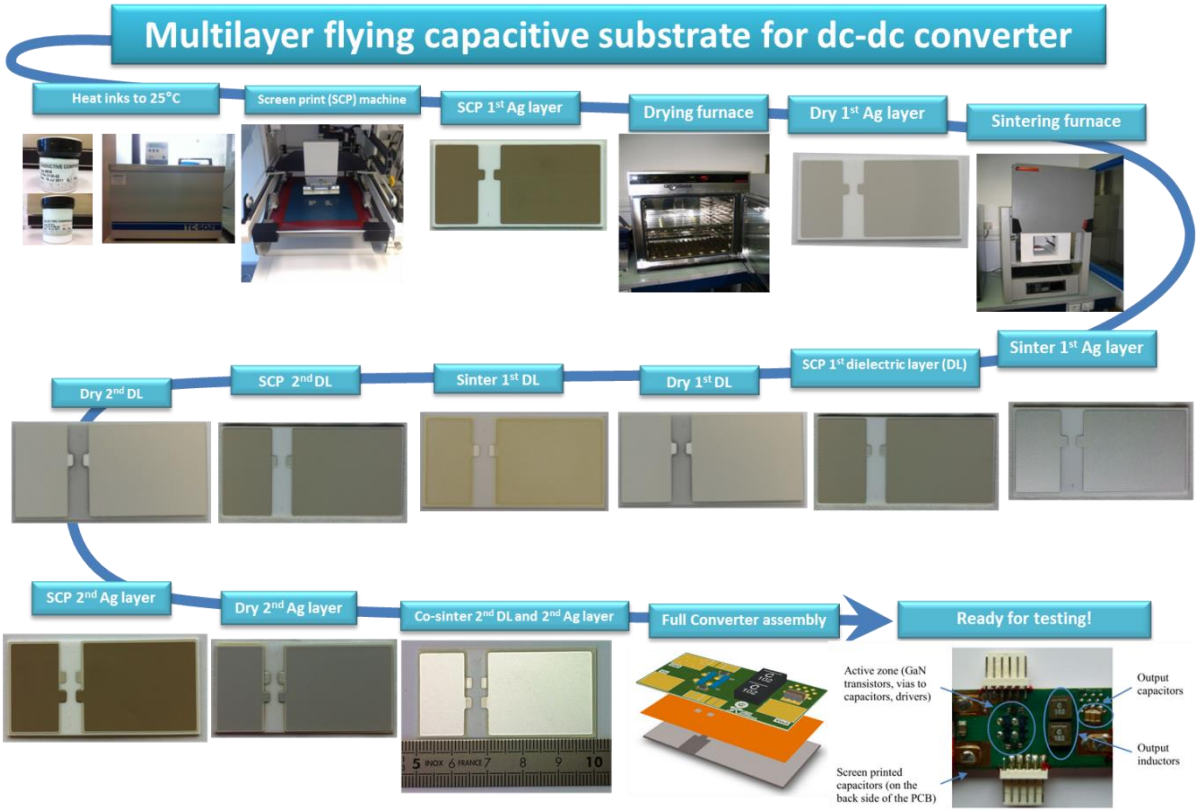


Figure 5.17: Process for fabricating flying capacitive substrate

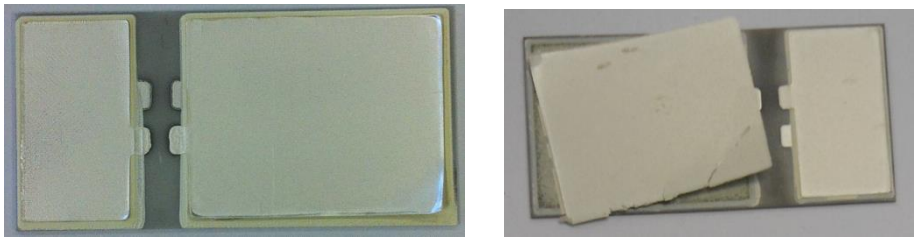


Figure 5.18: Poor adhesion of 1-layer screen-printed capacitor film on the AlN substrate.

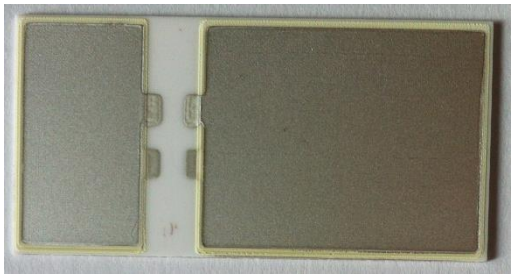
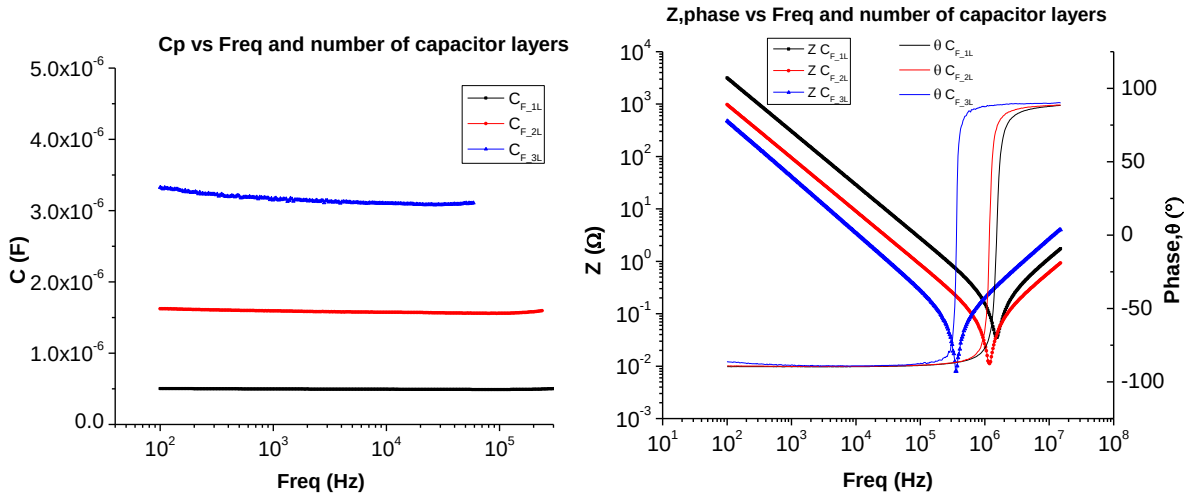


Figure 5.19: Good adhesion of 2-layer screen-printed capacitor film on Al_2O_3.

5.3.4 Characterization

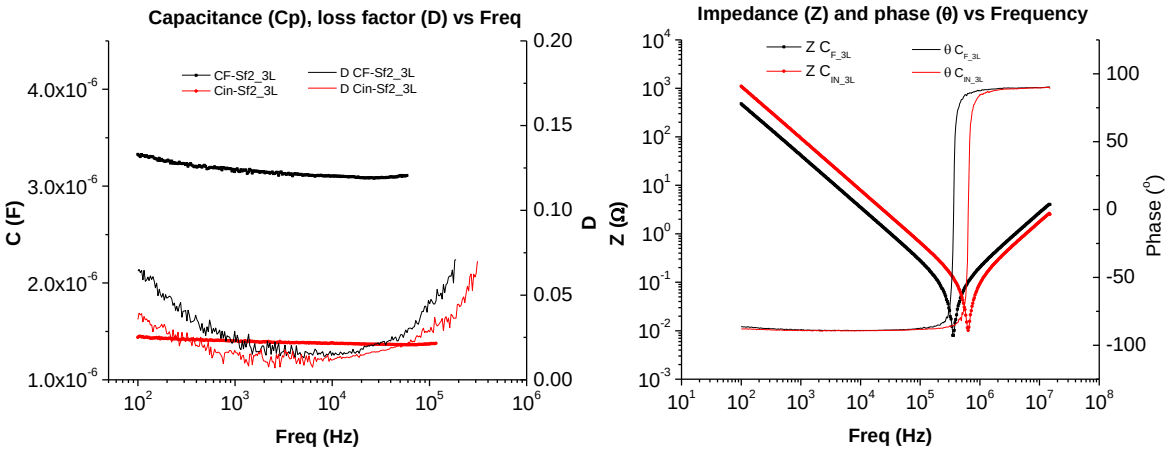
Electrical characterization is performed on flying capacitors and input capacitors using the same methods as those described in Chapter 3. Capacitance and impedance behavior are measured with an HP4191 gain/phase analyzer, and a KEITHLEY 2410 is used for determining leakage current and withstand voltage. Figure 5-20 presents the capacitance and impedance behavior changes of a flying capacitor with respect to the number of layers, under low voltage. The integrated capacitors present a self-resonant frequency around 1MHz related to the capacitance value: the larger the effective capacitor area, the lower the resonant frequency that is a classical result.



(a) (b)

Figure 5.20: Changes of the flying capacitor behavior with the number of layers: (a) capacitance r changes, (b) impedance changes.

Electrical characterization for both input and flying capacitors of the 3-layers substrate are shown in Figure 5.21. With a size of 29.48 x 24.4 mm^2, capacitor C_F presents a capacitance of 3.33µF, resulting in an effective capacitance density of 4.6nF/mm² under low voltage. Similarly, the smaller capacitor C_{IN} (12.57 x 24.4 mm^2) has a capacitance value of 1.44µF, resulting in a capacitance density of 4.7nF/mm² under low voltage. Figure 5.21(b) shows that the resonant frequency of these capacitors is also close to 1MHz.



(a) (b)

Figure 5.21: Behavior of 3-layers flying capacitive substrate: (a) capacitance behavior, (b) impedance behavior.

5.3.5 Full converter assembly

The different layers of full converter are shown in Figure 5.22. The active layer is a multilayer PCB substrate. GaN transistors, drivers and the output filter are located on the first layer. The second layer is a ground plane serving as a shielded layer in order to reduce the lateral power loop inductances, i.e. reduce switching losses and voltage overshoot [67], [68]. Compare to a DBC that has a better thermal features (typical thickness larger than 0.6mm), the PCB substrate is interesting since the insulation layer can be very thin (100µm) allowing to get a high field cancellation effect. The closer the two conductive layers, the smaller the inductances. The ground plane is also used as spreader layer, improving thermal aspects.

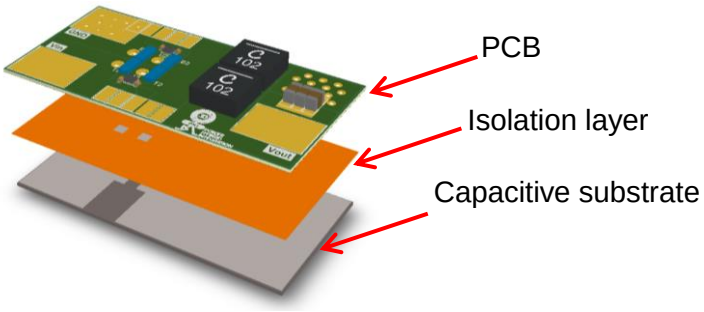


Figure 5.22: The 3D assembly of the full converter (capacitive substrate layer + shielded layer + active PCB layer)

5.3.5.1 **Shielded layer**

A shielded layer is used for propagation of the 0V around the motherboard. The advantages when using a shielded layer to separate active and passive parts are:

- Spreader effect allows limiting the parasitic loop and parasitic effects can be attenuated due to the lateral power loop.
- An opposite field is generated in the shielded layer which will decrease the global loop inductance [63]. This effect, which increases when the distance decreases, is maximized thanks to the small thickness, around 125µm, between the two layers of the converter
- The shieldedlayer also permits a reduction of parasitic loop inductances.

The assembly of the screen-printed capacitors is realized thanks to vias, and with Pyralux® FR200 as electrical insulation layer. The process consists of laminating PCB, Pyralux® FR200 and screen-printed capacitors together under a pressure of 20 bars at 200°C during two hours. This 50.8µm insulation layer provides high dielectric strength (118kV/mm) and a 0.2K/W thermal resistance.

5.3.5.2 **Driving eGaN FET**

For simplicity, the realization was made with half bridge LM5113 driver, which allows using two drivers to control the four devices. These drivers are used in a non-standard way. A driver doesn't control the two devices of a cell but the two top or bottom devices side as shown Figure 5.23(a). The first advantage of this solution is the possibility to separate physically the command from the power, thanks to the shielded layer used for the return path between the load and the source. The second advantage is that, with this configuration, the gate loop is reduced by using screen-printing capacitor as shown in Figure 5.23 (b) and Figure 5.23(c) where the gate loops are highlighted in white. The last advantage is that for more than two cells, the driver hasn't to support the input voltage but only a maximum transistor voltage. The driver is used in 12-bump DSBGA package allowing to be thinner than eGaN FETs in a double side cooling perspective.

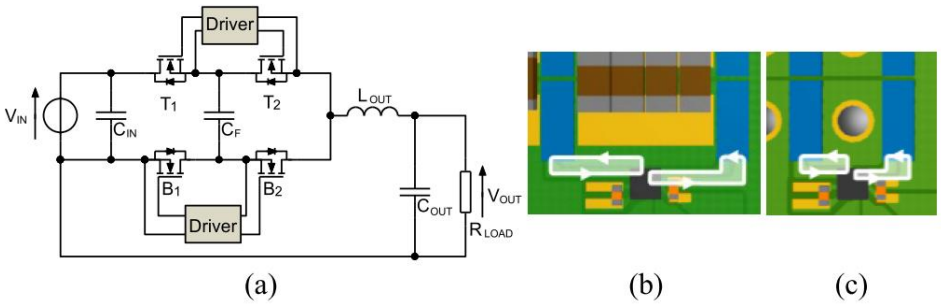


Figure 5.23: Non-standard use of the driver for a parasitic gate loop improvement.

5.3.5.3 **Prototype**

The prototype is shown in Figure 5.24, the active part is composed of eGaNFETs, the drivers, and connections to the capacitors. Since transistors are locally the thickest elements, a double-side cooling solution can be employed. Filtering input capacitor can also be seen in this figure. Its role is to filter the input voltage to limit spike, which is totally different of the function of the screen-printed capacitor located on the input bus. The input screen-printed capacitor C_{IN} is a decoupling capacitor and has to be very close to the commutation cell. Whereas the filtering capacitor can be far from the commutation cell.

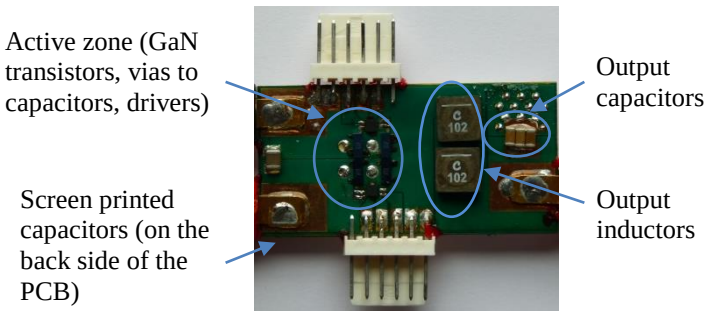


Figure 5.24: Full converter assembly.

5.3.6 Experimental results

The prototype is realized with two-layer screen-printed capacitors of 0.9µF (input) and 2.2µF (flying). The converter is made of four 40V rated GaN (EPC2015) with 4mΩ on-state resistance. The converter is a 48V-5V and has been tested up to 10A under forced air convection and with a maximal operation temperature of 50°C on eGaN FETs. (The dead time is 20ns and experimental waveforms are given in Figure 5.25 for an open loop control. From this figure, it can be seen that V_F, the output voltage before filtering, varies between 0V and 18V or 30V. The theoretical voltage is 24V and the variation is due to an unbalance of the flying voltage, this issue needs to be addressed in the future works. The voltage on inductor is reduced compared with a classical one-cell buck converter. The current on the output inductor I_{LOUT} has a ripple of 4.5A. The switching frequency is 310kHz and the effective output frequency is 620kHz, twice the commutation frequency. Spike on voltage waveforms are due to the parasitic elements of voltage probes (differential probes). The flying capacitor topology allows reducing the constraints on power devices, increasing the effective output frequency and reducing the voltage on output inductor.

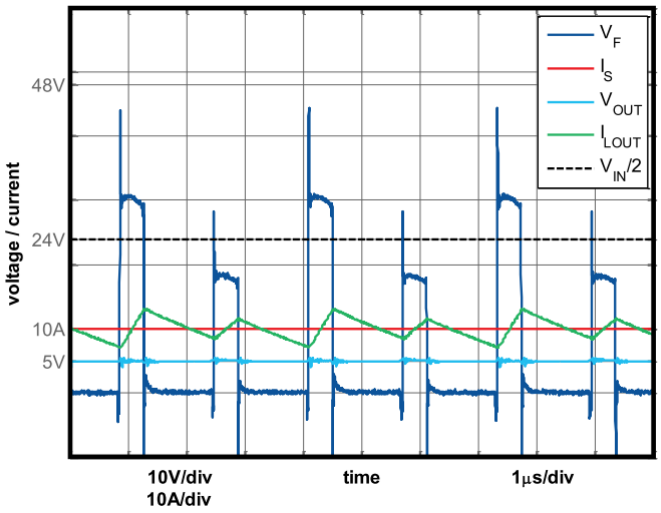


Figure 5.25: Experimental waveforms of voltage before filtering V_F; output voltage V_{OUT} ; current on output inductor I_{LOUT} and output current I_S (48V input and 5V/10A output)

5.4 Conclusions

This chapter implemented the various functions of an integrated capacitor in two proposed DC-DC converter topologies. CAD tools are used to design two different screen-printing masks for two specific application purposes. The integrated capacitors were fabricated successfully based on the process flow P1 proposed at the end of Chapter 2.

The decoupling function was implemented experimentally in a classical buck converter, using a planar, multilayer integrated capacitive substrate with semiconductor devices soldered directly onto the surface. 14 samples have been successfully tested under switching conditions but with capacitor values and voltage rating lower than the expected objective. The dispersion of the dielectric strength is another observation made throughout these tests. These limitations open the door for further research works on methods and process to obtain both a high capacitance value and the desired operating voltage level. An orientation could be to use more dielectric layers with a higher thickness in order to reduce the voltage sensibility of the permittivity while increasing the withstand voltage.

The decoupling in a flying capacitor converter was also implemented with tests on the FC converter in open-loop under 48V input and 5V/10A output. The converter can operate at switching frequency 310kHz and the effective output frequency is twice the commutation frequency. The feasibility of proposed solution using integrated capacitor for double side cooling and to reduce parasitic inductance is possible. The flying capacitor topology allows reducing the constraints on power devices, increasing the effective output frequency; and reducing the voltage on output inductor.

Conclusion and future work

General conclusion

Integrating passive components directly into circuit boards is a well-established idea, but an immature practice. In order to push this solution into commercial applications, it is necessary to determine the right material, technology, and performance level, as well as to obtain high economic benefits. Our work contributes to helping clear up the feasibility of 3D integrated passive components.

The first chapter provides a summary of the state-of-the-art of 3D passive component integration and provides the main objectives of this thesis. The introduction, concepts, benefits, and existing problems of integrated passive components are given and evaluated. An overview of related research presents the technological trend towards building a system-in-a-module for use in power electronics solutions. There are two main trends in passive component integration: the first focuses on integrating individual passive components, such as resistors, inductors, or capacitors; while the second concentrates on the combined integration of several passive components, such as LC and LCT. As any studied trend must be based on distinct materials for each type of passive, further research for optimizing material and technology for each kind of passive (inductive, capacitive, resistive) is still essential. Capacitive integration is more difficult among these passive components than with others due to the sensitivity of dielectric material with frequency and temperature. Though demonstrations of the vast range of available materials and technology have been presented, an absolute optimization still has not been identified. This motivated us in our work to focus on showing the feasibility of ferroelectric screen-printed capacitors for power electronics applications. Two main applied strategies are shown to implement and demonstrate decoupling and flying functions of integrated capacitors in DC-DC converters. The first objective was to implement an integrated DC-DC converter ($P = 2000W$, $V_{in} = 200V$, $I_{on} = 10A$, $F_{sw} = 100kHz$), while a second objective sought to obtain a step-down 48V/5V FC converter.

Chapter 2 presents and analyzes the pros and cons of available materials and technologies for integrating passive components. Among integrated passive technologies, such as LTCC, HDI, thin/thick film, and other PCBs, the screen-printing technique was chosen to print capacitors on the ceramic substrate, notably thanks to its simplicity and low cost. Ferroelectric ceramic, silver, and alumina materials were also selected for, respectively, the dielectric, electrode depositions, and substrate thanks to their compatibility to thick film

process. Moreover, the ferroelectric dielectric has high permittivity making it possible to reach high capacitance density, and low parasitic ESL and ESR. An optimized process is given, and was used to successfully fabricate a good number of different integrated capacitors.

Chapter 3 presents the methodologies for physico-chemical analysis and electrical characterization of integrated capacitors. Results show that integrated capacitors are well-recognized as offering high capacitance density, low parasitic losses, low leakage current, and high dielectric withstand voltage. The ability to establish interdigitated structure is also demonstrated to confirm that the planar, multilayer integrated capacitive substrate is possible.

Chapter 4 presents improvements for integrated capacitor parameters, notably thanks to cold isostatic pressing (CIP). Results show that CIP is an effective way to obtain higher capacitance values for alternative applications in power electronics.

Chapter 5 covers the designs, developments, electrical characterizations of two capacitive substrates for two DC-DC converter topologies. Tests on a full converter unit show the electrical performance in power electronics applications. The decoupling function is implemented experimentally and tested. The flying function is also observed with the converter under 48V input and 5V/10A output. The effective output frequency is 620kHz, twice the commutation frequency, thanks to the flying capacitor topology. The interest of flying capacitor topology in the field of low voltage and low power is shown, and it is demonstrated that flying commutation cells with low stray inductance can be built to allow using today's GaN transistors with promising characteristics. The proposed converter increases efficiency and specific power, reduces constraints on passive and active components, and increases the effective frequency. Integrated screen-printed capacitors are used to allow double-side cooling and to reduce stray inductance on both the power loop and the driver loop. The prototype proves the concept and its feasibility, as a 48V to 5V converter with an output current of 10A.

Future works

Future research work is recommended to further enhance higher levels of integration, notably to:

1. Continue improving the parameters and configuration of ferroelectric integrated capacitors with respect to thermal management and ageing issues to finding greater opportunities for applications. The limitation of integrated capacitors in this research highlights the conflict between the operating voltage, frequency, and capacitance value required for power electronics applications. When capacitance value increases due to a larger number of capacitive layers, both the breakdown voltage and self-

resonant frequency decrease. It is therefore necessary to study innovative configurations to open a broader application range. Thermal management and ageing issues should be studied, with a focus on evaluating the possibilities of specific applications in electronic products.

2. Propose research to demonstrate the applied abilities of integrated capacitors using CIP process. We suggest further studies to demonstrate the performance of integrated capacitors fabricated by processes including cold isostatic pressing. Higher capacitance values can bring stronger effects for decoupling and filtering purposes.
3. Increase the level of integration for FC converters by integrating all capacitors, and even the output inductor, on the same substrate. Embedded technology is an appropriate choice for integrating both capacitors and inductors. With flatter structure, dimensions and the parasitic loop are reduced while the ability for cooling is increased.

Appendices

Appendix A : Screen printing technique

Table A.1-1: Dielectric paste data provided by manufacturer (ESL 4200-C).

RHEOLOGY	Thixotropic, screen-printable pastes
VISCOSITY (Brookfield RVT, ABZ Spindle, 10 rpm, 25.5°C±0.5°C)	210±30 Pa•s
COLOR	Yellow-tan
SHELF LIFE (at 4°C)	6 months
PROCESSING	
SCREEN MESH/EMULSION	200/37.5 µm
LEVELING TIME	10-15 minutes
DRYING AT 125°C	10-15 minutes
FIRING TEMPERATURE RANGE	850°C - 930°C
OPTIMUM	900°C
TIME AT PEAK	10 minutes
TOTAL FIRING CYCLE	60 minutes
SUBSTRATE FOR CALIBRATION	96% alumina
THINNER	ESL 401
SCREEN CLEANER	Acetone, isopropanol, and polar organic solvents
TYPICAL PROPERTIES (Properties based on measurements of 1 mm x 1 mm test capacitors)	
FIRED THICKNESS	**4202-C** 40-55 µm **4212-C** 35-50 µm
DIELECTRIC CONSTANT (k) AT 1kHz (Fired at 900°C, 9516 conductor, measured at 25°C)	
Nominal Value **4202-C** 2,000±300 **4212-C** 12,000±1500	**Capacitance Density** 500 pf/mm^2 3,200 pf/mm^2
DISSIPATION FACTOR AT 1 kHz (25°C)	≤ 3.0%
INSULATION RESISTANCE AT 100 VDC (as fired)	≥ $10^9\Omega$
INSULATION RESISTANCE AT 100 VDC (overglazed with 2 layers of G-481)	≥ $10^{10}\Omega$
BREAKDOWN VOLTAGE (VDC/25 µm, 25°C in air, as fired)	≥ 100
BREAKDOWN VOLTAGE (VDC/25 µm, 25°C in air, overglazed with 2 layers of G-481)	≥ 200
RECOMMENDED CONDUCTORS	9916, 9516, 8816
OVERGLAZES (2 layers separately fired)	G-481

Table A.1-2: Conductive paste data provided by manufacturer (ESL 9916).

RHEOLOGY	Thixotropic, screen-printable paste
VISCOSITY (Brookfield RVT, ABZ Spindle, 10 rpm, 25.5°C±0.5°C)	200±25 Pa•s
SHELF LIFE (at 25°C)	6 months
PROCESSING	
SCREEN MESH/EMULSION	325/25 µm
LEVELING TIME	5-10 minutes
DRYING AT 125°C	10-15 minutes
FIRING TEMPERATURE RANGE	850°C - 930°C
OPTIMUM	900°C
TIME AT PEAK	10 minutes
RATE OF ASCENT/DESCENT	60°C-100°C/minute
SUBSTRATE FOR CALIBRATION	96% alumina
THINNER	ESL 401 or 413
SCREEN CLEANER	Acetone, isopropanol, and polar organic solvents
TYPICAL PROPERTIES (Properties based on measurements of 1 mm x 1 mm test capacitors)	
FIRED THICKNESS	**12.5±2.5µm**
PRINTING RESOLUTION (Line/Space)	125 mm/125 mm
RESISTIVITY	≤ 2.0 mΩ/sq.
SOLDER LEACH (No. of 10 sec. dips to double resistance of 0.25 mm wide x 100 mm long conductor, 62 Sn/36 Pb/2 Ag, 220°C±5°C)	≥7
ADHESION (90° pull, 2.0 mm x 2.0 mm pads, 62 Sn/36 Pb/2 Ag, 220°C±5°C)	
Initial pull strength	≥80 N
Aged 48 hours at 150°C	≥65 N

A.1 Substrate preparation

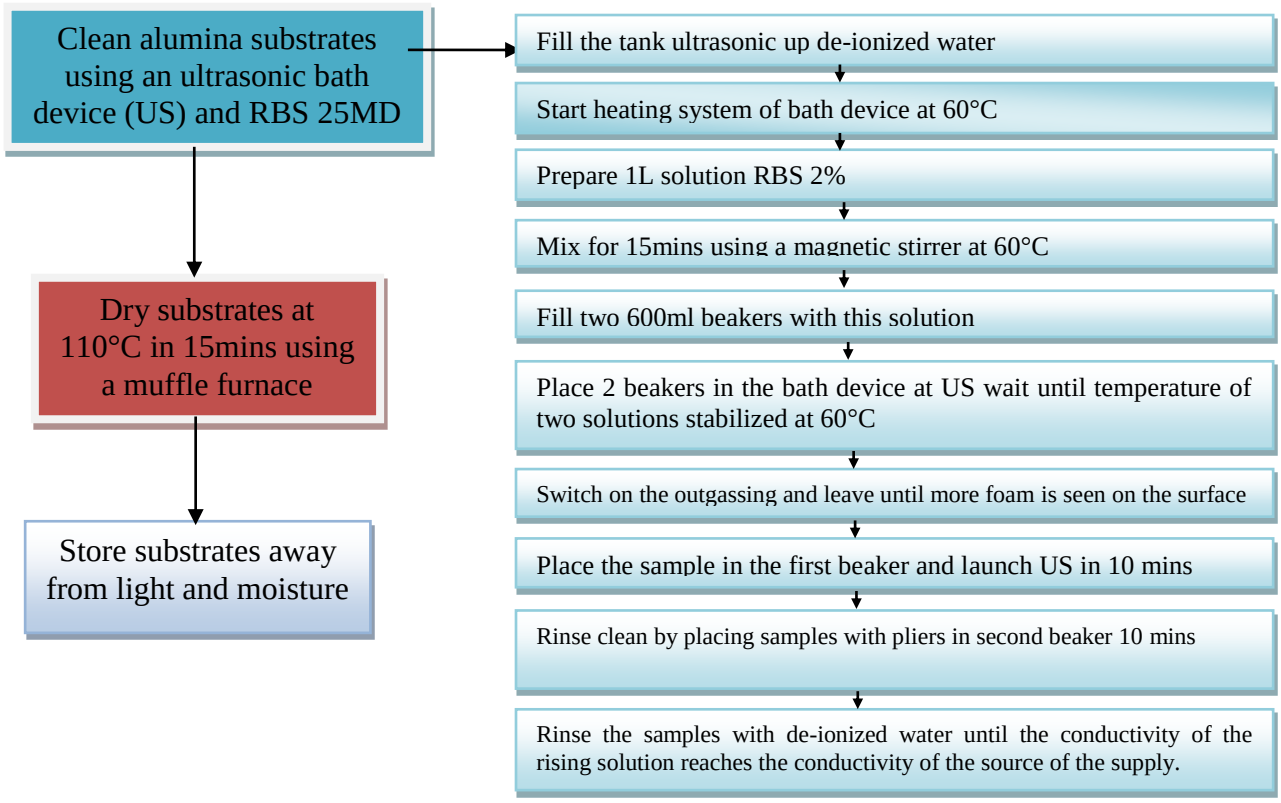
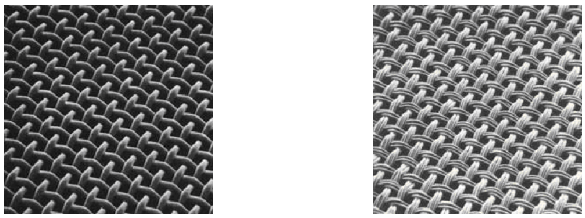


Figure. A-1: Schematic structure for cleaning alumina substrate.

A.2 Screens

Screens are made of stainless steel mesh, which offers the best dimensional stability and a high percentage of open area, allowing paste to pass more easily through the screen. Two types of threads are used for the screen fabric:

- Monofilament (see figure A.2 (a)) - single strands woven into fabric:
  -Primarily used in commercial printing and other applications.
  -Advantage: Monofilament is easier to clean than multifilament.
- Multifilament (see figure A.2 (b)) - multiple strands wound together like rope, then woven into fabric:
  - Primarily used in textile printing.
  - Disadvantage: ink tends to build up on the screen, making it more difficult to clean.
  -



a) Monofilament b) Multifilament

Figure A-2: Screen thread types (source Bopp).

Screen mesh dimensions:

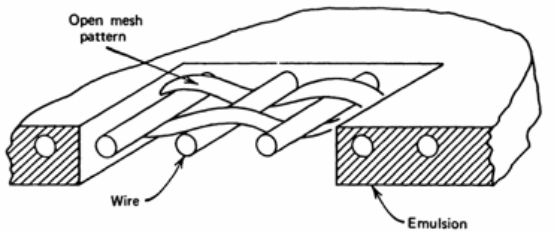


Figure A-3: Print-screen cross-section (source AMI).

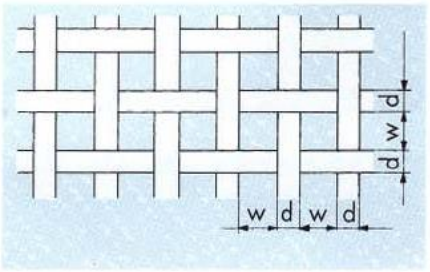


Figure A-4: Mesh dimensions (source Bopp)

w: Width of mesh or mesh opening
d: Wire diameter
Example: Mesh 90/40 means w = 90µm, d = 40µm.

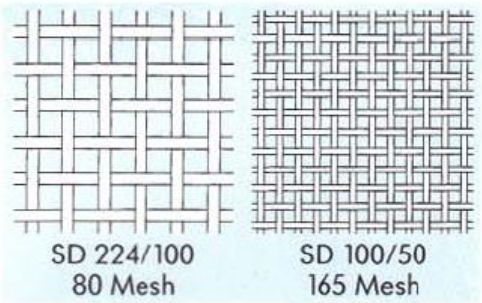


Figure A-5: Mesh count (source Bopp).

Mesh count:

$$\text{MESH}=\frac{24.5(mm)}{w(mm)+d(mm)}$$

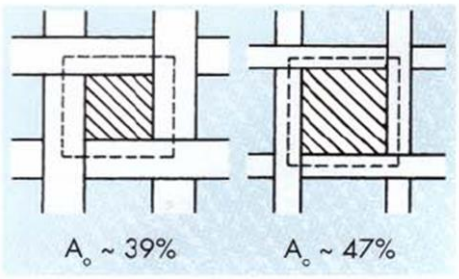


Figure A-6: Mesh surface opening (source Bopp).

Surface opening A_o:

$$A_0 = \left(\frac{w}{w+d}\right)^2 * 100$$

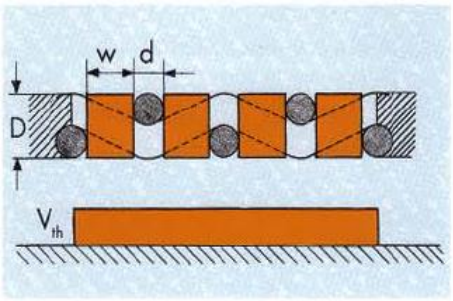


Figure A-7: Theoretical deposited ink volume (source Bopp).

Generally, ink manufacturers suggest a mesh type to suit their materials and provide an appropriate starting point: 200-mesh and 325-mesh stainless steel are probably the most commonly used grades of wire mesh.

The theoretical deposited volume V_{th}

$$V_{th} = \left(\frac{w}{w+d}\right)^2 * D$$

$$V_{th} = TCV = \frac{A_0 * D}{100}$$

V_{th} is expressed in cm^3/m^2. Also called TCV: Theoretical Color Volume, this corresponds to the thickness of the theoretical coating expressed in microns.

A.3 Squeegee

Among all the equipment involved in the screen-printing process, the squeegee is very important because it can affect the overall quality of the product directly. A dull or nicked squeegee does not allow the ink to transfer evenly through the screen. Two squeegees may operate in parallel in different screen-printing modes. The first squeegee pushes the ink through the screen in order to print the mesh pattern onto the substrate. The second squeegee is referred to as the opposite squeegee, whose role is to bring the residual paste across the screen back to the starting position to be ready for the next print. Along with screen mesh and emulsion thickness, the squeegee plays a key role in determining the thickness of the printed material layer. By altering pressure and speed it is possible to vary print thickness by ±20%.

There are three types of squeegees: trailing edge, diamond edge, and knife-edge squeegees, as shown below in Figure A.8:

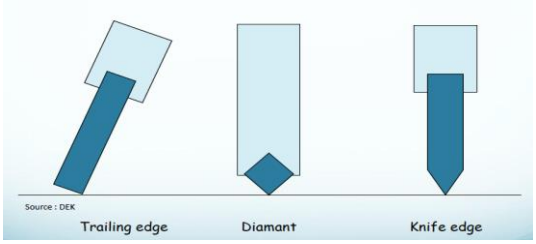


Figure A-8: Types of the squeegee (source DEK)

The trailing edge squeegee is more flexible than the diamond edge or knife edge squeegees. It can yield better results and with more uniformity on uneven substrate surfaces. However, diamond edge and knife edge squeegees are symmetrical, which means that they can print in both directions.

Hardness is the first factor to determine when selecting a squeegee. Plastics/squeegees are measured in various scales of hardness. Shore A scale is the most widely used for measuring squeegee material. Squeegee hardness is evaluated as soft (60A), medium (70A), hard (80A), and extra hard (90A). Squeegee color is used to express its hardness (Figure A.9)

Soft squeegees can provide good prints on uneven surfaces, with thicker coverage, and fewer holes in the printing, but narrow lines may expand and create bridges. Hard squeegees can print surfaces with better definition on other flat surfaces.

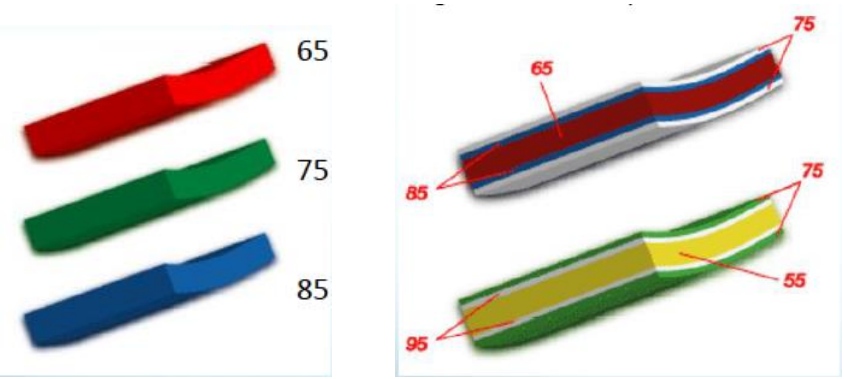
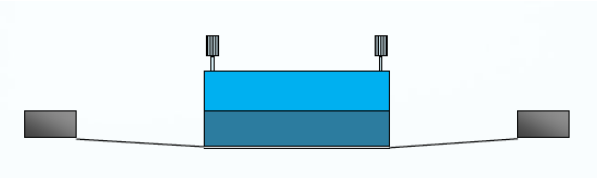
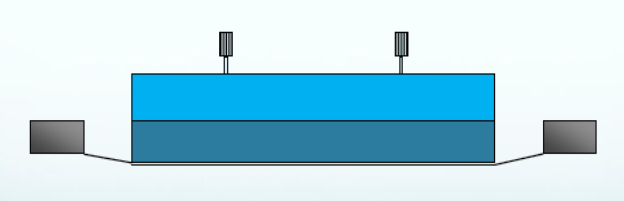


Figure A-9: Squeegee hardness (source DEK).

Squeegee width must be chosen according to the width of the image, generally 20 to 40 mm larger than the image. A squeegee that is too wide requires more downward force onto the screen and may stretch the mesh, which decreases screen life and gives a distorted impression, as shown in Figure A.10.



a) Typical squeegee.



b) Squeegee too wide.

Figure A-10: Effect of squeegee width (source DEK).

Squeegee pressure may be adjusted either by mechanical adjustment or by allowing the squeegee to pivot on its mount. An appropriate speed and consistent squeegee pressure create high quality and uniform thick-films on the substrate. In addition, these factors can avoid smudged prints, print distortion, and screen damage. Thus, proper values are 5-20cm/s and 0.2-0.4kg/cm of squeegee width, respectively. As shown in Figure A.11, when squeegee pressure is too high, it makes an indentation on the screen, which influence subsequent screen-prints.

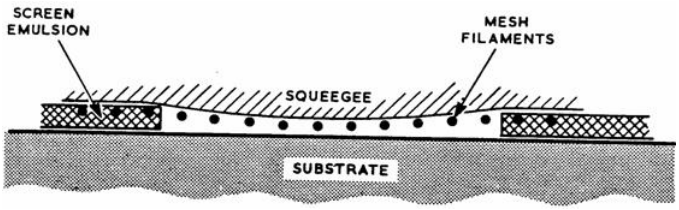


Figure A-11: Effect of excessive squeegee pressure (source AMI).

Squeegee angle is measured between the squeegee and the screen in the direction of the printing stroke. The effective angle is the "real" angle of the squeegee angle during printing. Each printed pattern not only has length and width, but also thickness. The thicker the layer deposited, the more difficult the filling operation. The angle of the front face of the squeegee, in combination with its speed of travel, controls the amount of time available for filling the screen's open areas. Figure A.12 shows how the blade angle affects the filling action. As the angle is reduced horizontally, so is the effective force applied, and the ink can escape under the edge because of the reduced scraping action. Conversely, if the squeegee is overly upright, flexibility and filling time are reduced. It is thus important to choose an angle that offers the best compromise.

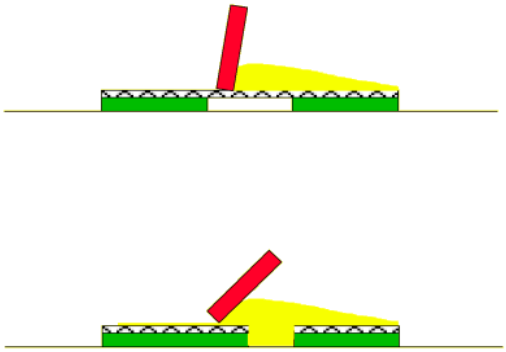


Figure A-12: Effect of squeegee angle (source DEK)

Experimentation showed that a blade with a presentation angle of 60 degrees, which becomes approximately 45 degrees when pressure is applied, gives satisfactory results for the large majority of applications as shown in figure A.13.

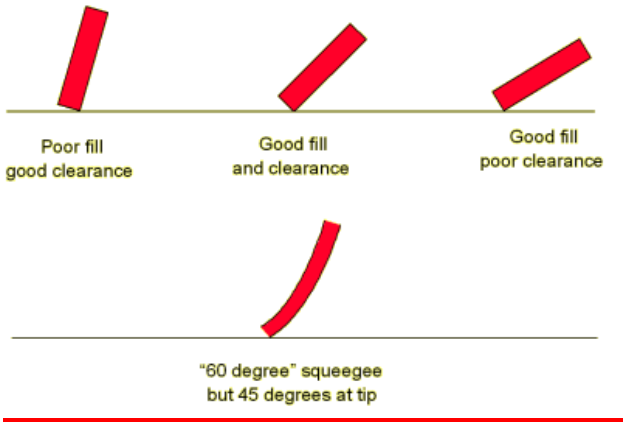


Figure A-13: Squeegee angles (source DEK).

Squeegee selection must take into consideration all the parameters involved for obtaining proper operation and long squeegee life. The squeegee blade is the element that brings the overall printing system together: re-press, image, ink, substrate, and press. Any of these variables that can be controlled must be considered both individually and together.

Appendix B : Main sections of the Aligent-HP4191A gain/phase analyzer

(Source: Agilent technologies)

+ Signal source section

The signal source section generates a test signal applied to an unknown device. The test signal frequency (f_m) and the output signal level are variable. The generated signals are output at the H_c terminal via a source resistor, and applied to the device under test (DUT). In addition to generating the test signal that is fed to the DUT, the reference signals used internally are also generated in this signal source section. Figure B-1shows the signal source section block diagram of the Agilent-HP 4191A precision impedance analyzer. Frequency synthesizer and frequency conversion techniques are employed to generate high-resolution test signals (1 MHz minimum resolution), as well as to expand the upper frequency limit up to 110 MHz.

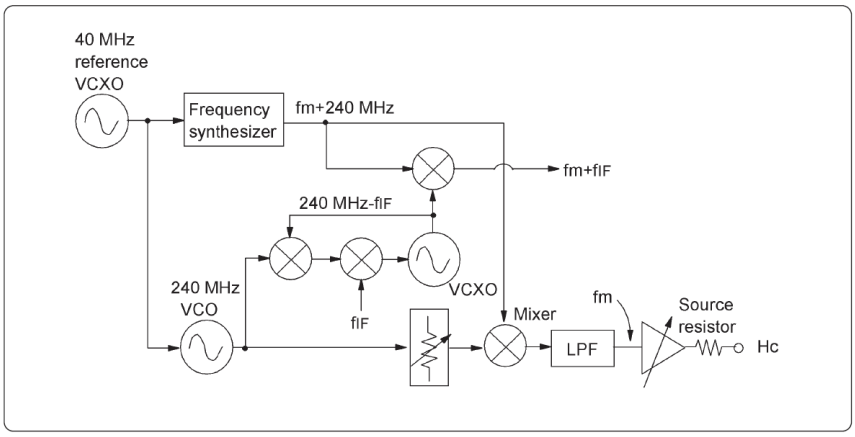


Figure. B-1: Signal source section block diagram.

+ Auto-balancing bridge section

The auto-balancing bridge section balances the range resistor current with the DUT current while maintaining a zero potential at the Low terminal. Figure B-2 (a) shows a simplified circuit model that expresses the operation of the auto-balancing bridge. If the range resistor current is not balanced with the DUT current, an unbalance current equal to $I_x - I_r$ flows into the null detector at the Lp terminal. The unbalance current vector represents how much the magnitude and phase angle of the range resistor current differ from the DUT current. The null detector detects the unbalance current and controls both the magnitude and phase angle of the OSC2 output so that the detected current goes to zero. Low frequency instruments, below 100 kHz, employ a simple operational amplifier to configure the null

detector and the equivalent of OSC2 as shown in Figure B-2(b). This circuit configuration cannot be used at frequencies higher than 100 kHz because of the performance limits of the operational amplifier. The instruments that cover frequencies above 100 kHz have an auto balancing bridge circuit consisting of a null detector, 0°/90° phase detectors, and a vector modulator as shown in figure B-2 (b); (c). When an unbalance current is detected with the null detector, the phase detectors in the next stage separate the current into 0° and 90° vector components. The phase detector output signals go through loop filters (integrators) and are applied to the vector modulator to drive the 0°/90° component signals. The 0°/90° component signals are compounded and the resulting signal is fed back through range resistor (R_r) to cancel the current flowing through the DUT. Even if the balancing control loop has phase errors, the unbalance current component, due to the phase errors, is also detected and fed back to cancel the error in the range resistor current. Consequently, the unbalance current converges to exactly zero, ensuring $I_x = I_r$ over a broad frequency range up to110 MHz. If the unbalance current flowing into the null detector exceeds a certain threshold level, the unbalance detector after the null detector annunciates the unbalance state to the digital control section of the instrument. As a result, an error message such as “OVERLOAD” or “BRIDGE UNBALANCED” is displayed.

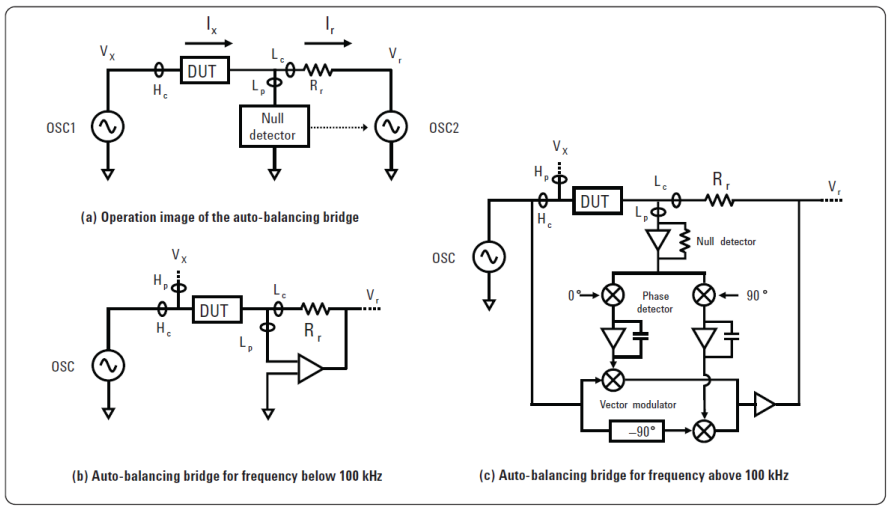


Figure. B-2 : Auto balance bridge section block diagram.

+ Vector ratio detector section

The vector ratio detector (VRD) section measures the ratio of vector voltages across the DUT, V_x, and across the range resistor (V_r) series circuit, as shown in Figure B-3 (b). The VRD consists of an input selector switch (S), a phase detector, and an A-D converter, also shown in this diagram.) The measured vector voltages, V_x and V_r, are used to calculate the complex impedance (Z_x) according to this equation:

$$Z_x = \frac{V_x}{I_x} = R_r \frac{V_x}{V_r}$$

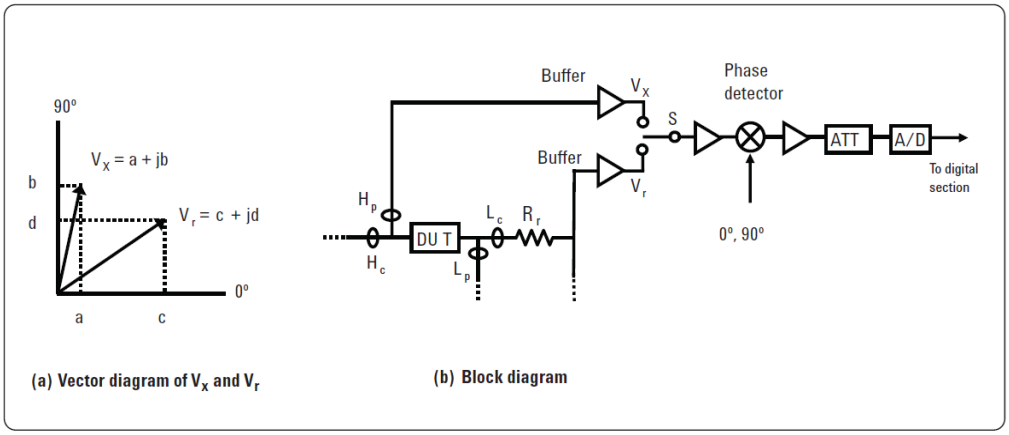


Figure B-3: Vector ratio detector section block diagram.

In order to measure the V_x and V_r, these vector signals are resolved into real and imaginary components, $V_x = a + jb$ and $V_r = c + jd$, as shown in Figure B-3(a). The vector voltage ratio of V_x/V_r is represented by using the vector components a, b, c, and d as follows:

$$\frac{V_x}{V_r} = \frac{a + jb}{c + jd} = \frac{ac + bd}{c^2 + d^2} + j\frac{bc - ad}{c^2 + d^2}$$

The VRD circuit is operated as follows. First, the input selector switch (S) is set to the V_x position. The phase detector is driven with 0° and 90° reference phase signals to extract the real and imaginary components (a and jb) from the V_x signal. The A-D converter next to the phase detector outputs digital data for the magnitudes of a and jb. Next, S is set to the Vr position. The phase detector and the A-D converter perform the same operation for the Vr signal to extract the real and imaginary components (c and jd) from the V_r signal.

The equation representing the complex impedance Zx of the DUT is derived as follows:

$$Z_x = R_x + jX_x = R\frac{V_x}{V_r} = R_r\left[\frac{ac + bd}{c^2 + d^2} + j\frac{bc - ad}{c^2 + d^2}\right]$$

The resistance and the reactance of the DUT are thus calculated as:

$$R_x = R_r\frac{ac + bd}{c^2 + d^2} \qquad X_x = R_r\frac{bc - ad}{c^2 + d^2}$$

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