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Abbreviations

BER	Bit Error Rate
BOX	Buried Oxide
BW$_{EO}$	Electro-Optic -3dB bandwidth
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CoRx	Coherent Receiver
CPS	Coplanar Strip line
CPW	Coplanar Wave guide
DCA	Digital Communication Analyzer
DEMUX	Demultiplexer
DSP	Digital Signal Processing
EAM	Electro Absorption Modulator
ECL	Emitter Coupled Logic
EIC	Electronics Integrated Circuits
ER	Extinction Ratio
EVM	Error Vector Magnitude
FOM	Figure Of Merit
FS-MMSE	Fractal Spacing Minimum Mean Square Error
HPC	High-Performance Computing
InP	Indium Phosphide

IQ	In phase Quadrature Modulator
ISI	Inter Symbol Interference
LES-SiP MZM	Lumped Element Segmented Silicon Photonics Mach-Zehnder Modulator
LiNbO3	Lithium Niobate
LSB	Least Significant Bit
MEMS	Micro Electro Mechanical Systems
MMSE	Minimum Mean Square Error
MOSCAP	Metal Oxide Semiconductor Capacitor
MPP	Modulator Power Penalty
MSB	Most Significant Bit
MUX	Multiplexer
MWP	Multi Project Wafer
MZM	Mach-Zehnder Modulator
NRZ	Non Return to Zero
OBPF	Optical Band-Pass Filter
OOK	On-Off Keying
OSNR	Optical Signal to Noise Ratio
PAM-4	Four-level Pulse Amplitude Modulation
PIC	Photonics Integrated Circuits
PRBS	Pseudo Random Bit Sequence
QAM	Quadrature Amplitude Modulation
OMA$_N$	Normalized Optical Modulation Amplitude
RF	Radio Frequency
RTO	Real Time Oscilloscope
SiP	Silicon Photonics

SiGe	Silicon Germanium
SISCAP	Semiconductor Insulator Semiconductor Capacitor
SOI	Silicon On Insulator
TA-CPR	Training-aided carrier phase recovery
TA-FOC	Training-aided frequency ofset compensation
TSV	Through Silicon Via
TW	Traveling Wave
TW-SiP MZM	Traveling Wave Silicon Photonic Mach Zehnder Modulator
VCSEL	Vertical Cavity Surface Emitting Lasers
WDM	Wavelength Division Multiplexing
3D	Three Dimension

Variables and Symbols

$\mathbf{C}_i$	Capacitance
D	Distance between two adjacent points in constellation diagram when there is no impairment from SiP TW IQ modulator
d	Distance between two adjacent points in constellation diagram when all the impairment sources of a SiP TW IQ modulator are considered
Gbaud	Giga baud
Gb	Giga bit
GHz	Giga hertz
$\mathbf{g}_m$	Intrinsic transconductance of a MOS device
$\mathbf{g}_{ds}$	Output conductance of a MOS device
$\mathbf{I}_D$	Current density
$\mathbf{I}_s$	Current source
$\mathbf{J}_D$	Charge density
L	Length of the phase shifter in a SiP MZM
M	Modulation order in PAM modulation
n	Dopant type n
$n_{o,g}$	Group index of the optical signal
$n_{RF,L}$	RF effective index of the loaded CPS transmission line
p	Dopant type p
$\mathbf{P}_{\alpha L}$	Power penalty induced by optical loss in a SiP MZM
$\mathbf{P}_{ER}$	Power penalty induced by modulation loss in a SiP MZM
$\mathbf{P}_{ISI}$	Power penalty induced by limited electro-optic bandwidth in a SiP MZM
pJ	Pico joule

ps	Pico second
$\mathbf{P}_{in}$	Input optical power
$\mathbf{P}_{out}$	Output optical power
R	Resistance
T	Period of a square wave form
$\mathbf{t}_r$	Rise time
$\mathbf{V}_{ref}$	Reference voltage
$\mathbf{V}_{CLK}$	Clock signal
$\mathbf{V}_{in}$	Input voltage
$\mathbf{V}_{p-p}$	Peak to peak voltage
$\mathbf{V}_b$	Bias voltage
$\mathbf{V}_{RF}$	RF voltage
$\mathbf{V}_{DC}$	DC voltage
$\mathbf{V}_\pi$	Half wave voltage of the modulator
W	Width of a MOS device
α	Optical loss induced by a pn doped optical waveguide
$\Delta\phi$	Phase shift from a pn doped optical waveguide due to applied reverse voltage
$\Delta\tau$	Delay between two adjacent driving channel in CMOS driver
Δ_{ISI}	Difference between the infinite bandwidth eyeopening and the limited bandwidth eye opening
Ω	Ohm
θ_0	Initial phase deference between two arms of a MZM

To my parents,
Esmaeil and Keshvar

"Don't be satisfied with stories,
how things have gone with others.
Unfold ***your own*** *myth."*

Rumi

Acknowledgement

I would like to express my special appreciation and thanks to my Ph.D. director, Professor Wei Shi and co-director Professor Leslie A. Rusch, for all they taught me during my Ph.D. studies. For a multi-discipline project with extensive experimental studies, I faced many challenges but I never felt alone in this way and always had their support and help. Wei is someone you will instantly like and never forget once you meet him. With his ambitious attitude in science, he has been always supportive and has given me the freedom to pursue various projects without objection. He has also provided insightful discussions not only about my researches, but also about my personal life. I am also very grateful to Leslie for her scientific advices and knowledge and many insightful discussions and suggestions. Her patience and passion in teaching and guiding students is unforgettable. Next, I would like to thank the post-doc researcher Dr. Jiachuan Lin with who I spent a lot of my time in the laboratory. I would also like to thank my colleague Amin Yekani who helped me in processing the captured data and simulations. A special thanks to my family. Words cannot express how grateful I am to my mother and father for all of the sacrifices that you've made on my behalf. Your prayer for me was what sustained me thus far. I would also like to thank all of my friends at COPL who supported me in writing, and incented me to strive towards my goal. Omid, Amin, Reza, Sasan, Alessandro thanks for the good times we spent together. At the end I would like express appreciation to my beloved fiancée Barbara, who was always my support in the moments when there was no one to answer my queries.

Foreword

Three chapters of this thesis (chapter 2, 3, and 4) are based on materials published in conference and journal papers. Most of the contents in these three chapters are the same as the journal papers; however, some modifications are made to the introduction of chapters and some supportive material are added for better coherency. I was the main contributor to these papers.

Chapter 2: H. Sepehrian, A. Yekani, L. A. Rusch and W. Shi, "CMOS-Photonics Co-design of an Integrated DAC-Less PAM-4 Silicon Photonic Transmitter," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 12, pp. 2158-2168, Dec. 2016.

This paper demonstrates a Silicon Photonic (SiP) electro-optic transmitter for four-level Pulse Amplitude Modulation without needs for an external electrical digital to analog converter (DAC). This transmitter includes a segmented SiP Mach-Zehnder modulator (MZM) and a co-designed three channel CMOS driver in 130 nm RF IBM CMOS platform. The three segment SiP MZM uses a conventional lateral pn junction process. The three channels CMOS drive receive 2 bits of the input data and map it to driving signal for the three segments of the modulator. Experiment results shows data transmission up to 38 Gb/s. Amin Yekani helped me with post data processing and calculating the bit error rate. I have done the design, simulation and characterization of the segmented SiP electro-optic modulator and its CMOS driver. I have also did the data transmition and prepared the captured data for post processing by Amin Yekani. I wrote the paper and it was revised by the co-authors.

Chapter 3: H. Sepehrian, A. Yekani, W. Shi and L. A. Rusch,"Assessing Performance of Silicon Photonic Modulators for Pulse Amplitude Modulation," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 24, no. 6, pp. 1-10, Nov.-Dec. 2018.

This work investigates the limiting factors that affect the overall performance of a SiP modulator in an optical link running PAM-M modulation format. We have proposed, for the first time, a new figure of merit (FOM) that in contrast to the prior FOMs for SiP modulators, not only consider the modulation efficiency but also the bandwidth limitation of the modulator. We show how this new FOM can be used to design a SiP modulator that presents the minimum power penalty in an optical link. We proved with simulation that the

new FOM could also be used to select optimum SiP process to minimize the power penalty induced by the SiP modulator. I have done all the simulations (Optical and Microwave). I have also used analytical solution to define the new FOM in a closed form function. Wei Shi proposed the initial idea of the new FOM including BW and suggested the definition of normalized OMA. Coauthors were involved in finding exact formation of the FOM through discussions. I have wrote draft of the paper and it was revised by the coauthors, mainly Leslie Rusch.

Chapter 4: H. Sepehrian, Jiachuan Lin, L. A. Rusch and W. Shi, "Silicon Photonic IQ Modulators for 400 Gb/s and beyond," Submitted to IEEE journal of Lightwave Technologies.

In this work, for the first time we present a new design approach for ultra high-speed SiP modulators. As a specific case, we design and optimize a TW-SiP in-phase and quadrature (IQ) modulator for 16-QAM modulation format running at 60 Gbaud. This modulator was fabricated trough IME SOI process. Analyzing the measurement results from data transmission proves that the design procedure proposed in our work is a promising solution to optimize the SiP modulator design or operation condition in order to minimize the power penalty induced by these modulators to an optical link. I have proposed the optimization procedure and proved its reliability trough simulation. I have also done the design, simulation and characterization of the modulator. Jiachuan Lin helped me by the data transmission setup and post processing of the data to plot the bit error rate (BER) for different optical signal to noise ration (OSNR) levels. I have wrote the paper and it is revised by the co-authors.

Chapter 1

Introduction

1.1 Brief history of Silicon Photonics

Researches in Silicon Photonics (SiP) started in 1980s, when for the very first time optical waveguides in silicon-on-insulator (SOI) wafers were investigated [1]. Shortly after, in 1989 Bookham Tech Ltd started to commercialize SiP products. First commercially available SiP devices were limited to some integrated sensory devices (i.e. integrated gyroscopes and pressure sensors) [2]. Shortly thereafter its initial launch, SiP reveals its potential for wavelength division multiplexing application in telecom. Low-cost integration capabilities of the SiP platform paved the way for high-density chips that can perform the multiplexing of many data channels into a single fiber. Realisation of modulators in SOI platform [3] as well as photodetectors based on Ge [4] attracted further attentions to SiP as a practical solution for data transmission applications.

Nowadays, silicon photonic 100 Gb/s transceivers are widely in use for applications such as high-performance computing (HPC), datacenter interconnect, and optical telecommunications. Figure 1.1 shows the main application of the SiP devices. Compatibility with mature

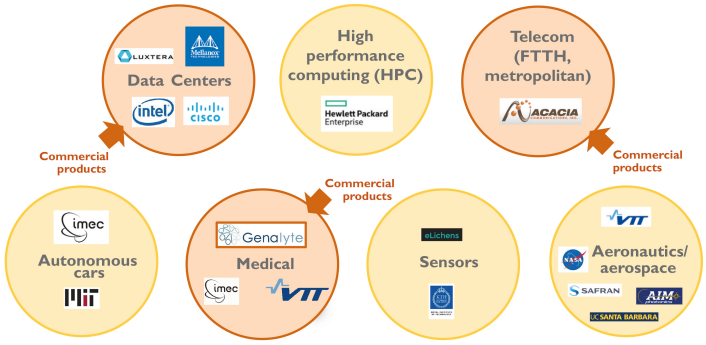
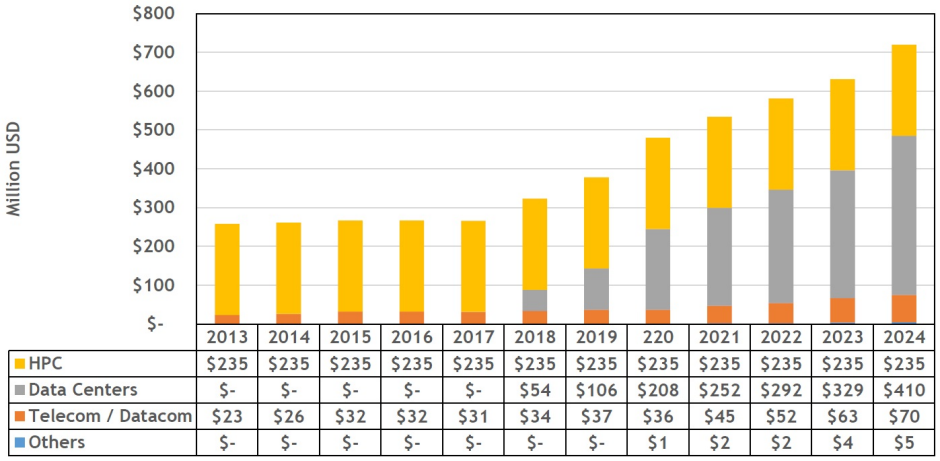


Figure 1.1 – Silicon Photonics application range, Silicon Photonics 2018 report, Yole Développment, January 2018, http://www.yole.fr

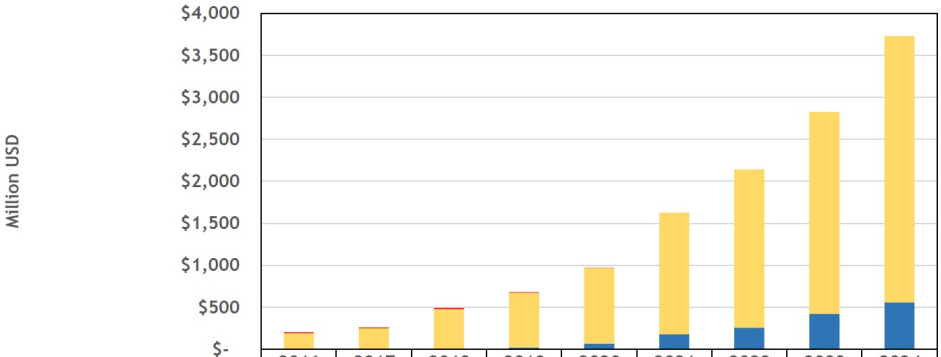
CMOS fabrication process is the main driving force behind silicon photonics platform. This is a key enabling parameter for employing photonics to a range of application where the costs of implementation using traditional photonic elements (i.e. discrete component used for the telecommunications industry) would be prohibitive. This interest in SiP can be observed in figure 1.2 in terms of investment in optical links based on SiP devices. This figure shows that the market interest in SiP is expanding almost exponentially in the next decade.

In spit of SiP advantages and exponential increase in the market interest to optical system based on SiP, there are several challenges in the design of optical systems employing SiP devices. In the next section some of the main challenges will be discussed.



	2013	2014	2015	2016	2017	2018	2019	220	2021	2022	2023	2024
HPC	$235	$235	$235	$235	$235	$235	$235	$235	$235	$235	$235	$235
Data Centers	$-	$-	$-	$-	$-	$54	$106	$208	$252	$292	$329	$410
Telecom / Datacom	$23	$26	$32	$32	$31	$34	$37	$36	$45	$52	$63	$70
Others	$-	$-	$-	$-	$-	$-	$-	$1	$2	$2	$4	$5

(a)



	2016	2017	2018	2019	2020	2021	2022	2023	2024
40G SiP Tranceiver	$11	$9	$12	$9	$4	$-	$-	$-	$-
100G SiP Tranceivers	$191	$251	$475	$651	$900	$1,448	$1,884	$2,401	$3,169
200G/400G SiP Tranceivers	$-	$-	$5	$21	$68	$179	$257	$424	$559

(b)

Figure 1.2 – Silicon Photonics market forecast. a) for different application. b) for different SiP transceivers. Silicon Photonics 2018 report, Yole Développment, January 2018, http://www.yole.fr

1.2 Challenges in SiP integrated circuits

On its way to replace other optical platforms (especially in optical data transmission systems), SiP still faces several challenges that must be addressed. We briefly review these challenges that are shown in figure 1.3.

I. **On-chip laser source:** Replacing external-lasers by on-chip lasers can improve the power efficiency and decreases overall cost of SiP integrated circuits. Although laser sources from III–V material wafers are integrated to SOI wafer using bonding or flip chip [5], [6], implementing low-loss interface between these laser source and SOI waveguide and heat management of the III–V is still challenging.

II. **MUX and DEMUX:** Passive on-chip wavelength multiplexer (MUX) and demultiplexer (DEMUX) are critical for wavelength division multiplexing (WDM) applications. Although arrayed-waveguide grating and echelle–grating [4] are used in SiP integrated circuit to implement MUX and DEMUX function, high optical loss and polarization sensitivity are the main drawbacks of MUX and DEMUX devices implemented in SOI that must be addressed.

III. **Fiber attachment:** Packaging is probably the most expensive part of developing a SiP product. Most of SiP designs use surface grating coupling or edge coupling to couple light into the SOI waveguides. However, high coupling-loss from fiber to wafer and polarization sensitivity of the grating couplers are the main weakness of these coupling solutions that have to be addressed to present a low power SiP product.

IV. **Integration with CMOS:** Cost-efficient and low-power high-speed electro-optic devices need heterogeneous (chip-to-wafer or wafer-to-wafer bonding) or monolithic integration of complementary metal oxide semiconductor (CMOS) drivers to silicon photonics modulators to shorten the electrical signal path (from driver to modulator) and eliminate unwanted parasitic capacitance or inductance from RF signal routing [7], [8], [9]. Although monolithic integration of photonics integrated circuits (PIC) and electronics integrated circuits (EIC) has been recently introduced [10], it is not widely available

Figure 1.3 – Main challenges in Silicon Photonics integrated circuits

mainly because of its high optical loss and bandwidth limitations. Hence, hybrid integration of CMOS and SiP still remains the most promising integration approach [11]. Two main heterogeneous integration approaches for CMOS and SiP chips that are commercially available are hybrid 2.5D and 3D integration:

a) Hybrid 2.5D integration: The 2.5 D approach is based on placing a silicon interposer between the diced die from different technologies and a substrate. The substrate material includes laminates (a form of printed circuit board with fine copper lines), ceramic or silicon. Silicon photonic can benefit from this mature integration technology used in EIC, simply by replacing the silicon interposer [12].

b) Hybrid 3D integration: 3D packaging (heterogeneous chip-to-wafer or wafer-to-wafer bonding of CMOS to silicon photonics) is probably the best available solution for SiP-CMOS integration. Different implementations of this solution have been extensively investigated [13], [14], [15].

V. **Efficient electro-optic modulators:** In optical transmitters, modulation is generally performed by either directly modulating the laser, or by using an external modulator to modulate the output of a laser source. Direct modulation can be more compact, simpler, and cost-effective. However, external modulation can reach higher speeds, has larger modulation-depth, and introduces less distortion. In addition, external modulation can allow other modulation formats such as quadrature phase shift keying. In contrast to other optical material employed to design electro-optic modulators (i.e. LiNbO3, InP) that benefit from their inherent linear electro-optic effect, Silicon is not an ideal material to implement electro-optic modulators. When it comes to design an optimized SiP modulator for a specific system-level application, low modulation efficiency and the lack of a comprehensive figure of merit that could justify the performance of a SiP modulator are the major concerns that must be addressed.

After this summary about the main challenges in the design of silicon PICs, we assess the electro-optic modulation in SiP. Then, we review and compare different modulation methods in SiP and different SiP modulator structures.

1.3 Modulating light in silicon

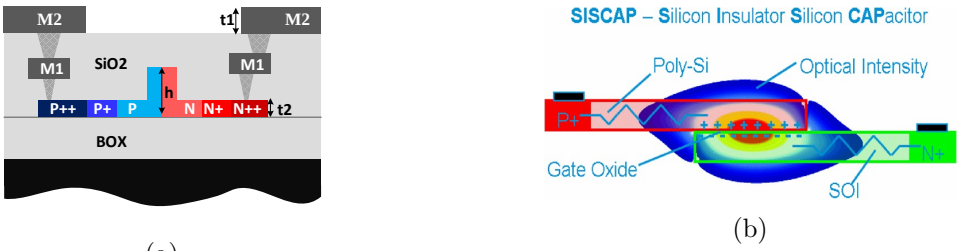
Modulation in silicon is typically accomplished by a change in the effective index or a change in absorption (electro-absorption modulators). A change in effective index causes a change in phase of the optical wave, which can be transformed into a change in intensity using interference, resonance, or slow-light behavior. As it was mentioned in the previous section, silicon by itself does not have any inherent electro-optic effect to be used in light modulation. Although the thermo-optic effect [6] or optical structures based on microelectromechanical

systems (MEMS) [16] can be used for light modulation in silicon, modulation speeds are very limited in these solutions.

The plasma dispersion effect (carrier depletion or accumulation) is the most popular solution for high-speed external modulation in silicon since the beginning of SiP era. Plasma dispersion effect in silicon can be introduced by carrier accumulation, carrier depletion, or carrier injection. Very efficient modulation can be achieved by employing carrier injection to change the carrier densities and modulate the input light. However, due to the long lifetime of the carrier it cannot be used for high-speed modulation (usually limited to less than 1 GHz). In contrast, carrier depletion and accumulation are widely used to implement ultra-fast electro-optic modulators [17], [18], [19]. Diode structures embedded in the center of a silicon waveguide is the most common approach to manipulate the carrier concentration in silicon. Figure 1.4b presents the two most popular diode structures in recently reported works, [20]. Beside these solutions in pure silicon, others materials with strong electro-optic effect can be added to the silicon platform to achieve high-speed modulation. SiGe [21], graphene [22], organics and III–V compounds [23]are some of the materials that are used in silicon platforms to introduce high-speed hybrid modulators. While modulators implemented using these materials recorded very high modulation speeds, complicated fabrication processes and incompatibility with CMOS process limit their presence in SiP products.

1.3.1 SiP electro-optic modulators

An electro-optic modulator is a key component in all data transmission-related applications of SiP platform. As demand for more compact SiP transceiver increases, lower power-consumption reveals its importance in SiP modulator design. Modulators based on resonator or slow-wave structures could be good solutions to decrease the die area and the required driving voltage. Nevertheless, their high sensitivity to the fabrication process, thermal variation, their narrow optical-bandwidth and trade-off between the extinction-ratio and modulation speed, limit their applications. Active feedback has to be implemented for wavelength control



(a) (b)

Figure 1.4 – a) Cross section of lateral P-N junction waveguide employing carrier depletion in A∗STAR's IME, Singapore h= 0.22, t1 = 2, t2 = 0.9 (all the dimensions are in μm). b) Cross section of a SISCAP structure employing carrier accumulation phenomena presented in [20]

which increases the overall power consumption. High-speed electro-absorption modulators (EAM) (usually implemented by using SiGe [7] or the III-V compounds in SOI platform [5]) are the other candidates for compact and low-power SiP electro-optic modulators. In spite of their small foot print, low power-consumption, and high-speed modulation in both sub-micron and multi-micron waveguide platforms, silicon photonics electro-absorption modulators suffer from low extinction ratio and limited optical operating bandwidth.

Conversely, Mach Zehnder modulators operate over wide optical bandwidth and, theoretically, are not sensitive to the temperature variations. Silicon optical modulators based on Mach Zehnder interferometer (SiP MZM) that employ plasma dispersion effect to modulate the light present sufficient reliability for commercial products. They can be fabricated in multi-project wafer runs (MWP) that reduce their fabrication cost especially for fab-less companies. Plasma dispersion SiP MZMs based on carrier-accumulation phenomenon improve modulation efficiency by a factor of five compare to their carrier-depletion counterparts. However, the complex fabrication process to implement doped polycrystalline silicon and the high optical loss are two main down sides of the modulators employing carrier-accumulation to manipulate the refrective index and modulate the input light [24], [25]. On the other hand, as the modulation efficiency in plasma-dispersion SiP MZMs based on carrier-depletion phenomenon is low (in the order of $V_\pi L \approx 1$ V.cm for the best reported phase shifters), these SiP MZMs are long devices as they need long phase-shifter to achieve the appropriate phase shift. This means that traveling wave electrodes have to be used to apply the driving signal to the phase-shifter. Even with such a long phase shifter in the range of several millimetres, SiP MZMs need a large drive signal (due to high V_π of the modulator). Static power consumption of the traveling wave SiP MZM (due to the match load at the end of transmission line) in addition to the high driving voltage lead to high power consumption in the range of few pJ/bit. Impedance matching and managing the velocity mismatch between the RF driving signal and optical signal passing along the phase shifter are the main challenges in design of traveling wave Silicon Photonic Mach-Zehnder modulators (SiP TW-MZM). After all, SiP Mach Zehnder are still the most reliable choice for high-speed modulation in Silicon. Recently, SiP TW-MZM with electro-optic with bandwidth up to 41 GHz has been reported paving the way for design of ultra-high-speed SiP transceivers [26].

1.4 CMOS-SiP transmitters

One of the main driving forces behind the SiP integrated circuits is their compatibility with CMOS process. Integration of optical modulators and CMOS drivers is crucial for high-speed silicon photonic transmitters to reach their full potential for low-cost, low-power electronic-photonic integrated systems. Innovative design solutions in both CMOS and SiP must be employed (i.e. [27]) to achieve this goal. These new solutions should address the high driving voltage of the SiP MZMs by developing new high-speed CMOS circuits or making the

modulators more compatible with typical voltage headroom in sub-micron CMOS platforms (< 2 V). For example, employing multi-segments phase shifter instead of using a single long phase shifter proved to be a promising solution that increases the modulation depth without scarifying the electro-optic bandwidth [28]. Improving the modulation-efficiency of the phase-shifter is another solution that simplify the design of CMOS driver by decreasing the required driving-voltage swing [24], [29], [30]. On the driver side, several successful demonstrations of CMOS or BiCMOS driver are presented [10], [31], [32], [33], [34]. In the next section, we review the design considerations in CMOS drivers. These concerns are different for a multi-segment SiP MZM from a single TW electrode SiP MZM.

1.4.1 Design challenges in CMOS drivers for SiP modulators

When it comes to design the CMOS drivers for SiP MZMs, traveling wave (TW) or segmented electrode modulators have different CMOS design considerations. Drivers for SiP TW-MZMs tend to have lower power consumption compare to their counterpart for multi segment SiP MZM especially at higher baud rates. Authors in [35] proved this fact through an analytical approach. For their specific SiP process, TW drivers are more power efficient compared to multi-segment ones for baud rates higher that 30 Gbaud. However, multi-segment modulators can potentially eliminate the electrical DAC to generate higher order modulation formats and decrease the overall power consumption of a PAM-M or QAM-M transmitter. Challenges in the design of drivers for these two approaches could be summarized as:

I. **Multi-segment SiP MZMs:** In multi segment SiP-MZMs, if each segment is not terminated with load impedance (they are short enough to be considered as a lumped element in the desired frequency range i.e. in [36] and [37]), a full voltage swing can be achieved as each segment presents a capacitive load. CMOS inverter-based structures are the most common driving stage for lumped element segmented SiP MZMs (LES-SiP MZM), where stacked CMOS devices are used to provide higher voltage swing without over stressing the CMOS devices. Combination of lumped-element segmented SiP MZM and their distributed CMOS driver could achieve higher extinction ratio and optical modulation amplitude. However, due to the limited speed of the transistors to charge the capacitive load of each segment, these transmitters are limited in their speed.
   On the other hand, in a LES-SiP MZM, although each segment is free of velocity mismatch between electrical and optical signals, still a precise control of the delay should be realized between RF signals applied to two adjacent segments to prevent velocity mismatch. Although different innovative relative-delay implementations are proposed (i.e. [36] and [37]), the generation of small delays (for higher speed transmitters) with high fabrication-yield is still challenging.

II. **Traveling wave electrode SiP MZMs:** Traveling wave electrode drivers usually use current mode logic (CML) or emitter coupled logic (ECL) stage to drive the resistive

load from the transmission line. However, microwave losses and the limited bandwidth of the transmission line implemented in SiP platform limit the overall bandwidth of the modulator. Moreover, propagation loss in these transmission lines leads to lower modulation depth for p-n junctions placed far from the launched point of the RF driving signal. It means that the input light is not modulated efficiently (evenly) along the phase shifter length. Also, due to the resistive load (from termination in traveling wave electrode), providing full voltage swing needs large current flow from the last stage of the CMOS driver. However, the parasitic capacitance from wide paths (to support high current flow) in layout of the CMOS driver limits the bandwidth of the driver.

So far, challenges in the design of silicon photonics modulators and their CMOS drivers have been reviewed. The next section presents the structure of this thesis as well as our motivation to perform research in CMOS compatible silicon photonic optical modulators.

1.5 Thesis structure

1.5.1 Motivation

Co-design of SiP PIC and CMOS EIC is crucial to reveal the great potential of SiP for integrated, high-capacity and cost-efficient optical transmitters. Co-designed SiP-CMOS transmitters target short/mid-reach applications, where integrated high-capacity transmitters are highly demanded. Although there are some demonstrations of co-designed SiP PIC and CMOS EIC, either custom SiP process is used to implement the transmitter [31] or the transmitter is just capable of low spectral-efficiency modulation formats (i.e. on-off keying (OOK)) [37]. There is a high demand for new co-designed SiP CMOS transmitters that not only employ widely available generic silicon photonic process but are able to perform higher order modulation formats (i.e PAM-M). Moreover, a figure of merit is needed to quantify the performance of a SiP modulator. None of the previous efficiency-based FOMs (V_π.L or $V_{\pi\cdot\alpha}$.L) is able to predict the system level performance of the SiP modulator in a real optical link. This limitation can be attributed to the absence of the modulator electro-optic bandwidth in the FOM. A new figure of merit must be developed that includes not only the optical loss (α) and efficiency (V_π.L), but also the SiP modulator electro-optic bandwidth, BW_{EO}. This new FOM could map SiP modulator physical design parameters to its system-level performance, facilitating both device design and system optimization. Finally, when it comes to the design a modulator, minimizing the power penalty induced by the modulator is a crucial factor to maximize its system-level performance. A system-oriented design methodology must be developed to optimize SiP modulators' design or bias point for a specific system-level concept. After presenting our motivation for this thesis, in the following we briefly describe each chapter of this thesis and highlight the main contributions in each of them.

1.5.2 Chapter 2: SiP modulators for PAM modulation for short/mid-reach applications

Four-level pulse amplitude modulation (PAM-4) is under standardization and active development as a cost-effective solution for emerging 100 Gb/s and 400 Gb/s short/medium-reach systems. However, cost and power consumption of the electrical DAC required for multi-level signal generation is the main drawback of the PAM-4 modulation format that grows exponentially as the number of optical links increases in data centers and interconnects. In the first chapter, we investigate the co-design of CMOS and SiP by design, simulation, and characterization of a DAC-less PAM-4 transmitter. This transmitter includes a three-segment SiP MZM and a three-channel CMOS driver. This demonstration paves the way for fully integrated DAC-less optical links in short/mid reach applications. According to the target baud rate (20G baud), each segment of the SiP MZM is designed as a lumped element that eliminates the 50 Ω match load for each segment. This approach helps to save power compared to the traveling wave structure while making it possible to have a full voltage swing from the CMOS driver for each segment. In the CMOS driver, a new strategy for delay generation between the two adjacent driving channels is proposed and implemented. As the new delay management scheme is based on the difference between the generated delays rather than its absolute value, it decreases the effect of process variation on small delay generation. The CMOS driver uses a high-speed decoder to map the input binary data to the number of segments that have to be driven. Current mode logic latches are used in the input decoder to satisfy the bandwidth requirement. In the output stage of the driver we have used an inverter based stacked CMOS structure to prevent over stressing of CMOS devices. This DAC-less SiP PAM-4 transmitter is the first one of its kind using a lateral p-n junction for SiP modulator. I have designed both the CMOS driver and the SiP modulator. Also, I have done their characterization and the data transmission. My colleague Amin Yekani did the off-line data processing of the captured data.

Main contributions:

1) Designed and characterized a SiP transmitter that generated PAM-4 without need of a DAC.
2) Co-designed a CMOS driver compatible with the Segmented SiP PAM-4 modulator.
3) Investigated effect of delay errors on output of the transmitter.
4) Developed novel delay management for robustness to fabrication errors.

1.5.3 Chapter 3: Tools for Design and Performance of SiP MZM for PAM

Several high performances SiP modulators are reported. Although these modulators have achieved low bit error rates (BER) at high symbol rates, they have not necessarily achieved an optimal design for a given system context. To design an optimized electro-optic modulator,

specific system-level criteria and performance quality factors have to be considered. These factors could be different for an integrated optical modulator compared to its stand-alone discrete counterpart. To date, the efficiency V_π.L is employed to quantify SiP modulation performance. Although this figure of merit clearly shows the trade-off between the modulator length and the required voltage for π radian phase shift, it does not include the significant optical loss introduced by the phase shifter. More recently, $V_\pi \alpha$L (known as efficiency-loss) is used to quantify SiP modulation performance, where α parametrizes optical loss induced by the phase shifter. Moreover, in contrast to other electro-optic platforms (i.e., LiNbO3), V_π of a SiP modulator is not a linear function of L (nor the applied voltage). Hence, the efficiency of the SiP modulator changes with its length. None of the prior efficiency-based FOMs (V_πL or $V_\pi \alpha$L) are able to predict the system level performance of the modulator in a real optical link. This limitation can be attributed to the absence of the modulator electro-optic bandwidth in these FOMs. For the first time, we introduce a new figure of merit that includes not only the efficiency of the modulator, but also the bandwidth limitation from SiP electro-optic modulators. The new FOM translates the system-level requirements of a PAM-M optical link to the device-level design parameters. Amin Yekani helped me in the initial simulation process by verifying the equations that predicts the pulse response of the modulator.

Main contributions:

1) Introduced a comprehensive equation for the system power penalty of a PAM SiP modulator (MPP) including optical loss, modulation loss and limited bandwidth.
2) Demonstrated current figures of merit (FOMs) do not optimize MPP.
3) Demonstrated via simulation that optical modulation amplitude is a reliable indicator of MPP.
4) Developed a novel and simple closed-form figure of merit (FOM) that can optimize MPP using parameters that are readily measured.
5) Demonstrated the new FOM can predict the optimum phase-shifter length, bias voltage or driving signal in a specific process.
6) Investigated the effect of variation in process on performance of the SiP modulators via the new FOM.

1.5.4 Chapter 4: Optimization of Silicon Photonic IQ Modulators for 400 Gb/s and beyond

Next-generation coherent optical transceivers, targeting 400 Gb/s and beyond, are under active research and development. In spite of several successful demonstrations with high-capacity systems, both with direct or coherent detection, a gap between optimization efforts in the design of SiP modulators and in the choice of system-level operating points still exists.

A joint optimization of both modulator design and system parameters, could further push performance. Most of the previously reported work focused on maximizing the electro-optic bandwidth of the modulator (BW_{E-O}) or on increasing the modulation efficiency by lowering the modulator V_π (to make it more compatible with small-swing CMOS drivers). Three main factors affect the output of the modulator and limit the optical signal to noise ratio (OSNR): optical loss, modulation loss (coming from limited extinction ratio due to high V_π), and inter-symbol interference (ISI) induced by limited electro-optic modulator bandwidth. These three penalty sources are intricately intertwined. Minimizing each of them separately does not necessarily minimize the overall modulator-induced penalty. Inspired by our investigation in the previous chapter, we propose a new design minimizing the modulator-induced power penalty for quadrature amplitude modulation (QAM) transmission. We target 16-QAM at 60 Gbaud to achieve 200 Gb/s per channel for a single polarization. To verify the proposed optimization approach experimentally, we isolate the SiP modulator imperfections from other transmitter impairments (e.g., from the digital to analogue converter (DAC)). We do not pre-compensate for the limited bandwidth of the modulator. We push the baud rate up to 70 Gbaud, despite exceeding the device bandwidth, to probe the device's capacity. Jiachuan Lin helped me with the data transmission setup and post processing of the data to plot the BER for different OSNR levels.

Main contributions:

1) Developed a novel design technique to minimize MPP for a CMOS-compatible SiP In phase Quadrature (IQ) modulator for various modulation formats and rates.
2) Designed and characterized the first system-oriented optimized IQ modulator using lateral pn junction SiP traveling wave MZM.
3) Experimentally proved the reliability of the proposed design technique.
4) Experimentally demonstrated modulation beyond 400 Gb/s with this modulator.

Chapter 2

CMOS-Photonics Co-design of an Integrated DAC-less PAM-4 Silicon Photonic Transmitter

Résumé — La co-conception et l'intégration de modulateurs optiques et du controleur CMOS sont cruciales pour que les transmetteurs photoniques sur silicium à haute vitesse atteignent leur plein potentiel en tant que des systèmes intégrés électroniques-photoniques en terme de faible coût et à faible puissance. Dans ce chapitre, nous présentons un transmetteur optique multiniveau SiP controlé par une puce CMOS mis en œuvre en utilisant un processus de jonction p-n latérale commercial. Il utilise un modulateur Mach-Zehnder segmenté pour augmenter la vitesse et abaisser la puissance requise par segment jusqu'à un niveau réalisable avec une puce CMOS. Un controleur multicanal est conçu et implémenté dans un une puce CMOS RF en utilisant la technologie 130 nm, pour une oscillation de 4 V dans une configuration push-pull à 20 Gbaud. Les données binaires à l'entrée de la puce CMOS sont manipulées via une logique numérique pour produire les signaux d'attaque par segment appropriés ; ceci dans le but de générer un signal optique à modulation d'amplitude d'impulsion à quatre niveaux. La modulation à plusieurs niveaux est obtenue en utilisant uniquement des signaux binaires en entrée (sans DAC). La co-simulation des circuits optiques et électriques sont cohérents avec les résultats expérimentaux . Une transmission fiable a été obtenue sans post-compensation à 28 Gb/s et à 38 Gb/s en post-compensation.

Abstract — Co-design and integration of optical modulators and CMOS drivers is crucial for high-speed silicon photonic transmitters to reach their full potential for low-cost, low-power electronic-photonic integrated systems. In this chapter, we present a CMOS-driven SiP multi-level optical transmitter implemented using a commercially available lateral p-n junction process. It uses a Mach-Zehnder modulator segmented to increase speed and to lower the required power on a per segment basis to a level achievable with CMOS. A multi-

channel driver is designed and implemented in 130 nm RF CMOS technology, providing a swing of 4 V in a push-pull configuration at 20 Gbaud. Binary data at the CMOS input is manipulated via digital logic to produce the proper per-segment drive signals to generate a four-level pulse-amplitude modulation optical signal. Multi-level modulation is achieved using only binary signals as input (DAC-less). Co-simulation of the optical and electrical circuits shows good agreement with experiment. Reliable transmission is achieved without post-compensation at 28 Gb/s, and at 38 Gb/s when using post-compensation.

2.1 Introduction

Power and cost-efficient data transmission solutions through optical interconnects are required for rapidly growing short and mid-reach markets such as data centers and ultra-high-speed computing. Data hungry applications (social media, video streaming, big data, etc.) are growing at a fast pace, driving the need for high-capacity data transmission. Next-generation optical interconnects in data centers must run beyond 25 Gb/s per optical carrier. Four-level pulse amplitude modulation is under standardization and active development as a cost-effective solution for emerging 100 Gb/s and 400 Gb/s short/medium-reach systems [24], [25]. Optical interconnects were conventionally dominated by multimode fiber-optic links using vertical cavity surface emitting lasers (VCSELs) [38].

However, they suffer from severe modal dispersion and, in general, transmission is limited to several hundred meters [39], [40]. In the last decade, silicon photonics has quickly emerged to meet the demand for high-speed, low-power optical transceivers. Their commercialization is being studied for a variety of communications applications, such as intra-chip and inter-chip interconnects, short-reach communications in data centers and supercomputers, and coherent optical transmissions [31], [41]. As power consumption and cost are main concerns for these applications, hybrid integrated silicon photonics modulators combined with CMOS drivers are ideal embodiments of high-speed PAM transmitters.

Recent progress has revealed the great potential of silicon photonic PAM modulators [42], [43]. A silicon microring modulator achieved 80 Gb/s PAM-4 with an ultra-low power consumption below 7 fJ/bit [44]. However, microring modulators exhibit high thermal sensitivity. Precise wavelength stabilization circuits must be used to overcome this limitation. Wavelength stabilization will increase power consumption, one of the main concerns in short and mid-reach applications. Mach-Zehnder Modulators remain the most promising candidate for commercial systems because of their thermal insensitivity and high tolerance to fabrication imperfections. More compressive reviews on silicon photonic modulators can be found in [45], [46].

Traditionally, optical PAM is achieved by means of an electrical digital to analog converter furnishing a four-level electrical drive signal to an electro-optic modulator. Although flexible for advanced signal processing, the high-speed DAC is a significant source of power consumption; for PAM modulation that flexibility is usually unneeded. DAC-less PAM-4 can be achieved via segmented MZMs. Segmented silicon MZMs with high-power RF amplifiers achieved 100 Gb/s PAM-4 in [43], where two travelling-wave electrodes with different lengths were used for the least and the most significant bits (LSB and MSB).

Integration of CMOS drivers with SiP provides a low-power solution for high-speed optical transmitters [47], [19]. Recently several co-designs of segmented SiP MZMs with CMOS drivers been reported; for example, a 25 Gb/s on-off keying (OOK) transmitter [37], where

six lumped segments in an MZM were driven by a low-power driver in 65 nm CMOS. A DAC-less PAM-4/PAM-16 transmitter [31] is another example, where vertical pn-junctions were used as optical phase shifters in a segmented MZM.

In this chapter, we present a DAC-less PAM-4 transmitter which includes a multi-channel driver in 130 nm CMOS and a co-designed single-drive parallel push-pull SiP MZM. The segmented modulator is implemented by a commercially available lateral p-n junction process. Reliable transmission is achieved without post-compensation at 28 Gb/s, and at 38 Gb/s when using post-compensation.

The rest of this chapter is organized as follows. In section 2.2, an overview of design strategy is presented. The design and simulation of our proposed segmented MZM is presented in section 2.3. The principle and design of the CMOS driver is explained in section 2.4. Section 2.5 presents the co-simulation results of the CMOS driver and LES-MZM. Finally, we offer experimental system results in section 2.6 and concluding remarks in Section 2.7.

2.2 Overview of Design Strategy

2.2.1 Lumped Element Segmented MZM solution

The performance of an MZM is characterized by parameters such as analog bandwidth, voltage swing required for a π phase shift (V_π), and insertion loss [17]. Simultaneous achievement of low V_π and high bandwidth is crucial for low power operation at high data rates. Most of the existing SiP MZMs applied TW electrodes with continuous phase shifters [48]. High-speed optical modulation in silicon is typically achieved in reverse-biased p-n junctions embedded in optical waveguides. Due to the relatively weak electro-optic effect, a long optical phase shifter is required for a CMOS-compatible driving voltage, making high bandwidth challenging due to the RF losses along the p-n junction loaded electrodes and the velocity mismatch between RF driving signals and optical waves. In addition, a travelling-wave MZM (TW-MZM) requires 50 Ω termination, which is power consuming. As a result of these limitations, it is difficult to implement wide-band drivers using low power CMOS technologies for CMOS-SiP integrated transmitters.

We examine lumped-element segmented MZM (LES-MZM) first investigated on InP [49], as shown in figure 2.1. In this structure, each phase-shifter segment, including the electrode and p-n junction, can be treated as a lumped element in the desired frequency range. This approach overcomes the disadvantages of the TW-MZM. The velocity mismatch between RF and optical waves can be compensated by tunable delays between adjacent driving channels for a higher bandwidth. Therefore, a longer phase shifter, consisting of a sequence of lumped-element segments, can be implemented to reduce the driving voltage.

While PAM-4 modulation up to 56 Gb/s [19] (and more recently quadrature amplitude modulation [50]) was demonstrated using segmented MZMs with hybrid integrated CMOS drivers, these devices are based on a monolithic fabrication process or vertical carrier accumulation structure, requiring thin oxide gates and deposition of polycrystalline silicon (SISCAP), which are not widely accessible and are not compatible with other photonic components developed on popular 220-nm silicon-on-insulator (SOI) wafers.

Depletion-mode optical modulators with lateral p-n junctions are widely available in SiP foundry processes. However, as previously discussed, TW-MZMs suffer from trade-off between bandwidth, voltage swing, and insertion loss [51]. Since generating very high voltage swings is not practical in sub-micron CMOS processes, optical modulators with lower V_π are desired.

2.2.2 Flow of Design and Simulation

The complete simulation procedure of the PAM transmitter, including both the CMOS driver and SiP LES-MZM, is illustrated in figure 2.2. This flowchart can be divided in three parts: phase shifter, driver simulation, and LES-MZM model. Bulleted items (in red) are output parameters transferred as inputs to the next boxes. Based on this flowchart, a co-simulation has been done to predict the large signal electro-optic behavior of the PAM-4 transmitter.

2.3 SiP Segmented Modulator Design

The plasma dispersion effect is the most convenient method of achieving optical modulation in silicon where the concentration of free charges in silicon changes both the real and imaginary parts of the refractive index [44], [18]. The carrier densities in silicon p-n junctions can be modulated through carrier injection (in the forward bias condition) or depletion (in the reverse bias condition). Because the speed of carrier injection is limited by carrier lifetimes (less than 1 GHz), high-speed SiP modulators typically operate in the depletion mode (reverse biased p-n junction).

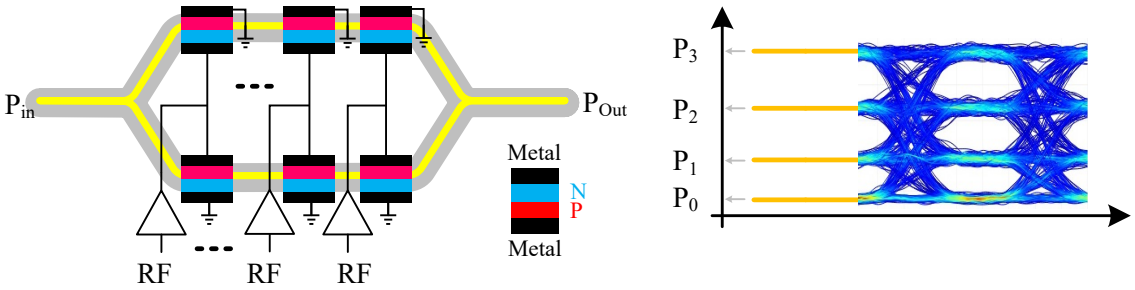


Figure 2.1 – LES-MZM and DAC less generation of multi-level signals (PAM-4 is shown here)

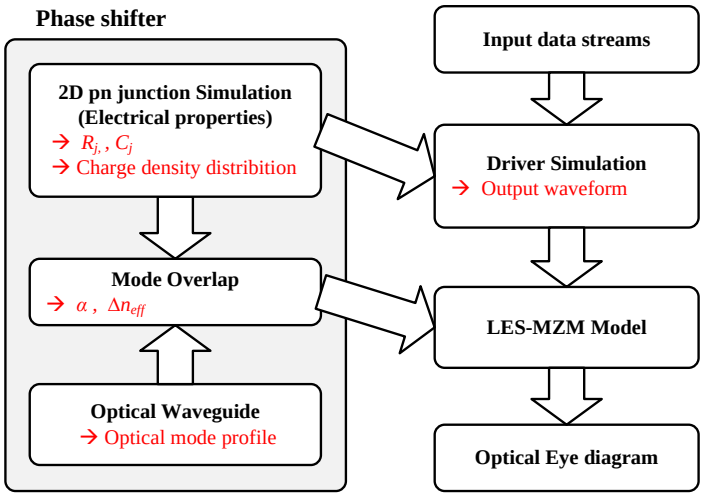


Figure 2.2 – Flow chart of the design and co-simulation.

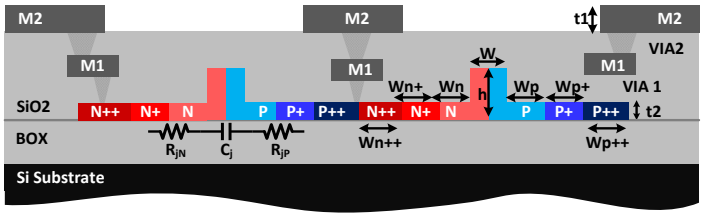


Figure 2.3 – Cross section of lateral P-N junction waveguide Wp++= 5.2, Wp+= 0.83, Wp= 0.37, Wn++= 5.2, Wn+= 0.81, Wn= 0.39, W=0.5, h=0.22, t1=2, t2=0.9 (all the dimensions are in μm).

For the reverse biased p-n junction, the depletion width depends on the bias voltage and doping concentrations. The charge density change associated with the depletion width change due to the bias voltage leads to a change in the refractive index and thus to phase modulation. After determining the effective index change, it is straightforward to calculate the optical phase modulation of a waveguide containing a silicon phase modulator by:

$$\Delta\phi = \frac{2\pi L \Delta n_{eff}}{\lambda} \tag{2.1}$$

where L is the phase modulator length, λ the wavelength of light in vacuum, and n_{eff} the waveguide effective index [51].

The SiP LES-MZM is designed based on a lateral p-n junction phase shifter where the p-n junction is embedded in an optical rib waveguide. It is implemented using a CMOS-compatible SiP process on a 220-nm SOI wafer with 2 μm buried oxide (BOX) [51]. The cross section of the modulator with an equivalent circuit model (including R_{jN}, R_{jP}, C_j) is illustrated in figure 2.3. A single-drive push-pull configuration drives each segment of the modulator, where the p-n junctions are connected in a parallel configuration. Although increasing the total junction capacitance, this configuration simplifies the CMOS design since it needs half

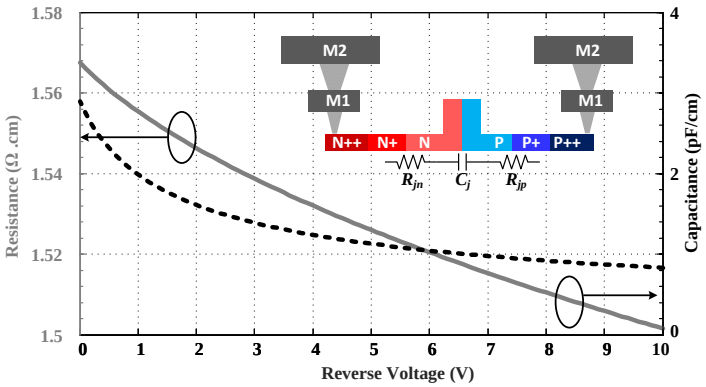


Figure 2.4 – C_j and R_j (=R_{jn} +R_{jp}) as a function of the applied bias voltage. The levels of doping used are 5× 10^{17}/cm^3 p-dopants and 3×10^{17}/cm^3 n-dopants.

the voltage swing compared to the series push-pull configuration [18]. To reduce the series resistance without significantly increasing optical propagation loss, intermediate P+ and N+ doping levels are used. Highly doped P++ and N++ regions are used for ohmic contact.

The p-n junction in each segment is modeled by a circuit of lumped capacitors and resistors, whose values depend on the applied voltage. A 2D simulation of the p-n junction is run to predict the electro-optic response of the phase shifter and to calculate the circuit components [51], [52]. The doping profile is simulated following the specifications of the SiP process. The spatial densities of the dopants are then used to predict the carrier distributions in the p-n junction for different reverse voltage values from 0 to 10 V. Resistance and capacitance of the p-n junction are simulated according to the predicted spatial charge distribution. Figure 2.4 shows the calculated junction capacitance (C_j) and resistance (R_j), which decrease when the reverse bias voltage increases. Lower C_j and R_j are desirable for a higher bandwidth. We have used the values at zero bias (3 pF/cm and 1.56 Ω.cm) in the circuit model for the driver design (Section IV) to ensure that the driver can drive the load in the worst case.

Optical properties of the phase shifter are calculated following the procedure in [51]. The optical mode profile in the doped rib waveguide is simulated using an optical mode solver [52]. The overlap between the optical mode and the carrier distribution is calculated to predict the optical phase shift and loss as functions of voltage [51]. The changes in refractive index and attenuation through the phase shifter as functions of reverse voltage are shown in figure 2.5.

Based on these simulations, a three-segment LES-MZM was designed, each segment having a length of 1 mm for a total length of 3 mm of the entire phase shifter. This allows for a simple configuration of a PAM-4 transmitter, as three is the minimum number of segments in order to achieve a four-level signal using a unified design of driving channel for all the segments.

Given the voltage swing limitation in the 130 nm IBM RF CMOS process (1.2V for a

single MOS device), 4 V_{p-p} is achievable in a parallel push-pull configuration. With this voltage swing, a 3-mm-long phase shifter can provide sufficient optical modulation amplitude without significant loss. For the CMOS driver, increasing the number of segments may reduce the burden of each driving channel but results in higher complexity in delay control and a larger footprint.

The designed LES-MZM is modeled using a photonic circuit simulator [52]. Ideal noise-free, square waveforms with 2-ps rise/fall times are used for the driving signals; thus the bandwidth limitation from the CMOS driver has been ignored, whose impact will be examined in Section V. An ideal model is used for the photodetector. The simulation results presented in figure 2.6 show an optical PAM-4 signal generated using two OOK data streams, one feeding the first segment for the least significant bit (LSB) and one feeding the other two segments for the most significant bit (MSB).

A delay of about 14 ps is introduced between two adjacent segments to compensate for the velocity mismatch. This indicates the co-designed CMOS driver must be able to generate such a delay between adjacent driving channels. Simulation results are presented for two different bit rates, 20 Gb/s and 34 Gb/s exhibiting 6.1 dB extinction ratio for constituent OOK data streams at 10 Gbaud/s and 17 Gbaud/s (for PAM-4 with 3 gaps this suggests approximately 2 dB extinction ratio between levels).

2.4 CMOS Driver

The main idea of the segmented structure, as shown in figure 2.1, is to break down the long phase shifter in a MZM into shorter segments that can be individually driven by low-power CMOS drivers for higher modulation depth and lower total power consumption by removing the need for an electrical DAC in higher order modulation formats (i.e.PAM-4, PAM-16). By

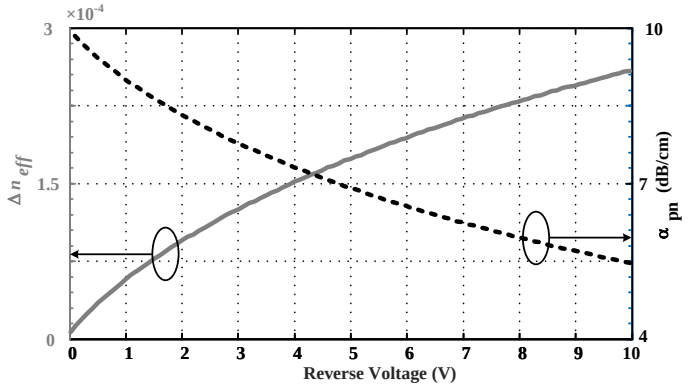


Figure 2.5 – Variation of the Δn_{eff} and optical loss according to the applied reverse voltage to the pn junction.

turning on and off different number of segments along the modulator, different optical power levels can be generated at the output of the modulator.

The entire block diagram of the transmitter, including driving circuits and the three segments LES-MZM, is illustrated in figure 2.7. Input data, terminating with on chip 50Ω resistors, are fed into a simple decoder to decide which segments should be turned on or off. The outputs of the decoder perform as inputs of the three CMOS drivers distributed along the optical path, with an adjustable delay between adjacent driver to match the electrical delay and optical group delay. Each CMOS driver should be connected to one phase-shifter segment on the SiP chip through wire-bonding or flip-chip bonding.

The number of on-state segments will be determined as a function of the input data to generate the desired optical power level at the output of the modulator. This can be implemented by mapping a binary code to a thermometer code. Consider our implemented LES-MZM with three segments. In this case, for inputs D_0=0 and D_1=0, no segment should be turned on. For inputs D_0=1 and D_1=1, all segments should be on. Assuming a linear relation between optical phase shift and p-n junction length for a given voltage on each segment, various optical power levels can be created. In this case, up to 4 levels can be generated through three segments for PAM-4 operation (see figure 2.1).

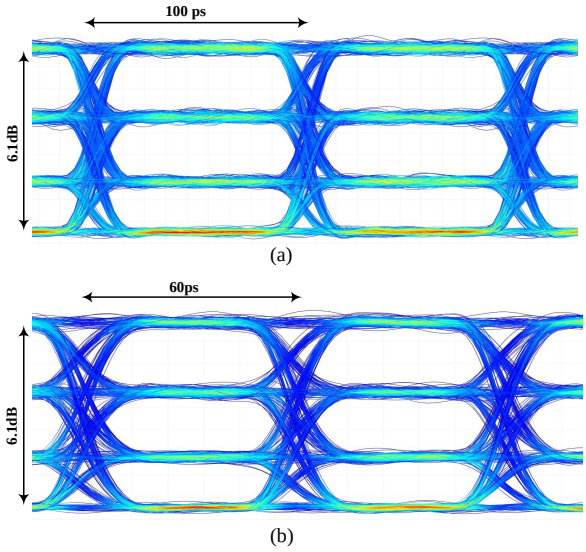


Figure 2.6 – Data transmission simulation results for a three segments LES-MZM. a) at 20 Gb/s, b) at 34 Gb/s. Eye opening is asymmetric (low levels less separated) due to the nonlinear relationship between the length of the phase shifter and output optical power. In this simulation extinction ratio for the lower, middle and top eyes are ∼1.74 dB, ∼2.2 dB, ∼2.25 dB at 34 Gb/s.

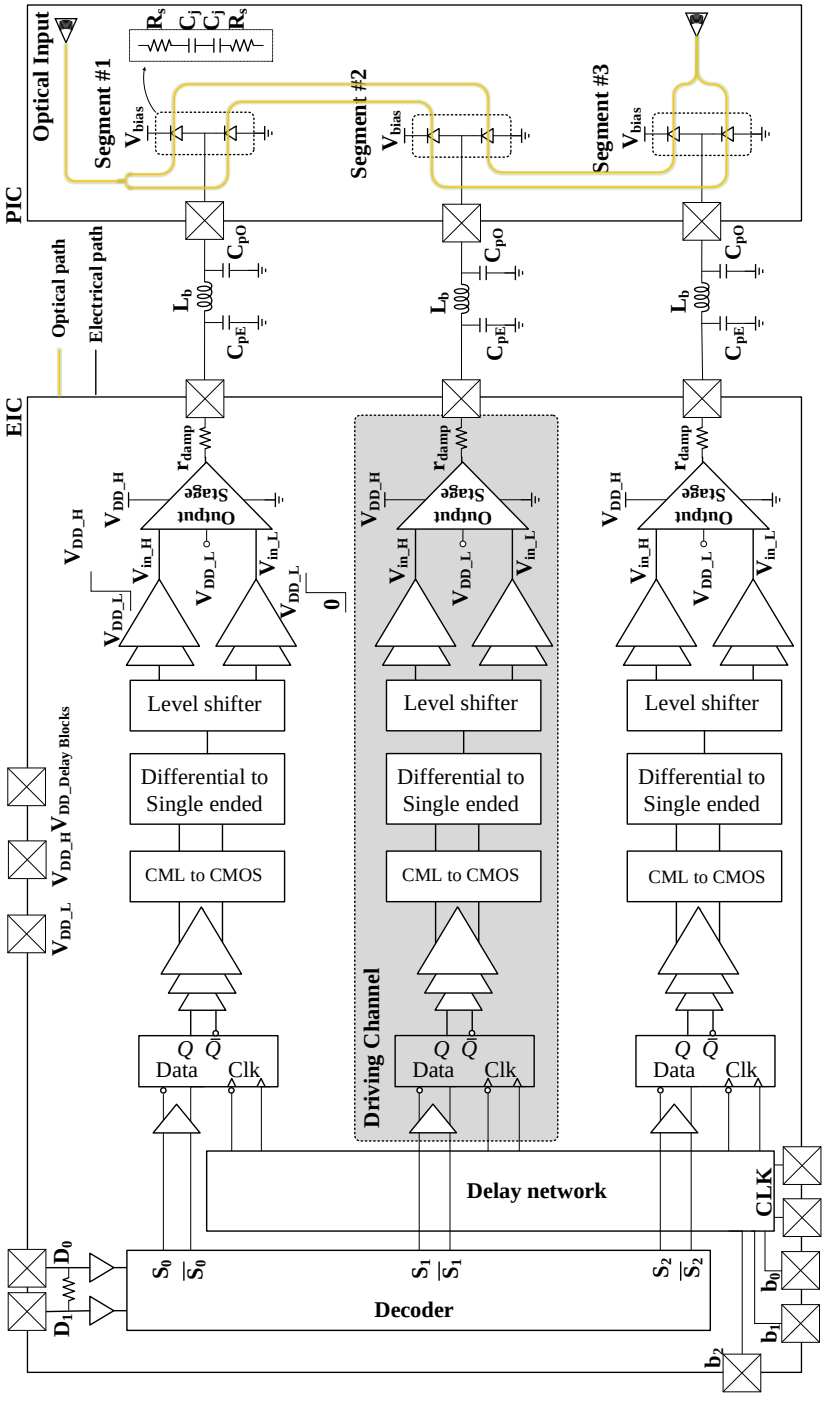


Figure 2.7 – Entire block diagram of the DAC less PAM-4 transmitter including the CMOS driver and LES-MZM. The driver utilizes three driving channel with a tunable delay between them. Each driving channel drives one of the three segments in the LES-MZM.

2.4.1 Delay Generation

As mentioned in section 2.3, in long MZMs mismatch between electrical propagation delay and optical group delay should be addressed to maximize the modulator bandwidth. In the proposed LES-MZM, although each segment is free of velocity mismatch between electrical and optical signals, still a precise control of delay should be realized between RF signals applied to two adjacent segments.

Delay Network

The clock input is fed into each driving channel after passing through a delay network whose block diagram is shown in figure 2.8. It comprises three delay blocks (i.e., $\Delta\tau_1$, $\Delta\tau_2$, and $\Delta\tau_3$) to generate the desired delays for respective driving channels. This delay network is based on the difference between the delays generated in two adjacent delay blocks, enabling precise delay control between two adjacent segments. This approach is more tolerant to variations than delay generation schemes using absolute delays.

The delay control is illustrated in figure 2.9. For the first delay block, only a fixed delay of 10 ps ($\Delta\tau_1$) is implemented for the purpose of differential delay control. The second delay block ($\Delta\tau_2$) consists of a coarse delay and a fine delay, both of which are tunable. The coarse delay is controlled by the control bit, b_0, switching between 17.5 ps and 27.5 ps. The fine

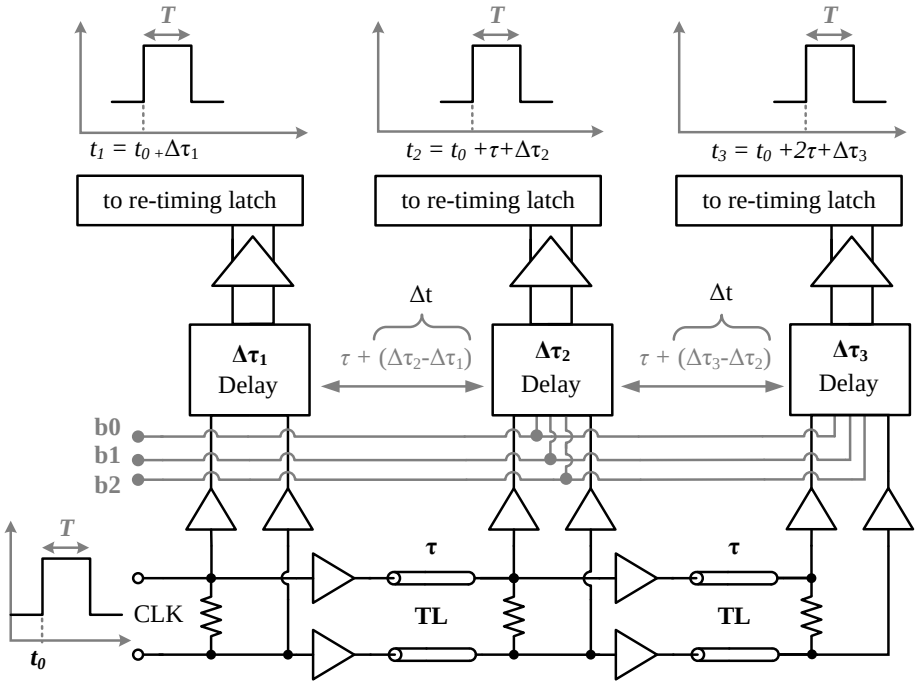


Figure 2.8 – Delay generation process, including tunable and fix delay block capable of generating a tunable delay up to ∼22.5 ps between two adjacent driving channels, according to the control bits.

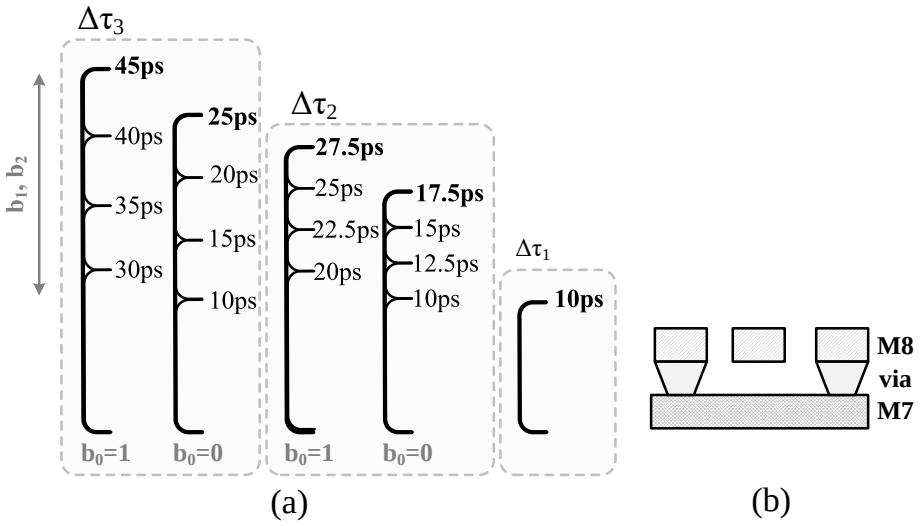


Figure 2.9 – (a) Delay generation in $\Delta\tau_1$ and $\Delta\tau_2$ with the control bits. One bit is assigned to the coarse delay and two others choose one of the fine delays. The maximum and minimum of the total delay between two adjacent channels is 5 ps and 22.5 ps (including the 5ps from transmission line). (b) Cross section of the transmission line for the fixed delay. The width of the signal path is chosen to be 4 μm while its length is 600 μm to generate 5ps fix delay.

delay adjustment is implemented by means of the control bits b_1, b_2 with a tuning step of 2.5 ps. Similarly, $\Delta\tau_3$ consists of a coarse delay of either 25 ps or 45 ps and a fine delay adjustable with a step of 5 ps (see Figure 2.9a).

As illustrated in figure 2.8, we assume the input clock signal is fed in at t_0. Taking into account the delay blocks and the transmission lines (TLs) between them, the clock signals arrive at the re-timing latches at times:

$$t_1 = t_0 + \Delta\tau_1 = t_0 + 10ps \tag{2.2}$$

$$t_2 = t_0 + \tau + \Delta\tau_2 = t_0 + \tau + (CorseDelay) + (k \times 2.5)ps \tag{2.3}$$

$$t_3 = t_0 + 2\tau + \Delta\tau_3 = t_0 + 2\tau + (CorseDelay) + (k \times 5)ps \tag{2.4}$$

where k$\in$ {0,1,2,3}is the number of fine tuning steps. Hence, the generated delay between two adjacent driving channels is $\Delta t = (t_i\text{-}t_{i-1}) = \tau + (10\times b_0) + k \times 2.5$ ps. This delay does not depend on the absolute value of the delay generated in each delay block. The minimum and maximum of the total delay between two adjacent channels are 5 ps and 22.5 ps, respectively.

Fixed and Tunable Delay Elements

Each delay block has a fixed delay (τ) from a single-wire shielded TL implemented on a thick metal layer for low RF losses. The cross section of the transmission line is shown in figure 2.9b. The tunable delays ($\Delta\tau_2$, $\Delta\tau_3$) are achieved by an inverter-based structure, as shown in

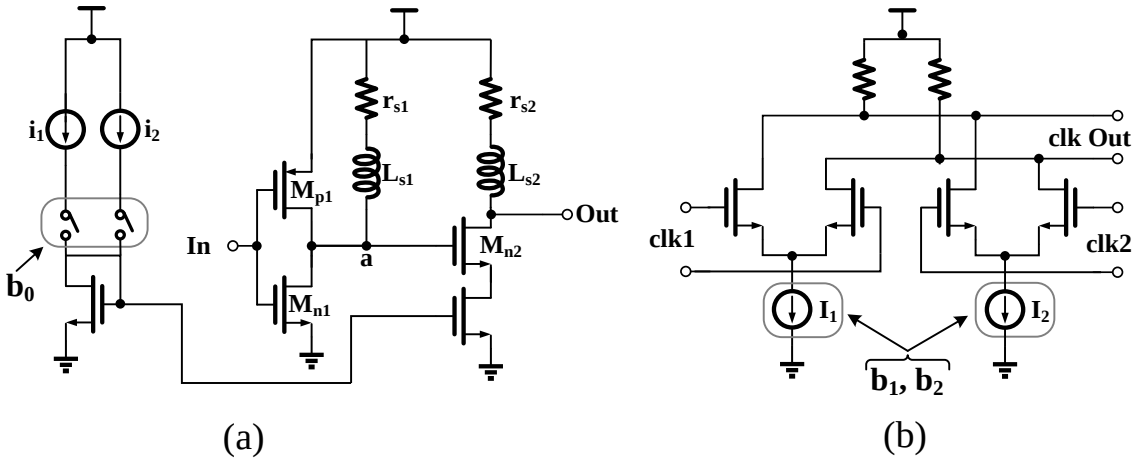


Figure 2.10 – (a) Tunable coarse-delay element capable of generating two delays, 17.5 ps and 27.5 ps in $\Delta\tau_1$, 25 ps and 45 ps in $\Delta\tau_2$. (b) Tunable fine delay element, mixing two clocks in different portions according to the tail current in each branch, to generate the output clock.

figure 2.10a. The parasitic capacitance limits the bandwidth of the inverter. An inductively enhanced design is adopted to improve the bandwidth, where an inductor (Ls) is used to compensate for the effects of the unwanted capacitor from the inverter and the buffer stage after the inverter.

Delay between input and output nodes of the inverter is controlled by changing the current passing through the inverter by means of b_0 for the coarse delays (17.5 ps and 27.5 ps in $\Delta\tau_2$, 25 ps and 45 ps in $\Delta\tau_3$). The fine delay element, as shown in figure 2.10b, needs two inputs. One input (clk2), which is connected to the output of the coarse delay, is delayed compared to the other input (clk1, i.e., the same input of the coarse delay) to generate the output clocks according to b_1, b_2 that control the tail currents. The fine delay adjustment is realized by changing the ratio of the currents (I_1 and I_2) passing through the two branches of the differential pair.

2.4.2 Driving Channel

A block diagram of each driving channel is given in figure 2.7. The clock and driving signals (S_i,$\overline{S_i}$, i=0,1,2) are applied to a high speed current mode logic (CML) latch for re-timing. Driving signals are applied to the driving channels as functions of input digital data (D_0, D_1) after certain delays as discussed above.

CML Latches

Figure 2.11 shows a circuit schematic of the CML latch. Generally, a CML latch consists of two main sub-circuits: an input tracking circuit (shaped by M_3 and M_4) and a cross coupled regenerative pair in output (M_{f1}, M_{f2}). When V_{CLK} is in the "high" state, the input voltage

is tracked by the input differential pair, while M_6 is blocking the current passing through the cross coupled regenerative pair in the output. When V_{CLK} is in the "low" state, the cross-coupled regenerative pair stores the tracked voltage at the output load capacitance.

There are three criteria that must be considered in designing a CML latch: output voltage swing, voltage gain of the input differential pair, and bandwidth. The maximum allowable differential output voltage swing in a CML latch can be expressed by $2r_{d1}I_{D,M1}$. As explained in [53], output voltage swing is limited by the threshold voltage of the NMOS devices in figure 2.11.

In a CML latch, output voltage slope at the rising and falling edges depends not only on the RC time constant at the output node, but also on the voltage gain of the input differential pair [53]. Hence, the following input differential pair voltage gain must be adapted correctly for an efficient design:

$$A_{V_Track} = \frac{r_{d1}g_m}{1 + Rg_{ds}} \approx r_{d1}g_m \tag{2.5}$$

where g_m and g_{ds} are the intrinsic transconductance and the output conductance of the MOS devices, respectively. As long as the voltage gain of the cross coupled pair in output stage(A_{VLatch} in the balanced condition,$I_{D,Mf1}$=$I_{D,Mf2}$) is higher than unity, output stage of the latch will work properly [54]. As a straight forward solution, A_{VLatch} can be chosen to be equal to A_{Track}. Although setting $A_{VLatch} = A_{Track}$ and taking identical current sources (I_{ss1}=I_{ss2}) for the track and regenerative pair stages makes it easy to select the transistors size (L=L_{min} and W_{Latch}=W_{Track}), it might not be the best choice for a power and bandwidth efficient design.

For proper operation of a CML latch at ultra high-speed data, a wide range of linearity

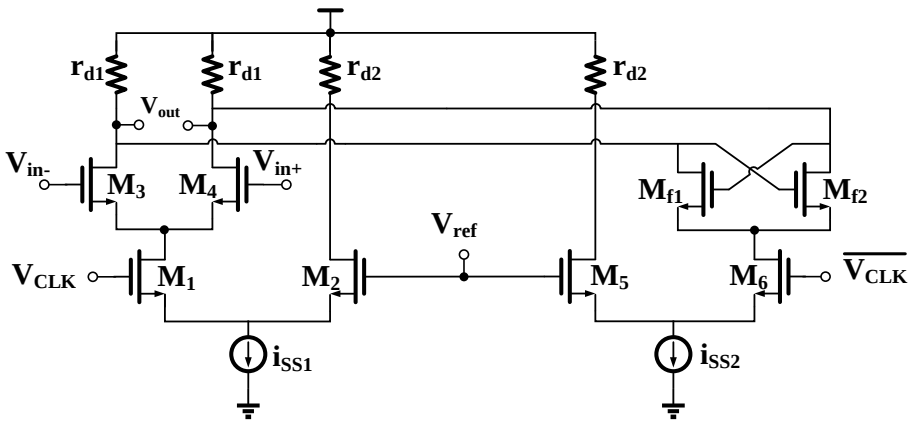


Figure 2.11 – CML latch with two different tail current for track and latch mode. Transistors sizing is as follow: $W_{3,4}$=29 μm, $W_{f1,f2}$=2.5 μm, $W_{1,2}$=45 μm and $W_{5,6}$=10 μm while for all of them L=0.13 μm. The resistor in the drain of the tow stage, r_{d1} and r_{d2}, are 150Ω and 100Ω, respectively.

and large transconductance is required from the input differential pair. Hence, the tail current for the input differential pair has to be significantly high. On the other hand, the cross-coupled regenerative pair at the output can have a smaller bias current than the input differential pair [21]. Using different bias currents for tracking and latching operations, as shown in figure 2.11, one can optimize each stage separately to satisfy the bandwidth requirements.

Design of CML gates has been investigated in depth [54], [55]. In our design, transistors were sized following the procedure given in [54] by choosing Av≈1.38, a differential output voltage swings $2r_{d1}I_{ss1}$ = 600 mV, and a proper $r_{d1}C_{total}$ time constant for the targeted 20 GHz bandwidth. Note that $C_{total} = C_{eq}+C_L$, C_{eq} is the equivalent capacitor at the output node due to parasitic capacitance of the transistors (in tracking and latch stages), and C_L is the load capacitance (input capacitance of the next stage of the CML buffers). In our design, 6.1 mA was assigned to the tracking stage (I_{ss1}) and 2.5 mA for the output stage (I_{ss2}). V_{ref} is chosen to ensure I_{ss1} and I_{ss2} are always in saturation.
The "high" and "low" levels of the V_{CLK} must be considered to ensure that:

1) during the track mode I_{ss1} passes through M_1 (and I_{ss2} through M_5)
2) during the latch period I_{ss1} passes through M_2 (and I_{ss2} through M_6)

This also impacts V_{ref}. In our design V_{ref} was set to 700 mV.

Since CML latches are used as data re-timers, the transient response of V_{out} with respect to V_{CLK} is more important than the small signal response [56]. Simulated step response of the CML latch with V_{CLK} as input is shown in figure 2.12a. We observe a 10% to 90% rise time of 27.1 ps while driving a CML buffer with W/L = 20/0.13. Frequency response of the CML latch is also illustrated in figure 2.12b, indicating a 3 dB bandwidth of 22.6 GHz.

As the output of the latch has a limited swing and driving capability, a chain of buffers is used to drive the CML to CMOS logic converter. The differential to single ended converter block is implemented by a single ended common source differential pair. Level shifter generates $V_{in,L}$and $V_{in,H}$ required by the cascoded output. As the output stage is using transistors with large dimensions, a large parasitic capacitance is introduced. Output of the level shifter is buffered to be able to drive the input nodes of the output stage. Design of the output stage that drives each segment of the optical phase shifter is presented next.

Output Stage

Simulation results in figure 2.6 were obtained by applying a $2V_{p-p}$electrical signal to drive each segment. Considering the limited voltage head room in sub-micron CMOS process, a cascoded configuration (figure 2.13) is adopted in order to achieve the required voltage swing,

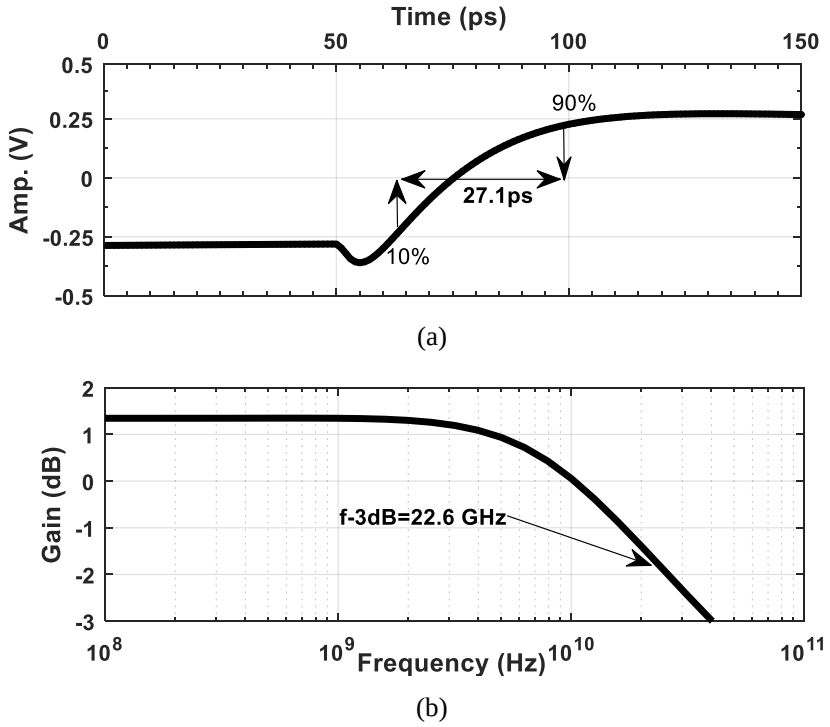


Figure 2.12 – Simulated responses of the CML latch (Vout with respect to V_{CLK}): (a) large-signal step response of the CML latch while driving a CML buffer with W/L=20/0.13. (b) frequency response.

which is widely used for optical modulators [57], [58]. The cascoded output stage used here needs two inputs voltage levels (see figure 2.13):

$$1.2V \leq V_{in,H} \leq 2.4V \quad and \quad 0V \leq V_{in,L} \leq 1.2V \tag{2.6}$$

applying this approach, the output swing can be doubled from V_{DD} to $2V_{DD}$ without over-stressing the NMOS and PMOS devices in the output stage.

The load capacitance at the output node of the driver, C_{Load}, includes the pn-junction capacitance (C_j) of the optical phase shifter and the parasitic capacitances from the output stage:

$$C_{Load} = 2C_j + C_{gd} + C_{db} \tag{2.7}$$

where $C_{gd}$is the total capacitance between the gate and drain terminals and C_{db} is the total capacitance between the drain and body terminals of M_{N1}, M_{P2}. The transistors in the output stage have to be sized according to the slew rate requirement for the desired data rate. For a 20 Gbaud transmitter, a slew-rate limited driver ideally must present a rise and fall time of no more than 17.5 ps. The required current to charge C_{Load} by V_{drive} is:

$$I_D = J_D W \geq \frac{C_{Load} V_{drive}}{t_r} \tag{2.8}$$

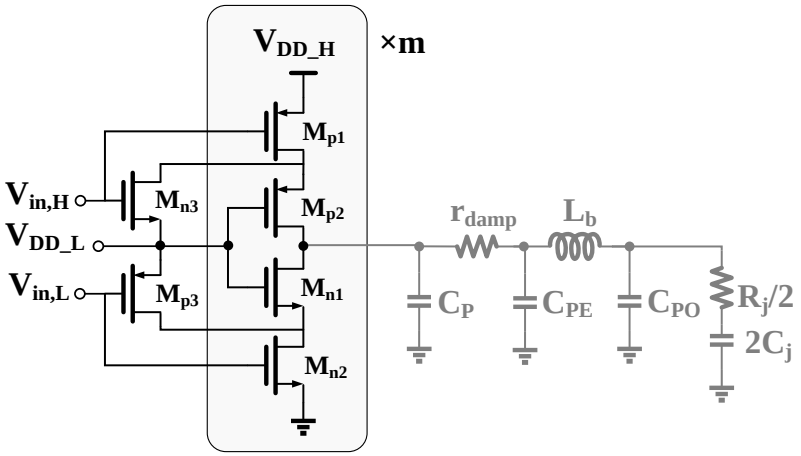


Figure 2.13 – Cascoded inverter output stage to double the voltage swing [57], M_{N3} and M_{P3} are used to prevent unwanted peaking during transition between two voltage levels. C_{PE} and C_{PO} are the capacitance comes from the pads in electrical and optical chips, respectively, r_{damp} is the damping resistor to decrease the overshoot in transient of output, L_b is the inductance from wire bounding, and C_P is the parasitic capacitance at the output node. V_{DD_L}=1.2 V, V_{DD_H}=2.4 V and unit size of the transistors is as follow: $(W/L)_{M_{P1}}$ = (50/0.13) and number of the fingers in layout, $N_{f_{MP1}}$=20, $(W/L)_{M_{P2}}$ = (12.5/0.13) and $N_{f_{MP2}}$=5, $(W/L)_{M_{N1}}$ = (62.5/0.13) and $N_{f_{MN1}}$=20, $(W/L)_{M_{N2}}$= (87.5/0.13) and $N_{f_{MN2}}$=30. As $M_{n,p3}$ are protection devices, they should be chosen as small as possible to be sure that their parasitic capacitances do not limit the overall bandwidth of the output stage $(W/L)_3$= (5/0.13).

where J_D is the transistor current density and W is the width of the transistor.
According to(2.7)and assuming V_{drive} = 2V and t_r =17.5 ps, the required current is calculated to be 35 mA. Transistors in the output stage have to be sized to supply this high current, while offering the highest possible bandwidth. This means that transistors must be sized for the current density at the peak f_T in the CMOS process used (≈0.127 mA/μm in our case) [59].

2.5 Results of the CO-Simulation

The optical transmitter is simulated following the procedure illustrated in figure 2.2. Two 20 Gb/s, 2^{15}-1 PRBS bit patterns (where skewed with respect to each other for decorrelation) are fed to the designed CMOS driver. The equivalent circuit elements extracted from the optical phase shifter simulation are used as the load in the CMOS driver model developed in section 2.4. The output of a single driving channel for different multiplicity factors is shown in figure 2.14, multiplicity factor m = 4 is chosen in our design to achieve the required voltage swing (2.14, eye diagram with darkest line).

Although the value of rise/fall time is far from its ideal value for a slew-rate limited driver, we still observe a clear eye at 20 Gbaud for 2 V_{p-p} swing in figure 2.14. This output stage is driven with two input signals, both with a full swing of V_{DD}, so the output stage

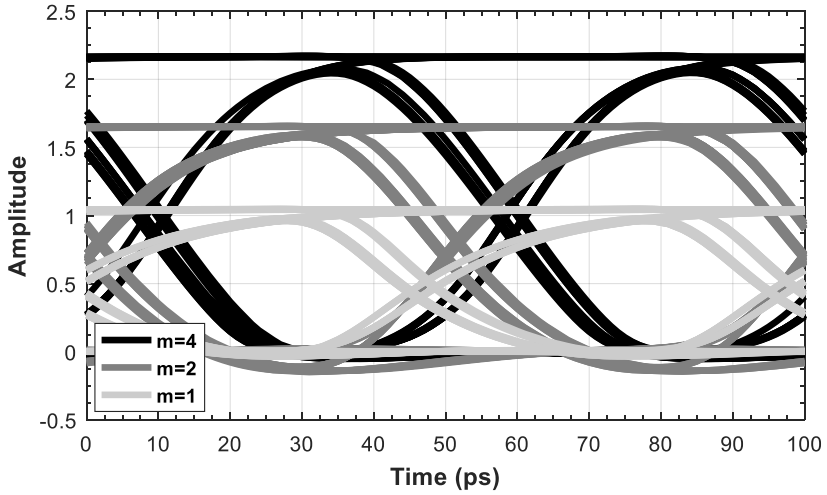


Figure 2.14 – Performance of the driving channel loaded by the equivalent lumped element circuit of one optical segment. Output eye diagrams for different values of multiplicity factor (m) in the output stage transistors.

does not have to offer a high value of gain to its inputs.

Simulated output waveforms of the CMOS driver are input to the optical model developed in section 2.3 for the three-segment LES-MZM. Simulated results of the optical transmitter for two bit-rates, 20 Gb/s and 34 Gb/s, are shown in figure 2.15.

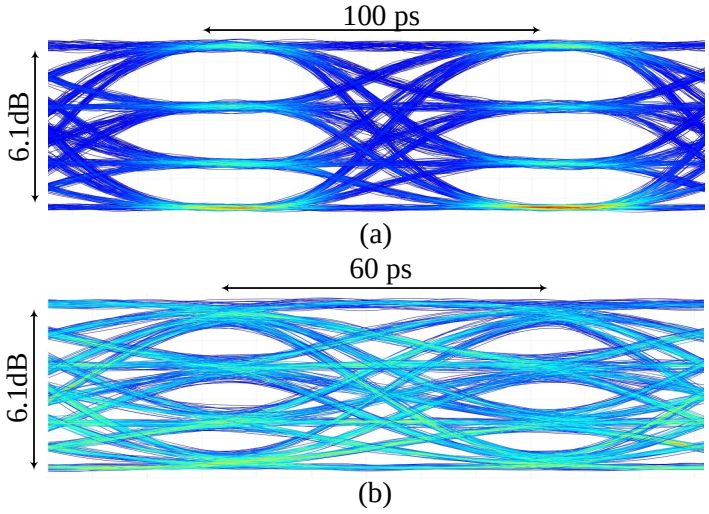


Figure 2.15 – Co-simulation results for a three segments LES-MZM. a) at 20 Gb/s with ER= 6.1 dB, b) at 34 Gb/s with ER= 6.1 dB. A 14 ps delay is set between the adjacent driving channels.

Compared to the results shown in figure 2.6 (where input electrical signals are ideal square waves with a 2.2V$_{p-p}$ swing), the results of the co-simulation clearly show the effect of

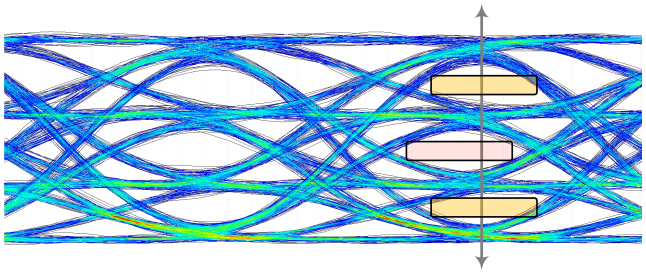


Figure 2.16 – Effect of failure in maintaining the required delay (14 ps) between driving channels on the output optical eye at 30 Gb/s. Center point of the middle eye opening is skewed from its ideal point. Delay between two adjacent channels, Δt, is set to be 10ps, which is 4ps less than the required 14 ps delay.

the bandwidth limitation from the driver on the output optical eye. It should be mentioned that during these simulations, the electrical signals and the photodetector are considered to be free of noise.

Eye openings in figure 2.15 are asymmetric (low levels are less separated than higher levels, same as the results in figure 2.6) due to the nonlinear relation between the length of the phase shifter and the optical power at the output. Hence a compensation technique could be used to equalize the eyes, by manipulating the phase shifter length in each segment. Proper delay generation between two adjacent driving channels affects the performance of transmitter. In figure 2.16, imperfection in the output optical eye due to failure in obtaining the required delay between two adjacent segments is shown. Skewed eye opening severely affects the BER performance of the transmitter, especially at higher baud rates where the bit duration is shorter.

2.6 Measurements and Discussion

The CMOS driver is fabricated in IBM 130 nm RF process. The entire die area of the driver is 1.5 mm^2 (1 mm$\times$1.5 mm). The photonic chip was fabricated at A*STAR's IME, Singapore. A photo of the LES-MZM and its co-designed CMOS driver is shown in figure 2.17. Wire bonding is used to connect the output of each channel in the CMOS driver to each segment of the MZM. The operating point of the MZM is adjusted by means of DC bias voltage to achieve maximum eye opening (as a result, the bias point is slightly shifted from the quadrature point of the modulator).

Driver Characterization

Figure 2.18 shows the experimental setup used to test our chips. At first, the output of the driving channels are examined. Figure 2.19 shows the output waveform of one of the driving

channels, (the others show similar behaviours) while driving a 50 Ω load. It shows a swing of 1.6 V_{p-p} at 20 Gbaud. The overshoots and jitters (5.4 ps) in the eye diagram are mainly from the inductance introduced by the wire bonds. Outputs of the three channels are shown in figure 2.19, where ∼7 ps delay between two adjacent channels is obtained at 20 Gbaud. In the following, the programmable delay is examined.

Figure 2.20 shows the measured results for the generated delay at different frequencies. The maximum and minimum delays generated from the fixed and tunable delay blocks are 14.5 ps and 10.6 ps, respectively, at 8 GHz. These values change to 12 ps and 7.2 ps, respectively, at 20 GHz. Tuning is achieved through three control bits (b_0 , b_1 , b_2). While a maximal delay of 22.5 ps between two adjacent driving channel was expected at 20 Gbaud (when b_0 =1) according to our simulation, only 12 ps was measured due to an unexpected issue in the coarse delay generation. We suspect this issue is related to a bug in the circuit implementation, resulting in failure to achieve the predicted value for the coarse delay (27.5 ps in $\Delta\tau_2$ and 45 ps in $\Delta\tau_3$) when $b_0 = 1$. As shown in the simulation results presented in section 2.5, figure 2.16, failure in applying the required delay between two adjacent segments causes skewed eye openings. At high baud rates, these skewed eye opening causes sever increase in BER of the transmitter. Figure 2.20 shows that, for baud rates higher than 17 GHz, the maximum delay achieved is less than 13 ps, smaller than the optimal value (14 ps) predicted by simulation. Total power consumption of the driver was 375 mW for 38 Gb/s. The breakdown of power consumption of the driver is shown in figure 2.21. The driver output stage consumes most of the power. CML buffers consume 30% of the total power. Power consumption decrease to 290 mW at 20 Gb/s.

Data Transmission

The transmitter is driven directly by binary signals, i.e., without signal processing. Two binary sequences of length 21^5-1 are generated by an SHF pattern generator; the bit rate is varied. The first signal (LSB) is fed to the first driving channel and the second signal (MSB)

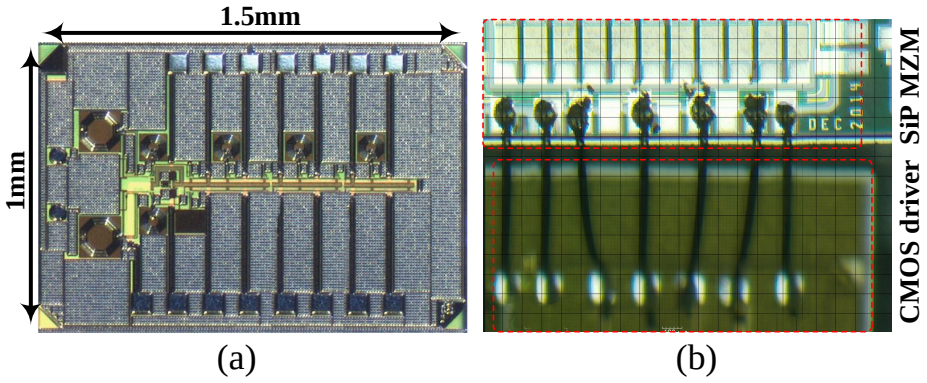


Figure 2.17 – (a) CMOS driver, (b) CMOS driver wire bounded to SiP LES-MZM

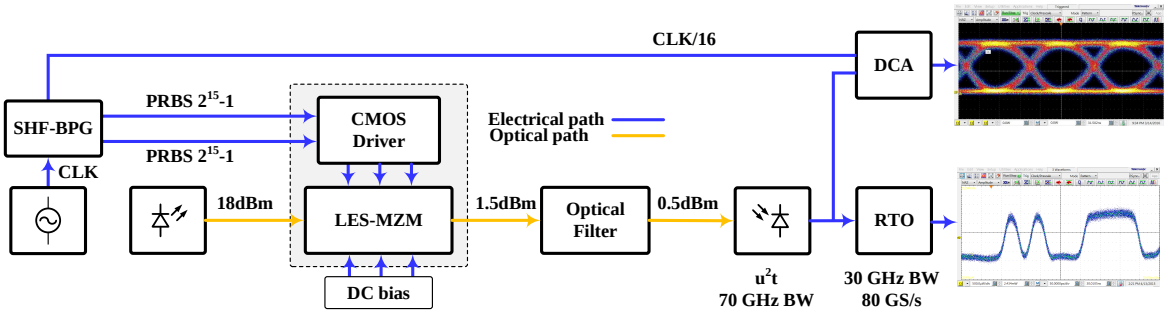
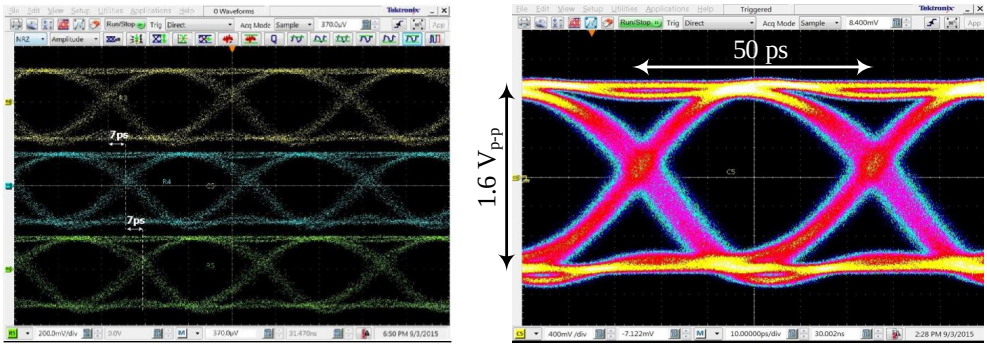


Figure 2.18 – Data transmission test bench. (DCA: Digital Communication Analyzer, RTO: Real Time Oscilloscope)

is split and fed to the second and third driving channels (based on the decision made by the decoder) to create a PAM-4 signal.

At the receiver side, the PAM signal is photodetected (by a u^{2}t Photonics A.G. photodetector with 70 GHz bandwidth), and captured using a 30 GHz real time oscilloscope (RTO) with sampling rate of 80 GSample/s. Also the optical eye diagrams are captured by means of a digital communication analyzer (DCA). Output optical eye diagram for two different bitrates (20 Gb/s and 34 Gb/s) are presented in figure 2.22. Although for 34 Gb/s eye diagram shows very close eye opening in each level of PAM-4, at 20 Gb/s the eye opening in PAM-4 levels are very clean and suggest a transmission with a very low BER.

Offline DSP starts with a super Gaussian 4th order low pass filter and bandwidth set to the PAM main transmission lobe for each bit rate. Three different post compensation methods are examined:



(a) (b)

Figure 2.19 – a) Output of different channels of CMOS driver at 20 Gbaud/s, 1.6 V_{p-p} and with ∼7ps delay between each of them. b) Measured eye diagram of electrical output signal at 20 Gbaud/s showing 1.6 V_{p-p} swing while it is driving a 50 Ω load.

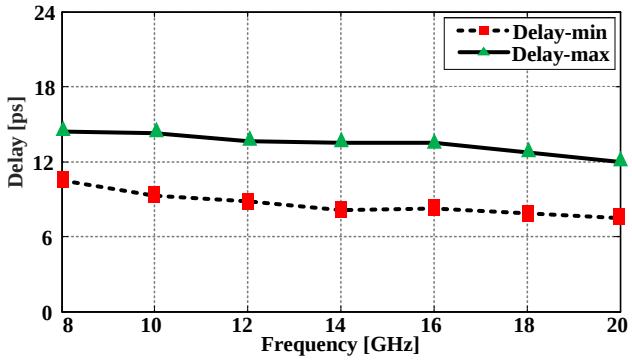


Figure 2.20 – Measured maximum and minimum achievable delay through the fixed and tunable delay blocks.

1) no post compensation
2) a minimum mean square error (MMSE) equalizer
3) a fractionally spaced MMSE (FS-MMSE) equalizer

For the first and second cases data is down sampled to one sample per symbol; for the FS-MMSE data is down sampled to 2 samples per bit period. Following a synchronization block, equalization is performed on a training sequence of length 1000 symbols, and BER is calculated. Figure 2.23 shows bit error rate for bit rates from 28 Gb/s to 40 Gb/s for the three compensation methods. The results show that without equalization the maximum bit rate under forward error correction (FEC) threshold of BER=3.7×10^{-3} is 28 Gb/s. Using MMSE and FS-MMSE increases system capacity to 34 Gb/s and 39.5 Gb/s respectively. This FEC

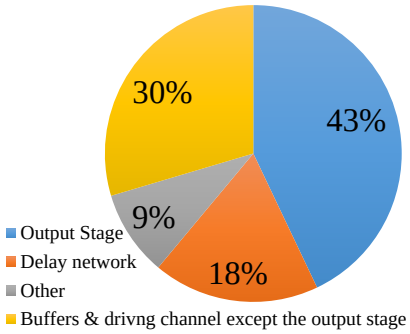
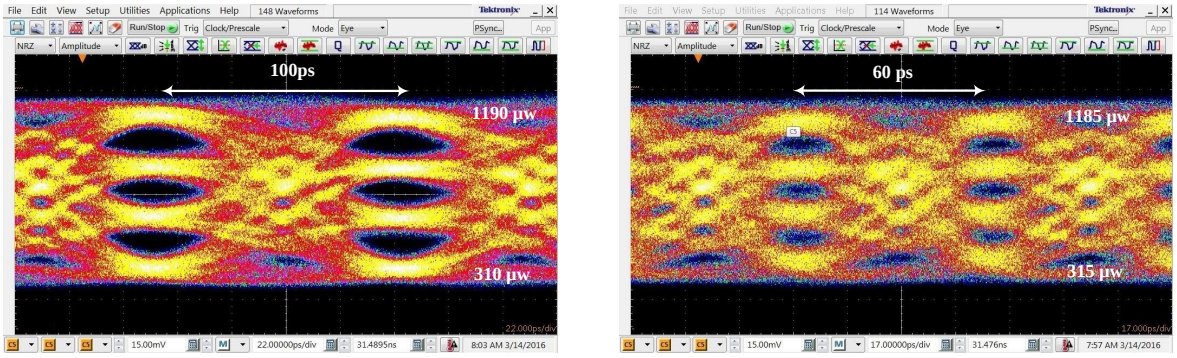


Figure 2.21 – Breakdown of power consumption of the CMOS driver at 38 Gb/s. Output stage is using most of the power ∼162 mW. Driving channel (except for the output stage) has the second place with ∼112 mW. The total power consumption in this case is simulated to be 380 mW



(a) (b)

Figure 2.22 – Output optical PAM-4 eye diagrams at (a) 20 Gb/s and (b) 34 Gb/s

threshold [60] offers a good compromise between bit rate overhead of 7% and data correction to 10^{-12} when used with two interleaved extended BCH (1020,988) codes.

The significant improvement in performance when using two sample per symbol FS-MMSE indicates that failure in the delay management (the limited maximum achievable delay, coming from the failure in the coarse delay generation) contributed significantly to the impaired PAM performance. Using a fractionally spaced equalizer with more samples per symbol did not improve performance, showing the jitter error is well bounded. We include FS-MMSE results to indicate the potential of the SiP/CMOS solution. Once timing mismatch between segments is properly controlled, a simple MMSE would be sufficient.

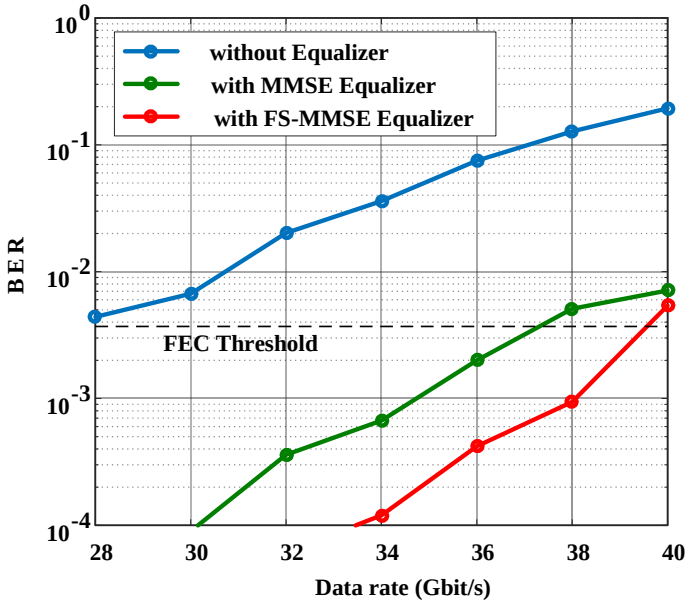


Figure 2.23 – BER vs. data rate of PAM-4 with no equalizer, an MMSE equalizer, and an FS-MMSE equalizer.

At bit rates less than 24 Gb/s, the BER was found experimentally to be less than 1×10^{-5}. Unfortunately, due to finite memory of the real-time oscilloscope, error free performance (BER order 10^{-12}) cannot be tested. The clear and open eye diagram in figure 2.22a for 20 Gb/s suggests error free operation at this bit rate. We calculated error vector magnitude (EVM) of the experimental received PAM-4 constellation and obtained 6.23% EVM when using optimal thresholds (found numerically for the asymmetric eyes). This EVM corresponds to an SNR of 24 dB, well beyond the requirement for error free operation.

2.7 Conclusion

In summary, a DAC-less SiP PAM-4 transmitter with a CMOS driver has been achieved, using a segmented MZM in the carrier-depletion mode with a lateral pn junction. Data transmission with bit error rate below 3.7×10^{-3} (with post-compensation) was achieved near 40 Gb/s with a driver power consumption of 9.8 pJ/bit. Based on EVM at 20 Gb/s (where the driver power consumption drops to 290 mW), error free operation is expected at this bitrate. Despite the higher unit-bit power consumption (14.5 pJ/bit at 20 Gb/s), lower baud rates eliminate the burden of digital signal processing (DSP) on the receiver side. Tradeoffs must be taken in real applications.

Our optical circuit model of the LES-MZM allows for efficient electrical and optical simulations of the PAM transmitter. Measured optical eye diagrams are in a fair agreement with the simulation results. According to simulation results, the bandwidth of the driver in 130 nm CMOS limits the performance of the optical transmitter, which can be improved by using more advanced CMOS processes. Delay management between the segments in the transmitter is a critical concern that should be addressed properly to benefit from the wide electro-optic bandwidth of the segmented MZMs.

Multi-segment transmitters can potentially remove the power consuming electrical DAC from optical links for low-cost applications. Most demonstrated DAC-less multi-level transmitters use either monolithic process [19] or vertical pn junctions [24], which are not widely available. Our results are achieved using commercially available CMOS and SiP processes, showing the efficiency of CMOS-SiP co-design and integration for low-power, high-speed multi-level transmitters.

Chapter 3

Assessing Performance of Silicon Photonic Modulators for Pulse Amplitude Modulation

Résumé — Les modulateurs opto-électronique photoniques sur silicium sont des composants cruciaux des transmetteurs optiques intégrés à bas cout. Les figures de mérite actuels pour les modulateurs SiP ne permettent pas de prédire les performances au niveau système des liaisons optiques, car elles ne tiennent pas compte des dégradations critiques du système : interférence intersymbole. Les FDM (figures de mérite) précédentes sous-estiment la pénalité de puissance, car elles ne tiennent pas compte de la limitation de la bande passante électro-optique. Cependant, nous montrons qu'en présence d'une bande passante électro-optique limitée du modulateur SiP, les FOM antérieures sont incapables de prédire le minimum de pénalité de puissance du modulateur. L'amplitude de modulation optique normalisée (OMA_N) est démontrée par simulation pour être un outil fiable pour prédire le point MPP minimal. Ensuite, nous introduisons une nouvelle figure de mérite qui inclut non seulement l'efficacité du modulateur, mais aussi la limitation de la bande passante du modulateur électro-optique SiP. la nouvelle FDM dérivé de OMA_N traduit les exigences au niveau du système d'une liaison optique PAM-M durant la conception au niveau du périphérique.

Abstract-Silicon photonic electro-optic modulators are key component in cost-efficient and integrated optical transmitters. Current figures of merit for SiP modulators cannot predict the system-level performance of optical links, as they do not include a critical system impairment: intersymbol interference. Previous FOMs underestimate the lower power penalty, as they do not consider the electro-optic bandwidth limitation. Nevertheless, we show that in presence of limited electro-optic bandwidth of SiP modulator, prior FOMs are unable to predict the minimum point for the modulator power penalty (MPP). Normalized optical modulation amplitude (OMA_N) is proved through simulation to be a reliable tool to

predict the minimal MPP point. Then, we introduce a new figure of merit that includes not only the efficiency of the modulator, but also the bandwidth limitation from SiP electro-optic modulator. The new FOM that is derived from OMA_N, translates the system-level requirements of an PAM-M optical link to the device-level design parameters. This FOM can be hired to optimize driving voltage swing, bias voltage, and phase-shifter length or to simply choose a SiP modulator with minimal imposed MPP.

3.1 Introduction

Silicon photonics is a promising solution for the next generation of integrated optical transceivers, from optical interconnect in short reach application to medium reach and even long-haul optical links. They are of interest as they can be integrated on complementary metal-oxide semiconductor platforms [61]. The combination of SiP electro-optic devices and CMOS integrated circuits, via monolithic or hybrid integration, paves the way for highly integrated CMOS-photonic solutions for optical transmission links [36], [31], [24], [37].

The electro-optic modulator is a crucial component in an optical transmission link, and SiP modulators have been widely examined as a cost-efficient, integrated solution. Among modulator structures, SiP micro-rings and traveling wave electrode Mach-Zehnder modulators are the two most often reported. SiP micro-ring modulators are of particular interest for short reach applications due to their small footprint and low power consumption [62], [63], [44].

However, due to their high thermal sensitivity and need for wavelength-stabilization, transmitters based on microring modulator require sophisticated circuits compared to TW-MZM. Several high performances SiP TW-MZM are reported [17], [26], [64]. Although these modulators have achieved low bit error rates at high symbol rates, they have not necessarily achieved optimal designs for a given system context. To design an optimized electro-optic modulator, specific system-level criteria and performance quality factors have to be considered. These factors could be different for an integrated optical modulator compare to its stand-alone discreet counterpart.

Traditionally, TW-MZMs were implemented in non-silicon based electro-optic platforms (i.e., LiNbO3), benefiting from the inherent electro-optic effect of the material. TW MZM for these low-loss optical platforms have performance determined by two parameters (assuming matched impedance): the required voltage to generate π radian phase shift, known as V_π, and the electro-optic bandwidth. The electro-optic effect has an almost linear relation between the phase variation and the applied driving voltage. The efficiency, defined as V_π.L, is employed to quantify the modulation performance. The bandwidth optimization and efficiency could be decoupled in this design, and V_π is independent of bias voltage.

While V_π and electro-optic bandwidth remain important optimization factors for SiP, on-chip optical loss is an additional challenge. The lack of an electro-optic effect in silicon leads to exploitation of the plasma dispersion effect in p-n doped silicon. Optical absorption in the p-n doped silicon waveguide is significant and potentially limits performance.

To date, the efficiency V_π.L is employed to quantify SiP modulation performance. Although this figure of merit clearly shows the trade-off between the modulator length and the required voltage for π radian phase shift, it does not include the significant optical loss introduced by the phase shifter. More recently $V_\pi.\alpha$.L (known as efficiency-loss) is used to quantify

SiP modulation performance, where α parametrizes optical loss induced by the reverse biased p-n doped silicon waveguide in the phase shifter [65], [66]. Moreover, in contrast to other electro-optic platforms (i.e., LiNbO3), V_π of the electro-optic modulators in silicon is not a linear function of L (nor the applied voltage). Hence, the efficiency of the SiP modulator changes with its length.

None of the previous efficiency-based FOMs (V_π.L or V_π.α.L) is able to predict the system level performance of the modulator in a real optical link. This limitation can be attributed to the absence of the modulator electro-optic bandwidth in the FOM.
A new figure of merit for SiP modulators was presented recently in [67] that takes into account system parameters such as peak-to-peak drive voltage, bit rate, modulator rise-fall time, and relative optical modulation amplitude, similar to the objectives of this paper. In that work, as in this, a low pass filter is employed to capture bandwidth limitations. While we use a theoretical prediction of bandwidth, they rely on measured rise times (i.e., a FOM useful for characterization rather than design).

In [67] they also employ a normalized OMA, focusing on extinction ratio. While we focus on intersymbol interference in PAM-M for our MPP, they focus on overall extinction ratio, and suggest the measured rise time could be modified to account for PAM-M signaling. Using the theoretical prediction of bandwidth, we arrive at a simpler equation for the FOM based on baud rate of the input data, electro-optic bandwidth and efficiency–loss of the modulator.

In this chapter, the modulator power penalty induced by the SiP modulator is used to study the system level performance degradation caused by a SiP modulator in an optical pulse-amplitude-modulation link. The SiP modulator limiting factors (optical loss, limited extinction ratio and electro-optic bandwidth limitation) are included in the MPP. A normalized optical modulation amplitude is shown via simulation to be a reliable predictor of the minimal achievable MPP.

Based on these insights, a new figure of merit is presented that includes not only the optical loss and efficiency, but also the SiP modulator electro-optic bandwidth, BW_{EO}. This new FOM can map SiP modulator physical design parameters to its system-level performance, facilitating both device design and system optimization.

This chapter is organized as follows: in Section 3.2 we describe SiP TW MZM simulation. Section 3.3 presents the definition of past MPPs and the new MPP including the BW_{EO} limitation. In section 3.4, OMA_N is presented and employed to define a new figure of merit. Various simulations are presented to demonstrate the utility of the FOM. After a discussion about the overall procedure of the FOM calculation in section 3.5, a summary of achievements in this work is presented in section 3.6.

3.2 SiP TW-MZM Modeling

3.2.1 SiP modulator model and operation

Traveling wave Mach-Zehnder modulators are the most promising candidates for commercial optical transmitters due to their thermal insensitivity and high tolerance to fabrication imperfections as compared to micro-ring modulators. Although we focus here on TW-MZMs, the procedures we describe could be extended to apply to other modulators as well.

Consider a typical traveling wave SiP Mach-Zehnder modulator that employs silicon waveguides with lateral p-n junctions. Figure 3.1 presents a schematic of a SiP TW-MZM driven in a series push-pull configuration. A negative voltage is applied between the two arms of the MZM, and the traveling wave electrodes are terminated through a matched load.

The cross section of the SiP MZM in a CMOS compatible SiP process on a 220-nm SOI wafer with 2 μm buried oxide (BOX) and lateral p-n junction (i.e., A$*$STAR's IME, Singapore) is the same as the one presented in figure 2.4 in the second chapter, section 2.3. We use the same procedure as the one presented in section 2.3 (figure 2.2), to predict the electro-optic characteristics of the the phase shifter in Lumerical software. We use the same doping densities and wavelength of $\lambda = 1550$nm, unless otherwise noted. We find the change in effective index, Δn_{eff}, in Lumerical as a function of applied reverse voltage. A plot of Δn_{eff} is given in figure 2.5b.

Let V_{in} be the RF input voltage that can be positive or negative and falls between -$V_{p-p}/2$ and $V_{p-p}/2$. The input voltage in combination with a bias voltage V_b is applied in the push-pull configuration seen in figure 3.1. Due to the inductive bias coupling, one arm sees RF voltage V_b plus $V_{in}/2$, while the other arm sees V_b minus $V_{in}/2$. The inset in figure 3.1a shows two types of input voltage V_{in}: a sinusoidal input and a PAM-4 signal. In push-pull operation and assuming two identical arms for the TW-MZM, the instantaneous modulator phase shift is given by:

$$\Delta\phi\left(V_{in}\right) = \left[\Delta n_{eff}\left(V_b + \frac{V_{in}}{2}\right) - \Delta n_{eff}\left(V_b - \frac{V_{in}}{2}\right)\right]\frac{2\pi L}{\lambda} \tag{3.1}$$

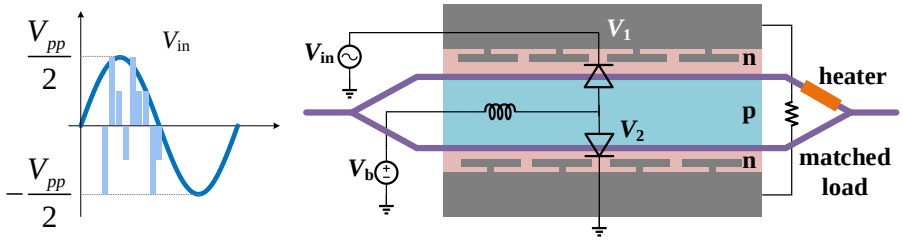


Figure 3.1 – Traveling wave electrode MZM in series push-pull driving scheme.

The instantaneous output power is given by:

$$P_{out} = P_{in}e^{-\alpha L}Cos^2(\frac{\Delta\phi(V_{in})}{2} + \theta_0) \tag{3.2}$$

The phase offset between the two arms is nominally set at $\theta_0 = \frac{\pi}{4}$, but can be tuned to any value by use of an on-chip heater. This default choice sets operation at quadrature. For zero input voltage, the output is at its median value (cosine squared is one-half). For an effective index change that is linear with applied voltage, at quadrature the output power is symmetric (vis-à-vis input voltage) about this median, and we can get maximum output swing.

3.2.2 Effect of nonlinear Δn_{eff} on push-pull operation

The input voltage swing to achieve an output swing from maximum to minimum of the cosine-squared function is called V_π. For effective index change that is linear with applied voltage (such as in lithium niobate) we have:

$$\Delta n_{eff}(V_{in}) = m.V \Rightarrow P_{out} \propto Cos^2(\frac{\pi L}{\lambda}mV_{in} + \frac{\pi}{4}) \tag{3.3}$$

Where m is a constant. Considering:

$$\Delta\phi = \frac{2\pi L\Delta n_{eff}}{\lambda} \tag{3.4}$$

in this case,

$$V_\pi = \frac{\lambda}{2mL} \tag{3.5}$$

which is independent of bias voltage.

For nonlinear effective index change, however, each bias voltage yields a different V_π. To find this value we define V_x as the voltage (a negative value) that achieves maximum cosine squared for a given V_b, and V_y as the voltage (a positive value) that achieves minimum cosine squared. Then solve:

$$\Delta n_{eff}(V_b + \frac{V_x}{2}) - \Delta n_{eff}(V_b - \frac{V_x}{2}) = -\frac{\lambda}{4L} \tag{3.6}$$

$$\Delta n_{eff}(V_b + \frac{V_y}{2}) - \Delta n_{eff}(V_b + \frac{V_y}{2}) = +\frac{\lambda}{4L} \tag{3.7}$$

$$\overset{(3.6),(3.7)}{\Longrightarrow} V_\pi = V_y - V_x \tag{3.8}$$

The output power is no longer symmetric (vis-à-vis input voltage) around its median value. The case for λ = 1550 nm, L = 5 mm, V_b = -0.25 V is given in figure 3.2 as a plot of transmission (normalized output power) vs. In general, the definition of V_π may encompass a voltage input range that is not desirable for all bias voltages. For instance, V_y may be larger than $|V_b|$, leading to forward bias operation.

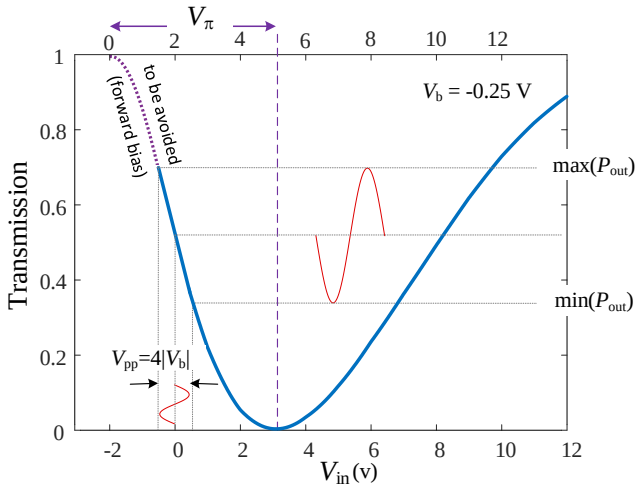


Figure 3.2 – For the SiP MZM in figure 3.1, operating at quadrature: instantaneous transmission for length L =5 mm for Vb = -0.25 V.

Forward bias is to be avoided for wide bandwidth operation. In a push-pull driving scheme where the RF input voltage is split in half, the bias voltage should be at least as negative as $V_{p-p}/4$. For maximum swing when operating at quadrature we choose $V_{p-p} = 4|V_b|$. Unlike $LiNbO_3$, each V_b generates a different transmission curve, and a different V_π. In the balance of the paper, all values of V_π are found using the nonlinear Δn_{eff} behavior found in Lumerical simulations of a specific phase shifter length L, and numerically solving (3.2) given the bias V_b being investigated.

3.3 MPP Including ISI

A figure of merit is only as good at the modulator power penalty from which it is developed. We start this section with the simple MPP developed for on-off keying (OOK) that took into account loss and limited extinction ratio of the modulator. We then expand the MPP to accommodate PAM-M signaling and the impact on this modulation of the modulator limited bandwidth.

3.3.1 Past MPP for OOK

Previous efforts to develop a figure of merit for silicon photonic modulators have by in large focused on OOK. In order to obtain the maximum optical eye opening, the modulator is operated at its quadrature point. The output excursions for this configuration result in a certain extinction ratio (ER) and optical modulation amplitude (OMA) defined as:

$$ER = \frac{maxP_{out}}{minP_{out}} \tag{3.9}$$

$$OMA = maxP_{out} - minP_{out} \tag{3.10}$$

Previous transmitter power penalty (MPP) take into account a reduction in output power due to loss and limited extinction ratio:

$$MPP_{old} = P_{\alpha L} + P_{ER(OOK)} \tag{3.11}$$

The first term, $P_{\alpha L}$ reflects the high optical loss introduced by the phase-shifter. The second term, $P_{ER(OOK)}$, accounts for reduced extinction ratio for a fixed driving voltage swing due to high V_π. For OOK, the penalty from limited extinction ratio is defined as the increase in average power needed to obtain the same bit error rate as an ideal pulse with infinite extinction ratio.

3.3.2 New MPP for PAM

For a multilevel modulation format (e.g., PAM-M) the received optical power has to be split among M symbols. Assuming thermal noise dominates, and equal separation between PAM levels [19], the power penalty from limited ER for PAM-M is

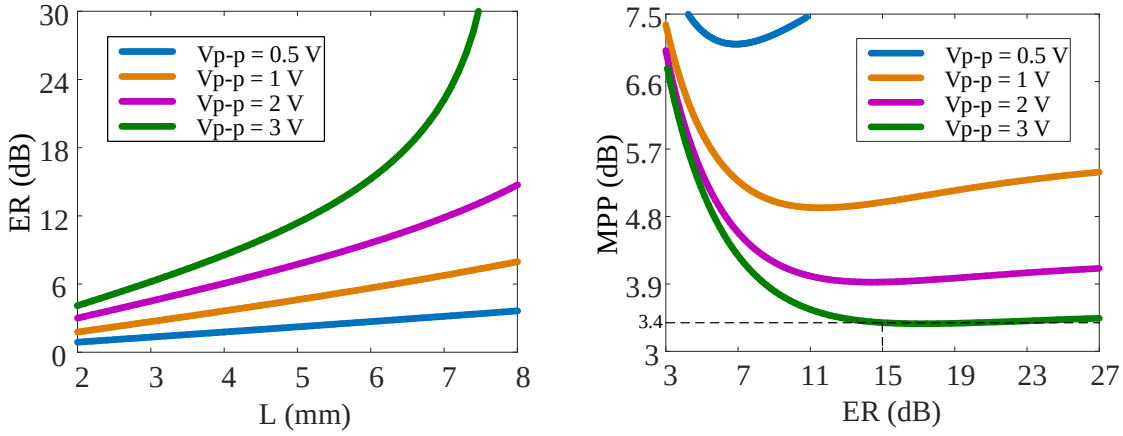
$$\begin{aligned} P_{ER(PAM)} &= P_{ER(OOK)} - 10.log_{10}\left(\frac{M-1}{log_2 M}\right) \\ &= 10.log_{10}\left(\frac{ER-1}{ER+1} \times \frac{M-1}{log_2 M}\right) \end{aligned} \tag{3.12}$$

Figure 3.3a shows how the extinction ratio, defined in (3.9), varies with phase shifter length for various bias points. The curves were found by examining the maximum achievable power swing, per (3.2), in the push pull configuration for these biases. Figure 3.3b takes these ERs and calculates the MPP (extended for PAM) due strictly to the new ER penalty, i.e., for $P_{ER(PAM)}$ replacing $P_{ER(OOK)}$ in (3.11).

3.3.3 New MPP for for limited electro-optic bandwidth

The bandwidth limitation of a modulator increases the link penalty by introducing inter symbol interference (ISI). ISI is often the ultimate limit to achievable bit rate in high performance systems. Hence, it is critical that the MPP encompass this limitation. In appendix A.1, we develop a simple predictor of the modulator -3 dB bandwidth, BW_{EO}, to quantify this limitation.

Focusing on PAM-M modulation, we further develop an estimate of the ISI penalty under several simplifying assumptions. Figure 3.4 gives an illustration of a typical PAM-4 eye diagram; the eye is noiseless and eye closing is strictly due to the finite rise and fall times. If the modulator had infinite bandwidth, the eye would be rectangular with eye opening equal to the distance between rails, as indicated in figure 3.4.



(a) (b)

Figure 3.3 – For PAM-4 modulation of SiP MZM in figure 3.1, operating at quadrature at various bias voltages with $V_{p-p} = 4|V_b|$. a) ER vs. modulator length L, and b) modulator power penalty (MPP) vs. extinction ratio.

The MPP in figure 3.3b does not include any bandwidth limitation, and is based on this ideal eye opening. The presence of a limited bandwidth, BW_{EO}, leads to the eye becoming less open. We define the ISI penalty, Δ_{ISI}, as the difference between the infinite bandwidth eye opening and the limited bandwidth eye opening. Note that to the right of the eye diagram we have labeled levels for an arbitrary M levels of modulation. We adopt the simplifying assumptions proposed in [68]. The first simplifying assumption in finding the ISI penalty is the pulse at the modulator output having a Gaussian shape that is parameterized by BW_{EO}. The eye diagram in figure 3.4 was plotted for this Gaussian pulse shape for $\text{BW}_{EO} = 18$ GHz

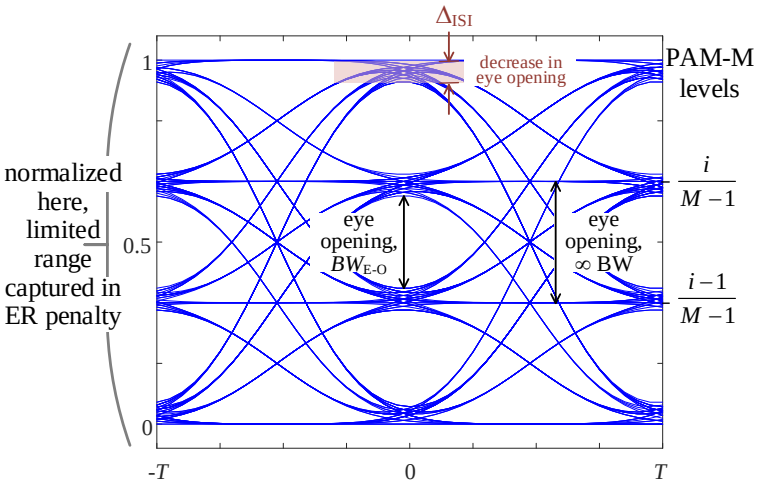


Figure 3.4 – Noiseless eye diagram for PAM-4 modulation format; Gaussian shaped pulses with $BW_{EO}/\text{BR} = 0.9$.

and BR = 20 Gbaud.

The next simplifying assumption is ISI dominated by contributions from the two nearest neighbors; contributions from more distant symbols are neglected. Finally, we find the decrease in the eye opening on the upper most eye, as illustrated in figure 3.4, and use it as the nominal ISI penalty. This simplification neglects the fact that eye opening varies across the M-1 eyes, but provides a tractable closed-form solution.

Recall that the term $P_{ER(PAM)}$ already accounts for multiple PAM eyes across a reduced extinction ratio. Under the assumptions described, the ISI leads to an additional power penalty in dB of:

$$P_{ISI} = 10.log_{10}\left(1 - M.erfc\left(\frac{\pi}{2\sqrt{ln2}}\frac{BW_{EO}}{BR}\right)\right) \tag{3.13}$$

where *erfc* is the complementary error function. Details of the derivation are provided in appendix A.2. We define a new MPP that includes effect of modulator bandwidth limitations:

$$MPP = P_{\alpha L} + P_{ER(PAM)} + P_{ISI} \tag{3.14}$$

3.3.4 Weaknesses of MPP neglecting bandwidth limitations

For a fixed value of RF driving voltage (V_{p-p}), increasing the phase-shifter length improves the extinction ratio (by decreasing the V_π), as seen in figure 3.3a. When the optical loss and limited extinction ratio are the only shortcomings of the modulator, higher extinction ratio leads to a lower (old) MPP, as seen in figure 3.3b.

There is some downside to the move to longer phase shifters; higher optical loss eventually overshadows ER advantages, i.e., higher extinction ratio will not always improve the old MPP. However, the old MPP vs. L has a very shallow bowl shape for long L. We see from figure 3.3b that bias voltage affects the shallowness of the bowl shape in SiP, as bias voltage affects V_π.

Consider now the new MPP that takes into account the bandwidth limitation of the modulator. In figure 3.5 we plot in pink dashed line (y-axis on the right) the dependence of this bandwidth, BW_{EO}, on L; see appendix A.1. All other plots in figure 3.5 refer to the y-axis to the left. The old MPP is included for easy reference in the dashed black curve. The new transmission power penalty (3.14) is shown in solid lines for several baud rates. We report multiple baud rates as it is the ratio of bandwidth to baud rate, implicit in (3.13), that determines the relative importance of the ISI contribution to MPP in (3.14).

At 14 Gbaud, the ratio BW_{EO}/BR is large for almost all L (see pink curve); therefore, ISI is negligible at 14 Gbaud. At this low baud rate, the old and new MPP nearly coincide (green, solid 14 Gbaud and black, dashed old MPP). This is to be expected, as (3.14) collapses to (3.11) for low ISI.

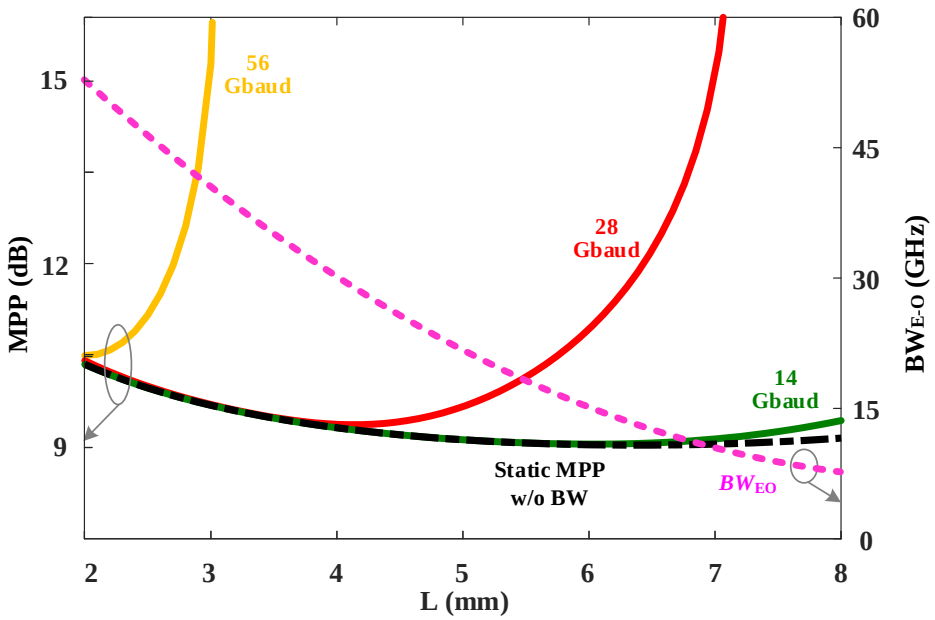


Figure 3.5 – New MPP from (3.14) for PAM-4 modulation format, with y-axis at left, for different baud rates (solid lines) when $V_{p-p} = 4|V_b| = 3V$; black dashed line is old MPP without bandwidth effects; pink dotted line is electro-optic bandwidth BW_{EO}.as a function of L, with y-axis at right.

Most modern communications systems are designed to push the baud rate to achieve maximal throughput for the network. We can see that as baud rates become more aggressive, the new MPP has a much steeper bowl shape than the old MPP. Hence, at these rates the old MPP is a poor guide to the best choice of phase shifter length. While the old MPP has a minimum in the region of 6-7 mm for the phase shifter, the new MPP tells us this value is only valid for low baud rates. At rates as high as 56 Gbaud, the minimum penalty is found at L = 2 mm. Even at 28 Gbaud, the optimal L is around 4.5 mm, far from the value predicted by the old MPP.

Previous FOMs have been based on minimizing the old MPP. These FOMs focused on behavior in figure 3.3a, improving ER by targeting a small V_π. From our examination of the new MPP, this approach will not guide the designer to an optimal choice of L. Efficiency-based FOMs ($V_\pi L$ or $V_\pi \alpha L$) cannot predict the system level performance for SiP as they overlook bandwidth constraints. In LiNbO3 modulators, bandwidth could be addressed without affecting efficiency. For SiP, bandwidth and efficiency performance measures are intricately intertwined. In the next section, we find a strategy to find an FOM that can nonetheless account for ISI.

3.4 MPP and FOM

Being now armed with an improved MPP that tracks the impact of a given design (phase shifter length L), and operating point (driving voltage and baud rate), we go in search of a useful figure of merit to optimize performance. We consider a normalized optical modulation amplitude as a good predictor of performance, and propose a FOM inspired by this quantity.

3.4.1 Normalized optical modulation amplitude

Consider optical modulation amplitude for a potential FOM. Higher OMA corresponds to more open optical eye, thus lower BER and consequently, lower MPP. With an interest in PAM-M modulation, we consider the following normalized version of the OMA.

$$OMA_N = \frac{1}{M-1}\left(\frac{\underset{(open-eye)}{max} P_{out} - \underset{(open-eye)}{min} P_{out}}{P_{in}V_{p-p}}\right) \tag{3.15}$$

This approach focuses on extinction ratio in the PAM-M eyes, and removes the dependence on input power and driving voltage. We compare via simulation the behavior of the new MPP and the normalized OMA_N for several baud rates. It is important to note that the output power extrema are defined over an open eye.

We generate random PAM-4 data at each baud rate. The square wave signals are passed through a low pass filter with a Gaussian shaped frequency response with a 3 dB bandwidth equal to BW_{EO} for the given modulator design (fabrication process and phase shifter length, L) and operating point ($\text{V}_{p-p} = 4\,|V_b|$). The filtered waveform is used to calculate the output power via (3.2) using Δn_{eff} found numerically for the given design. The maximum and minimum output power over an open eye are used in (10) to find OMA_N.

We simulated four baud rates, BR: 14, 28 and 56 Gbaud for PAM-4 modulation. In figure 3.6, we recreate in dotted lines the new MPP from figure 3.5 for each BR, referring to the left y-axis. The OMA_N (right y-axis) is presented in solid lines. We see that the OMA_N has inverse behavior to the MPP. An asterisk indicates the minimum values of the MPP, while triangle markers indicate the maxima of OMA_N, that is:

$$\underset{(asterisks)}{L_{OMA} = \underset{L}{min}(OMA_N)} \quad \underset{(triangles)}{L_{MPP} = \underset{L}{min}(MPP)} \tag{3.16}$$

Let ΔL be the difference between the true optimal L (minimum MPP) and the optimal L predicted by the OMA_N.

$$\Delta L = L_{OMA} - L_{MPP} \tag{3.17}$$

Let ΔMPP be the excess penalty of the best choice for L predicted by OMA_N, and the best choice of L predicted by the minimum MPP, i.e.

$$\Delta MPP = MPP\,(L_{OMA}) - MPP\,(L_{MPP}) \tag{3.18}$$

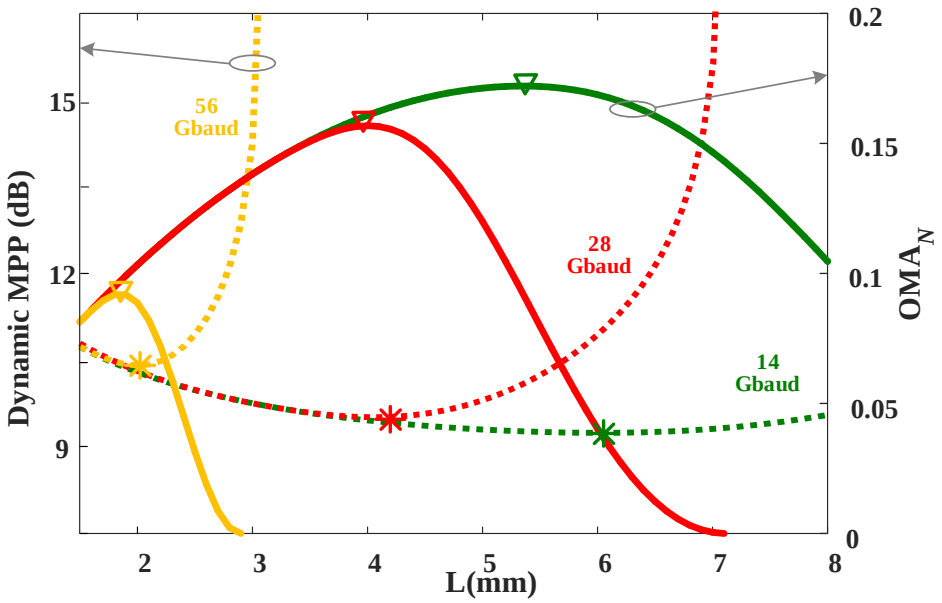


Figure 3.6 – New MPP (with bandwidth limitation) and normalize OAM for different baud rates when $V_{p-p} = 4|V_b| = 3V$; triangles indicate maxima of FOM, while asterisks indicate minima of MPP. Deviations in phase shifter length L at these extrema, and excess penalty are given in the table.

This is the excess MPP when using the OMA to design the phase modulator. Both ΔMPP and ΔL are given in the table table 3.1. We can see that the deviation and the excess penalty are small. Hence, normalized OMA can be used as a measure to predict an optimum modulator design for a given system operating driving voltage V_{p-p} (or equivalently, bias point V_b).

Table 3.1 – Changes in MPP and L for different baud rates according to figure 3.6

BR(Gbaud)	14	28	56
ΔMPP**(dB)**	0.03	0.03	0.1
ΔL**(mm)**	0.55	0.25	0.25

3.4.2 Figure of merit with bandwidth limitation

We begin with the normalized OMA in (3.15) and strive to reduce the terms to retain the essence of the MPP behavior, while highlighting the parameters wielding the greatest influence. We start with a discussion of how OAM_N could resemble previous FOMs, and how the bandwidth limitation manifested itself in OAM_N.

Suppose the modulator transfer function and Δn_{eff} are linear in applied voltage. In this

case the maximum modulator swing (highest PAM value less the lowest PAM value yields)

$$\begin{aligned} \underset{V}{max} P_{out} - \underset{V}{min} P_{out} &= P_{M-1} - P_0 \\ &= P_{in} e^{-\alpha L} \frac{V_{p-p}}{V_\pi} \end{aligned} \tag{3.19}$$

This only brings us to a denominator $e^{-\alpha L} V_\pi$. Assuming a Taylor expansion for the exponential in total loss (αL), this yields the previous efficiency-based FOM, $V_\pi.\alpha.L$.

We are missing the low-pass filtering present in the simulated OAM_N. The efficiency-based FOM is applicable to a DC input, or an infinite bandwidth response to a data modulated signal. The steepness in the inverted bowl of the OMA_N can be attributed to the ISI-induced reduction in the eye opening illustrated in figure 3.4, which is modeled mathematically by the low-pass Gaussian filter in the simulation. Therefore, we return to the MPP itself to introduce an ISI term.

$$FOM = V_\pi.\alpha.L \frac{M-1}{1 - M.efrc\left(\frac{\pi}{2\sqrt{ln}} \frac{BW_{EO}}{BR}\right)} \tag{3.20}$$

Note that BW_{EO} is a function of L and V_b. As discussed in appendix A.3, the complementary error function can be well approximated by an exponential in the region of $\frac{BW_{EO}}{BR}$ observed in typical optical communications systems. This approximation leads to:

$$FOM = V_\pi.\alpha.L \frac{M-1}{1 - \frac{M}{2}.exp\left(-4.34\left(\frac{BW_{EO}}{BR}\right)^2\right)} \tag{3.21}$$

where α represents the optical loss per unit length of the modulator in Np/cm, L is length of the phase shifter in centimetres, BR is the system baud rate, BW_{EO} is the modulator -3 dB bandwidth and M is the PAM modulation level. The V_π term is found as described in (3.8), and is a function of the system operating driving voltage V_{p-p} (or equivalently bias point V_b) and the modulator length, L. Hence the FOM is a function of the fabrication process (parameters used in Lumerical to find Δn_{eff}), the operating point (baud rate and driving voltage), and the phase shifter design (L which determines BW_{EO}).

In figure 3.7, we simulate four baud rates for PAM-4 modulation format, again recreating the new MPP from figure 3.5. The FOM (right y-axis) is presented in solid lines. We see that the FOM has the same steep bowl behavior observed in the MPP. Stars are used to indicate minima of FOM, while diamonds indicate minima of MPP. The excess MPP, ΔMPP, and ΔL the deviation in the FOM predicted optimal L and MPP predicted optimal L are reported in the table 3.2. We readily observe that the FOM has achieved our objectives:

i) it is an excellent predictor of optimal design with only minimal excess penalty.
ii) it is a simple function of system parameters both readily simulated and readily characterized experimentally.

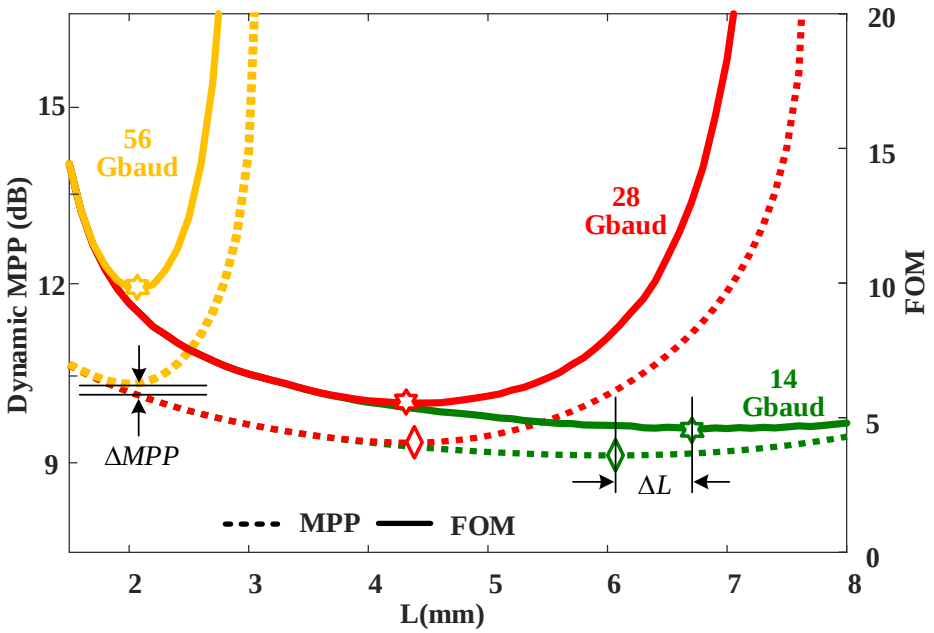


Figure 3.7 – New MPP (with bandwidth limitation) and new FOM for different baud rates when $V_{p-p} = 4|V_b| = 3V$; stars indicate minima of FOM, while diamonds indicate minima of MPP. Deviations in phase shifter length L at these minima, and excess penalty are given in the table.

Table 3.2 – Changes in MPP and L for different baud rates according to figure 3.7

BR(Gbaud)	14	28	56
ΔMPP**(dB)**	0.03	0.03	0.1
ΔL**(mm)**	0.6	0.15	0.2

3.5 Discussion

Previous results were limited to one choice of bias voltage and four baud rates. We simulated the excess MPP when sweeping both bias voltage (or equivalently driving voltage since we assume $V_{p-p} = 4\,|V_b|$) and baud rate. Results are presented in figure 3.8 as a color map. We observe that the excess MPP remains below 0.1 dB for the entire range of operating points and system baud rates. Indeed, the majority of the examined space has excess MPP below 0.05 dB.

We pause here to make a few observations about the FOM that has been developed. The mathematical model we assumed had two important characteristics, as illustrated in the block diagram of figure 3.9. We model the modulator as having a low pass impulse response following a Gaussian shape parameterized by a -3 dB bandwidth. The filtered signal is then assumed to experience an instantaneous nonlinearity described by the raised cosine function. In addition, there is the loss proportional to the phase shifter length in the modulator. Compared to the

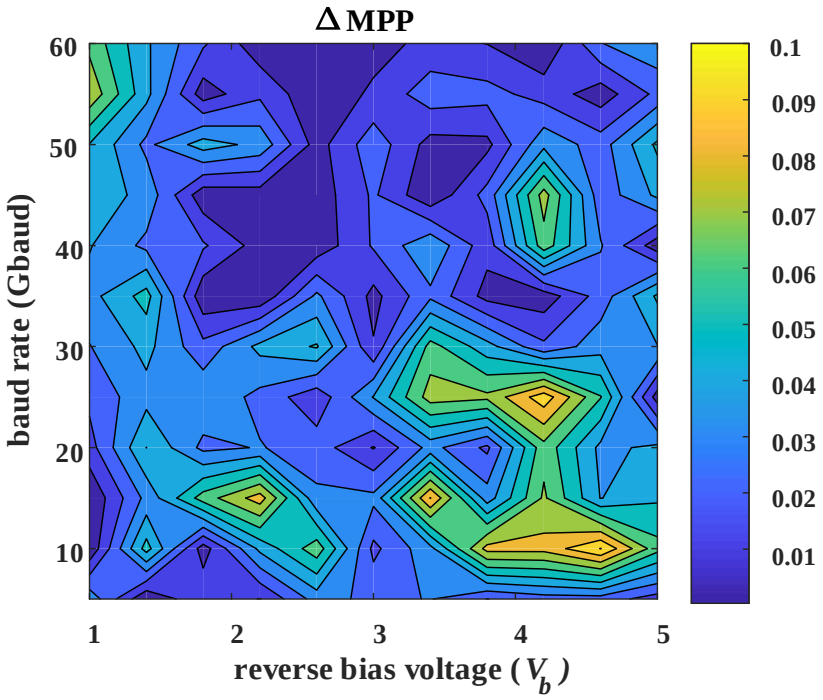


Figure 3.8 – Excess MPP in dB when using optimal L found from FOM, L_{FOM} rather than optimum L found from MPP directly, L_{MPP}.

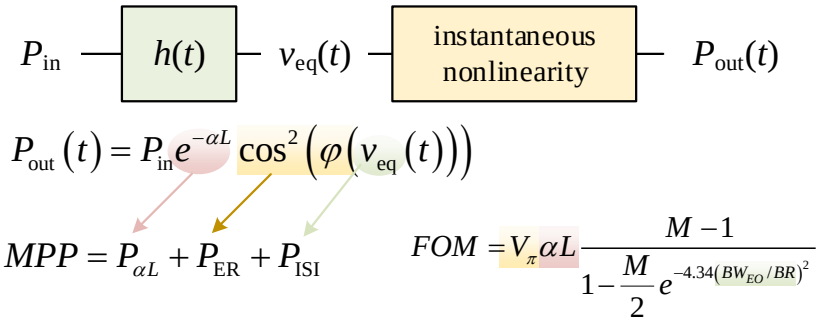


Figure 3.9 – Mapping of impairments to their representations in the transmission power penalty and the FOM.

FOM in [67], we both use a low pass filter whose shape is parameterized by a ratio capturing the relative importance of the bandwidth limitation: in our case $\frac{BW_{EO}}{BR}$, in their case the ratio of rise time to bit duration. In [67], the order of the low pass filter was assigned by fitting measured data for binary non-return-to-zero (NRZ); here, we used a theoretical approach. This allowed us to relate the low pass filter bandwidth to the phase shifter length L, as detailed in the appendix A.1. Next, a Gaussian shape filter is used to yield a closed form expression for the filtering effect (via the erfc). For this reason, our FOM has an exponential dependence on $\frac{BW_{EO}}{BR}$. Note that by basing our filter on phase shifter length, our FOM can be used directly for TW-SiP MZM design.

The low pass nature of the model captures the ISI produced by a limited bandwidth modulator. ISI appears in the MPP in the form of a power penalty due to decreased eye opening. ISI appears in the FOM in a simplified expression for that decreased eye. We note that our model ignores the instantaneous nonlinearity in the calculation of the decreased eye, i.e., that the low pass occurs before the cosine squared. We call this nonlinearity instantaneous because is assumes infinite bandwidth, that is, any change in input voltage is immediately observed as a change in output power. The true modulator may be a non-instantaneous, non-stationary nonlinearity.

The V_π term is deceptively simple. We must not forget that in SiP, V_π depends on the bias voltage as well as L. As previously discussed in section 3.2, the SiP FOMs cannot assume a constant product V_π.L, as is found in lithium niobate modulators. For an existing modulator, V_π can be readily measured; in developing a design it can be simulated by combining information on Δn_{eff} in Lumerical and information on the driving voltage.

We have focused on improving the sub-eye opening in PAM-M modulation format, not just the outer eye. By contrast, [67] focused on the overall extinction ratio (i.e., outer eye). That FOM has to be adjusted (through modification of the bit interval and the low pass filter order) for different modulation formats. The dependence on system and MZM parameters is directly visible in our FOM.

3.5.1 FOM for different doping concentration

In order to examine how the optimum point predicted by the new FOM changes when the process parameters change, we simulate FOM for a SiP TW-MZM in a lateral p-n junction process (see figure 2.4) with five distinct doping concentrations. In this set of simulations, we consider P3 (used to produce results throughout the paper, including figure 3.8) as a reference process, where doping densities are NA = 5×10^{17} cm^{-3} and ND = 3×10^{17} cm^{-3}. P1, P2, P4, and P5 are processes whose doping concentrations compared to P3 are modified by -50%, -25%, +25%, and +50%, respectively.

We have already established in figure 3.8 that the excess MPP is small for P3. Although not presented here, simulations for the other processes yielded similar results; the excess was small. Therefore, in this section we present instead the absolute MPP performance for different process choices. We plot the minimum MPP (by sweeping the phase shifter length) in dB for different baud rates and bias voltages for P1, P3 and P5. In figure 3.10a, 3.10b and 3.10c, respectively. When the doping concentration is relatively low, P1 case, the low efficiency of the phase shifter is the dominant limiting factor. A longer phase shifter is needed to achieve same MPP as P3. However, longer phase shifter will affect BW_{EO}. This effect could be observed in figure 3.10a, where compare to P3 in figure 3.10b, minimum MPP is more sensitive to the baud rate.

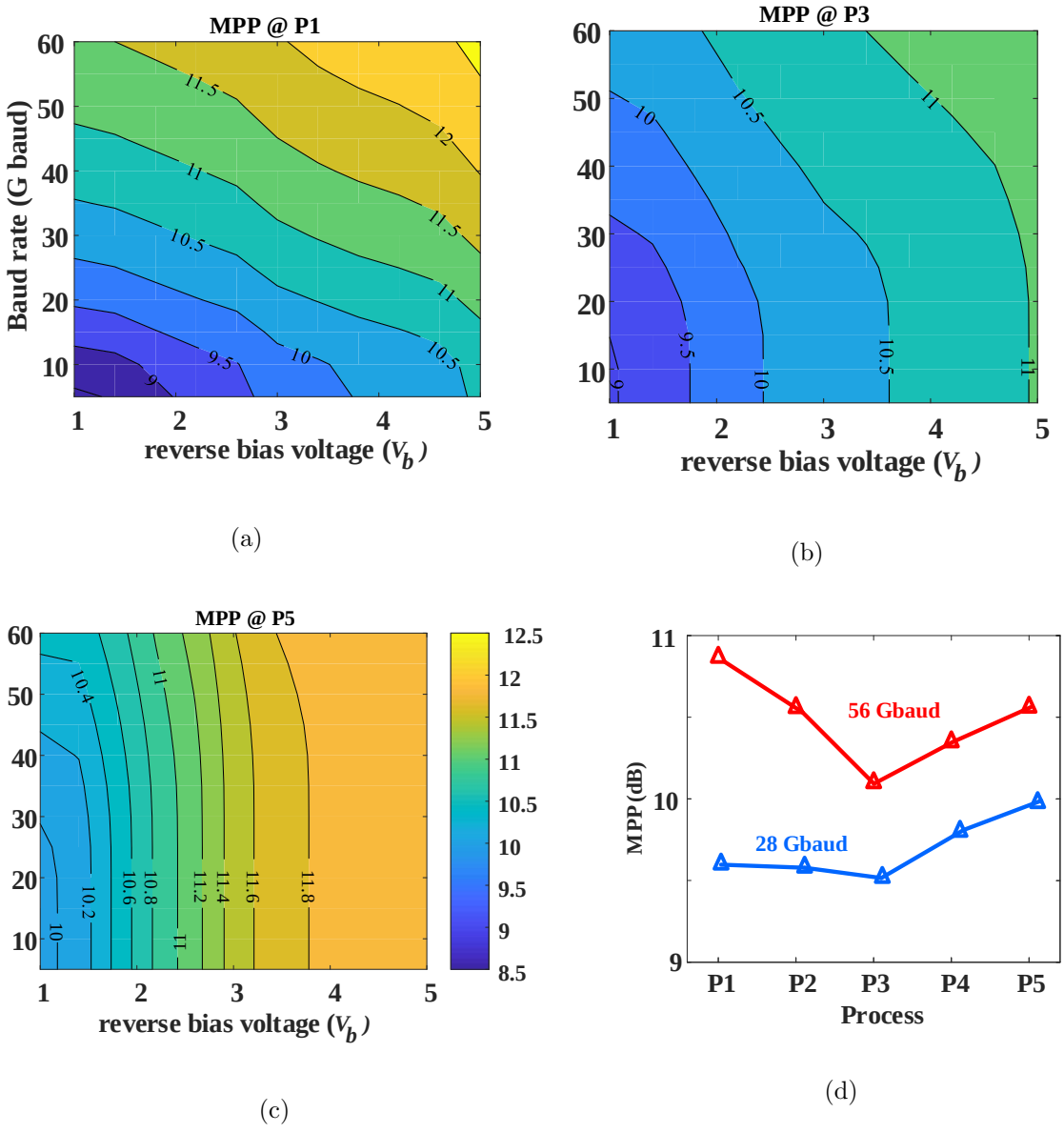


Figure 3.10 – All simulations are PAM-4 modulation of a modulator operating at quadrature. The excess MPP as a function of reverse bias and baud rate are given for doping concentrations of a) -50%, b) 0%, c) +50%; d) Effect of different doping concentration on MPP for two different baud rates at $V_{p-p} = 4|\text{Vb}| = 2$ V.

On the other hand, when the doping concentration is increased compared to P3, optical loss is the main limiting factor. To achieve the same MPP as P3, a shorter phase shifter is needed, translating into higher BW_{EO}. figure 3.10c shows that MPP is very sensitive to the reverse bias voltage that increases the optical loss, but less sensitive to the baud rate.

While these previous figures allow us to find performance for any operating point for three of the potential fabrication processes, suppose the operating point is fixed and we wish

to compare processes directly. We select $V_{p-p} = 4\,|V_b| = 2$ V for two transmission rates, 56 Gbaud and 28 Gbaud PAM-4. We plot the MPP versus the five potential fabrication processes in figure 3.10d. For either baud rate, P3 is the best trade-off, although the difference is marked at 56 Gbaud, and less critical at 28 Gbaud. This plot shows how the new FOM can be used to select a process according to system level requirements.

3.6 Conclusion

A simple closed-form expression is provided for a figure of merit to assess SiP TW-MZM modulator performance in an optical pulse-amplitude-modulation link. The FOM is a function of modulator parameters that can be easily found either via simulation (during the design process) or characterization (in selecting an appropriate, existing modulator). We show that, unlike the proposed FOM, traditional FOMs are unable to predict the effect of limited bandwidth in SiP modulators.

Extensive simulations validated the efficacy of the FOM to predict system performance as quantified by the modulator power penalty . The new FOM maps the physical and design parameters of a SiP TW-MZM to its system-level effect in a PAM-M optical link. One can use this FOM to choose the optimum bias and driving voltage, or optimally design a modulator for specific system-level criteria. The FOM allows us to observe how far the baud rate could be pushed for a tolerable range of MPP.

Finally, the effect of variation in process is also presented, confirming that the new FOM not only can be used to predict the optimum phase-shifter length, bias voltage or driving signal in a specific process, but also to select the optimum doping concentration to minimize the SiP TW-MZM MPP for a given system context.

Chapter 4

Silicon Photonic In-phase and Quadrature-phase Modulators for 400 Gb/s and beyond

Résumé- Les transmetteurs photoniques sur silicium ont un énorme potentiel qui peut etre utilisé dans des liaisons optiques cohérentes à très grande capacité. Une méthodologie orientée système est requise pour une conception de modulateur optimal dans un procédé de fabrication donné. Nous proposons une approche d'optimisation de la conception et du fonctionnement d'un modulateur IQ photonique en silicium, qui minimise sa pénalité de puissance introduite dans une liaison de transmission à modulation d'amplitude en quadrature. Nous examinons le compromis entre l'efficacité de la modulation et la bande passante pour la combinaison optimale de la conception et du fonctionnement du modulateur afin de maximiser la distance libre entre les points de constellation adjacents. Cet optimum dépend du débit en bauds et du format des données d'entrée et de la plage de variation de tension de controle. Nous démontrons une conception de modulateur IQ en mode depletion par ondes progressives optimisé pour QAM d'ordre supérieur en utilisant un procédé de fabrication compatible CMOS. Les résultats obtenus concordent avec la simulation et confirment nos prédictions en utilisant la méthodologie proposée. Des débits de données nets jusqu'à 232 Gb/s (70 Gbaud 16-QAM) sur une seule polarisation, ce qui indique un grand potentiel pour une transmission à double polarisation de 400^{+}Gb/s.

Abstract- Silicon photonic transmitters have enormous potential for ultra-high-capacity coherent optical links. A system-orientated methodology is required for an optimal modulator design in a given process. We propose an approach to optimization of design and operation of a silicon photonic IQ modulator, which minimizes its power penalty introduced to a quadrature amplitude modulation transmission link. We examine the trade-off between modulation efficiency and bandwidth for the optimal combination of modulator design and operation to

maximize the clear distance between adjacent constellation points. This optimum depends on baud rate and format of input data and the achievable driving voltage swing. We demonstrate a design of travelling-wave depletion-mode IQ modulator optimized for higher-order QAM using a CMOS-compatible process. Measured results agree well with simulation and confirm the prediction using the proposed methodology. Net data rates up to 232 Gb/s (70 Gbaud 16-QAM) on single polarization are captured, indicating great potential for 400^{+}Gb/s dual-polarization transmission.

4.1 Introduction

The fast growing demand for ultra-fast optical links reveals need for low-cost, integrated coherent transmitters. This driving force pushes research in silicon photonics because of its advantages over other platforms (i.e. LiNbO3 and InP), such as compatibility with CMOS fabrication process and the ability of on-chip polarization manipulation.

However, the design of high-capacity silicon photonic (SiP) modulators is in general more challenging. In spite of several successful demonstrations employed in high-capacity direct or coherent detection systems [69] [70], [71], [36] there still exists a gap between optimization of SiP transmitters and system-level applications. Most of the previously reported works focused on maximizing the electro-optic bandwidth of the transmitter (BW_{EO}) or on increasing the modulation efficiency by lowering down the V_π of the modulator to make it more compatible with small-swing CMOS drivers.

Next-generation coherent optical transceivers towards 400 Gb/s and beyond are under active research and development. For a given baud rate (usually limited by the driver swing or BW_{EO}), applying higher-order modulation is an effective way to increase the bit rates. Higher order modulation (i.e. 2^N-QAM, where N is the number of bits per symbol), is very sensitive to optical signal to noise ratio. Supposing noise contribution in OSNR is constant in the transmitter, the amplitude of modulated signal determines the quality of output signal.

When it comes to design of a modulator, minimizing the power penalty induced by the modulator is a crucial factor in order to maximize its system-level performance. In [32], authors tried to maximize the optical modulation amplitude in multi-level pulse amplitude modulation transmitter. This system-orientated approach accesses the power-penalty induced by the modulator in a transmission link, guiding the optimization of the modulator to increase the sub-eye opening in a multi-level modulation format; hence better bit error rate performance can be expected.

Three main limiting factors that could potentially affect the output of the modulator and limit the OSNR are optical loss, modulation loss (that comes from the limited extinction ratio due to high V_π), and inter-symbol interference induced by the limited electro-optic bandwidth of modulator. These three penalty sources are intricately intertwined. Minimizing each of them separately does not necessarily minimize the overall penalty introduced by the modulator.

In this chapter, we demonstrate an integrated in-phase and quadrature modulator using depletion-mode silicon phase shifters based on a 220-nm SiP foundry process. We propose a new approach to optimizing design and operation of a SiP IQ modulator through accessing and minimizing its power penalty for QAM transmission. For the given process, an unit-length design of Mach-Zehnder modulator can be optimized following the process specifications and

design rules.

However, the length and the bias voltage of the phase shifter must be optimized together in a system context (e.g., baud rate and modulation format). We target 16-QAM at 60 Gbaud for beyond 200 Gb/s per channel in single polarization. To verify the proposed optimization approach in experiment, we isolate the imperfection from the SiP modulator from other transmitter impairments, e.g., from the digital to analogue converter, and do not pre-compensate for the limited bandwidth of the modulator. We further push the baud rate up to 70 Gbaud to examine the capacity boundary of the device.

The rest of this chapter is organized as follows. In section 4.2, we present a general, unit-length MZM design and its optical and electrical characteristics. Section 4.3 optimizes the IQ modulator design. We examine power penalties induced by a SiP IQ modulator in a QAM transmission link; using the optical and electrical characteristics extracted in Section 4.2, we identify the optimal combination of length and bias voltage of the phase shifter, which gives the minimum total power penalty induced by the modulator. Electromagnetic simulation is also performed to avoid RF crosstalk between the I and Q branches. In section 4.4, our experiment setup and measured results are presented. Finally, Section 4.5 concludes this chapter.

4.2 Design and Characterization of TW-MZM

Figure 4.1 presents a schematic of the SiP IQ modulator that consists of a pair of MZMs nested in an MZ interferometer. Each MZM uses a phase shifter employing lateral pn junction and a traveling-wave electrode for high-frequency operation. The TW-MZM is driven in a series push-pull configuration. A negative voltage is applied between the two arms of each MZM; thus, the phase shifter works in the depletion mode.

4.2.1 TW-MZM Design

The cross-sectional schematic of the SiP TW-MZM (the same for I and Q) using a CMOS-compatible process (A∗STAR's IME, Singapore) on a 220-nm SOI wafer with 2 μm buried oxide is the same as the one presented in section 2.3 (see figure 2.3). The phase shifter is a lateral p-n junction embedded in the centre of a rib waveguide. While highly doped P++ and N++ regions are used for ohmic contacts, intermediate P+ and N+ doping levels are used to reduce the series resistance without significantly increasing optical propagation loss.

The phase shifter can be modeled as a series of lumped capacitors and resistors , whose values depend on the applied voltage. We reuse the 2D simulation conducted in Lumerical Mode and Device software at wavelength = 1550 nm in section 2.3 to characterize the phase shifter and to calculate the circuit components. Calculated junction capacitance (C_j) and

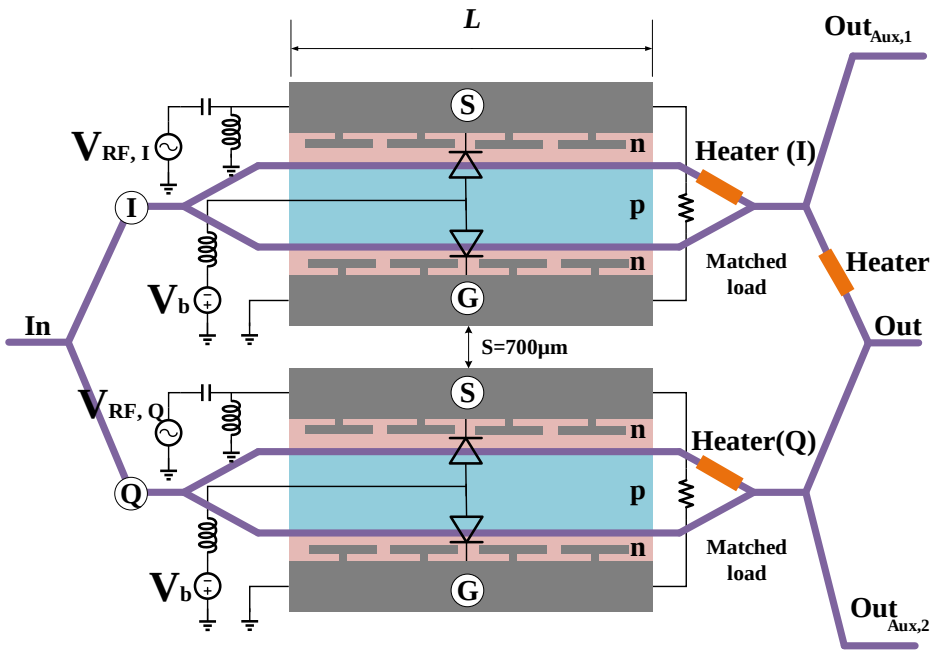


Figure 4.1 – Schematic of the IQ modulator using TW-SiP MZMs with the series push-pull driving scheme.

resistance (R_j) are presented in figure 2.4. The overlap between the optical mode and the carrier distribution is calculated to predict the changes in refractive index and loss as functions of voltage as shown in figure 2.5. More details can be found in [51].

4.2.2 TW-MZM Design

As shown in Figure 4.2a, the TW electrode has a coplanar stripline (CPS) configuration loaded by the pn-junction. For velocity matching between optical waves and RF driving signals, the RF effective index of the loaded CPS waveguide ($n_{RF,L}$) should be as close as possible to the group index of the optical mode ($n_{o,g}$). This can be achieved employing a slow-wave design with intentionally added metal capacitance to the transmission line to slow down the RF signal.

A "T" shaped extension for the metal capacitance has been added to the CPS transmission line to improve the velocity matching while maintaining a 50 Ω impedance. Detailed design procedures for slow-wave CPS transmission lines has been reported recently [26]. The bandwidth of the MZM is eventually dominated by the RF propagation loss in the pn-junction loaded CPS [51]. The TW electrode is terminated by an on-chip 50 Ω load implemented using N doped silicon.

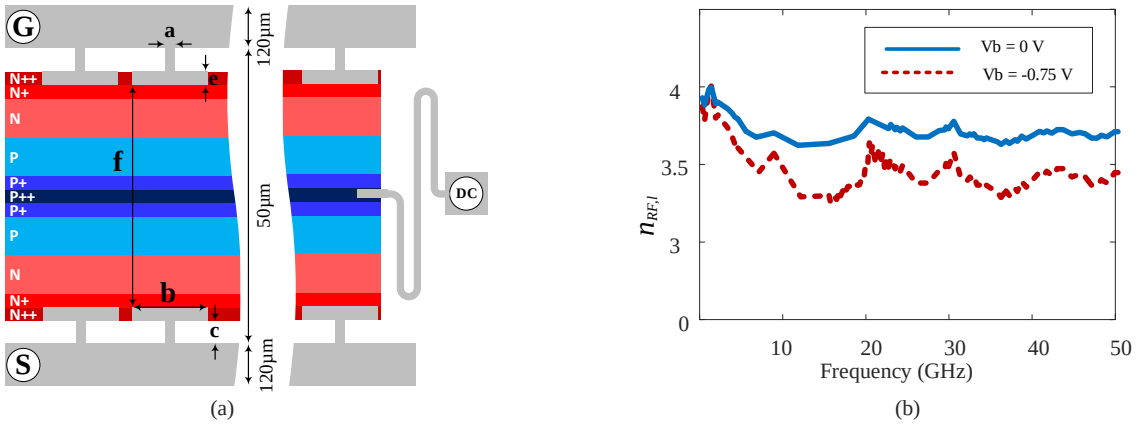


Figure 4.2 – a) Traveling wave electrode employing "T" shape extensions to increase the microwave effective index; a=2μm, b=47μm, c=9μm, e=10μm, f=12.5μm. b) Measurement results for Microwave effective index of the TW electrode when it is loaded by a pn doped silicon wave-guide.

4.2.3 RF characteristics

Small-signal frequency responses of a TW-MZM were measured using a 67 GHz Keysight network analyzer. After removing the effects of the RF probes, cables and unloaded section of the transmission line, we extracted the important RF parameters such as prorogation loss, effective index, and transmission impedance. Figure 4.2b presents the microwave effective index as a function of frequency. We can see that it changes from 3.65 to 3.5 at 30 GHz as the bias voltage V_b changes from zero to -0.75 V.

Despite this variation, it is very close to the optical group index of the silicon waveguide that is 3.89 according to our simulation. Microwave loss per unit length is presented in figure 4.3a that presents a quadratic dependency on frequency resulting in larger values at higher frequencies (e.g., about 3 dB/mm and 2.2 dB/mm for zero bias and -0.75 V, respectively). Figure 4.3b shows the characteristic impedance of the loaded transmission line. Good 50 Ω impedance matching has been achieved for up to 30 GHz. Due to variation in the capacitive load of the transmission line, fluctuation in the characteristic impedance around desired 50 Ω increases at higher frequencies.

4.3 Optimization for QAM

To generate 16-QAM, the driving voltages $V_{RF,I}$ and $V_{RF,Q}$ feed two uncorrelated four-levels signals to the I and Q branches as shown in figure 4.1 On-chip heaters are used to implement the 90 degree phase shift between the two branches. The electric field (E) of the output optical signal will be detected to extract the transmitted data. The TW-MZMs in I and Q branches are operated at their null point for maximized modulation amplitude of the E field.

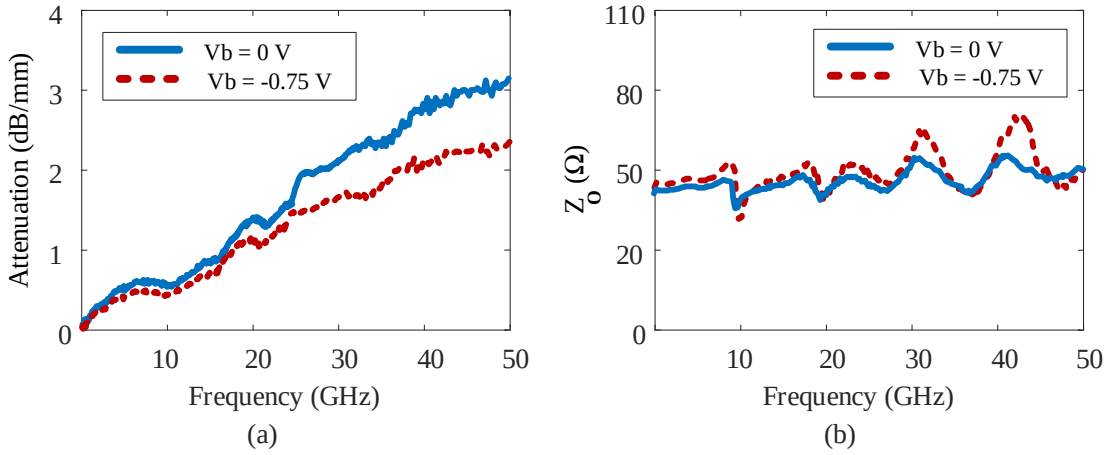


Figure 4.3 – a) Measurement results for microwave attenuation along the TW electrode, b) Characteristic impedance of the TW electrode loaded by pn junction.

This is achieved by adjusting the phase shift between the two arms of each MZM trough on-chip heaters (Heater (I) and Heater (Q) in figure 4.1).

There are three major sources of power penalty in SiP modulators: limited dynamic extinction ratio of the output E field due to limited swing of the driving voltage compared to the high V_π of the modulator (called modulation loss), optical loss of the phase shifter and limited bandwidth of the modulator. All of these impairments degrade the eye opening at the output of modulator, which leads to lower margin for detection hence, higher bit error rate. The effects of these impairments are illustrated in Fig. 4a, where we consider a four-level signal in one branch (I or Q).

In figure 4.4 , *h1*, *h2*, and *h3* present height of the outer eye opening after considering the effect of optical loss, modulation loss and inter symbol interference introduced by the limited bandwidth of the TW-MZM, respectively. ISI is often the ultimate limit to achievable bit rate in high performance systems. This figure gives an illustration of a typical four-level eye diagram where the eye is noiseless. Eye closing in *h3* is strictly due to the finite rise and fall times. In other words, if the modulator had infinite bandwidth, the eye would be rectangular with eye opening equal to the distance between rails, as indicated on the inset. Using the E field equation of a TW-SiP MZM employing single-drive series push-pull driving scheme, normalized output of the IQ modulator can be expressed as:

$$E_{out} = e^{-\alpha L/2}\left(\underbrace{E_0 \cos\left(\frac{\Delta\phi\left(V_{RF,I}\right)}{2}+\frac{\pi}{2}\right)}_{E_I} + i\underbrace{E_0 \cos\left(\frac{\Delta\phi\left(V_{RF,Q}\right)}{2}+\frac{\pi}{2}\right)}_{E_Q}\right) \tag{4.1}$$

where $E_0 = E_{in}/\sqrt{2}$ is the absolute value of the electric filed in I and Q branches, respectively,

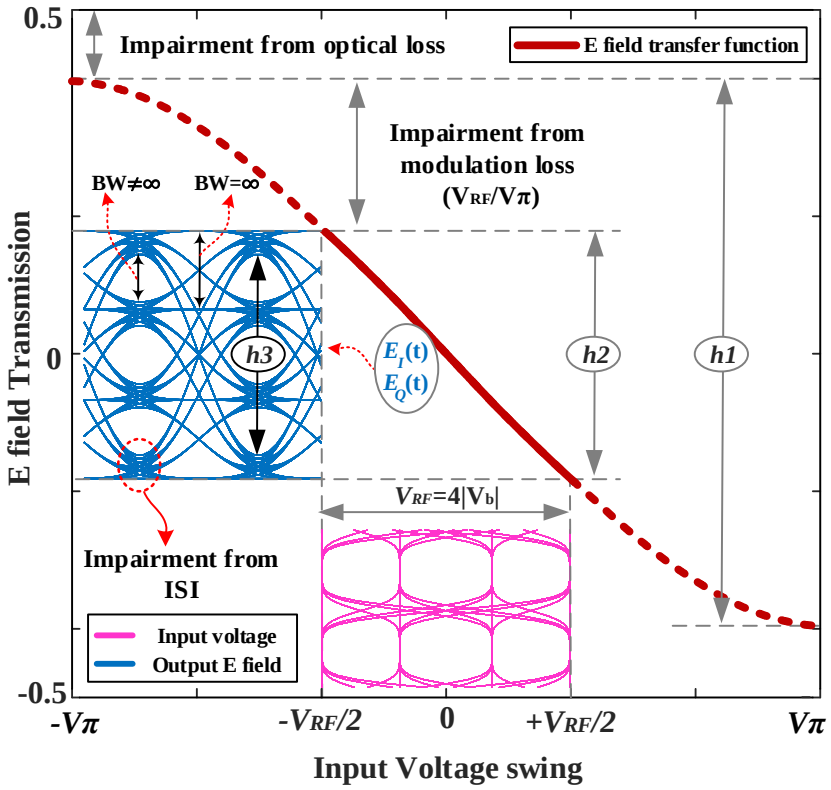


Figure 4.4 – a) Transfer function of the TW-SiP MZM in one branch (I or Q) operating at the null point. The insets show the noiseless eye diagrams of four-level modulation of Gaussian shaped pulses with $BW_{EO}/\mathrm{BR} = 30/20$.

and:

$$\Delta\phi\left(V_{RF}\right) = \left(\Delta n_{eff}\left(V_b + \frac{V_{RF}}{2}\right) - \Delta n_{eff}\left(V_b - \frac{V_{RF}}{2}\right)\right)\frac{2\pi L}{\lambda} \tag{4.2}$$

We adopt some simplifying assumptions to predict the effects of impairments at the output constellation diagram. We assume there is no loss imbalance between I and Q branches and the phase difference between I and Q branch is always set at $\pi/2$. This assumption ignores any phases drift between I and Q data. Another simplifying assumption is that ISI is dominated by contributions from the two nearest neighbours; contributions from more distant symbols are neglected.

Parameters extracted trough simulation in HFSS (small signal performance of the TW electrode), Lumerical Mode and Device (for the silicon wave guide) are used in Lumerical Interconnect to develop a model for the TW-SiP IQ modulator. This model is called by Matlab to run a back-back data transmission. Figure 4.5 shows the constellation diagram of

an IQ modulator using 4.5 mm phase shifter in each of the TW-SiP MZMs in I and Q branches. From figure 4.4 and figure 4.5, we can observe how each of the impairments in TW-SiP MZM can affect the output constellation diagram and make the constellation points closer to each other. When it comes to minimizing the penalty induced by each of those impairments, there is a trade-off. These three penalty sources can be affected by each other. Minimizing each of them separately does not minimize the total power penalty of the transmitter. For example,

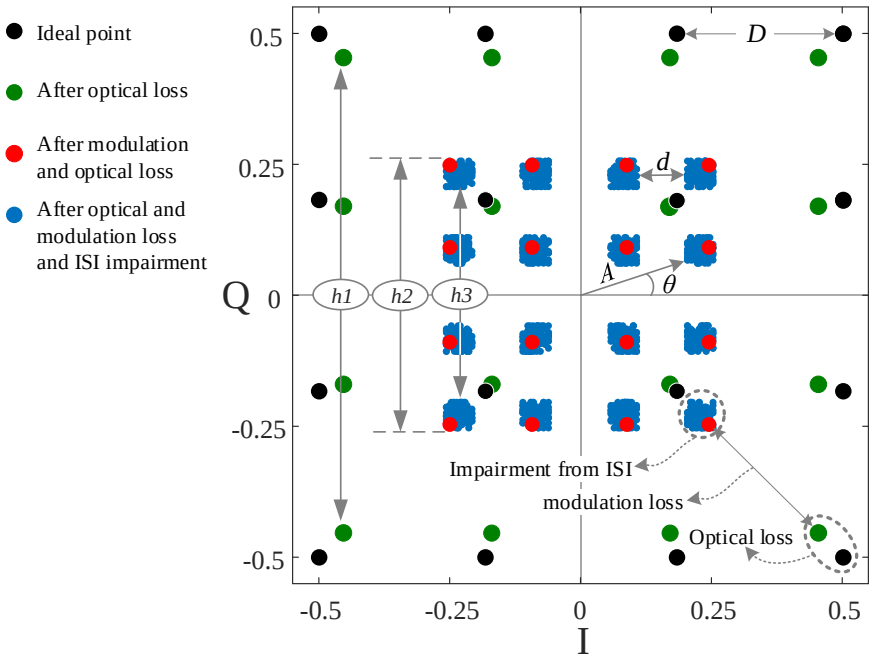


Figure 4.5 – Constellation diagram of output data for 16-QAM. Black dots present the ideal constellation points when there is no impairment from the modulator. Green, red and blue dots present the constellation points when the optical loss, optical loss plus modulation loss and when all the impairment sources are included in the simulation, respectively. V_{RF}=2 $|V_b|$= 2V, Br = 60 Gb/s, $BW_{EO} \sim$ 20GHz, $V_\pi \sim$ 6.4 V, L = 4.5 mm.

for a fixed swing of the driving voltage (V_{RF}), decreasing the modulator length decreases the optical loss and increases the electro-optic bandwidth, but increases modulation loss (as a result of increased V_π and lower extinction ratio of the modulator) and limits the output eye opening.

On the other hand, using a longer phase shifter reduces BW_{EO} of the modulator and increases the total optical loss ($\alpha.L$). Hence, the total penalty from the transmitter has to be minimized by simultaneously considering all of the penalty sources.

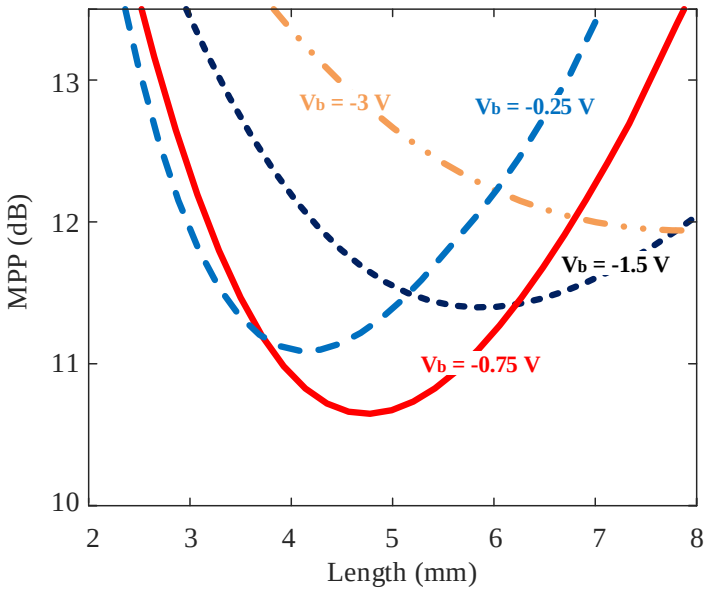


Figure 4.6 – Modulator power penalty as expressed in (4.4) for 16-QAM at 60 Gbaud. The MPP is minimized when the phase shifter length is between 4.5mm to 5mm and is biased at V_b= -0.75 V.

4.3.1 Modulator power penalty in QAM constellation

In the output from an IQ transmitter, separation of the nearest constellation points (d in figure 4.5) is the main parameter to evaluate the performance of the transmitter (assuming no impairment in the receiver and local oscillator). These constellation points are defined by the absolute value (A) and phase (θ) of the detected in-phase and quadrature-phase electric fields that carry the data.

$$A = \sqrt{E_I^2 + E_Q^2} \qquad \textit{and} \qquad \theta = \tan^{-1}\left(\frac{E_Q}{E_I}\right) \tag{4.3}$$

In order to find the optimal length of the phase shifter, we define the modulator power penalty as the ratio of the limited clear distance (d) to the ideal value (D), which is proportional to those impairments noted in figure 4.5:

$$MPP = -10\log_{10}\left(\frac{d}{D}\right) \propto (P_{\alpha L} + P_{ER} + P_{ISI}) \tag{4.4}$$

where $P_{\alpha L}$, P_{ER}, P_{ISI} present power penalty from the optical loss, modulation loss and limited BW of the modulator, respectively as presented in [72]. The output from the IQ modulator is a coherent combination of the two MZMs. As a result, the d is also affected by the impairments that limit the sub-eye opening in each MZM as shown in figure 4.4.

In figure 4.6, for a 16-QAM at 60 Gbaud, we sweep the phase shifter length and plot the modulator penalty from (4.4) for several reverse bias voltages while the RF voltage swing is set to be $V_{RF} = 2\ V_{p-p}$ (limited by the maximum achievable swing by instruments available in

our lab). We examine multiple values of bias voltage as it determines the relative importance of each penalty source contribution to MPP in(4.4). $P_{\alpha L}$, P_{ER}, P_{ISI} are calculated from a numerical model for TW-MZM developed in Lumerical software.

When lower reverse bias voltage is used, the optimal length (L_{opt}) is relatively shorter due to bandwidth requirement. Conversely, for a higher reverse bias, a longer phase shifter presents lower penalty. This is because a higher bandwidth is available as reverse bias voltage increases, which compensates for the reduction in bandwidth due to the longer phase shifter.

Figure 4.6 also shows that for various bias voltages, there exists an optical combination of the phase-shifter length and the bias voltage, which gives the lowest MPP. In this case, the MPP curve of V_b = -0.75V presents the overall minimum point near 5.75 mm with little change in the range from 4.4 mm to 5 mm. Based on this result, we choose a 4.5-mm-long phase shifter in our IQ modulator design and bias it at V_b = -0.75 V in experiment.

4.3.2 RF crosstalk between I and Q branches

Due to the weak electro-optic effect in silicon, all-silicon TW-MZMs usually have several millimetres in length (4.5 mm in this case). Placing such long TW electrode too close to each other may excite unwanted RF modes and affect the overall performance of the IQ transmitter. Specifically, when two CPS transmission lines are too close to each other, the signal and ground of one CPS and the ground of the other CPS form an asymmetric coplanar waveguide (CPW). This causes excess RF loss and crosstalk.

In order to avoid this unwanted phenomenon, the two MZMs need to be placed far enough from each other. Using the RF characteristics extracted in section 4.2, a 4-port electromagnetic simulation of two 4.5-mm-long CPS transmission lines is performed in HFSS. A distance of 700 μm is found to be a safe design where the crosstalk between two adjacent CPS transmission lines is less than -30 dB in the entire simulation frequency range up to 45 GHz.

4.4 Experimental results

Figure 4.7 sis a photograph of the fabricated SiP IQ modulator in the test configuration. A RF probe with GSSG pin configuration is used to the drive the modulator and a DC probe controls the bias voltage and thermal phase shifters. We use a fiber array for optical IO through surface grating couplers. Each of the TW-MZMs (in I and Q branches) is characterized individually through the auxiliary optical outputs (Out_{Aux1}, Out_{Aux2} in figure 4.1).

We measured the small signal responses of the MZMs. The Q branch shows slightly better small signal performance than the I branch due to fabrication errors. We present results for the I branch. Figure 4.8a presents the S_{11} at various bias voltage. We can see that even in the

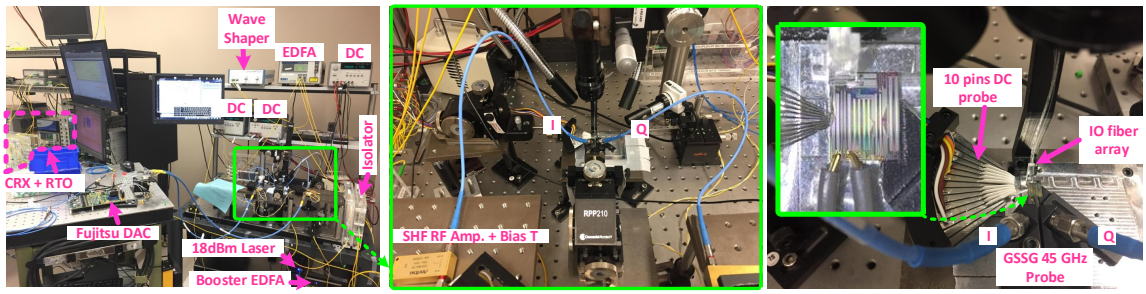


Figure 4.7 – Photograph of the fabricated TW-SiP IQ modulator and the measurement setup in Lab.

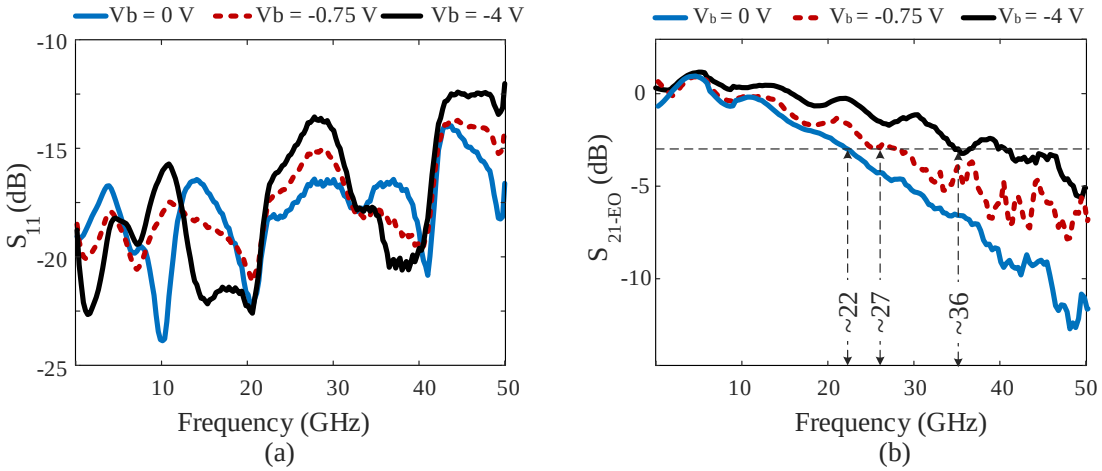


Figure 4.8 – Small signal electro-optic performance of the TW-MZM employing 4.5 mm phase shifter normalized at 1.5 GHz. a) S_{11} parameter of the MZM in the I branch. b) Electro-optic performance of the modulator in the I branch.

worst case (V_b = -4 V) the reflection is still well under -12.5 dB. The modulation bandwidth (S_{21}) is measured to be 36 GHz at V_b = -4 V (figure 4.8b) and decreases to 27 GHz for V_b = -0.75 V. The average static V_π at V_b = -0.75 V is 7.3 V ($V_{\pi(I)}$ = 7.8 V, $V_{\pi(Q)}$ = 6.9 V). On-chip insertion loss of the IQ modulator is measured to be 6.8 dB. The coupling loss from the fiber array to the SiP chip is 8.5 dB.

4.4.1 Data transmission setup

Following characterization, we ran data transmission experiments using the experimental setup in figure 4.9. We use an EDFA to boost a continuous wave carrier at 1530 nm from an external cavity laser (ECL) to 22 dBm before coupling onto the chip. We use on-chip heaters to implement the 90 degree phase shift between the two branches. The TW-MZMs in the I and the Q branches are operated at their null point to maximize the modulation amplitude of

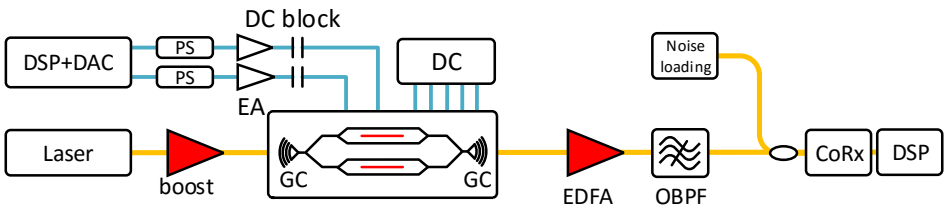


Figure 4.9 – Experimental setup. PS: phase shifter; DC: direct current; GC: grating coupler: OBPF: Optical band-pass filter.

the E field. We achieve this by adjusting the phase shift between the two arms of each MZM through on-chip heaters, Heater (I) and Heater (Q) in figure 4.1.

To generate 16-QAM, the driving voltages $V_{RF,I}$ and $V_{RF,Q}$ feed two uncorrelated four-level signals to the I and Q branches as shown in figure 4.1. We amplify two outputs of an 84 GSa/s, 8 bit DAC with two SHF 50 GHz, 18 dBm drivers and apply the signal to the modulator using an RF probe. In the transmitter digital signal processing (DSP) before uploading to the DAC, the QAM data is grey mapped from a pseudo random bit sequence (PRBS) of order 19. We apply a pre-emphasis filter to compensate the DAC, RF amplifier and RF probe frequency response. This allows us to investigate the impairment from the modulator. The pre-emphasized symbols are further pulse shaped by a raised cosine filter with roll-off filter of 0.01. RF phase shifters are used to precisely de-skew the I and Q channels. We control the optical operation point of each MZM using the DC probed heaters. We amplify the modulated optical signal with a two-stage EDFA. We place an optical band-pass filter (OBPF after the second EDFA to reject out-of-band amplified spontaneous emission (ASE) noise. To sweep OSNR, we load the signal with ASE noise at the receiver end. The output optical signal is mixed with a 14 dBm local oscillator (LO) and fed to a 70 GHz coherent receiver (CoRx) formed by a discreet optical hybrid and 70 GHz balanced photodetectors. We use a Keysight real-time oscilloscope (RTO) with a 60 GHz analog bandwidth to sample the output of the CoRx at 160 GSa/s.

4.4.2 Experimental characterization for MMP

In order to verify our design methodology and the numerical model, we experimentally characterize the MMPs of the IQ modulator at various bias voltages and compare them with simulation results. Imperfection from optical loss is applied by applying the measured optical loss of the modulator versus applied reverse bias voltage. To estimate the $P_{\alpha L}$, V_{π} at different reverse bias voltages are measured; the modulation loss is then calculated for a driving voltage of 2 V_{pp}. The experimental characterization for P_{ISI} requires a more complex procedure that is described as follows.

To quantify the penalty from the bandwidth limitation of the modulator (P_{ISI}), a training-aided channel estimation method is employed. We load the DAC with a Nyquist-

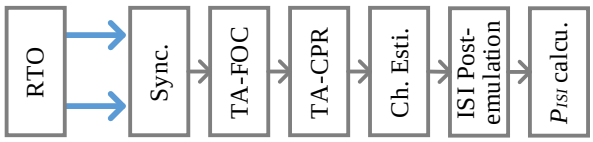


Figure 4.10 – Flow chart of training aided channel estimation.

16QAM training sequence with a roll-off factor of 0.01, where the frequency responses of the DAC, the RTO and other RF components (such as drivers and RF cables) have been digitally pre-compensated, ensuing a flat spectrum in the driving signal of the modulator. The ISI penalty of the modulator is then estimated following the signal-processing flow as shown in 4.10. The data samples are first synchronized and framed according to the training sequence. After the training-aided frequency offset compensation (TA-FOC) and the training-aided carrier phase recovery (TA-CPR), the channel response is estimated by the minimum mean square error (MMSE) calculation and is averaged over 100 frames to minimize the impact from noise and numerical errors. Since no adaptive equalizer is applied and the frequency responses of other RF components have been de-embedded through the pre-compensation of the training sequence, the obtained MMSE channel response represents the response of the modulator alone.

Using the estimated channel response, we run a post-emulation to visualize the ISI by the convolution of the averaged channel response with an ideal 16QAM signal. Note that the modulator stays in the linear regime for the given voltage swing, thus nonlinear modulation distortion is negligible in this case. Due to the relatively narrow analog bandwidth ($<$ 20 GHz at -3 dB) of the DAC, the accuracy of the ISI emulation degrades drastically at a higher frequency. Therefore, we have only characterized P_{ISI} for up to 30 Gbaud for the purpose of verification.

Finally, the total MPPs of the modulator under test at different bias voltages are calculated using equation 4.4 for 20 Gbaud and 30 Gbaud. The results are shown in figure 4.11 . For the lower baud rate (i.e., 20 Gbaud), the electro-optic bandwidth of the modulator is large enough even at zero bias (22 GHz in figure 4.8.b) with little ISI penalty. In this case, the total MPP increases as the reverse bias voltage due to the higher V_π and thus higher modulation loss. However, for the higher baud rate (i.e., 30 Gbaud), PISI becomes dominant over the modulation loss ($P_{\alpha L}$) at zero bias. Increasing the reverse bias to 0.75 V achieves the minimum MPP thanks to the best trade-off between the bandwidth (27 GHz in figure 4.8.b) and the modulation loss as discussed in the previous section.

As shown in figure 4.11, the simulation results match very well with the measured MPPs. Although the MPP can only be accurately measured at a relatively low baud rate due to the narrow bandwidth of the DAC used in our experiment, the same physics should work at higher baud rates. Hence, we expect that the simulation results shown in figure 4.6 also present the

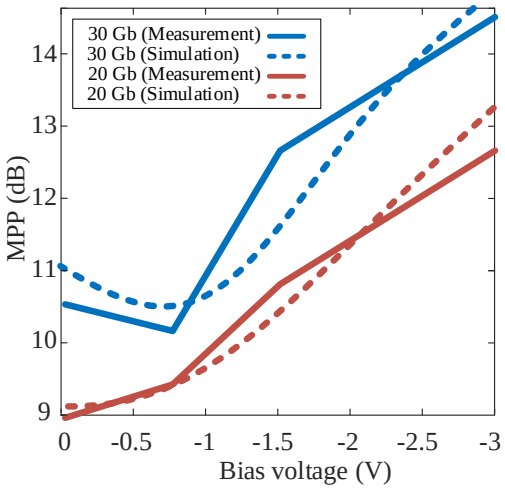


Figure 4.11 – Simulation and measurement results for MPP versus reverse bias voltage for two different baud rates.

optimum modulator design for 60-Gbaud 16 QAM modulation. In continue we will present data transmission results to evaluate the system-level performance of the designed modulator.

4.4.3 BER performance

Experiments are run at 60 Gbaud (240 Gb/s) for three different bias voltages. The BER performance of 16-QAM with an RF voltage swings across 2 V peak-to-peak is shown in figure 4.12. Two forward error correction (FEC) thresholds are indicated: a 7% overhead FEC threshold at BER = 3.8×10^{-3}, and a 20% overhead FEC threshold at BER = 2.4×10^{-2}.

In figure 4.12, we observe that increasing the bias voltage from Vb = 0.25 V (where the diodes are slightly forward biased but there is still no current passing trough diodes) to 0.75 V significantly improves the BER performance of the modulator. In this case, the bandwidth achieved from stronger reverse bias of the phase shifter compensates the modulation loss penalty due to higher V_π at Vb = 0.75 V. The MPP simulation predicted this behaviour, as shown in figure 4.6. Lower MPP (figure 4.6) indicates a larger clear distance between the constellation points, leading to better BER performance. Pushing the phase shifter to stronger reverse bias does not improve the BER performance due to a lower efficiency. For example, Vb = 3 V shows the worst BER of all the three curves in figure 4.12 despite the highest bandwidth.

We further investigate the achievable baud rate of the modulator. Figure 4.13 shows the BER at 40, 60 and 70 Gbaud when the reverse bias voltage is Vb = 0.75 V and the RF voltage swings across 2V peak-to-peak. A large margin is available at 40 Gbaud. The BER performance is below the 20% FEC threshold up to 70 Gbaud (net bit rate of 224 Gb/s). A

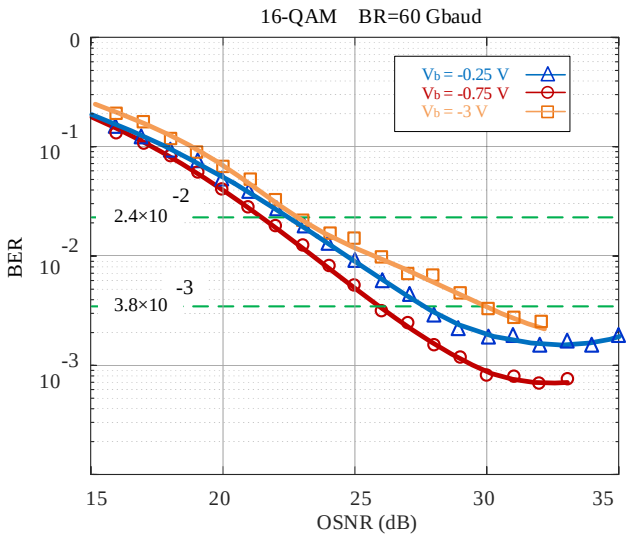


Figure 4.12 – BER performance for different reverse bias voltages at 60 Gbaud.

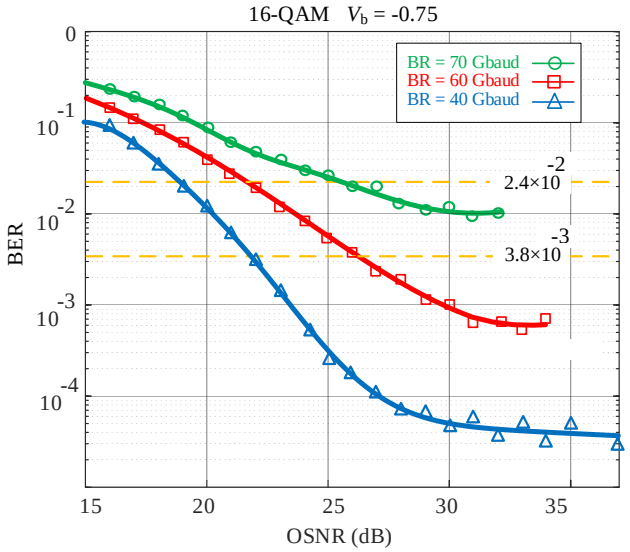


Figure 4.13 – BER performance for different baud rates at V_b = -0.75V.

400 Gb/s dual-polarization transmitter can be achieved by integrating on the same chip two IQ modulators, a polarization rotator (from TE to TM) and a polarization combiner.

4.5 Conclusion

We have experimentally demonstrated an integrated IQ modulator based on a SiP foundry process. Our results show that all-silicon modulators have great potential for high-baud-rate coherent optical communications systems. We demonstrated that the performance of the SiP IQ modulator can be effectively optimized by minimizing the modulation-induced power penalty in an optical transmission link. The design and operation of the TW-MZMs were optimized for 16-QAM at 60 Gbaud. The experimental results verified our theoretical prediction. This system-orientated optimization methodology can also be used in other contexts with various modulation formats and rates. Using the SiP IQ modulator, we have achieved single-polarization 16-QAM at 60 Gbaud (BER at the 7% FEC threshold) and at 70 Gbaud (BER below the 20% FEC threshold), giving a net data rate of 224 Gb/s and 233 Gb/s, respectively. This indicates a promising solution for 400^{+} Gb/s dual-polarization transmitter. Note that these results were achieved without pre-compensating for the impairments from the modulator. More sophisticated digital or optical pre-emphasise could be done to overcome the limitations of the modulator and further push the bit rate.

Chapter 5

Conclusion and future works

In this thesis our first contribution was to demonstrate an integrated, DAC-less, PAM-4 optical transmitter using a commercially available Silicon Photonics platform. This transmitter includes a three-segments lumped element segmented Silicon Photonics Mach-Zehnder modulator and its co-design CMOS driver. To the best of our knowledge, it was the first demonstration of a DAC-less PAM-4 SiP transmitter using a generic silicon photonic process with lateral pn junction. Most of reported DAC-less multi-level transmitters use either monolithic process, or vertical pn junctions, which are not widely available. Our results are achieved using commercially available CMOS and SiP processes, showing the efficacy of CMOS-SiP co-design and integration for low-power, high-speed multi-level transmitters. A novel delay management for robustness to fabrication errors is developed and effect of delay errors on output of the transmitter has investigated. Based on EVM at 20 Gb/s (where the driver power-consumption drops to 290 mW), error free operation is expected at this bitrate. Despite the higher unit-bit power consumption (14.5 pJ/bit at 20 Gb/s), lower baud rates eliminate the burden of digital signal processing on the receiver side. We further pushed the baud rate and by employing post-compensation, bit rates up to 38 Gb/s with error rate below 3.7×10^{-3} was achieved that indicates power consumption of 9.8 pJ/bit.

In our second contribution, we studied the Performance of Silicon Photonic Modulators for pulse amplitude modulation in an optical link. We introduced a comprehensive equation for the system-level power-penalty of a SiP PAM-M modulator, including optical loss, modulation loss and limited electro-optic bandwidth. We have shown trough simulation that Current figures of merit for SiP modulators cannot predict the system-level performance of optical links, as they do not include a critical system impairment: inter-symbol interference. We proved through simulations that normalized optical modulation amplitude is a reliable tool to predict the minimal MPP point. Finally, for the first time, we introduced a new figure of merit that includes not only the efficiency of the modulator, but also the bandwidth limitation from SiP electro-optic modulator. The new FOM that is derived from normalized optical modulation amplitude translates the system-level requirements of a PAM-M optical link to the

device-level design parameters. We also investigate the effect of variation in process. Extensive simulations confirms that the new FOM not only can be used to predict the optimum phase-shifter length, bias voltage or driving signal in a specific process, but also to select the optimum doping concentration to minimize the SiP TW-MZM MPP for a given system context.

In our third contribution, for the first time we developed a novel design technique to minimize MPP for a CMOS-compatible SiP in-phase Quadrature modulator for various modulation formats and baud rates. We designed and characterized the first reported ultra-high-capacity IQ modulator using lateral pn junction SiP traveling wave MZM. The design and operation of the TW-MZMs were optimized for 16-QAM at 60 Gbaud by our proposed design methodology. Our theoretical prediction in optimization of the modulator was verified by the measurement results. Using this device, we have achieved single-polarization 16-QAM at 60 Gbaud (BER below the 7% FEC threshold) and at 70 Gbaud (BER below the 20% FEC threshold), giving a net data rate of 224 Gb/s and 233 Gb/s, respectively. This indicates a promising solution for the next generation of 400 Gb/s dual-polarization SiP transmitters.

For the future, there are different directions and aspects of SiP modulators that could be studied. Here, we briefly review them:

I. We successfully demonstrated co-design of a CMOS-SiP transmitter for PAM-4 modulation, this design could be expanded to implement an CMOS-SiP multi-segment IQ transmitter (employing high-order modulation format such as 16-QAM, 256-QAM) without need for an electrical DAC. Other optical modulator structures (i.e. segmented micro ring, segmented slow-light modulators, ...) could also be used to implement very low power (in the range of few fJ/b) and compact DAC-less transmitter.

II. As it is shown in this thesis, prior FOMs are not reliable tools to compare different modulators designs nor to predict performance of the SiP modulators in an optical link. The new FOM presented in this thesis targets SiP MZM for PAM-M modulation. Our approach to define the new FOM can be expanded for other modulator (i.e. micro ring modulators) and modulation formats (i.e. M-QAM). Hence, different modulators could be optimized for different modulation format and system level criteria. In addition, experimental validation of the new FOM proposed in the second chapter could be done. It could be investigated by comparing the performance of SiP modulators with several different design parameters on same wafer in a specific SiP process or by comparing the performance of same SiP modulator design implemented in different SiP process.

III. In our new system-orientated design methodology for IQ modulators, numerical simulation method is used to predict the optimal phase shifter length and bias voltage. An analytical method could be applied to develop an equation for MPP of the IQ modulator for QAM modulation. This equation should include all the penalty sources (optical loss, modulation loss and ISI).

IV. In this thesis, we have developed a single polarization IQ modulators using our proposed design methodology. It could be used to developing a dual polarization IQ transmitter, which could potentially double the channel capacity and pave the way for 400+ Gb/s/ch optical links. To further increasing the capacity of the SiP transmitters, an on chip COMB generator (to implement a WDM system) beside polarization multiplexing, can increase the capacity of SiP transmitter to more than several Tb/s and even Pb/s.

V. As the number of RF and DC inputs increases from a single TW-MZM to and IQ modulator, RF packaging reveals its importance. RF signal carrier with minimum crosstalk between RF signal paths has to be developed to be able to practically use the dual polarization IQ modulators.

VI. Optical DACs are already implemented using segmented SiP modulators. Developing optical ADCs could be a very interesting topic. As monolithic processes that include both optic and electronic devices are available these days, developing optical ADCs could be a big improvement in the design of electrical-optical-electrical links used in die to die or board to board data transmissions.

Appendix A

Appendix

A.1 E-O bandwidth: estimation

The electro-optic 3-dB frequency, BW_{EO}, of a TW-MZM modulator can be estimated based on the principles of an MZI. We assume that there is no velocity mismatch, but rather a microwave loss that is estimated by $\alpha_m(f) = \alpha_0\sqrt{f}$, where α_0 is the low frequency microwave power attenuation coefficient, in per cm, and f is the frequency. For a voltage $V_A.e^{-\alpha_m(f)z/2}$ injected at the input of the electrode, it propagates as along the traveling wave electrode (z-axis). The optical phase shift at the end of the phase shifter can be expressed as:

$$\Delta\phi(f) \propto \frac{\partial \Delta n_{eff}}{\partial V}|_{V_A}.V_A \int_0^L e^{-\frac{z\alpha_0\sqrt{f}}{2}} dz \tag{A.1}$$

where L is the TW electrode length in cm and α_0 is in dB/cm. The 3-dB phase shift, $\Delta\phi_f$, relative to the phase shift at a nominal low frequency signal (typically 1 or 2 GHz) can be estimated via:

$$\sqrt{\frac{1}{2}} = \frac{\Delta\phi(BW_{EO})}{\Delta\phi(f_{ref})} \frac{\int_0^L e^{-\frac{z\alpha_0\sqrt{BW_{EO}}}{2}} dz}{\int_0^L e^{-\frac{z\alpha_0\sqrt{f_{ref}}}{2}} dz} \tag{A.2}$$

where BW_{EO} is the 3-dB bandwidth.

A.2 ISI effect with Gaussian response

As mentioned in section IIB, limited electro-optic bandwidth induces ISI. To facilitate calculations, we assume the pulse shape is Gaussian, the output of a filter with impulse response:

$$h(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{t^2}{2\sigma^2}} \tag{A.3}$$

As the Fourier transform of a Gaussian is also Gaussian, the transfer function of this filter is also Gaussian. The 3 dB bandwidth of the filter determines the parameter σ. Fig. 4 illustrates

the eye diagram of the output of such a filter for a typical case - a ratio of 0.9 of bandwidth (BW_{EO}) to baud rate (BR). The input is a sequence of rectangular pulses spaced at T = 1/BR seconds. We can see there are M-1 eyes, each diminished by a somewhat different value of intersymbol interference. Our goal is to determine a simple expression for the decrease in eye opening due to a limited bandwidth filter.

We use the approximations suggested in [15]. We neglect ISI from distant pulses, and consider only the contribution for the time adjacent input rectangular pulses. We find the worst case (top of upper-most eye), Δ_{ISI}, calculated for this simple case. With no bandwidth constraint, a middle eye would have opening of 1/(M-1). We assume the worst case ISI level is present at each symbol transition. This leads to an average ISI level on a given eye of:

$$\frac{M}{M-1}\Delta_{ISI} = \frac{M}{M-1} efrc\left(\frac{T/2}{\sigma\sqrt{2}}\right) \tag{A.4}$$

$$= \frac{M}{M-1} efrc\left(\frac{\pi}{2\sqrt{ln2}}\frac{BW_{EO}}{BR}\right) \tag{A.5}$$

where $erfc$ is the complementary error function (the result of the convolution of a rectangular pulse of width T with the Gaussian impulse response with variance σ). The ISI penalty can be found from the ratio of eye opening for limited bandwidth to eye opening with infinite bandwidth. Hence:

$$10log_{10}\left(\frac{\left[\frac{1}{M-1} - \frac{M}{M-1} efrc\left(\frac{\pi}{2\sqrt{ln2}}\frac{BW_{EO}}{BR}\right)\right]}{\frac{1}{M-1}}\right) \tag{A.6}$$

$$= 10log_{10}\left(1 - M.efrc\left(\frac{\pi}{2\sqrt{ln2}}\frac{BW_{EO}}{BR}\right)\right) \tag{A.7}$$

is used in our TPP to represent the ISI penalty, P_{ISI}.

A.3 FOM ISI term

The $erfc$ can be well approximated by an exponential over a limited range of the argument. The majority of optical communications systems would have BW_{EO}/BR in the range of 0.4 to 2. A larger number would be under utilizing the available bandwidth resource, while a smaller number would have too high an ISI penalty. In this range:

$$\frac{M}{M-1}.efrc\left(\frac{\pi}{2\sqrt{ln2}}\frac{BW_{EO}}{BR}\right) \approx \frac{M}{M-1} 0.506 e^{-4.34\left(\frac{BW_{EO}}{BR}\right)^2} \tag{A.8}$$

$$\approx \frac{M}{M-1}\frac{1}{2} e^{-4.34\left(\frac{BW_{EO}}{BR}\right)^2} \tag{A.9}$$

This gives a good approximation of the decrease in PAM-M eye opening due to the presence of ISI. The ISI penalty can be found from the ratio of eye opening for limited bandwidth to

eye opening with infinite bandwidth. Hence the ratio of eye opening for limited bandwidth to eye opening with infinite bandwidth is:

$$\left[\frac{1}{M-1}-\frac{M}{M-1}\frac{1}{2}e^{-4.34\left(\frac{BW_{EO}}{BR}\right)^2}\right]=1-\frac{M}{2}e^{-4.34\left(\frac{BW_{EO}}{BR}\right)^2} \tag{A.10}$$

and is used in our FOM to represent the ISI penalty.

Publication list

1 H. Sepehrian, A. Yekani, L. A. Rusch and W. Shi, "CMOS-Photonics Codesign of an Integrated DAC-Less PAM-4 Silicon Photonic Transmitter," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 12, pp. 2158-2168, Dec. 2016.

2 H. Sepehrian, A. Yekani, W. Shi and L. A. Rusch,"Assessing Performance of Silicon Photonic Modulators for Pulse Amplitude Modulation," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 24, no. 6, pp. 1-10, Nov.-Dec. 2018.

3 H. Sepehrian,J. Lin, L. Rusch and W. Shi,"Silicon Photonic IQ Modulators for 400 Gb/s and beyond," Submitted to IEEE journal of Lightwave Technologies.

4 Wei Shi, Yelong Xu, Hassan Sepehrian, Sophie LaRochelle and Leslie A Rusch,"Silicon photonic modulators for PAM transmissions" Journal of Optics, vol. 20, no. 8, p. 083002, 2018.

5 H. Bahrami, H. Sepehrian, C. S. Park, L. A. Rusch and W. Shi, "Time-Domain Large-Signal Modeling of Traveling-Wave Modulators on SOI," in Journal of Lightwave Technology, vol. 34, no. 11, pp. 2812-2823, June1, 1 2016.

6 H. Sepehrian, L. Rusch and W. Shi, "Multi-stage 20 Gbaud driver in 130 nm CMOS for segmented Mach-Zehnder optical modulators," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 201-204.

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10 J. Lin, H. Sepehrian, W. Shi and L. Rusch, "Phase drift in depletion-mode silicon photonics modulators," 2017 Conference on Lasers and Electro-Optics (CLEO), San Jose, CA, 2017, pp. 1-2.

11 J. Lin, H. Sepehrian, L. A. Rusch and W. Shi, "Flexible on-chip frequency comb generation using a SOI dual-drive MZM," 2017 IEEE Optical Interconnects Conference (OI), Santa Fe, NM, 2017, pp. 27-28.

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