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Chapter 1: Introduction

1.1 Motivation

Internet of Things (IoTs) enhance the interconnection between devices. Such devices including but not limit to wireless sensor nodes, computing and mission systems, consumer electronics, hand-held battery powered portable devices. Powering these devices can be challenging because these devices are usually powered by the batteries. Since batteries need to be recharged or replaced periodically, in such sense, it can be inconvenient or expensive. However, energy harvesting system provides a good solution to this problem. It uses ambient energy sources such as vibration, thermal, solar and RF and transfers these energies to electrical energy through different transducers. With power management circuits and systems, it collects these energies, and either be directly used or stored for the future use. Energy harvesting greatly helps to extend the battery lifecycle for those devices, or even for some low-power applications it can helps the system standalone which without using any battery [1-3].

The main challenging of energy harvesting system is to firstly extract maximum power from the source. Secondly, to design an energy-efficient power management circuit (PMC) which conditioning and deliver energy with minimal losses. With these two conditions, the maximum power to the storage or the load can be obtained. This concept can be seen in the Figure 1.1. Also, since each energy source has its own electrical characteristics after generated by the transducer such as ac, dc, frequency of interest, non-linearity and so on. The PMC system should be customized to meet the source requirement to achieve maximum power delivery.

This project is targeting to the ambient light energy, specifically, indoor light energy. The goal is to develop an energy harvesting circuit system that can effectively and efficiently transfer the energy from an PV cell or PV panel to storage element such as capacitors and batteries.
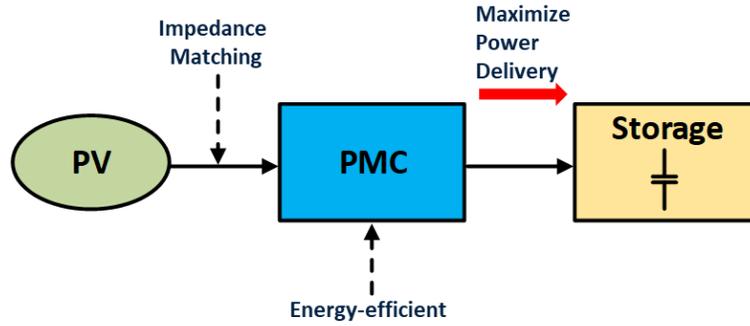
Figure 1.1 Solar energy harvesting system

1.2   Scope of the Proposed Research

Typical solar energy harvesting focuses on the outdoor ambient solar energy. The power scale is usually large, and grid connected. Also, to utilize maximum power point tracking, power-inefficient current sensor and computing unit such as DSPs and microcontrollers need to be used. The emerging vision of Internet of Things (IoTs) is pushing the connectivity to a new level. Wireless sensor node network is a very important part of IoTs. Powering these wireless sensor nodes can be difficult.

This proposed research aims indoor solar energy harvesting, especially in factories environment where the light energy is abundant. Possibly, the proposed energy harvesting circuit system can converse the solar energy to electrical energy and power wireless sensor nodes. Moreover, these wireless sensor nodes can monitor the environmental parameters such as temperature, humidity, and noise level etc. The IoTs network can be power independent, endurable or standalone.

1.3   Proposed Approach and Technical Contribution

The proposed energy harvesting system adopts dual-input dual-output non-inverting buck-boost (DIDOBB) converter as power stage and constant on-time pulse skipping modulation (COT-PSM) as main control scheme to achieve energy conversion and voltage regulation. The maximum power point tracking (MPPT) technique is utilized to extract maximum power from the PV panel continuously. The major technical contribution is this proposed MPPT method utilizes two existing methods perturb & observe (P&O) and fractional open-circuit voltage (FOCV) at different circuit operation state in a time manner and invent a new FOCV method

with an adaptive fraction approach. Taking the advantages of both methods, the proposed MPPT has high adaptability with minimal circuit and power overhead. It can apply to big variety of PV panels and still keep reasonable accuracy. Moreover, the proposed MPPT method doesn't require any current sensor to help power measuring and any computing unit such as DSP. Fully digital and customized controller is designed to achieve the desired functionality with minimal overhead.

The proposed power management circuits were designed in Cadence Virtuoso Environment and laid out in TSMC BCDMOS 180 nm process. Post-layout simulations were performed to provide the evidence for the functionality and performance of the IC post-fabrication.

1.4   Organization of this Thesis

The organization of this thesis is as follows. Chapter 2 studies the necessary background information to understand the basic solar energy transducer, PV cell and its modeling method. Then, the current existing MPPT methods are studied. The pros and cons are analyzed to have better understand the feasibility of the proposed MPPT method. Previous works will be then studied to get knowledge of current state of art. Chapter 3 discusses the proposed design by firstly introducing the operation of the power stage and how dual-input dual output is defined in different scenarios and its corresponding control scheme. Then, the proposed MPPT method will be explained in detail. Chapter 4 presents schematic and post-layout simulation results of this design in the Cadence design environment. Finally, Chapter 5 will draw the conclusions, summarized the possible improvement can be made in the future work to make the energy harvesting system more reliable and efficient.

Chapter 2: Preliminaries

To fully understand and design an energy-efficient power management system for indoor solar applications, the characteristics of the PV cell, the modeling method of the PV cell, the maximum power extracting strategies, and some previous designs are studied in this chapter to get knowledge of current state of arts.

2.1 PV Panel Characteristics and Modeling

A photovoltaic (PV) panel converts solar energy into electrical energy. The basic element to form a PV system are PV cells. PV cells can be grouped to form panels or arrays. PV system may connect directly to power lighting system or some DC-powered applications such as LED lights or phone charger etc. More complicated applications may need DC-DC converters to condition the electrical power from the PV system. These DC-DC converters may be used to regulate the voltage and current at the load and control the power flow into the load [4]. These techniques are called maximum power extraction.

In order to study the PV system along with power conditioning circuit. One firstly needs to know the characteristics of PV cells. PV cells exhibit a non-linear I-V characteristic. Such behavior is because the PV cell is basically a semiconductor diode whose PN junction is exposed to light [4]. The detailed physics of PV cells is considerably complicated and is out of the scope of this study. The major focus in this study is only considering the electrical characteristic of the
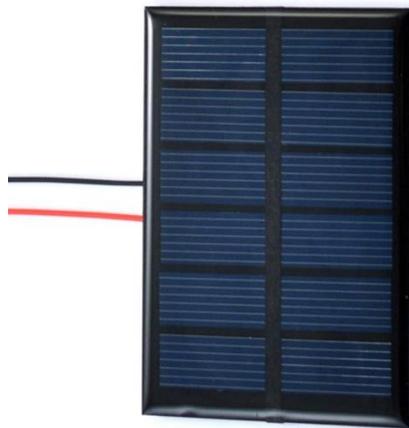
Figure 2.1 Typical commercial PV panel

two output terminals of the PV devices. The typical commercial small-scale PV panel is shown in Figure 2.1.

2.1.1 PV Non-linear IV characteristics

The IV characteristics of PV panels are different from linear circuit. The relationship between voltage and current does not exhibit linearity. Based on fundamental DC circuit theorem which states that the maximum power operation condition is located at half of the open-circuit voltage (V_{OC}) and half of the short circuit current (I_{SC}). An example of the IV characteristics of the PV panel is shown in the Figure 2.2.
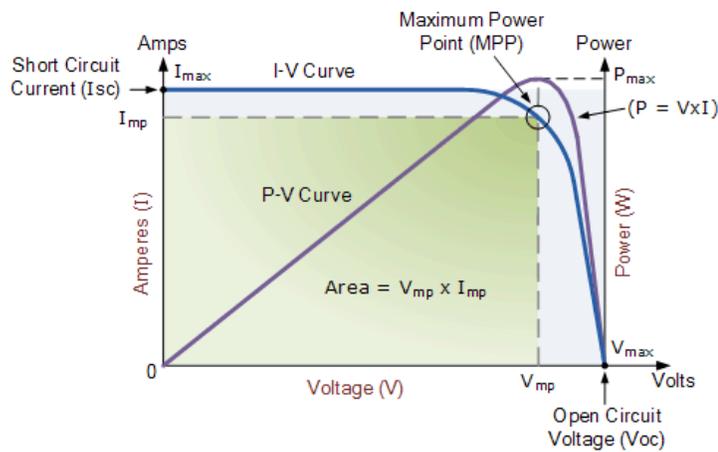
Figure 2.2 PV panel IV characteristics

It shows that when PV output voltage gradually increases from 0, the PV output current decreases from the short circuit current. However, the rate of this decrease trend is very small. Until at certain point, the output current drops rapidly. This phenomenon is very similar to the semiconductor diode characteristics, which there is a threshold voltage required to turn on the device on and let the current pass through. Also, from the power curve in Figure 2.2, one can also find that the maximum power point (MPP) is not located at half of the open-circuit voltage. According to [4], the MPP can be influenced by the illumination level, temperature, internal series and parallel resistance. Among these parameters, only illumination level and temperature will change the MPP location dynamically and significantly. An intuitive diagram is shown in the Figure 2.3 to demonstrate the impact on the I-V characteristics by the illumination level with the same PV panel.

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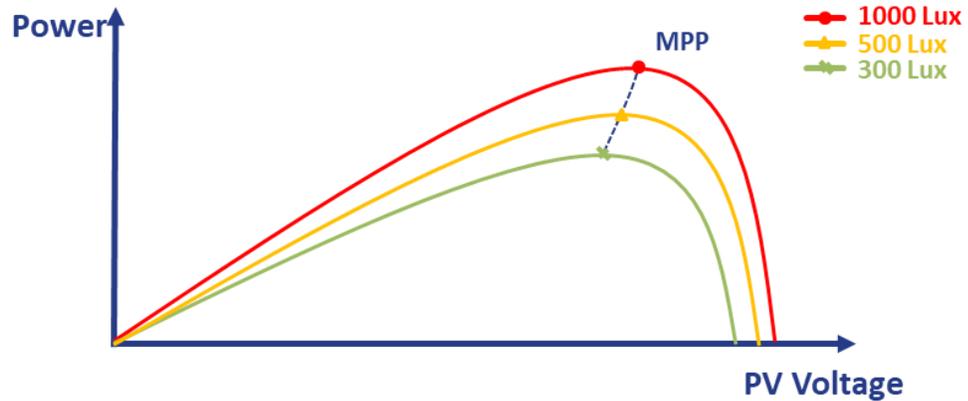
Figure 2.3 The influence of illumination level on the same PV panel I-V characteristics

Moreover, among different PV panels, the I-V characteristic can vary more significantly because the area, the layout of solar diode and the connection pattern is different. An intuitive diagram is shown in the Figure 2.4 to demonstrate the impact on the I-V characteristic by different PV panels under the same illumination level.
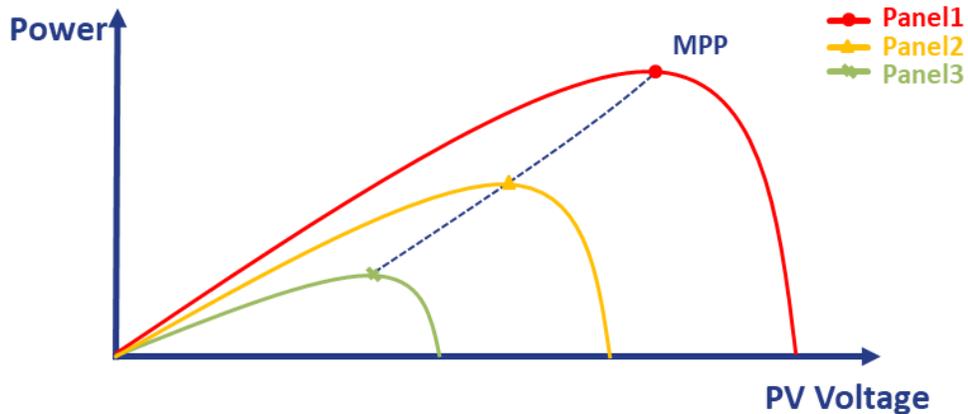
Figure 2.4 Different PV panel I-V characteristics under the same light condition

Thus, since these variation and uncertainty of maximum power point (MPP), a circuit called MPP tracker need to be implemented to search for the circuit optimal operating point by itself to accommodate first the change of environment, second different PV panels.

2.1.2 PV Modeling Method

To imitate practical PV panel electrical behavior, equivalent circuit modeling is required to perform simulation along with PMC. There are many modeling methods were introduced base

on the previous studies [4], one of them is widely use and called one-diode model which is shown in Figure 2.5.
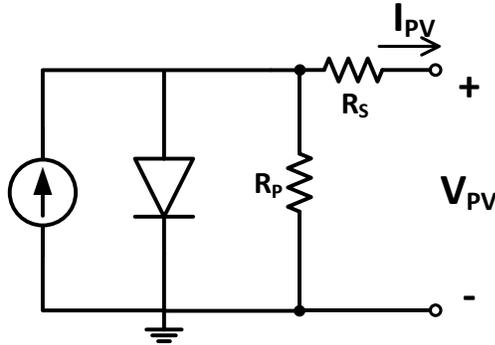
Figure 2.5 One-diode model

One diode consists of one current source, one diode, and parallel and series resistance. This equivalent circuit model has a good compromise between simplicity and accuracy. In this study, the diodes coming with process design kit (PDK) were used in Cadence simulation environment to perform simulation. The current source was used to imitate short-circuit current, parallel and series resistance were adjusted to match with practical PV panels MPP location.

2.2 Maximum Power Point Tracking Strategies

Due to non-linearity of PV characteristics, the uncertainty of MPP is one of the common solar energy harvesting issue. To extract the maximum power from the PV panel dynamically, maximum power point tracking (MPPT) is commonly used. According to [5], lots of MPPT methods were investigated and developed. Two of these methods are widely used. One is called fractional open-circuit voltage (FOCV), and another is called perturb and observe (P&O) or hill climbing. In this section, two methods will be explained, and their advantages and disadvantages will be studies.

2.2.1 Fractional Open-circuit Voltage

Based on [6-9], the approximately linear relationship between MPP and V_{OC} of the PV panels, under dynamic illumination level and temperature, has developed to fractional open-circuit method (FOCV) method.

$$V_{MPP} \approx k \cdot V_{OC} \tag{2.1}$$

Where k is a constant of proportionality. Since different PV panels may have different k value, it must be pre-determined either by empirical test or given from the datasheet. Once the factor k is known, the circuit can measure the open-circuit voltage periodically by disconnecting the power converter. Then one can apply a closed-loop control to regulate the PV voltage around V_{MPP}. A typical equivalent block diagram is shown in the Figure 2.6.
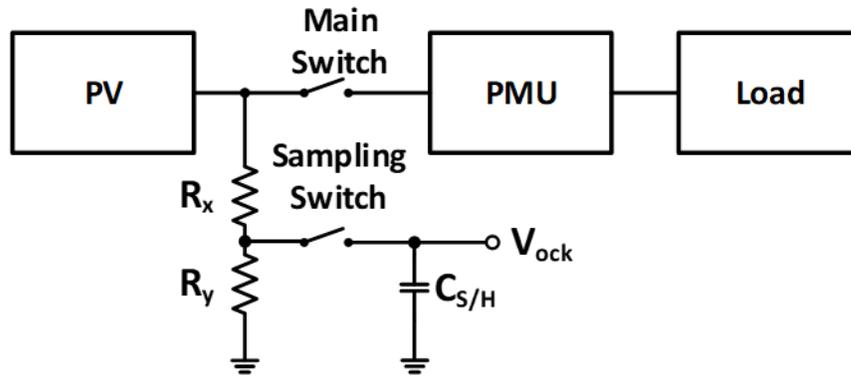
Figure 2.6 Common FOCV structure

Where the voltage divider $R_x/(R_x+R_y)$ is used to determine the factor k. $C_{S/H}$ will hold the sampled value and used to as reference voltage in the closed-loop control. Several disadvantages were reported in [5]. Since the power converter needs to be disconnected momentarily, it causes power loss temporarily and interrupts the energy harvesting process. Another one is that the factor k is only an approximation, so the PV panel technically never operates at the optimal power point. Even this method has some errors, in some applications, this method is adequate. Also, since this method is very easy to use and cheap to implement which doesn't require any sensor and data processing such as using micro-controllers or DSPs, FOCV method is still widely used in different situations.

2.2.2 Hill Climbing or Perturb & Observe

Lots of focus has been on hill climbing or perturb & observe (P&O). Based on [5], hill climbing involves a perturbation in the duty cycle of the power converter, and P&O involves a perturbation in the operating voltage of the PV panel. Perturbing the duty cycle of power converts result in perturbing the PV operating voltage consequently. Thus, these two different perturbing parameters are different methods to envision the same idea.
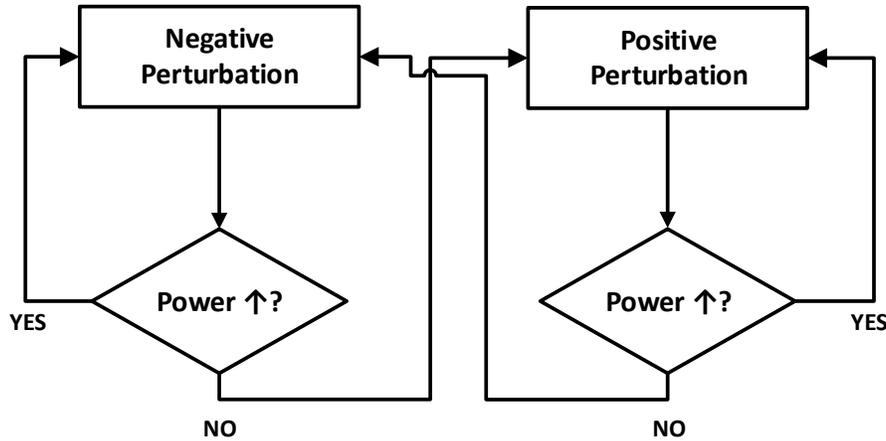
Figure 2.7 P&O algorithm

Based on [10-13], a common search algorithm is summarized and shown in the Figure 2.7. It says when a positive (negative) perturbation is performed, if the power observed from the PV panel is increased. The subsequent perturbation should keep the same direction to reach the MPP and if the power is decrease, then the perturbation should be opposite. This process is repeated until the MPP is reached. The system then oscillates around MPP. This method has good accuracy even different PV panels are used. Not like FOCV, the energy harvesting process will not be interrupted. However, the accuracy is dependent on the step size of each perturbation. If the step size is set to small, the good accuracy can be achieved. However, it slows down the search speed. Moreover, in order to serve large variety of PV panels, large search window should be prepared. The power converter design should comprise certain accuracy and large search window. Another disadvantage of this method is that comparing the power, it usually requires current sensor to sampling the current from PV panel, then implement multiplication of voltage and current. This complex task can be done by micro-controller or DSP such as [12]. However, those devices contain computing unit usually consumes large amount of power which is not suitable for indoor solar applications because of the power scale available from the ambient is relatively low.

2.3 Power Converter Design

The conventional non-inverting buck-boost converter is shown in Figure 2.8 (a). This converter consists of 4 MOSFET switches. S1 and S2 are two on switches. During on period, S1, and S2 will be turned on, V_{in} will energize the inductor to store current like in Figure 2.8 (b). S3

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and S4 are off switches. During off-period, S3 and S4 will be turned off, inductor will de-energize and discharge the current to the load. Thus, this type of power converter can either step
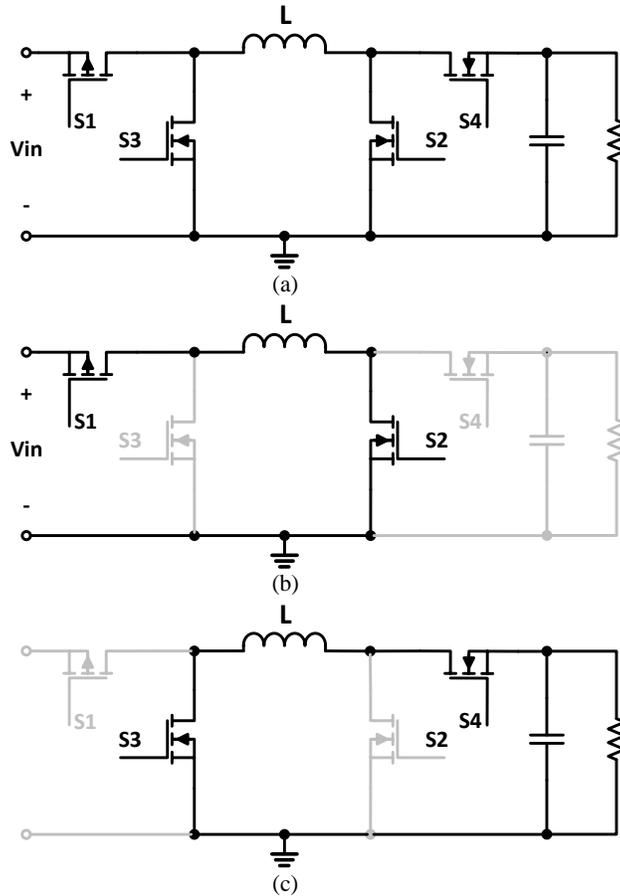
Figure 2.8 (a) Conventional non-inverting Buck-boost converter (b) Charging period (c) Discharging period

up or step down the input voltage depending on the duty ratio. This topology also gives non-inverting output which compared to typical buck-boost converter, the output is negative. One needs to flip the voltage by extra circuit.

The power converter is fully synchronized which no diode will be used to save power. One pair of switches will be controlled together means that it's easy to control. One disadvantage of this topology is that there are 4 switches on the power stage, and it cause relatively higher switch conduction, switching and driving losses. On the IC, since the switch size is large so it may not really area efficient.

2.4 Impedance Matching

Impedance matching is an important concept for energy harvesting. Extracting maximum power from the energy sources is crucial for all type of energy harvesting. According to [1, 14-16], buck-boost running at discontinuous conduction mode (DCM) can be used for impedance matching. Refer to [15], the summarized relationship about input impedance among different type power converter at CCM and DCM operation mode are shown in the Table 1. As one could be seen, all the converter when running in CCM mode, the input impedance is dependent on the load condition. In such a case, the input impedance is very hard to control. However, there is a solution which is buck-boost converter running in the DCM. The input relationship is only dependent on duty cycle and switching period once the inductance is fixed. In such a case, one can easily control the input impedance by controlling either duty ratio or switching period (or switching frequency) of the power converter.

Table 1 Input impedance equations for buck, boost and buck-boost running CCM, DCM

Operation	Buck	Boost	Buck-Boost
CCM	$R_{in} = \dfrac{R_L}{D^2}$	$R_{in} = R_L(1-D)^2$	$R_{in} = \dfrac{R_L(1-D)^2}{D^2}$
DCM	$R_{in} = \dfrac{2L}{(1-M)D_1^2 T_s}$	$R_{in} = \dfrac{2L}{(D_1+D_2)D_1 T_s}$ $R_{in} = \dfrac{2L}{D_1^2 T_s}\left(1 - \dfrac{V_{in}}{V_{out}}\right)$	$R_{in} = \dfrac{2L}{D_1^2 T_s}$

$$where, \ M = \frac{2}{1 + \sqrt{1 + \dfrac{8L}{D_1^2 R_L T_s}}}$$

2.5 Previous Works

To get knowledge of current state of arts, two research works which adopt two different MPPT methods and corresponding control scheme are analyzed.

In [17], Bandyopadhyay et al. present an architecture that using boost converter in discontinuous conduction mode (DCM). Multiple inputs and multiple outputs sharing one inductor topology has also been used. For impedance matching, the circuit controls the duty cycle of a fixed switching period to changing the input impedance of the converter. However, the impedance matching is followed by some approximation. They adopt perturb & observe (P&O) method for maximum power point tracking which based on a sensor-less time-based power monitor circuit to sample and comparing the results. In this thesis work, same power monitor circuit is used. In [17], the PV voltage is not directly been controlled or within any feedback loop. The disadvantage out of this control scheme is the stability issue if some perturbation is injected to the system. The system may take longer time to recover or may lose control. Secondly, the boost converter topology is not perfect for time-based power monitor circuit. In this paper, the author states the limitation is that the power measuring circuit only works under assumption that input/output conversion ratio is high enough, then the approximation error can be ignored. Another limitation of this architecture is that the input range is limited by the boost converter because the input voltage can only be lower than output voltage.
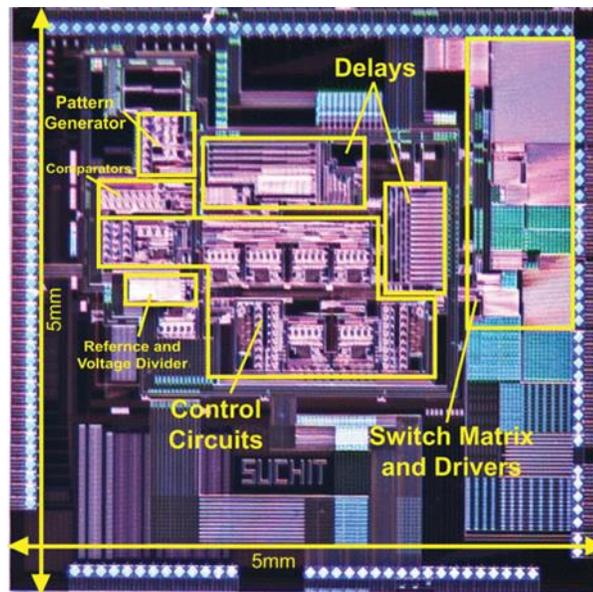

Figure 2.9 Die photo of the first previous work [17]

In [18], Wang et al. presents a circuit system which using only 3 switches buck-boost converter to achieve dual-input dual output. Impedance matching is also achieved by using buck-boost converter running in the DCM. Constant on-time pulse skipping modulation is adopted.

FOCV is used as main MPPT technique. Thus, the drawbacks of FOCV method are that firstly, the energy harvesting circuit will be disconnected periodically so the harvesting process will be interrupted. Secondly, the FOCV method will maintain the operation point at fixed ratio, and this fixed point may not be true maximum power point (MPP). However, the FOCV method is simple and easy to implement. Another limitation is same as above, the input voltage is limited by the buck converter which the input voltage can only be higher than the output voltage.
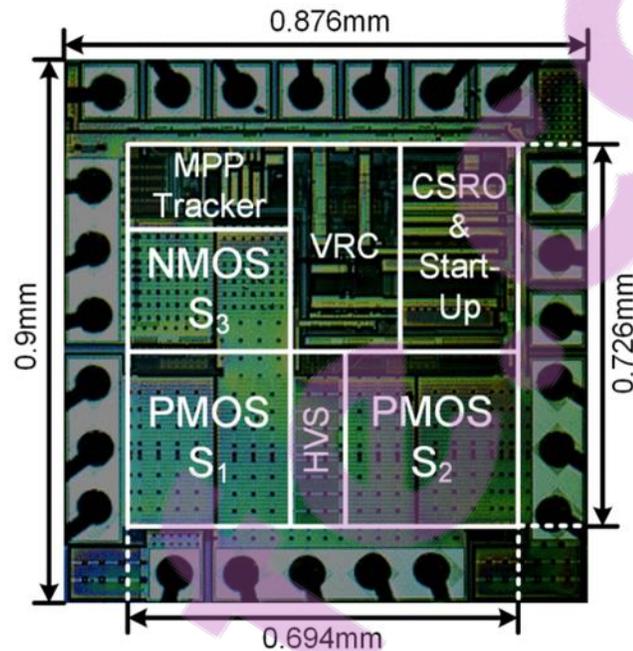
Figure 2.10 Die photo of the second previous work [18]

2.6 Chapter Summary

In this chapter, PV characteristics and modeling method were introduced. Conventional maximum power point tracking strategies and their advantages and disadvantages are analyzed based on recently studies. The common buck-boost operation mode and its advantage of achieving impedance matching were shown in the Table 1. Two previous indoor solar energy harvesting works are studied.

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Chapter 3: Proposed Energy Harvesting Circuit

Some design specification criteria should be justified for proposed energy harvesting circuit for indoor solar applications based on the ambient environment and circuit requirements. First, the circuit should sustain long lifecycle. In another word, even the environment is completely dark, there should be power source to support load to working properly. Second, the circuit should take different kind of PV panels, means that the input voltage/power range should be as large as possible. Third, the maximum power tacking strategy should be power efficient and possibly have good compromise of certain accuracy and large search window. Lastly, the power management circuit should be power efficient itself, any power-hungry circuit should be avoided to use.

This chapter describes the detail design of the proposed power management circuit to achieve the specification criteria above. Section 3.1 describes the power stage circuit and explains the detailed operation and its control method. Section 3.2 illustrates the proposed MPPT strategy which is an improvement from the two common method introduced in the Section 2.2. Section 3.3 introduces some basic building blocks and the circuit operation is explained in detail.

3.1 Dual-input Dual-output Buck-boost Converter (DIDOBB)

3.1.1 Power stage Operation

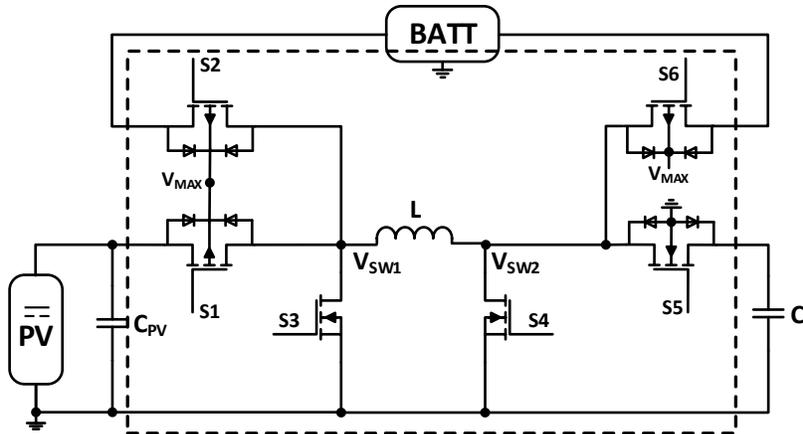The power stage circuit is shown in the Figure 3.1

Figure 3.1 Dual-input dual-output buck-boost converter (DIDOBB)

The dashed-line region includes DIDOBB, which consists of six switches. The power stage circuit is very similar to 4-switch non-inverting buck-boost converter. The only difference from Figure 3.1 is that S2 and S6 for extra input and output. This topology can have freedom to change the configuration to have more inputs and outputs by just adding necessary switches and only one inductor is sharing [19]. The operation is also very similar to 4-switches non-inverting buck-boost converter. Also, the bulk connection needs to be carefully connected to correct potential, to make sure body diodes are reverse-biased to prevent leakage.

In this power stage circuit, battery is both used as input and output. Since the indoor solar energy may not be available, the load still demands power. In such a case, the battery will provide power to compensate power shortage. Vice-versa, when load doesn't require too much power and indoor solar energy is sufficient. The excessive energy will be stored in the battery as secondary load for the future usage. In this way, PV doesn't have wasted energy, and energy usage efficiency can reach maximum. With this energy recycling, the battery can be treated as energy buffer and large capacitor can be avoided. In this way, the load response time can be faster.

3.1.2 I/O Configurations

Since multiple inputs and outputs are used, selecting the correct corresponding input/output based on the incident of events would be essential to this I/O control. Three incidences, PV, Batt, CL were chosen to determine the combination of the I/O ports. These incidences are from the output of three clock comparators with comparing with the reference to

indicate energy level. Thus, energy charging information are transfer to digital logic information, and these three logic signals are denoted as Φ_{PV}, Φ_{Batt}, Φ_{CL}. For example, Φ_{PV} is high means the current V_{PV} is higher the PV reference voltage. ThuS, there is enough energy to be harvested. Opposite, if Φ_{PV} is low means the PV energy is not available at current operating cycle. Based on this, three logic input can form combinational relationship to determine the IN/OUT ports. The relationship is shown in the Table 2.

Table 2 I/O configuration combinational logic

ΦPV	ΦBatt	ΦCL	Input	Output	Converter
L	L	L	-	-	Deactivated
L	L	H	-	-	Deactivated
L	H	L	Batt	CL	-
L	H	H	-	-	Deactivated
H	L	L	PV	CL	-
H	L	H	PV	Batt	-
H	H	L	PV	CL	-
H	H	H	-	-	Deactivated

Where in the table, deactivated means no input/output will be selected by simply turning off S1-S6.

3.1.3 Constant On-time Pulse Skipping Modulation (COT-SPM)

Constant On-time pulse skipping modulation is used as control scheme of the power stage. It's achieved based on the output of the I/O configuration block. Using PV as an example, Whenever, PV is selected as the input, the on-time generation block will generate a constant on-time pulse which in this design is 300 ns. Thus, the PV will deliver an energy packet to either battery or capacitor load, C_L. This cause the PV voltage decreases, so the PV voltage will drop

below the current PV reference voltage and recover after this energy delivery process finishes. Whenever, PV voltage is recovered above reference, it will reinitiate energy delivery process. The system clock skipped between these two events is the skipped pulses. In the Figure 3.2, it illustrates the pulse skipping as the example described above.
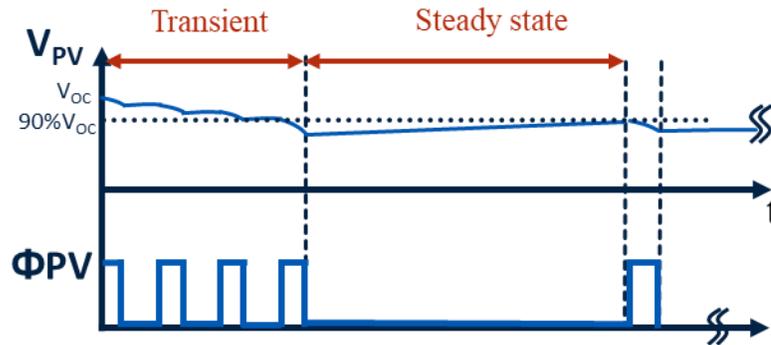

Figure 3.2 Pulse skipping modulation for PV

Thus, in steady state the peak voltage will stay at the 90% of the V_{oc} for example. The voltage ripple will be decided on the fixed on-time and input capacitance. Every two Φ_{PV}, the time difference in between, is the equivalent frequency for the buck-boost converter which is able to generate at certain impedance to running at such PV voltage. In this way, one can achieve voltage regulation both for input and output.

3.1.4 Zero Current Detection

For buck-boost converter running in the DCM mode, after inductor has been discharged, the switches on the discharging path should be all turned off when inductor current touches zero. Otherwise, it cases energy leakage which waste of power. Zero current detection was found in many works, and one of the methods was adopted in this work [2, 14, 15, 17, 18]. The voltage V_{sw1} in the Figure 3.1 is compared with ground or the drain and source voltage of M3 is compared by a clocked comparator. Wherever the drain/source voltage of M3 flips that's the point where inductor touches zero. The waveform is shown in the Figure 3.3. Thus, in the Figure 3.4, if V_{sw1} is larger than ground, the positive terminal of clocked comparator will generate a pulse which to trigger the discharging path switches to turn off. Also, turning off the oscillator and clocked comparator to save the power. This ZCD circuit can be re-initiate when the next ZCD need to be used.
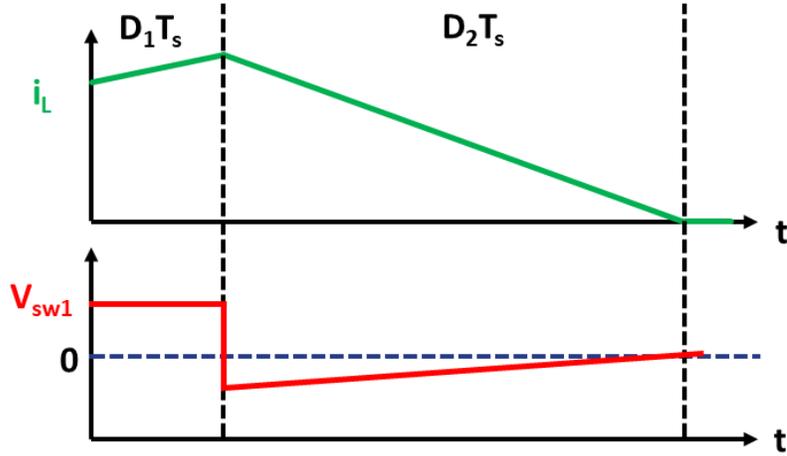
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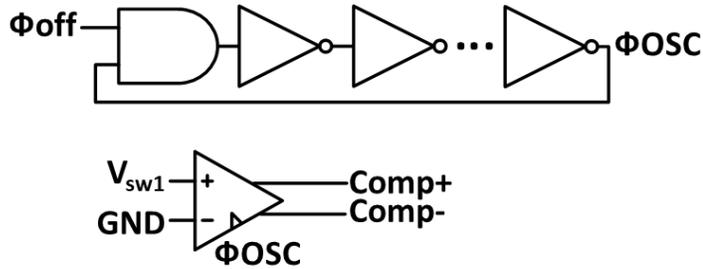Figure 3.3 V_{sw1} and i_L waveform when zero current switching occurs

Figure 3.4 Zero Current Detection (ZCD) Circuit

3.2 Proposed MPPT method

In this section, the proposed MPPT method will be explained. Combining section 2.2, the pros and cons of each MPPT method will be analysis. The primary advantage of proposed MPPT method is fully digitalized, simple and one universal search window with certain accuracy and large search window.

3.2.1 Method Overview

In this proposed MPPT method, we used both perturb and observe (P&O) and fractional open-circuit (FOCV) method. The flowchart of this algorithm is shown in the Figure 3.5. Firstly, in the P&O mode, the circuit will sample the open-circuit voltage and start perturbing process. The perturbing parameter is usually either PV voltage directly or load impedance of PV panel indirectly. In this proposed design, we perturb percentage (ratio), k, respect to open-circuit

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voltage sampled. Observing process will be done by power measurement circuit. The next perturbing direction will be determined based on the power measurement circuit compared results. Until we find optimal ratio k, we will leave P&O mode, and entering periodical FOCV mode. Since the indoor solar environment is very stable, the illumination level won't change much. The assumption is made here that optimal ratio k doesn't shift significantly.
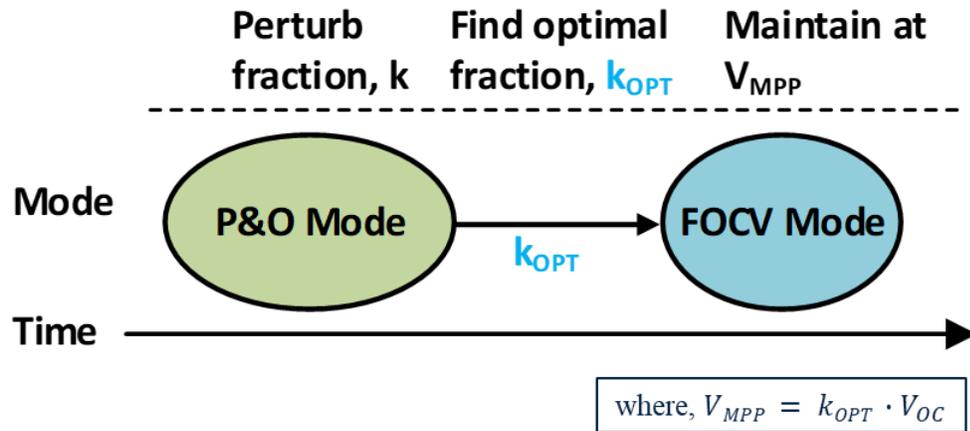

Figure 3.5 Algorithm of the proposed MPPT method

3.2.2 P&O Mode

The open-circuit voltage will be sampled based on the method described in [18]. The sampling circuit is shown in the Figure 3.6, where Ss is the sampling switch, S1, S3 are the switches in the power converter. $C_{S/H}$ is the sample/hold capacitor to store the open-circuit voltage. The value of sample/hold capacitor $C_{S/H}$ needs to be carefully picked by considering the leakage of capacitor charge and hold time. Starting from open-circuit voltage, the circuit will initiate the perturbing process. The perturb range in this design is set to be from 100% to 60% (if the open circuit is included). 5% interval between is the resolution. This can be achieved by using a 3-bit digital controlled reference ladder as shown in the Figure 3.7. V_{OCK} <0:2> are 3 digital controlled bit and associated with 3 switches to either short the corresponding resistance R0-R3 respect. The resistance value is adjusted based one the binary order, for example, R1 = 2R0, R2 = 4R0. R_x and R_y divider network are used to set up the first search point at 95%.
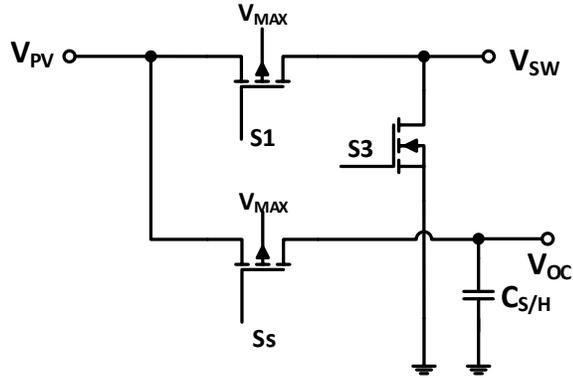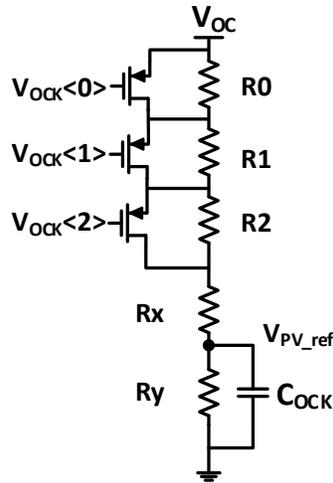
Figure 3.6 Open-circuit voltage sampling

Figure 3.7 3-bit digital controlled reference ladder to setup perturb region

For the observing process, the power needs to be measured, stored, and compared in sequence. According to [3, 17], the relationship was found that for buck-boost converter, inductor discharging time D_2T_s (also called off-time: t_{off}) and the output is regulated. The t_{off} and input power have relationship as describe in (3.1). The detailed derivation can be found in the Appendix section.

$$t_{off} = \frac{1}{V_{Load}} \cdot \sqrt{\frac{2 \cdot L \cdot P_{in}}{f_s}}$$

(3.1)

$$t_{off} \propto \sqrt{P_{in}}$$

(3.2)

In equation (3.2), it says off-time is directly proportional to square root of input power. Thus, with the help of this relationship, we don't need to know the exact value of the input power. However, we can get the trend out of it such as increment or decrement. By directly measure the time information of the off-time. We can tell the input power is either increased or decreased. From this concept, we can get rid of sensor which is dissipated power.

The actual power measurement circuit is shown in the Figure 3.8. It consists of primary output ZCD circuit, 8-bit Sample/Hold/Compare unit, and a P&O Logic circuit. Primary ZCD circuit will transform the pulse width information into clock information. Based on counting clock edges by the 8-bit counter from PV to CL energy deliver path, pulse width information becomes binary digits. Then it will be stored in an 8-bit D flip-flop for the current cycle. When the data from the next cycle comes, they will be compared by the 8-bit magnitude comparator. The compared result will be sent to the P&O logic block. In this design, A input is the current cycle data, denoted as n cycle, and B input is the previous cycle data, denoted as (n-1) cycle. Thus, every two successive data will be compared until the magnitude finds A is less than B, it will output 1, otherwise the output remains 0. In this 8-bit Sample/Hold/Compare unit, the synchronous operation based on the separate Samp_CLK which is generated by CLK generation blocks followed by the system CLK. The circuit implementation is shown in the Figure 3.9. This configuration is simply a frequency divider. In this design, the sampling clock period is around 512 μs and 50% duty cycle (SYSCLK/2^9). This sampling frequency is much slower than the system clock. This is because several sample can be recorded, and average value can be compared. In this way, the ripple of regulated output and input disturbance will be minimized by averaging.
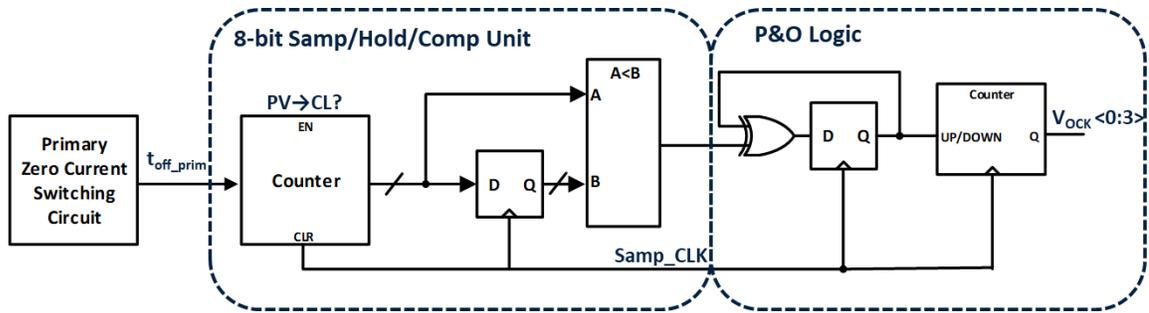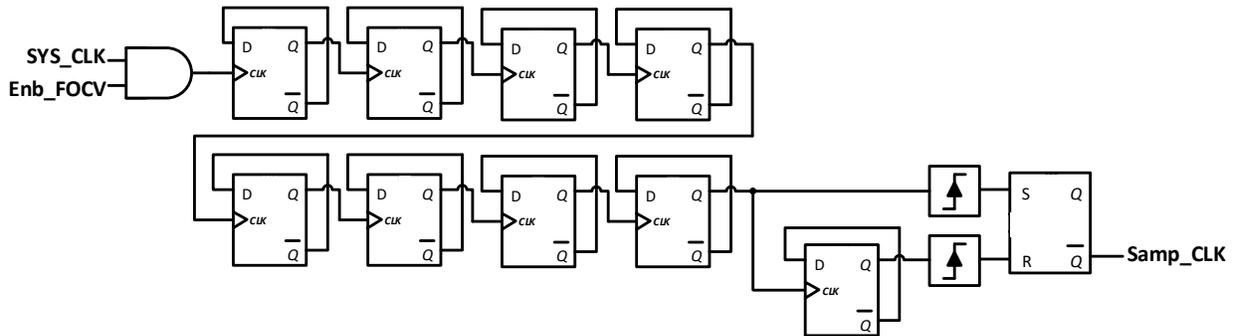
Figure 3.8 Power Measurement Circuit

Figure 3.9 Sampling CLK signal generation

The P&O logic circuit is implemented as shown in Figure 3.8, based on [14, 20]. The feedback connected XOR gate and D filp-flop consists the main circuit part. The logic flow can be better demonstrating from Figure 3.10. Starting climbing from open-circuit voltage (V_{OC}), the perturbing direction will not change because the power of nth point will be found always bigger than the power of (n-1)th point. The output of magnitude comparator will always hold at 0, and output Q of D flip-flop will also hold at 0 and feedback to another input of XOR gate. Thus, this loop will not break until the output of the magnitude comparator changes. On the power curve, it shows the operating point will keep climbing which matches with the circuit. Until the first point is found where the power of that point is smaller than the power of its previous point. Then, the perturbing direction start oscillating. The order is 5-4-3-4-5-3. A 3-bit up-down counter is used to change the reference point of PV. 0 indicates up, and 1 indicates down. In this design, to make the operating point is at maximum power point at majority of the time. The MPP searching process will be stopped after the first time it bounces back to point 4. In this way, the MPPT controller can be turned off to save power. However, the circuit can be stopped at this fixed point because we made assumption that the indoor light condition will not change much. Otherwise, tracking is necessary in case that MPP shifts when environment changes.
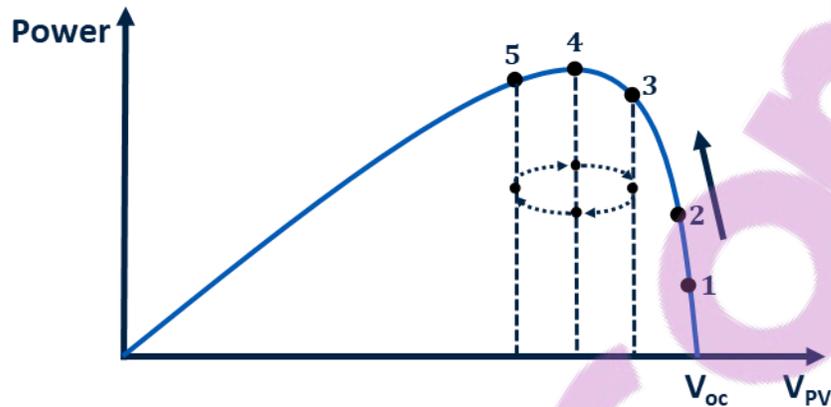
22

Figure 3.10 Perturb process on the power curve

3.2.3 FOCV Mode

After optimal ratio k is found, the circuit will enter periodic FOCV mode like in [18]. The block diagram for FOCV mode is shown in the Figure 3.11. As main switch is disconnected, the PV voltage will recover back the open-circuit voltage. The sampling switch will be closed to sample the open-circuit voltage in the S/H capacitor. This voltage reference is then sent to the reference ladder shown in the Figure 3.7. The sampling behavior waveform is shown in the Figure 3.12. Meanwhile, another feature to have back-up battery is that during sampling period, PV is disconnected from the load and no energy is transferred. Then battery will continuously deliver energy to the load. Thus, load power will not be interrupt comparing with typical FOCV method with single path architecture. Since the indoor environment doesn't change much, so open-circuit voltage would not shift significantly. Thus, longer sampling period can be used, such as 16 or 32 seconds. Since the simulation tool such as Cadence in this design doesn't suitable for running such long simulation. The clock to generate long sampling clock is intended to be off-chip and leave the freedom to external changes.
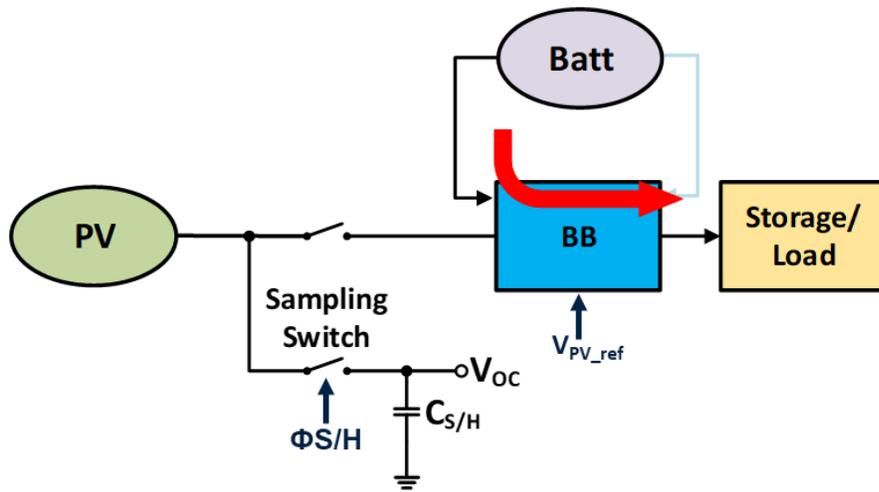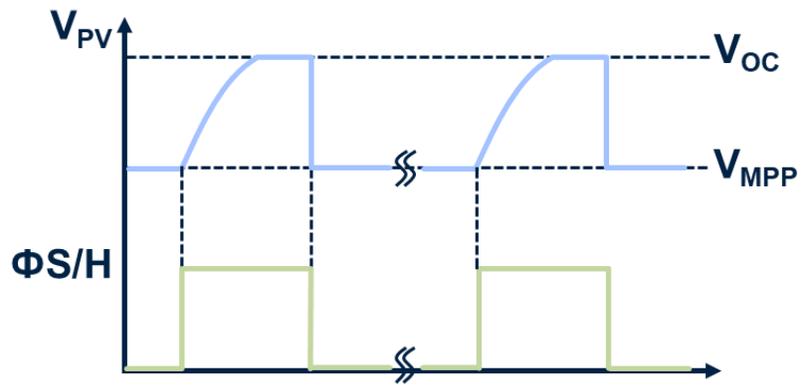
Figure 3.11 FOCV mode block diagram

Figure 3.12 Sampling behavior waveform

Chapter 4: Simulation Results

The circuit was designed and simulated using Cadence 6.1.6 version with TSMC BCDMOS 180 nm process design kit (PDK). To fully verify the actual performance after IC is fabricated, the post layout simulation adding parasites effected is simulated and verified. The die photo of the proposed circuit and system is shown in the Figure 4.1. The entire IC is 1.5 mm by 1.5 mm with active area around 1 mm by 1mm. The core is supplied by 1.8 V and the analog I/O is supplied by 5 V.
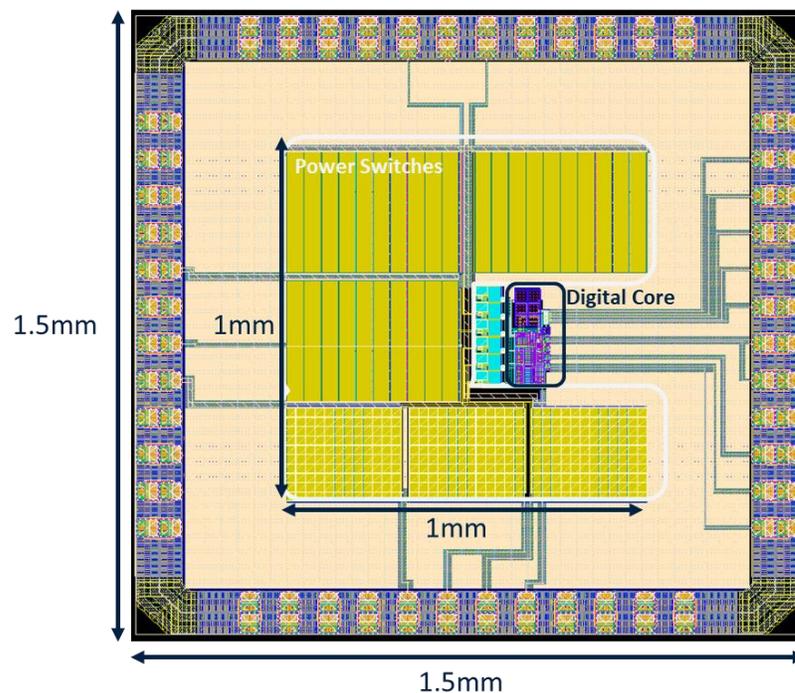

Figure 4.1 Die photo of the proposed circuit and system

4.1 Capture Results

4.1.1 Solar Panel simulation

The I-V characteristics and power curve of modeled solar panel are shown in the Figure 4.2. The short-circuit current is 1 mA, and open-circuit voltage is 3.89 V. The maximum power point is located at 3.45 V which is 88.7% of the open circuit voltage. The power available at operating condition is 3.32 mW.
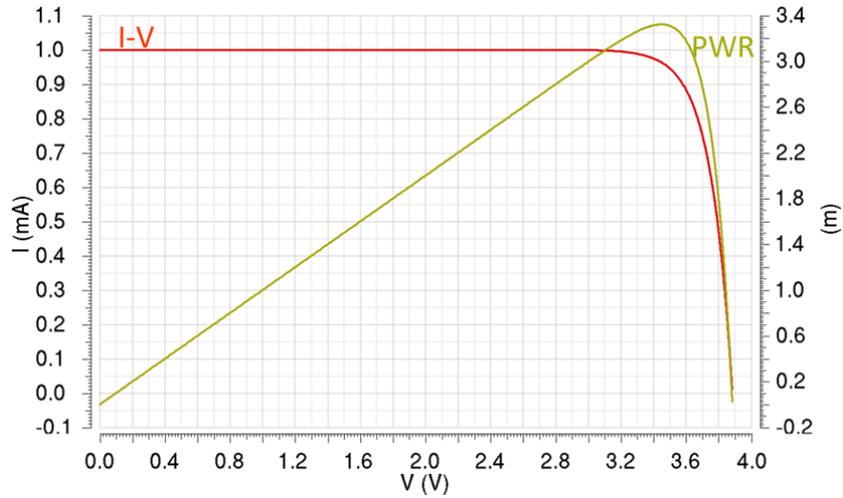
Figure 4.2 I-V characteristics and power curve of the solar panel used in this design

4.1.2 Zero Current Detection

The zero current detection is shown in the Figure 4.3. The ZCD circuit clock frequency is running at 35 MHz which compromise the good accuracy and power dissipations. When on-time finished, the ZCD circuit will start by initiating oscillator. During ZCD operation, the positive input terminal, V_{SW1} is compared with GND continuously. Until V_{SW1} is larger than GND, the point is exactly where inductor current reach zero. The positive output Comp+ will generate a pulse to indicate the zero-crossing point is found. The corresponding control signal will then turn off discharging-path switches. The offset is verified below 10 mV. After switches turned off, the parasitic capacitors and inductor will form a LC oscillator circuit. That's why the oscillation will be observed after all switches are turned off.
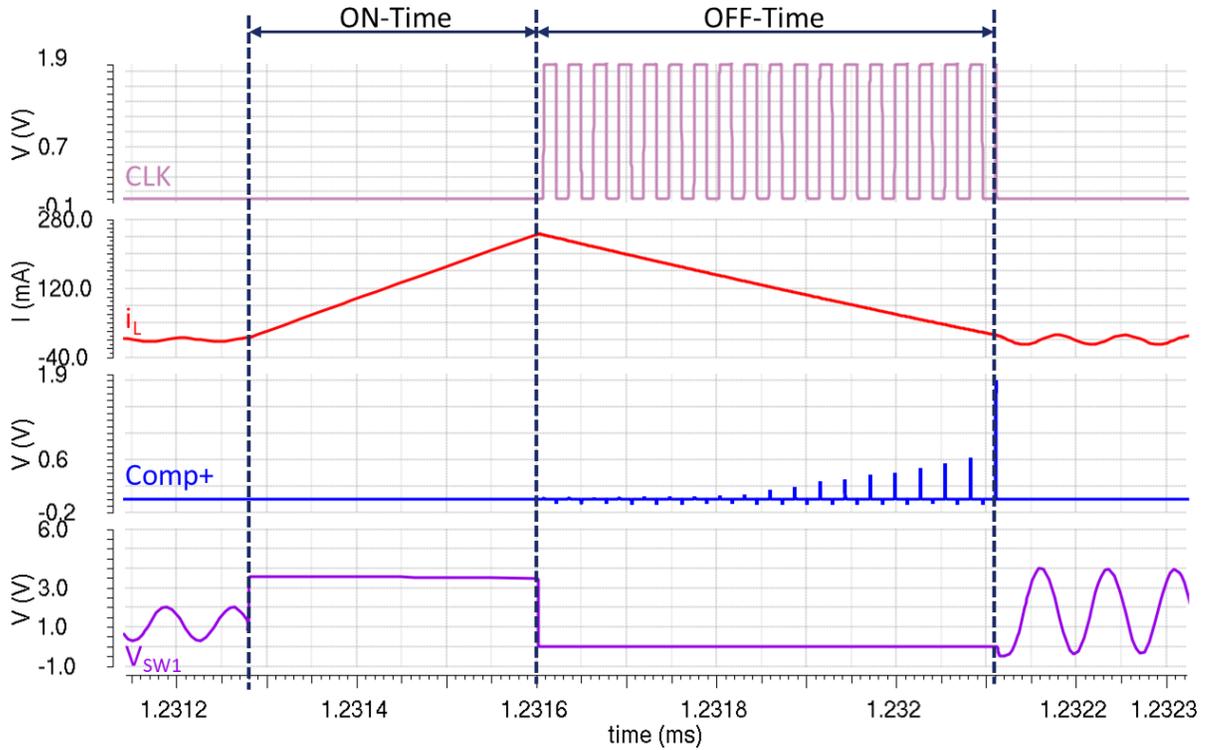
26

Figure 4.3 Zero current detection waveforms

4.1.3 Constant On-time Pulse Skipping and Voltage Regulation

In the Figure 4.4, it demonstrates how pulse skipping modulation works. Using PV as an example, when V_{PV} is higher than reference voltage, ΦPV will generate a pulse which enable constant on-time generation block, ΦOn. Thus, the corresponding switches will be turned on. An energy packet will be delivered from PV panel. Thus, the PV voltage, V_{PV} will decrease. At this moment, the PV voltage will below reference voltage. Since, the clocked comparator is comparing voltage with reference every system clock edge. Thus, in the following cycles, ΦPV will not generate any pulse until PV voltage is above reference again. This process is called pulse skipping modulation. The skipped pulses are highlighted in dash line and included by the red curly bracket in the Figure 4.4. The number of pulses which ΦPV skipped is dependent on the power/current available in the PV panel. In other word, the recover speed is dependent on the how much current PV panel can supply. In this way, we are regulating PV voltage around its reference voltage which is given by the MPPT controller. For impedance matching based on the equation in the Table 1, the circuit doesn't actively control any variable. Since on-time is constant, the impedance at certain regulated PV voltage can be represented by the equivalent

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ΦPV frequency, and this equivalent frequency is a circuit response by regulated voltage at PV reference voltage. Another benefit of this control scheme is that this is a closed-loop feedback system. Any disturbance or offset can be calibrated by this feedback system.
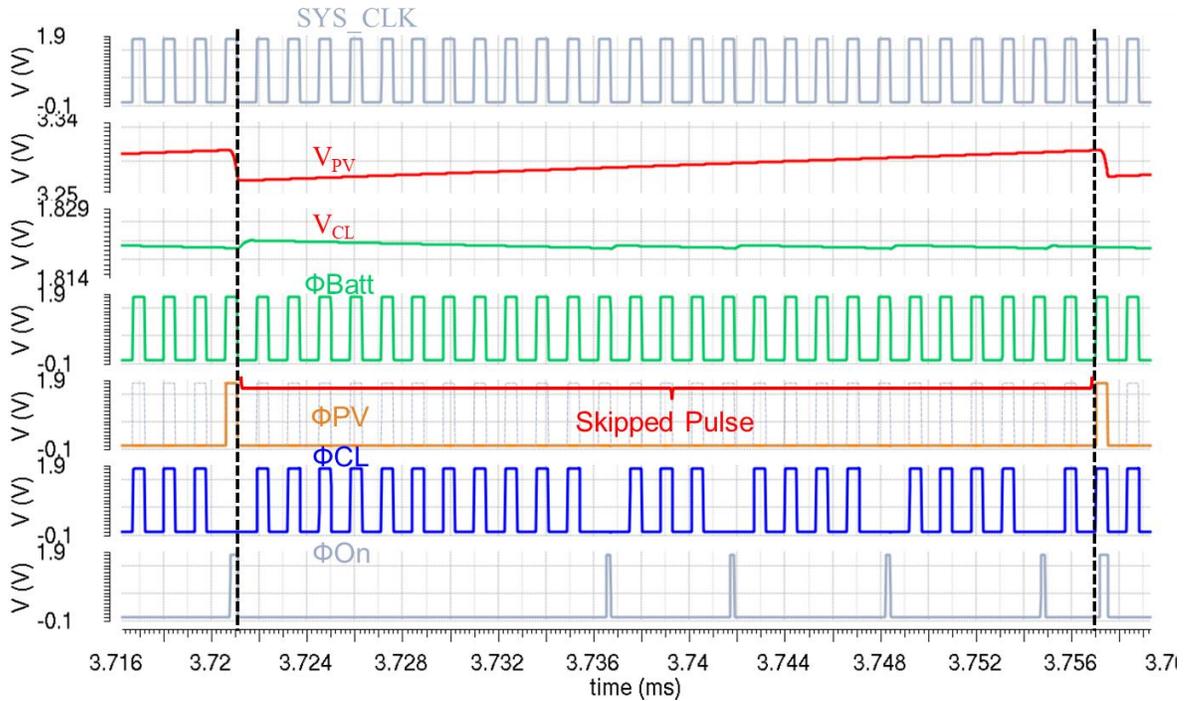

Figure 4.4 Pulse skipping Modulation Waveforms

The constant on-time generation is shown in the Figure 4.5. The current-starved topology is used in order to get longer delay with small area. Same purpose is for adding RC network. The hysteretic Schmitt trigger is used to filter any noise to have clean pulses. Thus, whenever there is a pulse at EN terminal, it will generate a constant time pulse. However, the delayed time should be smaller than EN terminal pulse.
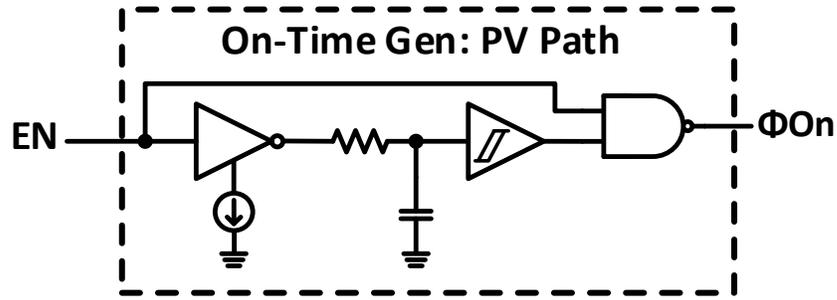
Figure 4.5 Constant On-time Generation Block

4.1.4 I/O Configuration

Based on the combinational logic relationship in Table 2, the simulation results are shown in the Figure 4.6. In the figure, it shows four different energy-delivery paths which are PV-Batt, Batt-CL, PV-CL and skipped. There is four input/output port can be selected which are PV as input, PV_IN; Batt as input, Batt_IN; CL as output, CL_OUT; Batt as output, Batt_OUT.
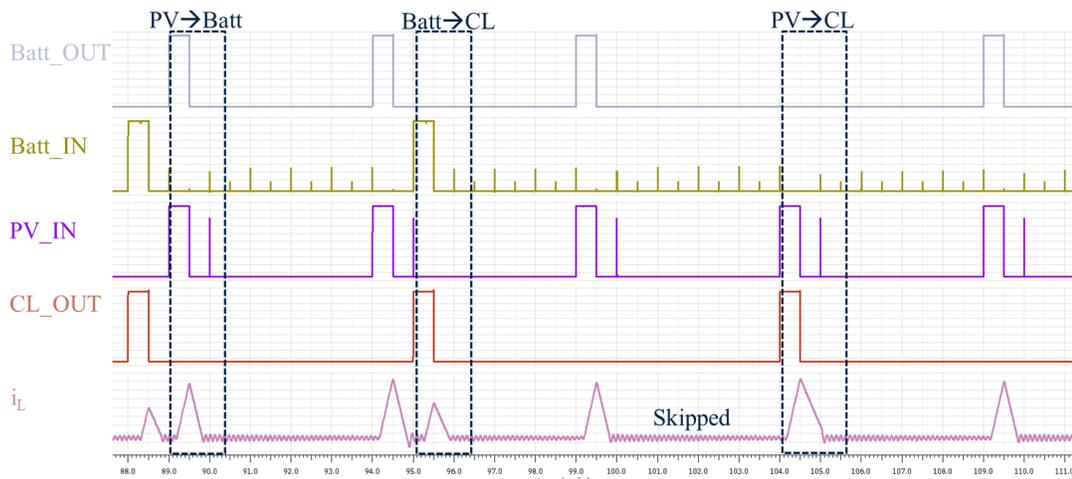

Figure 4.6 I/O Configuration under different combination cases

4.1.5 Perturb & Observe Mode

The P&O mode starts with open-voltage sampling, the process is shown in the Figure 4.7. As shown in the Figure 3.6, the sampling switch will be closed and charging the sample/hold capacitor. The value of this capacitor is selected based on the hold time. In this design, $C_{S/H}$ is 10 nF. After finishing open-voltage sampling, the normal process will start. In Figure 4.8, it shows the waveforms of the whole P&O process. V_{PV} indicates the current PV voltage. V_{PV_ref} is the current reference voltage to regulate PV voltage. Sample_CLK is the clock signal that controls

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all synchronous operation including that every clock edge, the data will be cleared in the counting element, the data will be passed to the storage element. One comparison will be performed and one perturbation (decision) will be made. From Figure 4.8, the Sample_CLK's period is 512 μs and with 50% duty cycle. Sample_EN is the signal which enable the counting element only when PV to CL energy delivery path is available. Since we only care about maximum power point of PV panel and CL output is regulated. Data bit is an 8-bit data which records the time information of inductor discharging time (t_{off_prim}). PH_Find is the signal that indicates the MPP is found and exiting search mode and locking the current optimal ratio, k.
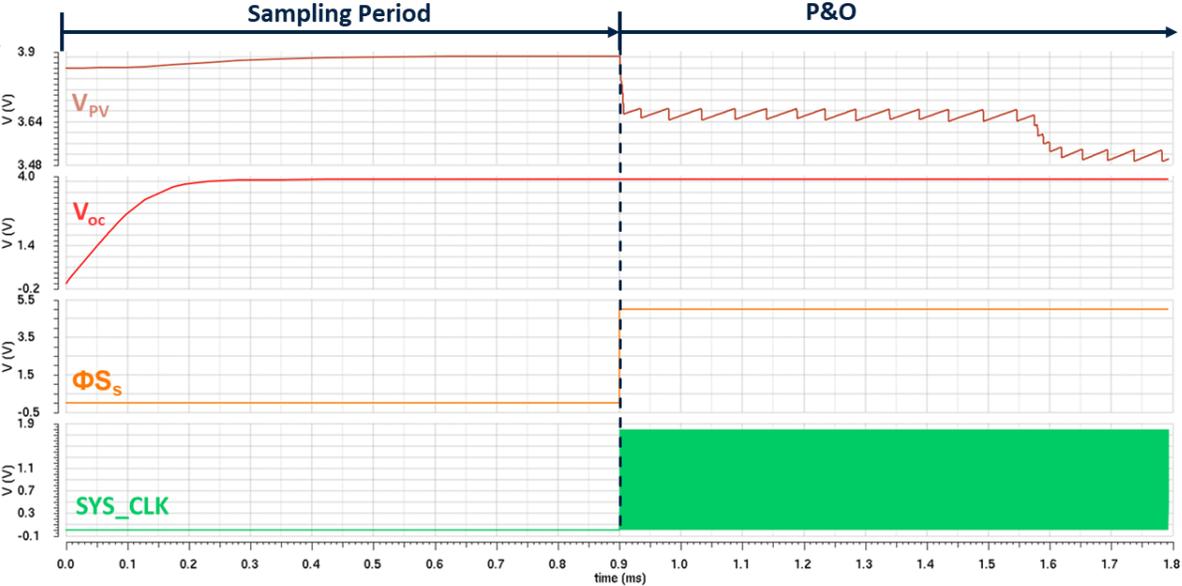

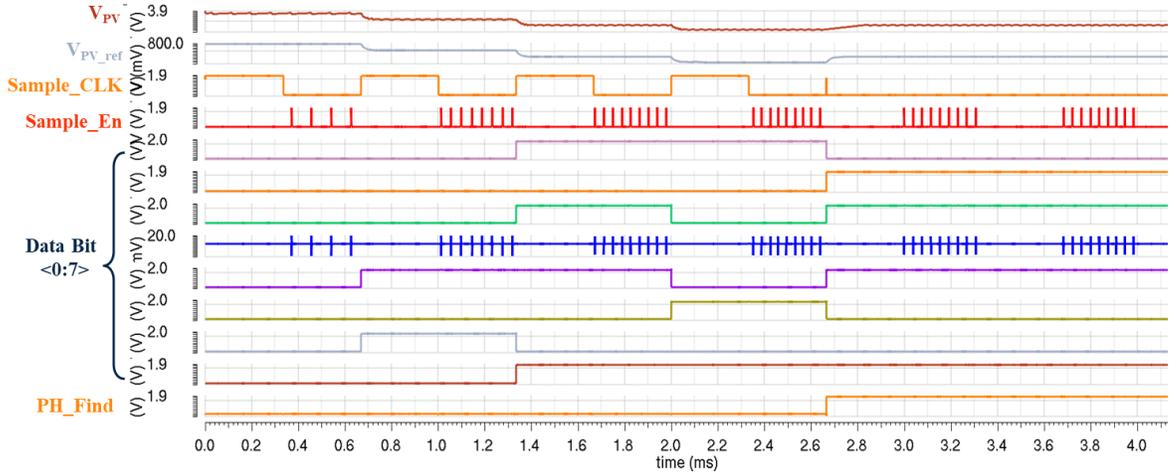Figure 4.7 Open-voltage sampling process

Figure 4.8 The perturb & observe process

The zoom-in version of Figure 4.8 is shown in the Figure 4.9. It illustrates that the reference is perturbed from 95% of the open-circuit voltage, each perturbation is 5%. Until the comparing unit found the total (t_{off_prim}) at 80% is smaller than where at 85%. It also implies that the average input power at 85% V_{OC} is bigger than its at 80%. The maximum power point (MPP) is then found and the circuit will step back one unit and lock the reference at 85% V_{OC}. Combing the results from solar simulation in Figure 4.2 where the MPP locates at 88% of the V_{OC}. In [3], the author defines a factor called closeness to maximum power.

$$\begin{aligned}
&Closeness\ to\ maximum\ power\ point \\
&= \frac{Power\ @\ Voltage\ where\ t_{off\_prim}\ is\ maximum}{Power\ at\ MPP}
\end{aligned} \quad (4.1)$$

The power at true MPP (88%) is 3.32 mW, and the power at actual MPP (85%) is 3.28 mW. Based on the definition above, the closeness to maximum power point is 98.8%.
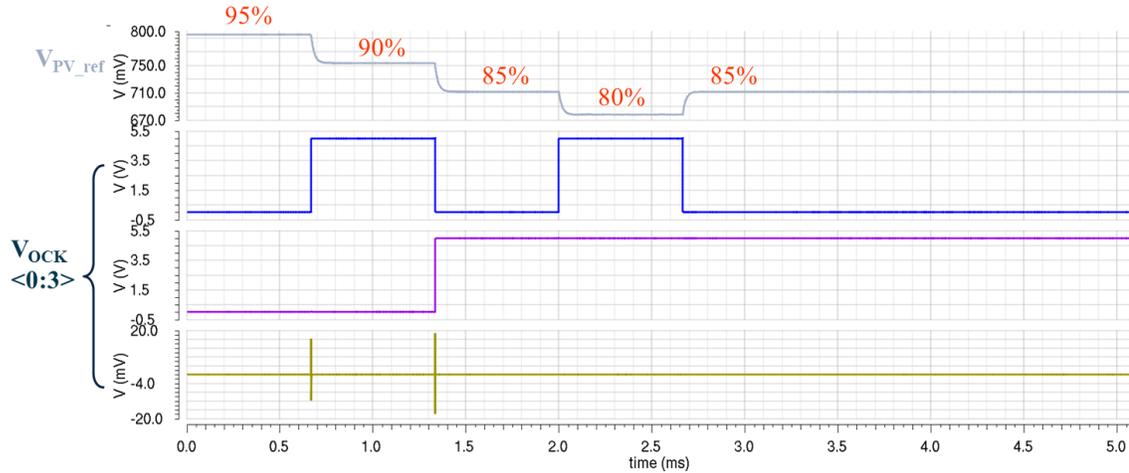
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Figure 4.9 Reference perturbing

The proposed MPPT method comparison with other works is shown in the Table 3. The proposed MPPT method uses both FOCV and P&O approach and perturb based on fractions to create adaptive fraction to accommodate different PV panels. For power measurement, no sensor is required for the proposed MPPT method in order to save power. The accuracy is sufficient for indoor solar applications.

Table 3 MPPT method comparison with other works

	Bandyopadhyay [JSSC 2012]	Wang [JSSC 2016]	Kim [TPE 2013]	Shao [TVLSI 2009]	This Work
MPPT Method	P&O	FOCV	P&O	P&O	P&O and FOCV
Perturb Param.	On-time with fixed frequency	-	SAR Logic	On-time with fixed frequency	Fractions
Sensor	Sensor-less	-	Voltage & Current sensor	Current sensor	Sensor-less
Power Measurement	Time-based	-	Analog multiplier	Analog switch capacitor	Time-based
Accuracy	Moderate	Low	High	Moderate	Moderate
PV Applicability	Tracking region limited	Fixed k	Tracking region limited	Tracking region limited	Adaptive k

The power stage is also been evaluated and the comparison is shown in the Table 4. As shown in the table, the proposed architecture provides largest load power range which is up to 126 mW. Since buck-boost converter is used which can either step up or step down the input voltage, the power stage in this proposed work can accept widest input voltage range. By using dual-path architecture which back-up battery, the power stage can have faster response when

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load is dynamically changing. In a light load case, excessive energy can also be stored in the back-up battery, then no energy is wasted.

Table 4 Performance comparison with other works

	Bandyopadhyay [JSSC 2012]	Wang [JSSC 2016]	Kim [TPE 2013]	Shao [TVLSI 2009]	This Work
Load Power Range	2.5 -10 mW	0-120 mW	-	-	0-126 mW
PV Voltage Range	0.15-0.75 V	1.5-5.5 V	1.5-5V	-	0.18-5.5V
Architecture	Dual-path Boost	Dual-path Buck	Buck	Switch-capacitor	Dual-path Buck-boost
Process	0.35 µm CMOS	0.5 µm CMOS	0.35 µm BCDMOS	0.35 µm CMOS	0.18 µm BCDMOS

Chapter 5: Conclusions

The proposed energy harvesting circuit used a synchronous dual-input dual-output non-inverting buck-boost converter operating in discontinuous conduction mode with constant on-time pulse skipping control scheme to achieve impedance match. The circuit achieved maximum power point tracking by utilizing sensor-less time-based power monitor technique to achieve fully digitalized controller.

In order to achieve better and simpler MPPT circuit, P&O and FOCV methods was combined to achieve wider search region with relative accuracy.

The proposed power management circuit was design in Cadence and layout in TSMC BCDMOS 180 nm technology. Post-layout simulations were performed to provide the evidence for the functionality of the IC post-fabrication.

5.1 Key Contributions

The proposed circuit design outlines an architecture for a synchronous dual-input dual output non-inverting buck-boost converter operating in discontinuous conduction mode with constant on-time pulse-skipping modulation control scheme. The new MPPT method is proposed in this work. Both P&O and FOCV methods are combined in order to have one large universal search window.

5.2 Future Work

Once the IC returns from foundry, the chip should be carefully tested to further verify the functionality of the whole chip. As far as the circuit design, there are few aspects where the design can be further improved.

- First, the MPPT can be further improved. The current version of the proposed circuit is based on the condition that environment will not be changed much. If there is a case that environment will change a lot. The maximum power point that the circuit found may not be optimal anymore. The circuit should reinitiate the search process by adding other constraints to regularly check whether the environment change significant or not.

- Second, the current search resolution is 5%. However, the current design will trade off between resolution and power dissipation. Possibly, other method can be tried to have good comprise of better accuracy and power dissipation.

- Third, the power stage can be further improved such as optimal power switch size and its corresponding drive size. There is an optimal balance point between switch conduction, switching loss and gate driving loss. Other topology or control scheme may be tried such as [18]. Thus, the power switches number can be reduced to save more chip area and power dissipation on the switches.

- Forth, the digital circuit part may be further simplified to reduce the number of logic gate it uses to reduce the power dissipation.

- Fifth, the clocked comparator can be improved from many aspects such as rail-to-rail input range, lower offset, faster evaluation and recover speed, lower propagation delay.

Appendix

A.   Sensor-less Time-based Power Monitor

The sensor-less time-based power monitor is further explained in this section. The derivation of the relationship between input power and off-time pulse-width t_{off} is referred [3, 17]. Consider the PV input and primary capacitive output CL in the Figure A-1. The average input power can be expressed as (A.1). For buck-boost converter, the off-time of primary output follows (A.2), where t_{on_PV} is the pulse width of PV on-time or inductor charging time.

$$P_{IN} = V_{PV} \cdot \overline{I_{IN}} \tag{A.1}$$

$$t_{off\_prim} = \frac{V_{PV} \cdot t_{on\_PV}}{V_{CL}} \tag{A.2}$$

The average input current can be derive based on the integral of current, and period shown in the Figure A-2. The average input current can be expressed as (A.3).

$$\overline{I_{IN}} = \frac{V_{PV} \cdot t^2_{on\_PV} \cdot f_s}{2L} \tag{A.3}$$

By using (A.1), (A.2), (A.3), the average input power can be derived at

$$P_{IN} = \frac{V^2_{PV} \cdot t^2_{on\_PV} \cdot f_s}{2L} \tag{A.4}$$

By rearranging (A.2) to express t_{on_PV} in terms of t_{off_prim}, we obtain

$$P_{IN} = \frac{V^2_{CL} \cdot t^2_{off\_prim} \cdot f_s}{2L} \tag{A.5}$$

By rearranging (A.5), we obtain

$$t_{off\_prim} = \frac{1}{V_{CL}} \cdot \sqrt{\frac{2 \cdot L \cdot P_{IN}}{f_s}} \tag{A.6}$$

By looking at (A.6), one can conclude that if primary output is regulated, and switching frequency and inductance is fixed. Pulse width of primary output discharge time is direct

proportional to the square root of average input power. We can use this relationship to measure input power by measuring time information and quantize the power into digital domain.
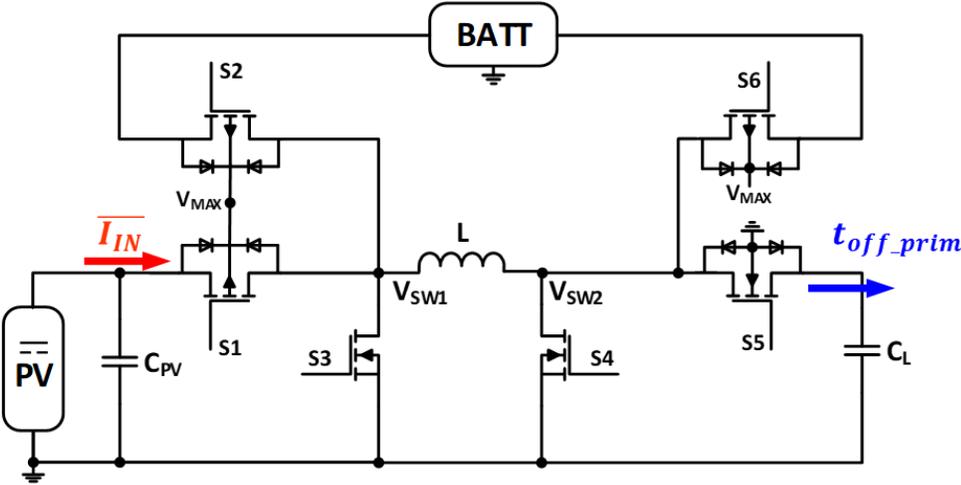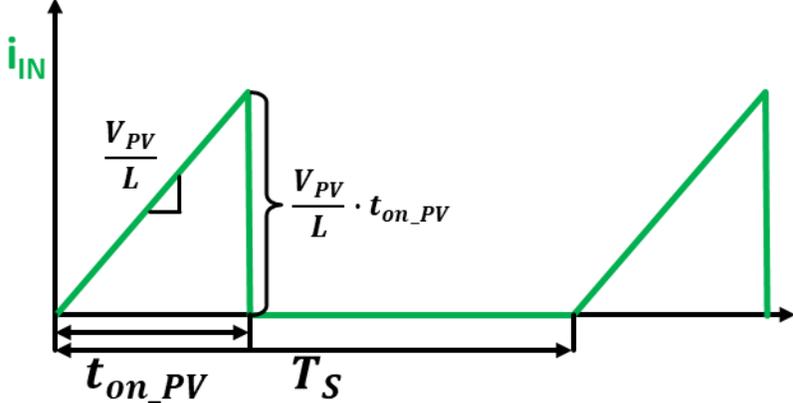

Figure A-1 Power stage Diagram

Figure A-2 Input current waveform for PV as input

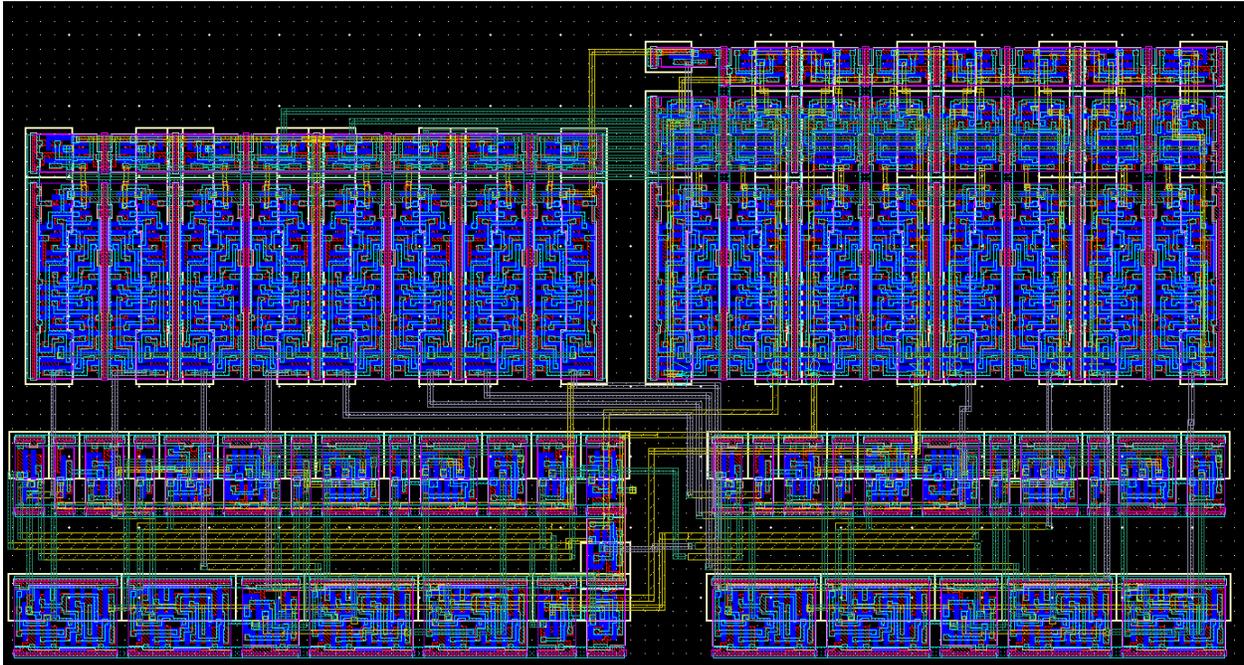# B.   Layout of Component Blocks
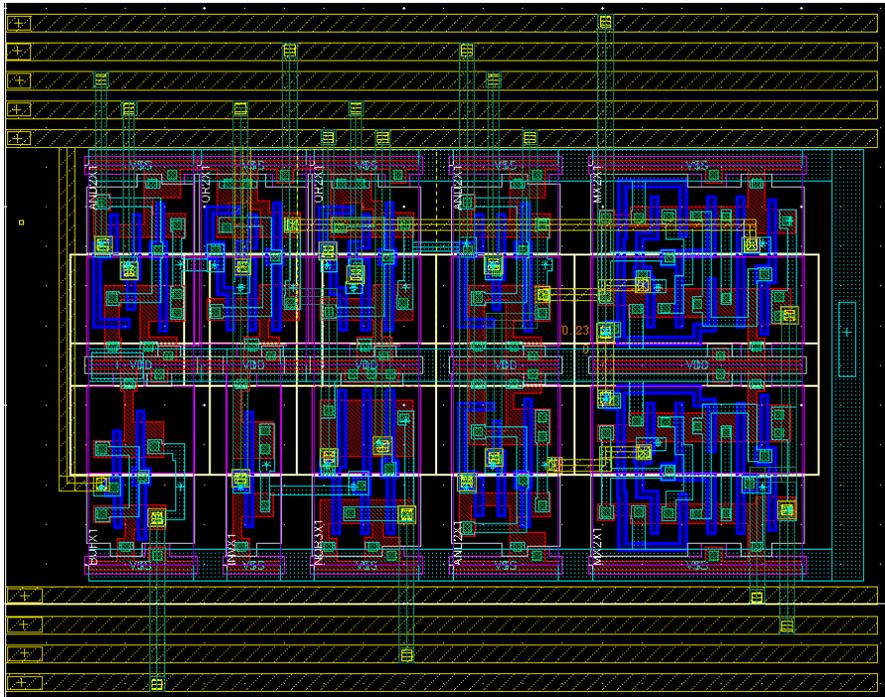

Figure B-1 8-bit Sample/Store/Comp Unit
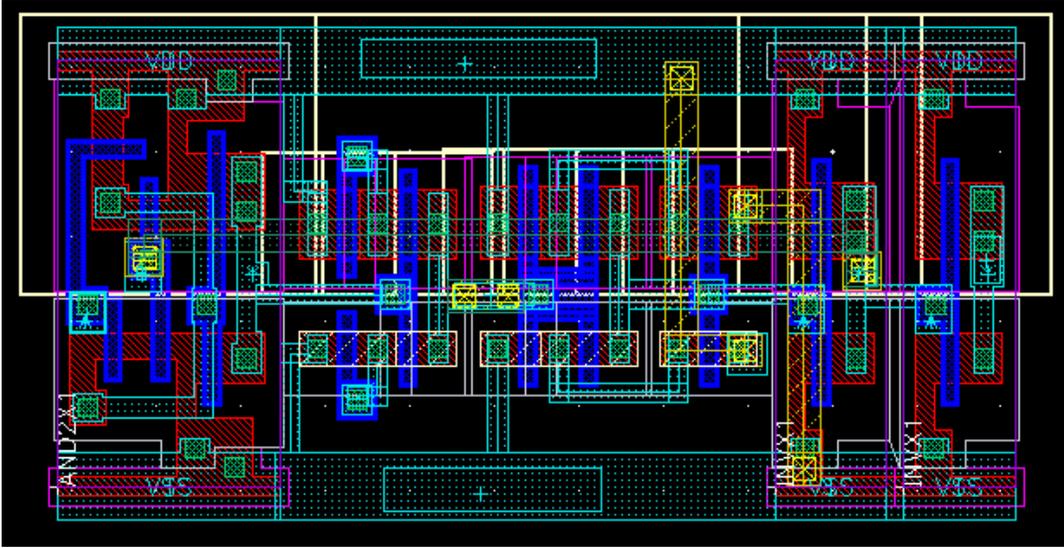

Figure B-2 I/O Configuration

Figure B-3 Ring Oscillator
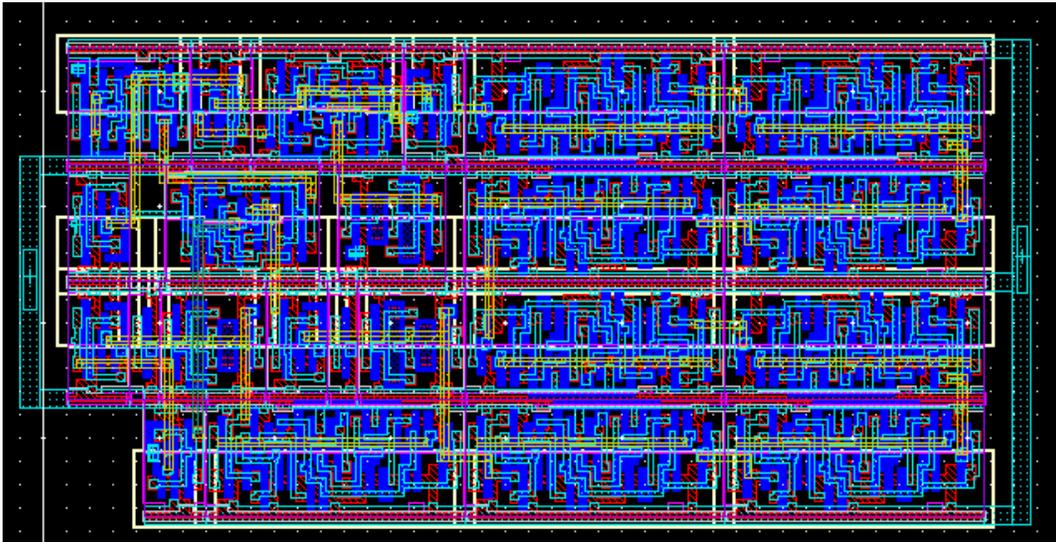
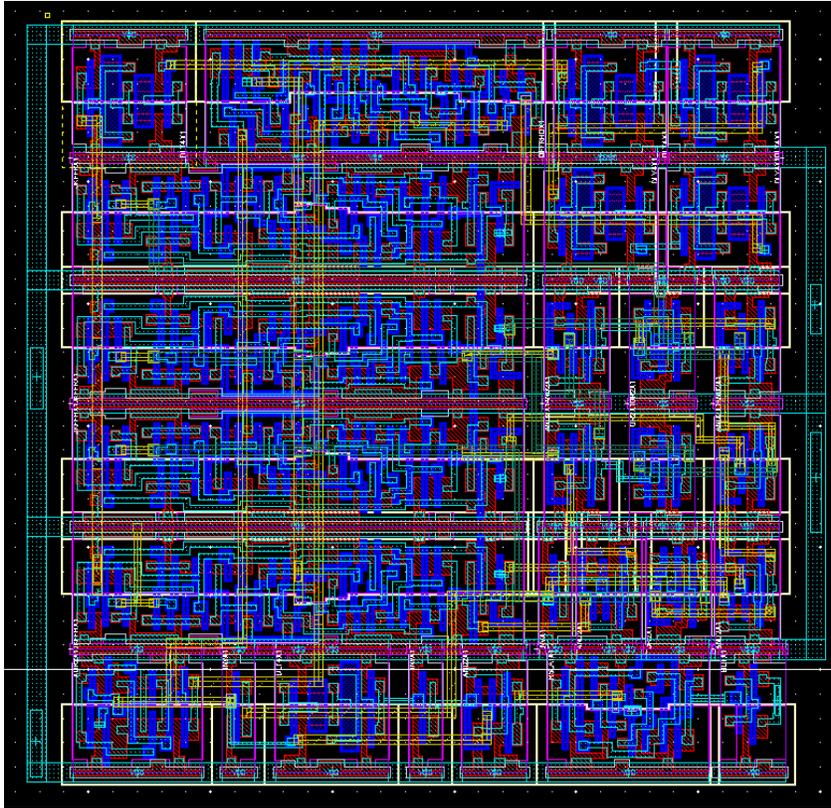Figure B-4 Sampling CLK Generation Block
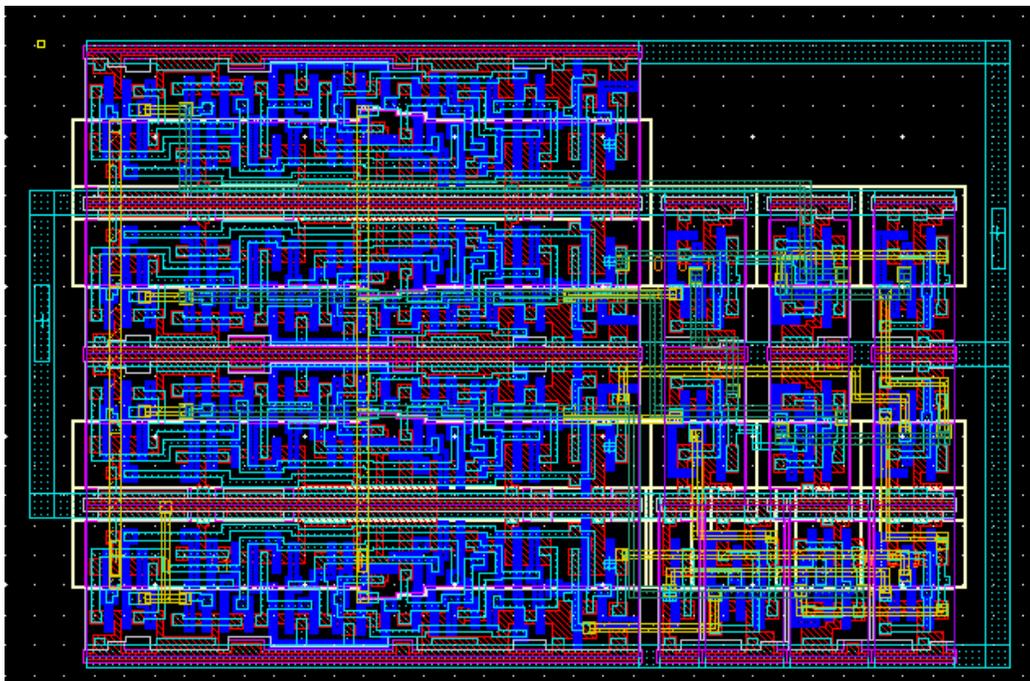
Figure B-5 P&O Logic Block
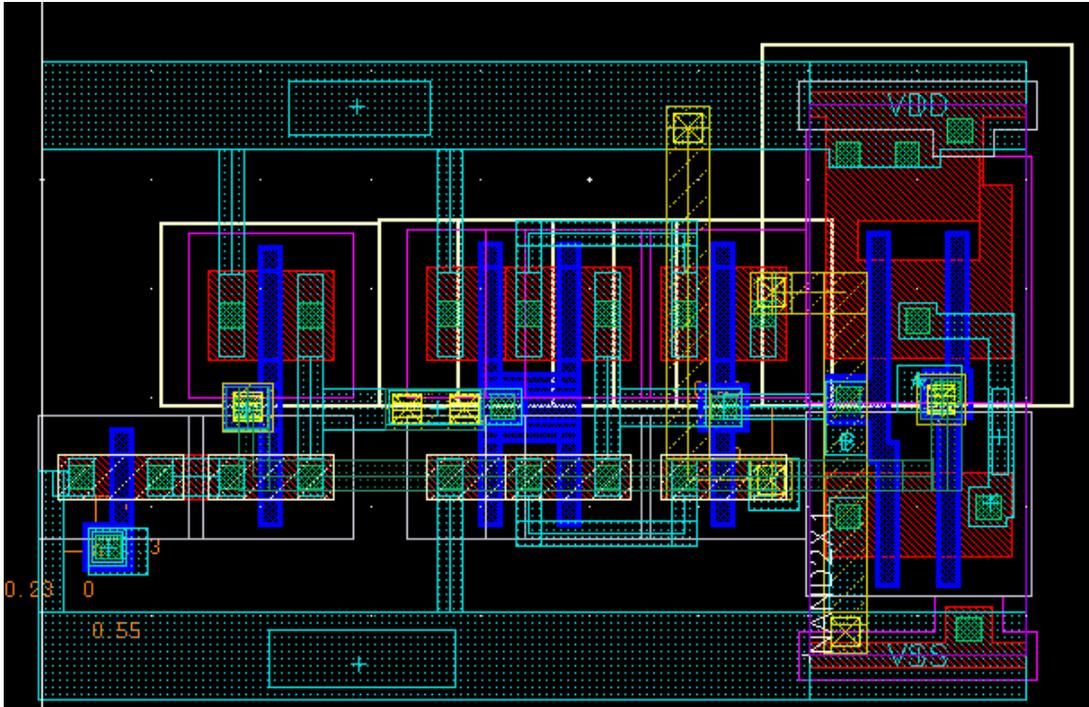

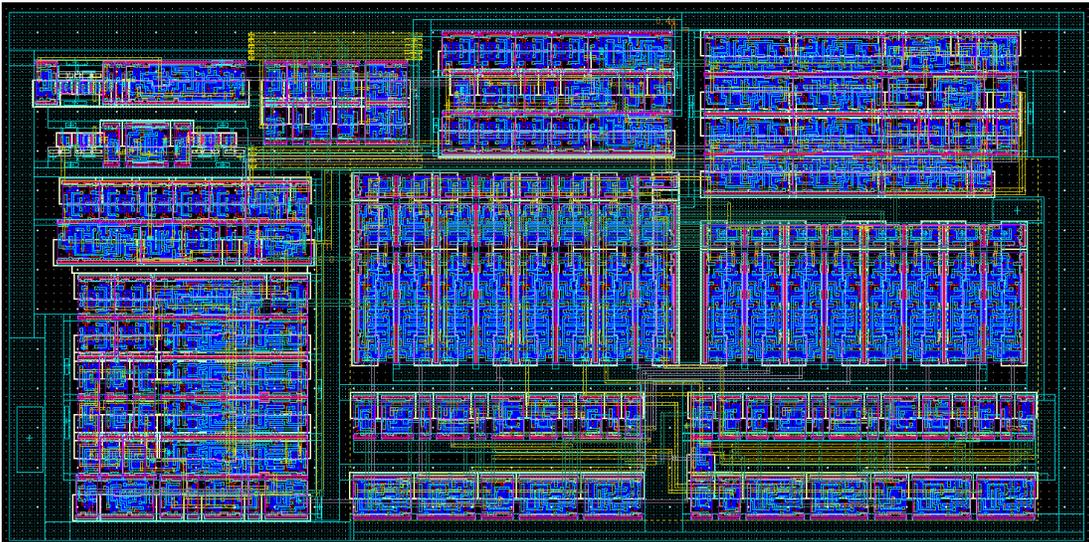Figure B-6 4-bit Up/down Counter

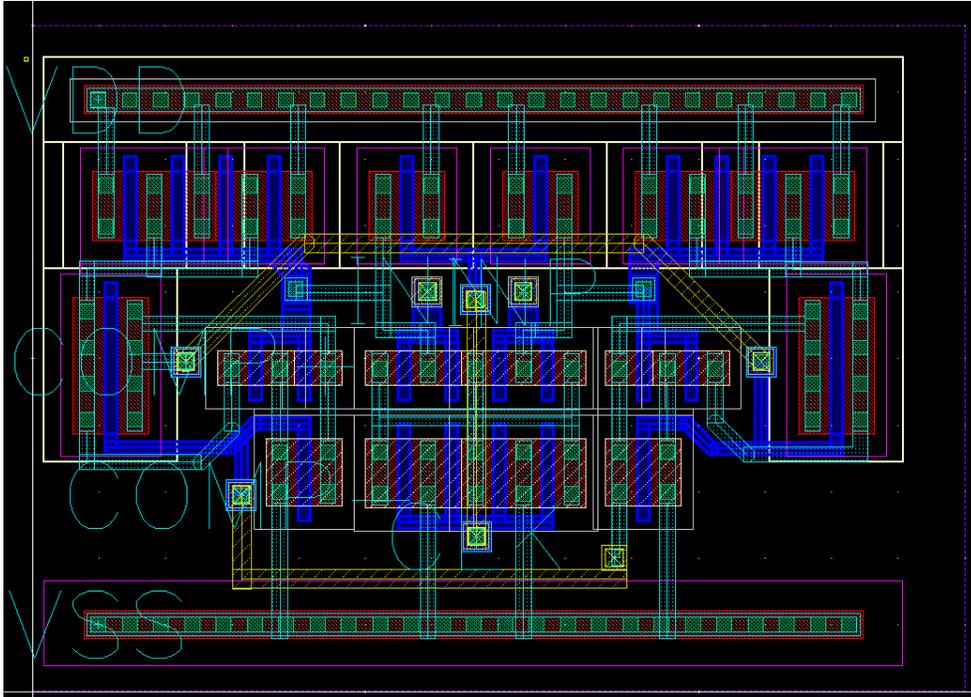Figure B-7 On-time Generation Block

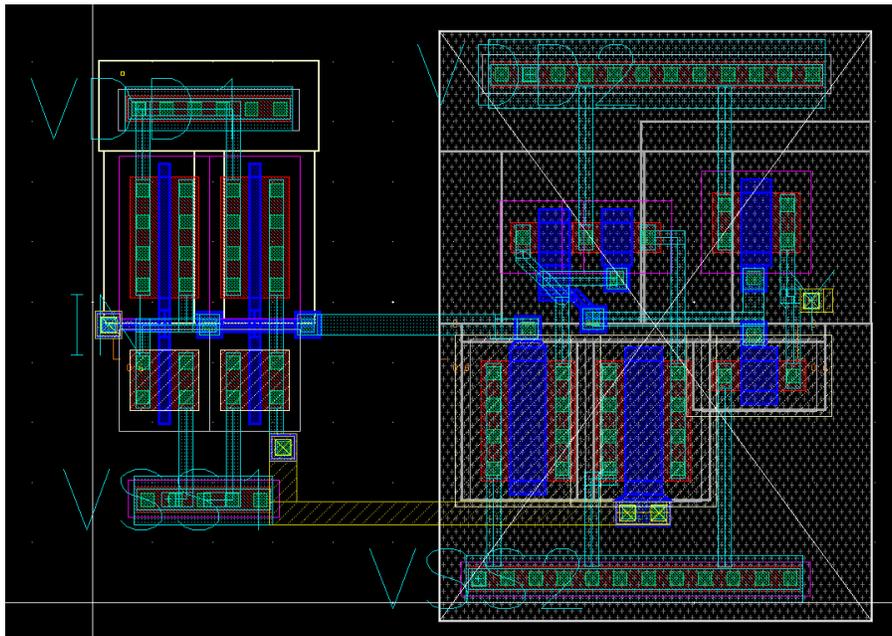Figure B-8 Digital Core

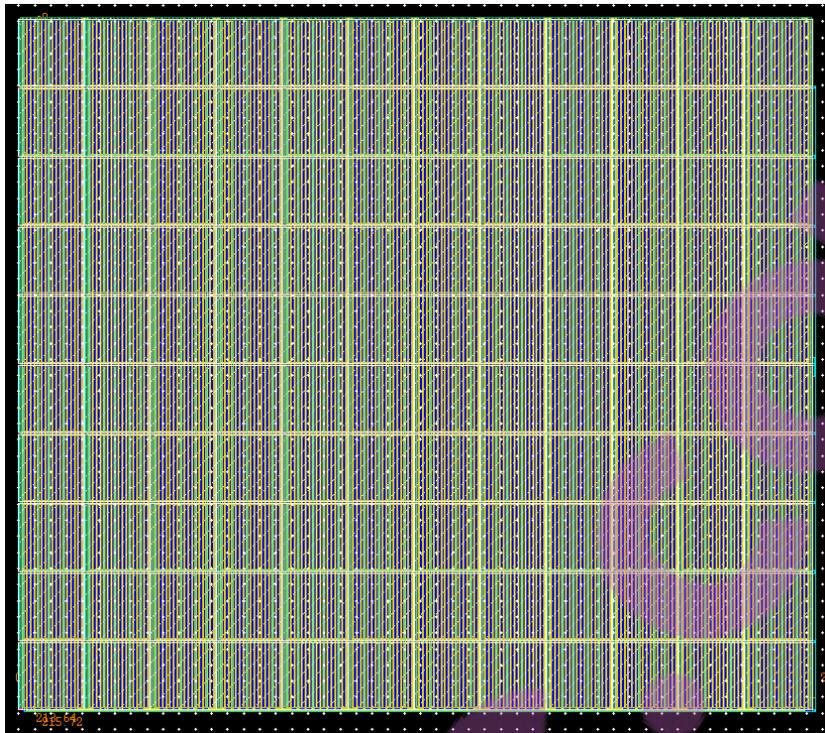Figure B-9 Clocked Comparator

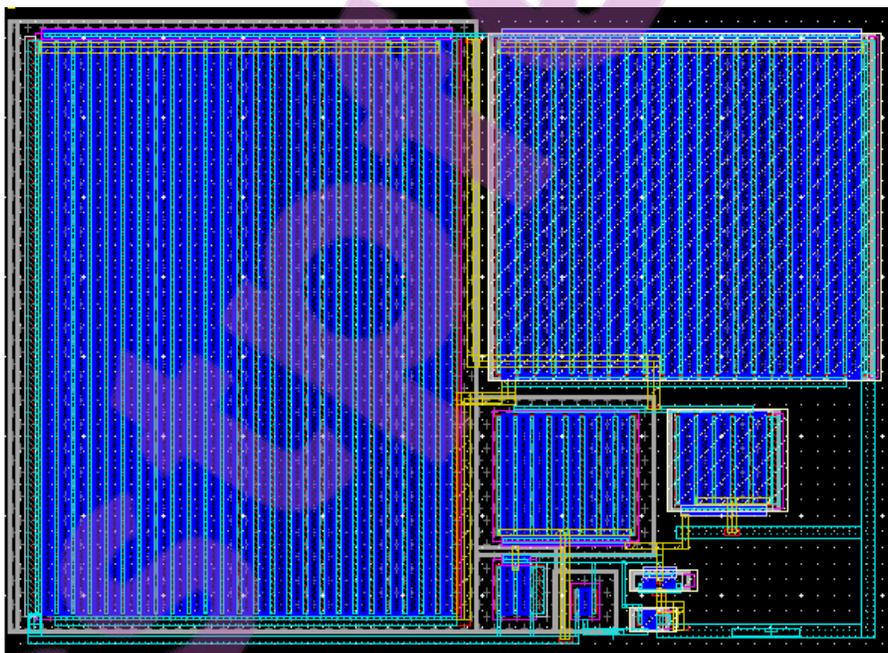Figure B-10 Level Shifter

Figure B-11 Power Switch

Figure B-12 Gate Driver

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