Table of Contents

List of Figures

List of Tables

Nomenclature

Acronym

ADC	-	Analogue to digital converter
ASIC	-	Application-specific integrated circuit
BiVAD	-	Biventricular assist device
CPT	-	Capacitive power transfer
ESR	-	Equivalent series resistance
FPGA	-	Field-programmable gate array
IPT	-	Inductive power transfer
IRH	-	Implantable replacement heart
ISHLT	-	The International Society for Heart & Lung Transplantation
LVAD	-	Left ventricular assist device
LDO	-	Low-dropout regulator
MATLAB	-	Matrix Laboratory
PI	-	Proportional and integral control
PLECS	-	Piecewise Linear Electrical Circuit Simulation
PSoC 5	-	Programmable embedded system-on-chip 5
REMATCH	-	Randomised Evaluation of Mechanical Assistance for the Treatment of Congestive Heart Failure
RVAD	-	Right ventricular assist device
RF	-	Radio frequency
SC-PPRC	-	Split capacitor push-pull parallel resonant converter
SR	-	Set-reset latch
TAH	-	Total artificial heart
TET	-	Transcutaneous energy transfer
VAD	-	Ventricular assist device
VCO	-	Voltage controlled oscillator
VHDL	-	VHSIC hardware description language
VHSIC	-	Very-high-speed integrated circuit
ZVS	-	Zero voltage switching

Symbols

A	-	Device area
C_p	-	Primary resonant capacitance
C_s	-	Secondary resonant capacitance
D_A	-	Blocking diode A
D_B	-	Blocking diode B
f_{lower}	-	Lower frequency limit (middle ZVS operation)
f_{offset}	-	PI frequency level shifting offset
f_{sw}	-	Switching frequency
f_{toggle}	-	Frequency to reset toggle variable
f_{upper}	-	Upper frequency limit (middle ZVS operation)
f_{zvs}	-	Zero voltage switching frequency
f_{zvs0}	-	Single ZVS frequency point before bifurcation
f_{zvs1}	-	Lower zero voltage switching frequency point
	-	Upper frequency boundary
f_{zvs2}	-	Middle zero voltage switching frequency point
f_{zvs3}	-	Upper zero voltage switching frequency point
f_0	-	Nominal frequency
k_c	-	Critical magnetic coupling level
$k_{\max}$	-	Maximum magnetic coupling level
G'_A	-	Basic mode gate drive signal for MOSFET Q_A
G'_B	-	Basic mode gate drive signal for MOSFET Q_B
G_A	-	Enhanced mode gate drive signal for MOSFET Q_A
		Gate drive signal for MOSFET Q_A
G_{A_RST}	-	Reset trigger from falling edge of G_A
G_B	-	Enhanced mode gate drive signal for MOSFET Q_B
		Gate drive signal for MOSFET Q_B
i_{in}	-	Primary input current

I_L	-	Load current
i_{Lp}	-	Primary resonant coil current
i_{Ls}	-	Secondary resonant coil current
i_{L1}	-	Current through DC inductor L1
i_{L2}	-	Current through DC inductor L2
I_{rms}	-	Root mean square current through MOSFET
i_z	-	Zener bias current
I_p	-	Primary resonant coil current
I_s	-	Secondary resonant coil current
L_p	-	Primary resonant inductance
L_s	-	Secondary resonant inductance
M	-	Mutual inductance
P_L	-	Load power
P_{Loss}	-	System power loss
Q	-	Quality factor
Q_A	-	Low side MOSFET A
Q_B	-	Low side MOSFET B
Q_g	-	Total gate charge
Q_p	-	Loaded primary side quality factor
Q_s	-	Loaded secondary side quality factor
Q_u	-	Unloaded quality factor
R	-	Equivalent load resistance seen by resonant tank
R_{Cp}	-	Primary resonant capacitor ESR
R_{Cs}	-	Secondary resonant capacitor ESR
$R_{ds(ON)}$	-	MOSFET ON state resistance
R_{eq}	-	Equivalent load resistance seen by resonant tank

R_{esr}	-	Equivalent series resistance of resonant coil
R_{in}	-	Input resistance
R_{Lp}	-	Primary coil ESR
R_{Ls}	-	Secondary coil ESR
R_{LOAD}	-	Load resistance
R_{L1}	-	ESR DC inductor L1
R_{L2}	-	ESR DC inductor L2
R_z	-	Zener bias resistor
T_{sh}	-	Resonant shorting period
T_{sw}	-	Switching period
T_{zc}	-	Zero crossing period
V_{AB}	-	Differential resonant tank voltage
$\hat{V}'_{AB}$	-	Differential resonant tank voltage peak
V'_A	-	Drain to source voltage of MOSFET Q_A
V_A	-	Comparator result of V'_A to ground
V_{A_SET}	-	Set trigger from falling edge of V_A
V_{A_DELAY}	-	Delay pulse with reference to V_A
$V_{A\_D\_SET}$	-	Set trigger from falling edge of V_{A_DELAY}
V'_B	-	Drain to source voltage of MOSFET Q_B
V_B	-	Comparator result of V'_A to ground
V_{B_SET}	-	Set trigger from falling edge of V_B
V_{B_DELAY}	-	Delay pulse with reference to V_B
$V_{B\_D\_SET}$	-	Set trigger from falling edge of V_{B_DELAY}
v_{Cp}	-	Primary resonant capacitor voltage
v_{Cs}	-	Secondary resonant capacitor voltage
V_{CT}	-	Shows presence of instant capacitor shorting
V_{CT+}	-	Current transformer positive output terminal

V_{CT-}	-	Current transformer negtive output terminal
$V_{\mathrm{CT\_stop}}$	-	Shows presence of instant capacitor shorting
V_{Comp}	-	Waveform for comparator to process
$\hat{v}_{ac}$	-	Secondary resonant tank voltage peak
v_{Cs}	-	Secondary resonant capacitor voltage
v_{out}	-	Output voltage
V_{ref}	-	Reference voltage for PI control
V_{diode}	-	Feedback reflecting the error to ZVS operation
V_{diode_ref}	-	Reference level for V_{diode} for regulate to
V_{diode_SET}	-	Set trigger from rising edge of V_{diode}
$V_{direction}$	-	Determines direction for PI control
V_{LOAD}	-	Load voltage
V'_{LOAD}	-	Stepped down version of V_{LOAD}
V_{sh_ref}	-	Shorting period reference
V_{sh}	-	Resonant shorting period represented by a voltage level
V_{ds}	-	Drain to source voltage of MOSFET
V_{in}	-	Input dc voltage
V_{IN}	-	Input dc voltage
V_{G}	-	Gate source voltage
V_{rms}	-	Resonant tank root mean square voltage
V_{oc}	-	Voltage induced at secondary
V_{r}	-	Reflected voltage at primary
$V_{\mathrm{Res\_shrt}}$	-	Shows presence of resonant shorting period
$V_{\mathrm{Res\_shrt\_ref}}$	-	Reference for $V_{\mathrm{Res\_shrt}}$ to compare with
V_{pk}	-	Resonant tank peak voltage
V_{z}	-	Zener voltage

Z_p	-	Resonant tank input impedance
Z_{sr}	-	Secondary impedance reflected to the primary
Z_s	-	Secondary impedance
ω	-	System frequency in radians
ω_0	-	Nominal frequency in radians
θ	-	Negative region of V'_B in radians
η	-	End-to-end efficiency

Chapter 1

Introduction

1.1. Background

Implantable medical devices have the potential to change a clinical condition almost instantly. One example is the use of a left ventricular assist device to restore blood flow when the natural heart is unable to maintain the flow rates required. Other examples of smart devices include pacemakers, nerve stimulators and drug pumps. These devices all require electrical power to operate, and the provision of power is a critical aspect of their design. This thesis addresses the issue of providing substantial power – sufficient for a heart pump operating continuously – for the remaining lifetime of a patient. The basis of what this thesis proposes is the use of inductive coupling and a magnetic field to move power from outside the body to inside. The key challenges are related to alignment of components and avoidance of any heating problems. New power electronic techniques have been developed to address these issues.

One current medical problem is that there are about 4.7 million Americans alone with heart failure, and each year 550,000 new cases appear, costing $10 to $40 billion annually [1]. Figure 1-1 shows reported heart transplantation by year (data collected by the International Society for Heart & Lung Transplantation (ISHLT)). This data shows only 3742 reported heart transplants in 2009, with a previous annual record maximum of only 4841 in 1993. The lack of available heart donors [2, 3] means that there is a good opportunity for heart assist devices to be researched and developed for medical use. There are different types of heart assist devices, depending upon the location of an operation within the heart; for example the left ventricular assist device (LVAD), right ventricular assist device (RVAD) or biventricular assist device (BiVAD). All of these are different from a ‘total artificial heart’ (TAH) whereby the heart is completely replaced by the device. Patients may be given a temporary mechanical circulatory support in the lead up

to a heart transplantation, as shown in Figure 1–2, the percentage of adult transplants bridged by mechanical circulatory support is on the rise: from 22% in 2006 to around 32% in 2009. The mechanical circulatory support in Figure 1–2 includes LVAD, RVAD or TAH. LVAD is the most common heart assist device, which operates to help the left ventricle pump blood by pulling blood first through its rotary motor from the left ventricle and then pumping it out into the aorta, which then flows to the rest of the body. Figure 1–1 and Figure 1–2 are related to each other, with the rising number of transplants being bridged by mechanical circulatory support, the total number of transplantation should also increase. Note that bridging means a heart pump is implanted while the patient waits for suitable donor heart and transplantation. Some discrepancy in the data trend could be caused by the limited coverage of the ISHLT registry for number of transplants.

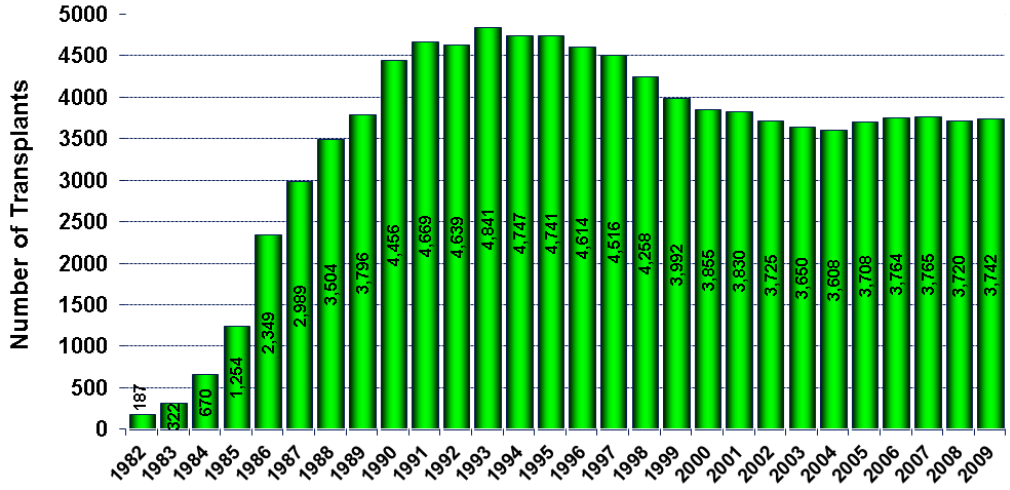


Figure 1–1 The number of heart transplants reported by year according to ISHLT registry [4]

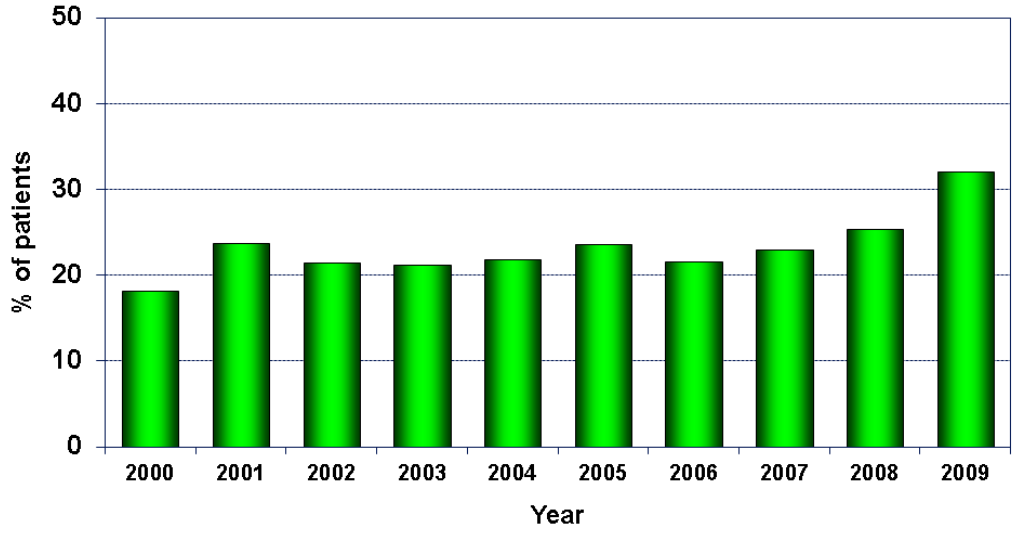


Figure 1–2 Percentage of adult transplantation bridged with mechanical circulatory support [4]

The Randomised Evaluation of Mechanical Assistance for the Treatment of Congestive Heart Failure (REMATCH) trial compared the survival rates for a group of patients who went through either optimal medical therapy or received a LVAD. The result shows that there is a 48% reduction in risk of death for the LVAD group compared with the medical therapy group. The survival rates when comparing the LVAD group to the medical therapy group were 52% to 25% for one year and 23% to 8% for two years. Therefore the use of an LVAD improves patient survival rates, quality of life, and is a good substitute for patients who cannot get heart transplantation [1]. The trial however also showed a need to reduce LVAD infection in order to improve patient survival and reduce morbidity [5].

Heart assist devices are designed to help damaged hearts maintain sufficient blood flow, with short term use required for patients recovering from heart attack or heart surgery and long term use for patients who are suffering congestive heart failure [6]. There are three categories that heart assist devices are used for: as a bridge to recovery, a bridge to transplantation, and as a destination therapy [7]. The ‘bridge to recovery’ use occurs when the device is used temporarily until the patient recovers from acute heart injury; ‘bridge to transplantation’ is when the device is used temporarily until the patient receives a donor heart, while ‘destination therapy’ is when the device is used permanently.

The development of heart assist devices started with the pulsatile pneumatic extracorporeal ventricular assist devices (VAD) and implantable pneumatic total artificial hearts (TAH); then these are followed by pulsatile electromechanical implantable devices. By 1998 continuous flow rotary blood pumps were introduced and soon these are followed by hydrodynamically and magnetically levitated rotary pumps [8, 9]. The future aim is a transcutaneous energy transfer (TET) based rotary pump total artificial heart device [10].

Heart pumps typically require 10W to drive their motors to create blood flow, and this power is delivered through a percutaneous driveline from external batteries. The percutaneous drive line provides a reliable, highly efficient method of getting the power from outside the body to the heart pump motor controller, but its major drawback is its requirement for penetration through the skin and the associated risks of infection (an example is given in Figure 1–3). A percutaneous driveline is the industry standard solution to power heart pumps. Figure 1–4 and Figure 1–5 show the HeartMate II LVAD

[11, 12] and the HeartMate XVE LVAD [7] from Thoratec Corporation respectively. Other examples include the Jarvik 2000 Heart from Jarvik Heart [13], MiFlow™ VAD from WorldHeart Corporation [14], HeartAssist 5© from MicroMed Cadiovascular, Inc. [15], INCOR® from Berlin Heart [16] and HVAD® pump from HeartWare International, Inc. [17].

Figure 1–3 The driveline exit site can lead to infections [11]

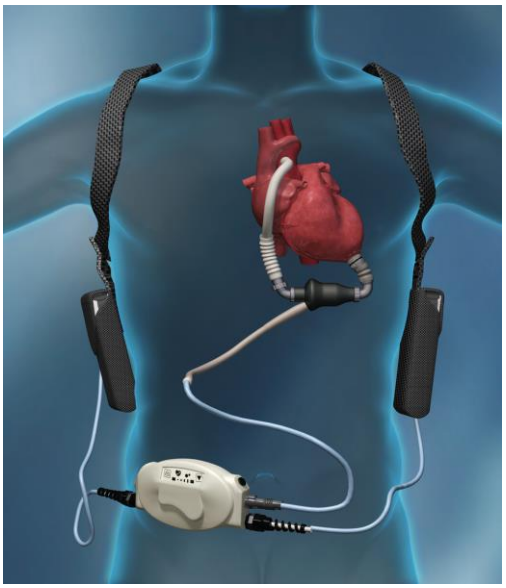


Figure 1–4 HeartMate II left ventricular assist device (LVAD) [11]

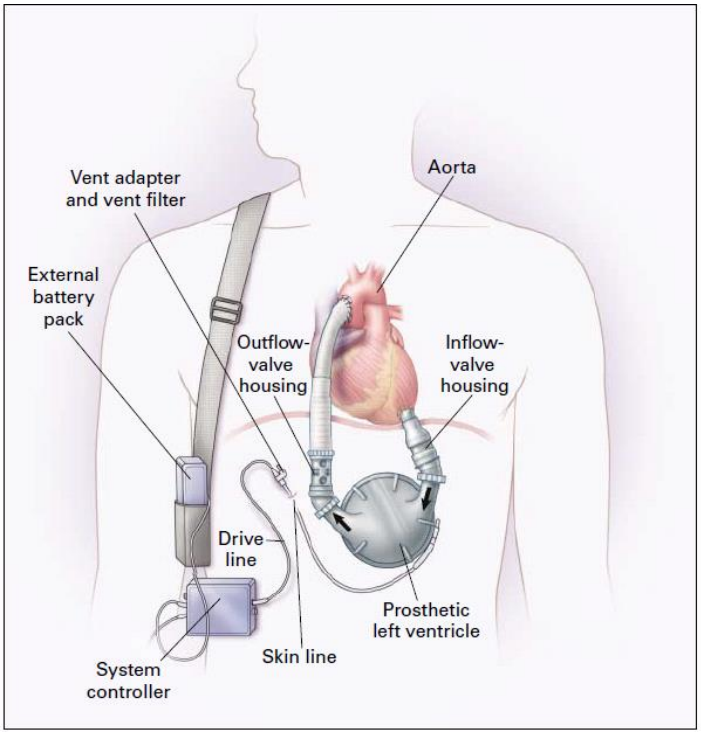


Figure 1–5 Components of the HeartMate XVE LVAD [7]

Table 1–1 Location of infections from INTERMACS (June 2006-Sept 2008)[18]

Location*	n	% of 682
Pump related		
drive line	140	21%
pump pocket	51	7%
pump interior	3	0.4%
Line sepsis	46	7%
Mediastinum	18	3%
Peripheral wound	22	3%
Pulmonary	116	17%
GI	39	6%
Urinary tract	111	16%
Positive blood cultures	218	32%
Other	100	15%
Unknown	7	1%
Total	682	

*More than one location can exist for one identified infection

The Interagency Registry for Mechanically Assisted Circulatory Support (INTERMACS) collects data on patients using VAD support. Holman *et al.* [18] have analysed the registry data from 2006 to 2008, and Table 1–1 shows that out of the total 682 device-related infections, 21% are driveline related. The driveline breaks the skin and the torque generated by everyday patient movements and the weight of the battery can damage this chronic wound, leading to relapsing infections and patient mortality. The initial driveline infection can spread elsewhere and cause bloodstream infection, recurring bacteraemia and device endocarditis [19]. Over time, driveline infections are very difficult to control

despite on-going efforts to treat them [20]. Eliminating this percutaneous driveline could significantly reduce the number of adverse infection effects [21].

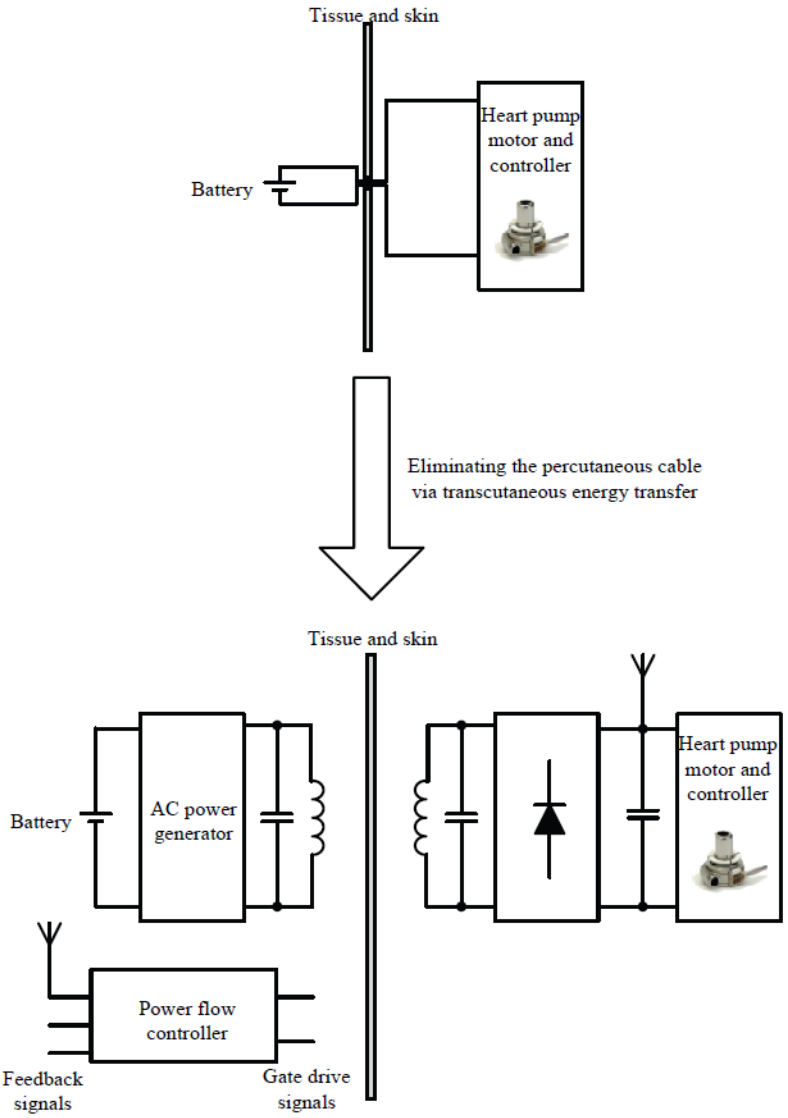


Figure 1–6 Removal of percutaneous cable

Transcutaneous energy transfer (TET) can eliminate the percutaneous driveline and its associated infection risks. Figure 1–6 compares a system before and after the removal of its percutaneous driveline.

The enthusiasm for TET is based on being able to supply energy to implanted devices without the need to break the skin barrier. At its most fundamental, TET requires charges that move outside the body to induce charges to move inside the body which can ultimately be used to supply energy to the heart pump. Two practical methods of achieving this are use of either capacitive or inductive coupling.

Capacitive power transfer (CPT) relies on establishing a time-varying electric field between two plates. If one plate were located inside the body and the other outside, then in principle, a TET system could be established. Examples of CPT can be found in work by Chao *et al.* [22, 23]. A challenge for CPT is to align the plates, and to date, no-one has demonstrated the ability to transfer power levels suitable for driving heart pumps (e.g. 10W) using plates small enough to consider implanting (e.g. diameter less than 100mm) over a plate separation distance realistic for patient use (e.g. 10mm).

The alternative approach is to use inductive power transfer (IPT). IPT is a method of delivering wireless power using an external primary coil to generate a magnetic field. The magnetic field passes through the skin and induces current in an implanted secondary coil. IPT also has to deal with the issues of coil alignment and size, but practical solutions for powering heart pumps have been demonstrated. IPT has been developed for a diverse range of applications. High power applications include electric vehicle charging [24-27] and factory material handling [28]. Examples of low power applications include the powering of mobile devices [29, 30], television [31], implantable telemetry sensors [32, 33] and implantable heart pumps [34, 35]. Figure 1–7 shows other implantable medical devices that may be powered by TET, such as retinal implants and implanted cardiac defibrillators [36] that require small amounts of power to operate. In comparison, the artificial heart requires a larger and on-going supply of power for correct operation.

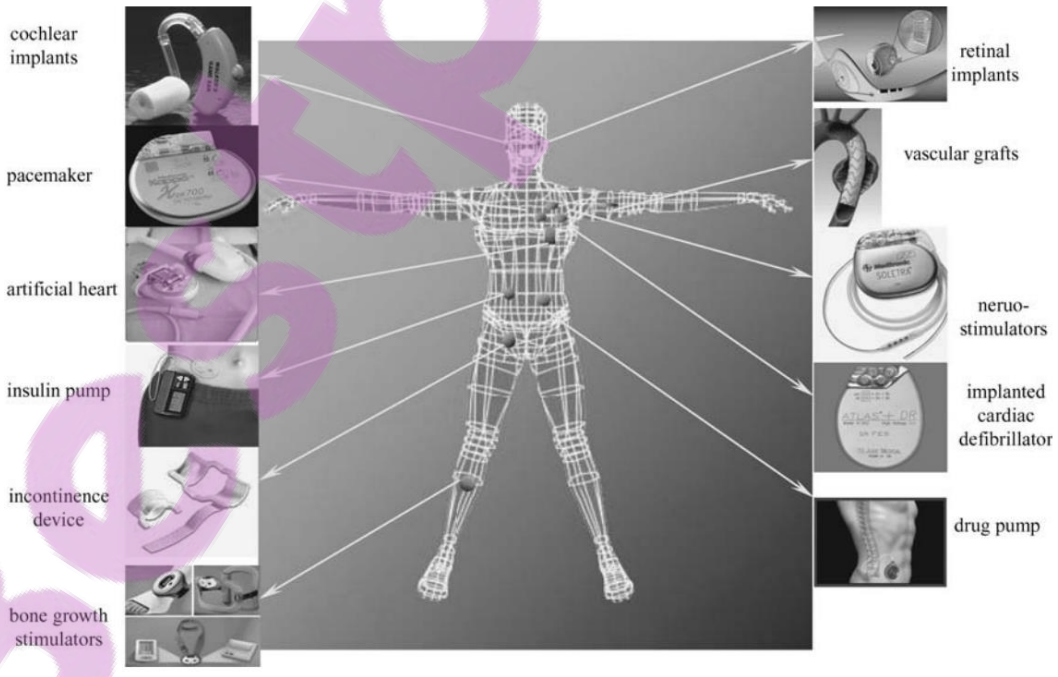


Figure 1–7 Schematic of applications of various implanted medical devices [36]

1.2. Challenges for Transcutaneous Energy Transfer

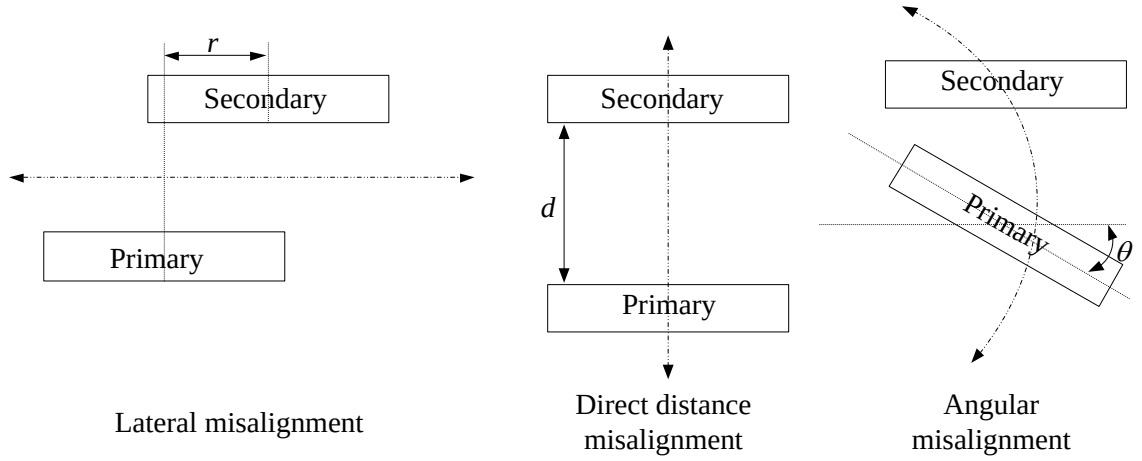


Figure 1–8 TET coil misalignments

The technical challenges for TET systems are power transfer stability, system efficiency and thermal effects [37]. TET coils can have lateral misalignment, direct separation or angular misalignments due to patient movement or tissue regrowth after implantation. These misalignments will result in variations in the magnetic coupling level between the primary and secondary coils. TET systems should be designed to maximise the coil misalignment while maintaining load regulation. Typical TET coil misalignments are depicted by Figure 1–8. Changes to patient or cardiac activity, patient physiological state or heart pump flow rate settings will also result in variations in power demand by the heart pump.

This thesis focuses on extending the system operation ranges, which are the magnetic coupling range, input voltage range and the output power range. Existing TETs have very limited magnetic coupling range, and this is a barrier to power transfer stability. A power flow controller is needed to regulate the heart pump power to compensate for variations in coil separation, in order ensure correct heart pump operation and blood flow rates. The maximum coil separation can be extended by increasing the TET coil size; but this is limited by size requirements for implantation, so the maximum coil separation should be designed for expected changes in tissue regrowth and patient movements, and also be elongated as much as possible through power flow controller designs.

The two other relevant operational ranges are the input voltage and output power ranges. The input voltage range is the boundaries for the input voltage where load regulation is maintained. This is relevant for load regulation when battery supply voltage varies over

use. A TET system can be designed to track its peak power capability so that the required input voltage can be reduced significantly to deliver the same output power. In addition, tracking the system peak capability will boost the output power range. The extent to which the maximum capability is utilised can be controlled by an additional power conditioner. These will be further explained later, in Chapter 5.

The operational range of the system can be improved by reducing power losses. It is always of interest to reduce power losses. Lower power losses are associated with lower temperature levels and which help to prevent thermal damage to the skin. This can be achieved by improving the circuit efficiency.

1.3. Current State of the Art for TET

1.3.1. TET System Overview

A typical TET system has a converter on the primary side to invert a dc voltage into a high frequency ac waveform at the resonant tank. By inductive coupling between the TET coils, a voltage is induced at the secondary resonant tank, and following rectification, dc power is available to the heart pump controller. Power flow controllers must control power switches on the primary or secondary side to achieve load regulation. Different tuning topologies can be employed between the primary and secondary, for example parallel-parallel tuning. Power flow controllers are usually used for load regulation, for example primary side variable frequency control.

1.3.2. Existing TET Systems for Heart Pump Applications

In 1983, an early TET system design by Berson *et al.* transmitted power from an external waist belt to an implanted belt, which then charged an internal battery and powered a heart pump [38]. The downside was a significantly large pickup coil requiring implant space, and the coil's diameter needed to be customised according to the size of each patient's waist (~500mm).

Over the past 30 years, significant advances both in core TET and related technology allowed more reliable products to be made for better end user safety and quality of life. Thoratec announced in 2011 that it would team up with Witricity to develop wireless power transfer systems for their heart pumps [39]. HeartWare, a heart pump manufacturer, announced in early 2012 that it would start developing TET [40].

TET powered heart pumps undergoing clinical trials include Arrow LionHeart [41, 42] and AbioCor® from Abiomed [3, 43, 44]. Other TET based heart pumps undergoing development include the implantable version of Jarvik 2000 Heart [13] and the fully sealed HeartMate II by Thoratec [45]. Examples of clinical trial feedback are as follows: El-Banayosy *et al.* reported two years of clinical experience with the LionHeart which suggested that the system components should be miniaturised [46]. Dowling *et al.* experimented with a TET powered AbioCor implantable replacement heart (IRH) (as shown in Figure 1–9) on cows and have found the TET system adequately powered the device without significant thermal injury [47]. Table 1–2 summarises TET developments by notable heart pump developers.

The advancing technology is also reflected by the number of patents filed in the area of wireless power delivery to heart pumps. For example, patents filed by Abiomed include an internal vibratory alarm for fault detection [48], multiple secondary coils as failure backup [49], battery charging modules [50], an accurate battery charge display system [51] and a TET coil with integrated RF antennas [52]. These technologies would assist in a safer and more user-friendly heart pump system for patient use.

Table 1–2 Existing TET developments in progress by heart pump developers [13, 17, 40, 53-56]

Name of device	Pump type	Flow Rate	Power	TET status
Lion Heart	LVAD	8 L/min	14 W	Ready
AbioCor	TAH	12 L/min	25 W	Ready
Heart Mate II	LVAD	10 L/min	20 W	Developing
Jarvik 2000	LVAD	6 L/min	7 W	Developing
HeartWare	LVAD	10 L/min	5 W	Developing

Figure 1–9 Internal components of AbioCor IRH include the thoracic unit, controller, battery, and TET coil [44]

Table 1–3 Existing TET developments in literature for heart pump applications [57-67]

Authors	Year	Coil		Efficiency	Power
		Diameter	Separation		
Mitamura *et al.*	1990	36 mm	3-8 mm	78 %	24 W
Ghahary *et al.*	1992	66 mm	10-20 mm	72 %	48 W
Bearnson *et al.*	1993	50-100 mm	-	70 %	60 W
Mussivand *et al.*	1996	50 mm	3-10 mm	70 %	50 W
Tsai *et al.*	2000	90 mm, 60 mm	6-18 mm	68 %	36 W
Homma *et al.*	2004	55 mm, 39 mm	-	86 %	60 W
Mizannojehdehi *et al.*	2006	-	10-24 mm	73 %	15 W
Okamoto *et al.*	2009	92 mm, 53 mm	5-15 mm	85 %	20 W
Dissanayake *et al.*	2009	50 mm	10-20 mm	80 %	15 W
Waters *et al.*	2012	31, 59, 59, 28, 9.5 cm	1000 mm	50 %	16 W

Apart from research and development driven by heart pump developers; there are many reports of TET related research in the literature as summarised in Table 1–3. Note that the separation by Waters *et al.* is the distance between the drive resonator and receive implantable resonator, which includes the three other intermediate resonators in between. In 1990, Mitamura *et al.* proposed a complete TET system that includes load power regulation, secondary back-up battery charging and control [57]. As shown in Figure 1–10, Mitamura *et al.* have used voltage-fed full bridge converter with a separate communication channel using frequency-voltage-frequency conversion. An alarm is used

to detect possible dislocation between TET coils, and a switch is used to toggle between TET power and backup battery. The system uses ferrite core (as shown in Figure 1–11) and is capable of delivering 24W at 5mm core separation with 78% overall efficiency. The regulated coil separation ranges from 3 to 8mm.

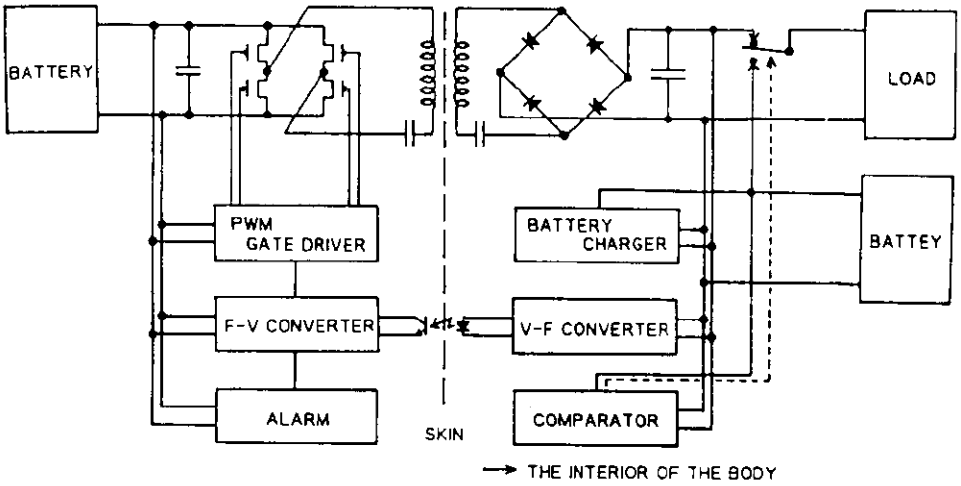


Figure 1–10 A voltage fed full bridge transcutaneous energy transmission system with automatic detection of coil dislocation to switch to backup battery [57]

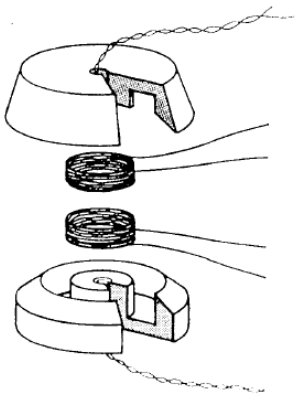


Figure 1–11 Concave/convex core-type transcutaneous transformer [57]

In 1993, Bearnson *et al.* reported that the University of Utah Artificial Heart Research Laboratory had developed a TET system which has a maximum power capability of 60W with 70% efficiency [58]. The TET coils in use were around 50-100mm in diameter. The system operated at 450kHz and an infrared communication link was established in the centre of the coils between the primary and secondary. As shown in Figure 1–12, the system was implanted in a calf; the implanted side contains the heart pump, the internal electronics package, coil and backup battery. The device was successfully implanted in the calf for sixty to ninety days.

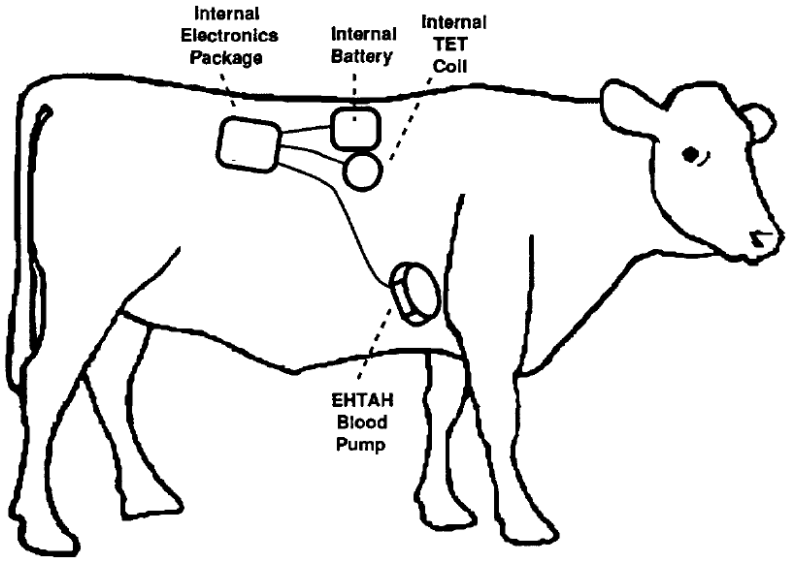


Figure 1–12 Short-term implantable EHTAH system in a calf [58]

In 2004, Homma *et al.* reported a TET powered total artificial heart with a transmission efficiency and maximum power transfer of 86% and 60W respectively [59]. The system used an external coil of 55mm and an implanted coil of 39mm in diameter. A communication channel was established between the primary and secondary side using a transcutaneous optical coupler, and feedback information was then sent for system control.

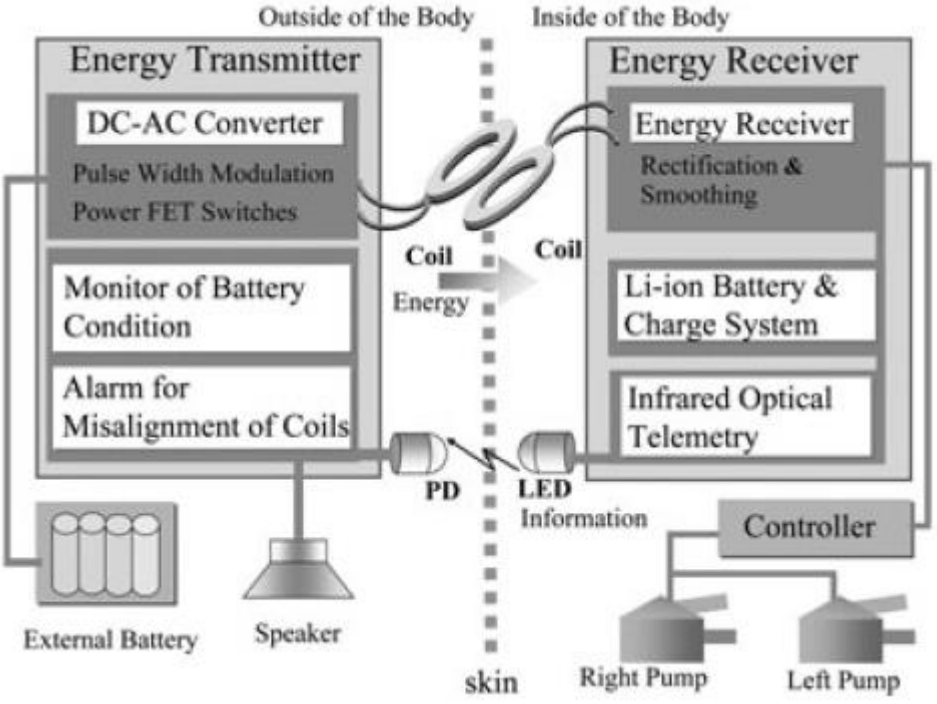


Figure 1–13 Configuration of TET system by Okamoto et al. [66]

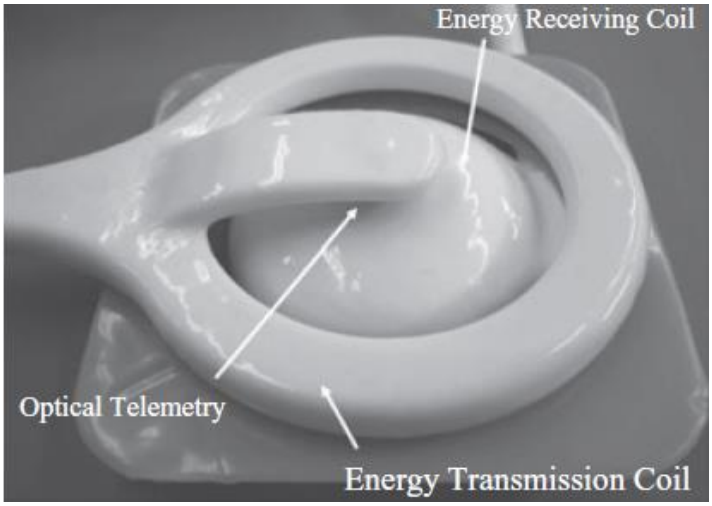


Figure 1–14 Hybrid energy coil at clinical stage [66]

In 2009, Okamoto *et al.* proposed a TET system shown in Figure 1–13, which had internal and external batteries, an alarm for coil misalignment, a monitor of battery condition and infrared communications. The transmitting and receiving coils are shown in Figure 1–14, where the primary is an air core of 92mm outer diameter and 70mm inner diameter, and the secondary is made partly of ferrite compounds. The system can deliver 20W at 85% efficiency with a skin thickness of 5mm-15mm [66].

1.3.3. Power Flow Controllers to Compensate for Variations in Coil Misalignment

Power flow controllers are necessary to maintain output power stability; their objective is to maintain the power as required by the heart pump while dealing with the prevailing misalignment of the TET coils. Different topologies can be applied on either the primary or secondary side to achieve load regulation. It is normal to focus controller functions on the primary side to make the implanted secondary side as simple, small and reliable as possible.

1.3.3.1. Primary Side Input Voltage Magnitude Control

In 2005, Wang *et al.* employed a Class-E topology as shown in Figure 1–15 with adjustable input supply voltage through a buck dc-dc converter to regulate load power. The coil separation is between 7 to 15mm, and the system is also capable of communicating between the primary and secondary. However, the power level is very low (250mW) [68, 69].

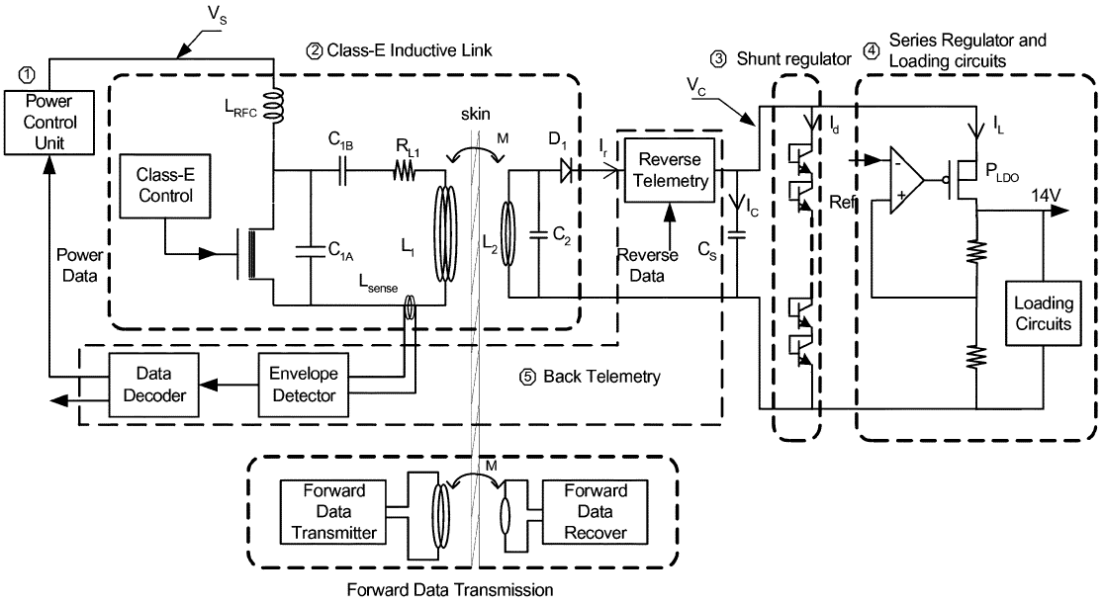


Figure 1–15 Dual-band telemetry system circuit architecture [68]

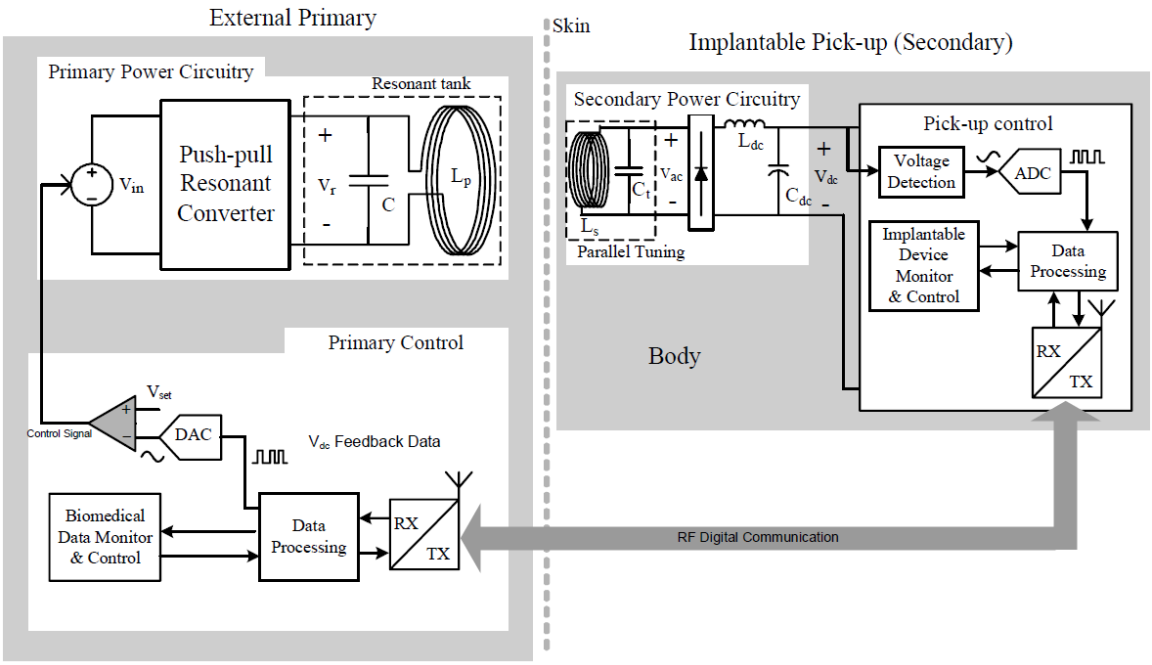


Figure 1–16 Wireless power supply system with magnitude control from external primary side [70]

In 2007, Si *et al.* proposed a simple approach to regulating load voltage by variable input voltage to the primary controller. If the load voltage decreases from a set point, the primary controller increases the applied voltage to its resonant converter. This approach has been used to energise telemeter systems implanted in a laboratory rat. By varying the input voltage, this TET based system can deliver a regulated 7V to the biomedical device at any location in the animal cage ($55\times30\times20\text{cm}^3$). The primary coil loop is large and is wound around the animal cage in which the secondary pickup is placed [70]. Figure 1–16

shows the magnitude control method – the system has a push-pull resonant converter driving a parallel tuned primary resonant tank and a parallel tuned secondary resonant tank. Device monitoring, control and data processing occur at the primary and secondary, which are linked by an RF digital communication channel. The feedback then controls the magnitude of the input voltage level to converge output voltage to a pre-set reference.

Also in 2007, McCormick *et al.* presented a novel method of powering an implantable telemetry device over a large area using multiple coils. It is however designed to power implantable devices in laboratory mice in a cage. In this example, the power delivered is only 100mW, and the distance between primary and secondary coils is up to 50mm [32]. Figure 1–17 shows how the system uses an H-Bridge or full bridge inverter connected to multiple resonant tanks with different resonance frequencies. Labview ensures that the correct coil is operating at all times; Labview then controls the load power using the buck converter. The buck converter essentially varies the magnitude of input voltage to the H-Bridge converter, which then controls the system power flow.

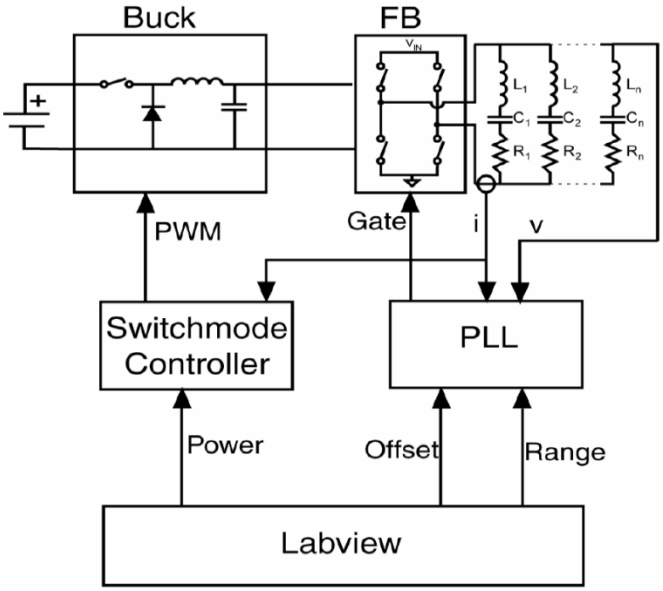


Figure 1–17 Block diagram of inverter and controller [32]

1.3.3.2. Primary Side Frequency Control

Primary side frequency control is a key method discussed in detail in Chapter 3 and 4. The method requires an understanding in the bifurcation of zero voltage switching frequency (ZVS), details of which can be found in Chapter 2 and further analysis are in works by Tang *et al.* [71] and Wu *et al.*[72].

In 1992, Ghahary *et al.* presented a frequency controlled full-bridge series resonant power converter for TET, to deliver 12-48W regulated power across an air gap of 1-2cm with a maximum efficiency of 72% [61].

In 1993, Mussivand *et al.* used a Class-E converter with frequency auto-tuning according to the phase difference between voltage and current of the primary switch as shown in Figure 1–18 [73]. Later in 1996, Mussivand *et al.* proposed another TET system that uses a separate infrared communication channel to transfer load voltage level back to primary, which then adjusts the load power by pulse-skipping and frequency variations [64]. The system was able to deliver 50W with 70% and have a regulated coil separation range from 3 to 10mm. The TET coil diameter is approximately 50mm.

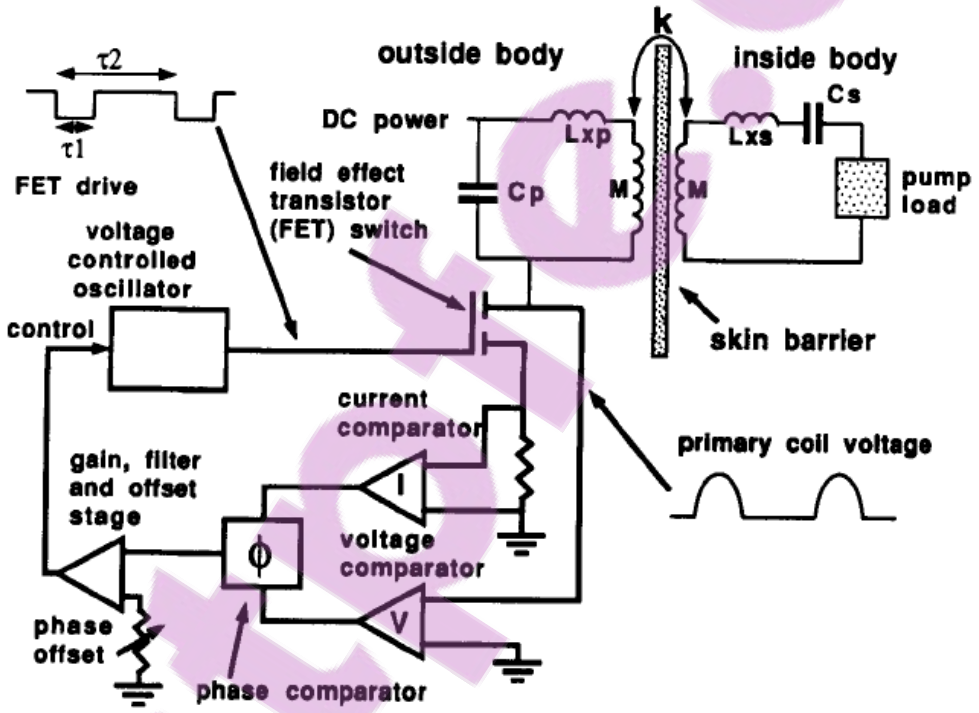


Figure 1–18 Autotuning TET block diagram [73]

In 2000, Tsai *et al.* presented a TET system based on a half-bridge series-resonant topology with a 68% overall efficiency when delivering 36W. The system employs variable frequency control by measuring changes in the phase of the input impedance. The regulated coil separation is between 6 to 18mm [62]. Figure 1–19 shows the system which has a dc-dc converter to step up the voltage and reduce current to limit circuit heating. A half-bridge series-resonant inverter is used on the primary with a full wave rectifier at secondary. The primary and secondary coil diameters are 90mm and 60mm respectively.

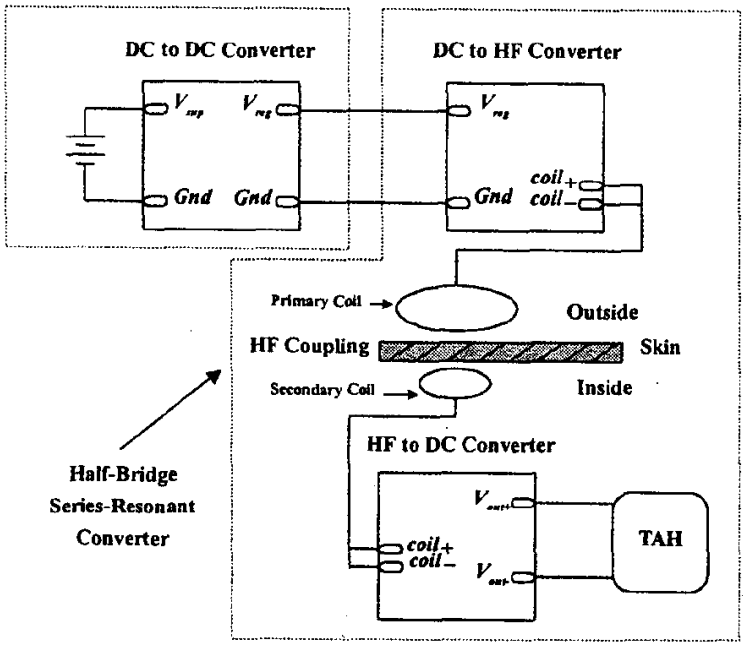


Figure 1–19 The wireless transcutaneous energy transmission system [62]

In 2006, Mizannojehdehi *et al.* investigated a Class-E topology (as shown in Figure 1–20) for TET systems. This can maintain 15W at the load via variable frequency with coil separation from 10mm to 24mm. [63]. The limitation is that the system fails to regulate for separation under 10mm.

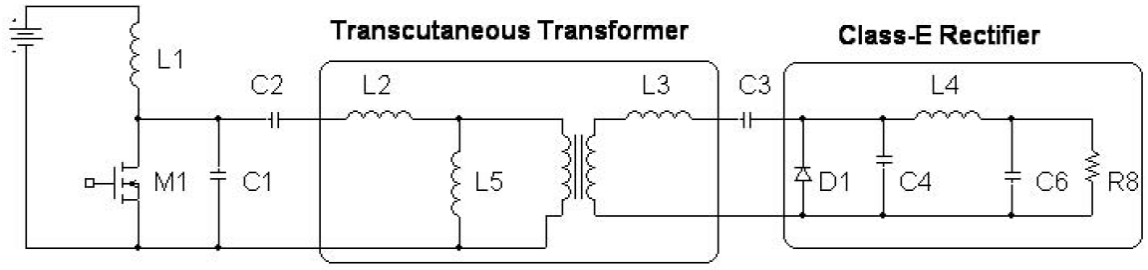


Figure 1–20 The Class-E TET [63]

In 2008, Si *et al.* also proposed a primary controller capable of 15W delivery across a 10mm air gap using the current-fed parallel-parallel tuned push-pull resonant converter by changing the effective resonant capacitance [35, 74]. The circuit schematic is shown in Figure 1–21. The load voltage is monitored and converged to a pre-set reference by variable effective resonant capacitance and variable frequency operation.

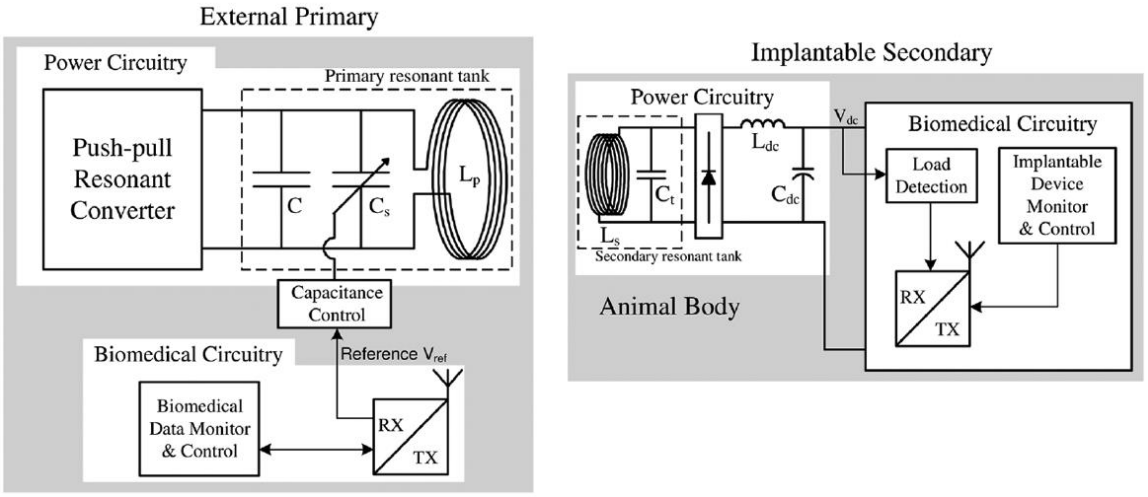


Figure 1–21 System configuration of proposed wireless power supply capacity, EMI, tissue heating, and ZVS operation [35]

In 2009, Dissanayake *et al*. implemented the variable capacitance and frequency system shown in Figure 1–22. The TET system can operate with a coil separation of 10 to 20mm and transfer a regulated 15W of power across the skin of a sheep over 24 hours (as shown by Figure 1–23). The system employs a parallel tuned push-pull converter at primary and a parallel tuned secondary. The system needs to have a start-up circuit to ensure initial dc currents at the primary dc inductors, to ensure the existence of ZVS points. Two additional capacitors and switches are added to vary the effective resonant capacitance and operating frequency. The secondary resonant tank was implanted in a sheep with the remaining rectifier and load left outside the body [34, 56, 60].

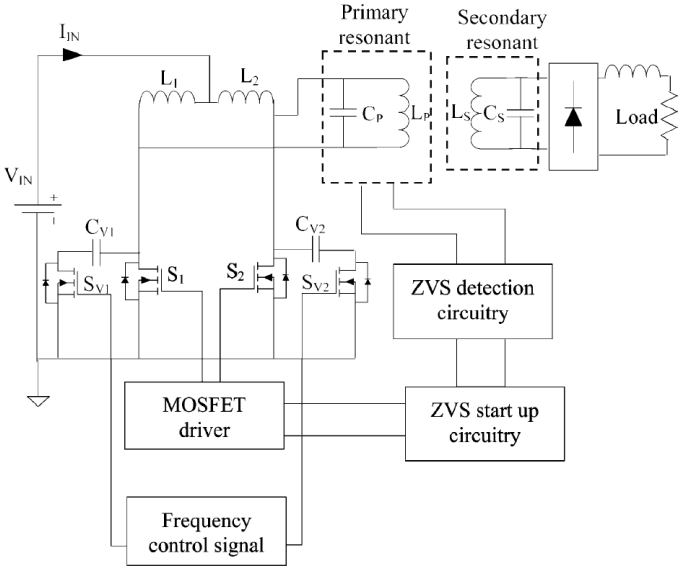


Figure 1–22 System based on primary frequency control [34]

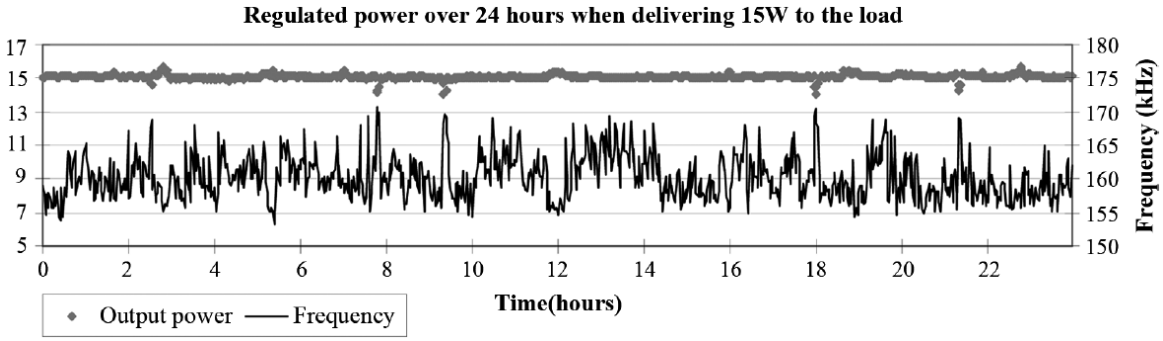


Figure 1–23 Regulated power of 15W being delivered to the load and the variation in frequency in the primary resonant tank over a 24-h period [34]

1.3.3.3. Secondary Side Control

In 2006, Si *et al.* presented an analytical method for secondary side dynamic detuning as shown in Figure 1–24, but experiments were not conducted to find the regulated coil separation range [75]. This is an example of secondary side power flow control, which has direct access to the load voltage and eliminates the need for radio frequency communication for primary side power flow controllers. This improves overall system reliability and safety. Further work can be found in Chapter 6 about a secondary or implanted power flow controller.

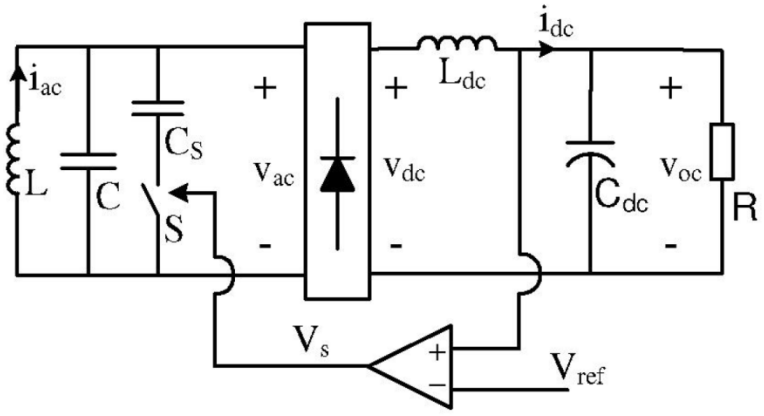


Figure 1–24 Power pick-up with dynamic detuning [75]

1.3.4. Reduction of Power Losses

Power loss reduction is of key importance, as it helps prevent thermal tissue damage in a transcutaneous energy transfer system. A summary of existing research includes applying synchronous rectification, identifying the thermal damage threshold, the system power loss break-down; conducting TET thermal experiments on sheep skin and applying component optimisation.

In 1996, Matsuki *et al*. used a push-pull and voltage doubler type topology as shown in Figure 1–25 to implement synchronous rectifiers. As shown by Figure 1–26, the conventional rectifier reached steady state temperature around 43 ℃, whereas the voltage doubler stabilised around 41 ℃ and the push-pull stabilised around 40.2 ℃ [76]. The rise in temperature of the voltage doubler topology is about half of that in a conventional rectifier, whereas the temperature rise with a push-pull topology is about one third of that in a conventional rectifier.

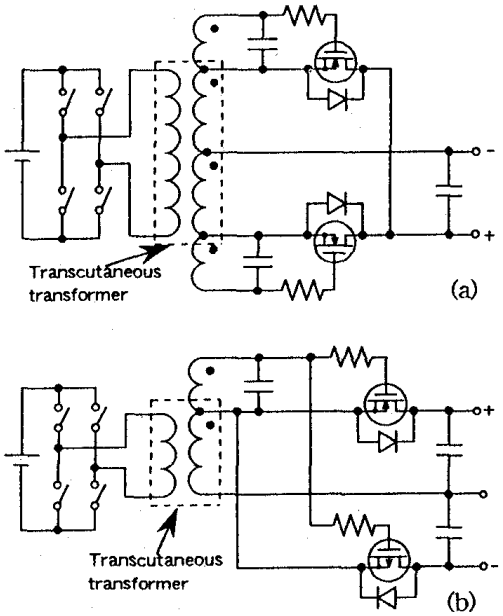


Figure 1–25 Transcutaneous dc-dc converter using a synchronous rectifier. (a) Push-pull type (b) Voltage doubler type [76]

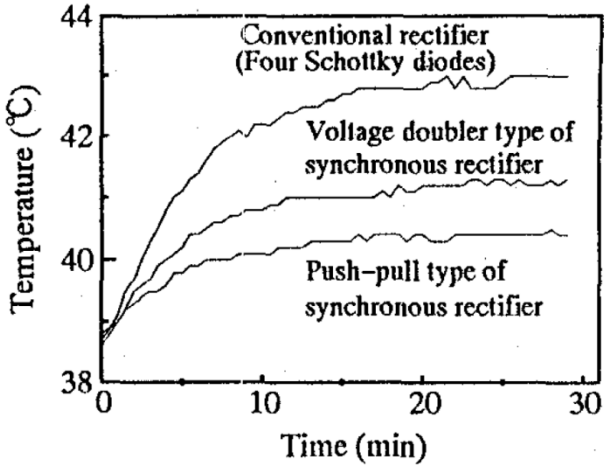


Figure 1–26 Temperature of internal rectifying circuits in a 39 ℃ atmosphere [76]

In 2004, Gowrishankar *et al.* used a mathematical analogy between local thermal and electrical models to solve the system model. This study found that 42 ℃ is the theoretical upper threshold before thermal tissue damage will occur [77].

In 2005, Miura *et al.* presented a synchronous rectifier as shown in Figure 1–27, which is controlled using a digital PLL technique and which has a maximum efficiency of 92% at 5mm coil separation [78]. Also in 2006, Miura *et al.* reported a push-pull synchronous rectifier as shown in Figure 1–28 with a dc-dc efficiency of 93.4% when delivering 46W at the load [79]. This is related to the work in Chapter 6 of this thesis, where two drive options for push-pull type synchronous rectifiers are proposed to lower system power losses and improve operation range.

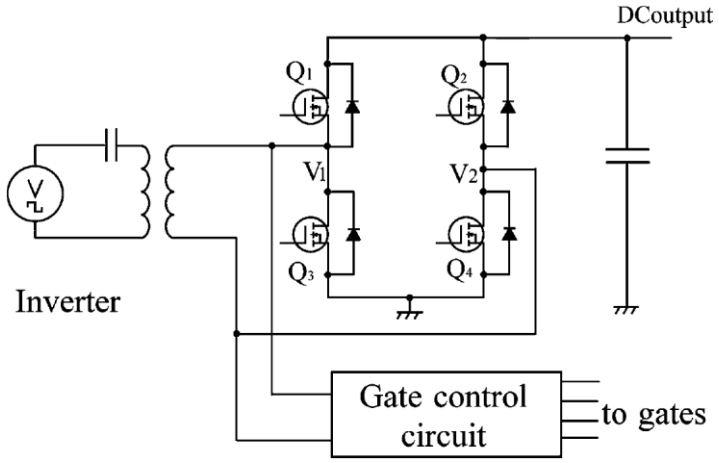


Figure 1–27 Circuit of the contactless power supply system with a synchronous rectifier [78]

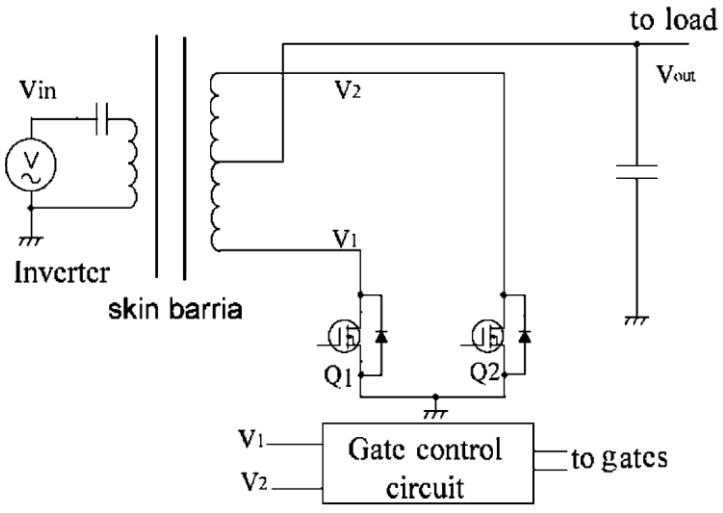


Figure 1–28 Circuit of the transcutaneous energy transmission system with the double-ended synchronous rectifier [79]

In 2007, Chen *et al.* analysed a 10W TET system with an autonomous push-pull primary for power loss distribution, which is shown in Figure 1–29. It is found that efficiency can best be improved by lowering losses at the power conditioning stage (rectifier), primary resonant inductor (L_p) and gate drive circuits (R_a+R_b) [80]. This detailed power loss breakdown identifies areas that require further improvements to lower losses. A

synchronous rectifier was employed in this study to lower losses at the power conditioning stage, and this will be discussed in Chapter 6.

In 2008, Dissanayake *et al*. conducted TET experiments on live sheep with a measured temperature rise of 5 ℃ during 15W power delivery [81]. Figure 1–30 shows a simulated temperature distribution on the coils and tissue during wireless power transfer.

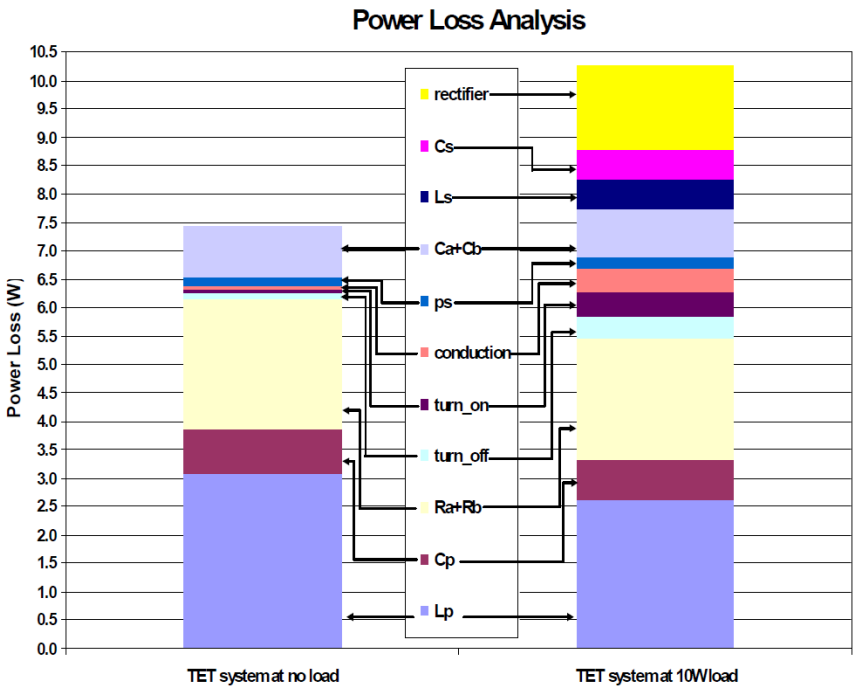


Figure 1–29 Loss distribution under 'load' and 'no load' condition [80]

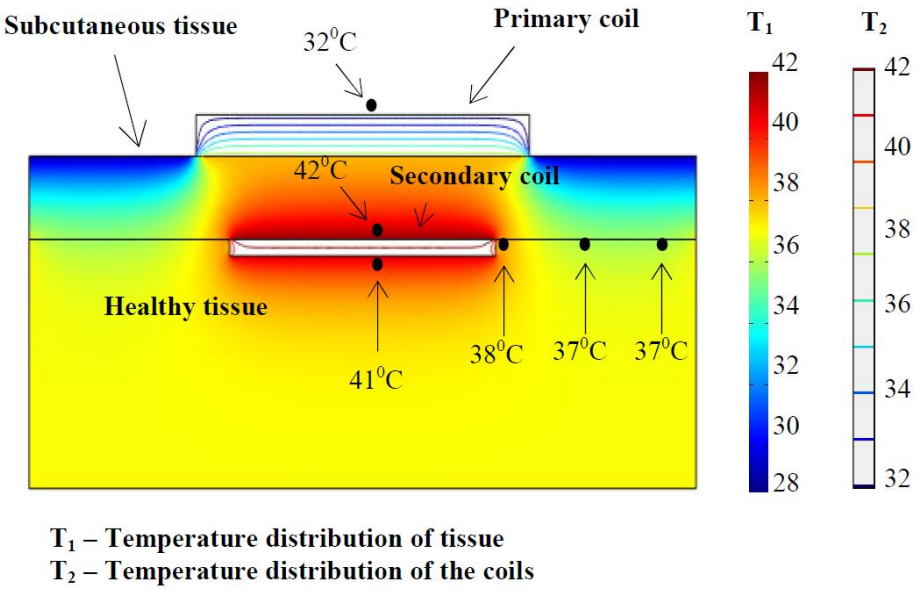


Figure 1–30 Heat distribution of the primary and the secondary coils when delivering 15W of power to the load [81]

In 2011, Leung *et al.* set an objective function to minimise the overall TET coil power losses. The method systematically finds the best resonant capacitors and assists TET designs to have lower heating and better frequency stability [82, 83].

1.3.5. TET Coil Compensation and Designs

TET coil design can improve power transfer and efficiency. Ferrite or amorphous based cores generally provide better power transfer, but air-core is usually preferred due to its flexibility and lightness for patients' comfort. Typical coil configurations are parallel-parallel, parallel-series, series-series and series-parallel as shown in Figure 1–31 to Figure 1–34.

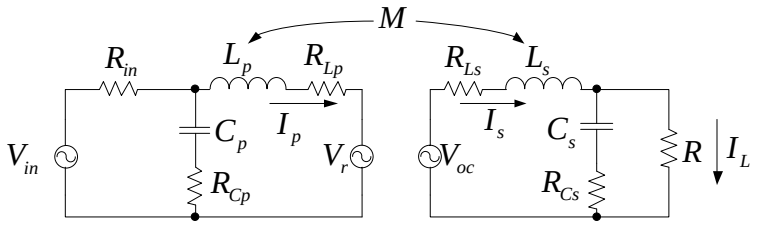


Figure 1–31 Parallel-parallel tuned

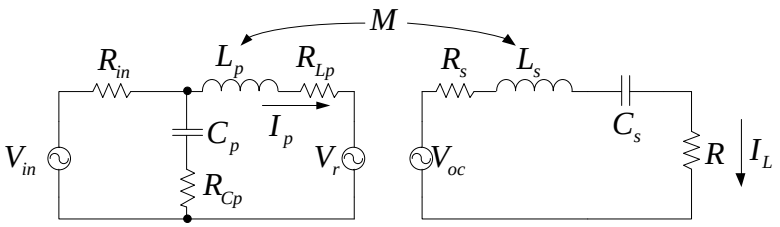


Figure 1–32 Parallel-series tuned

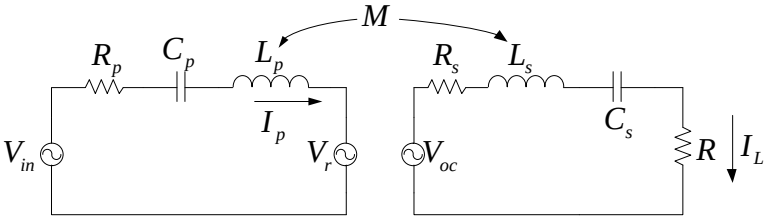


Figure 1–33 Series-series tuned

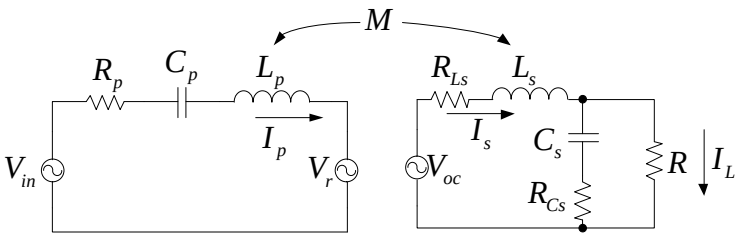


Figure 1–34 Series-parallel tuned

In 2009, Wu *et al.* integrated the dc inductors and resonant coil of a current-fed push-pull converter into a dual coil configuration (as shown in Figure 1–35). The system can achieve 90.5% dc-ac efficiency during 10W power delivery [84]. Although this implementation eliminated the bulky primary dc inductors in the existing systems, it now required two primary side TET coils, which are separated by 18mm to keep total harmonic distortion below 5%. The added TET coil introduces design complexity as its misalignments with respect to other TET coils need to be considered.

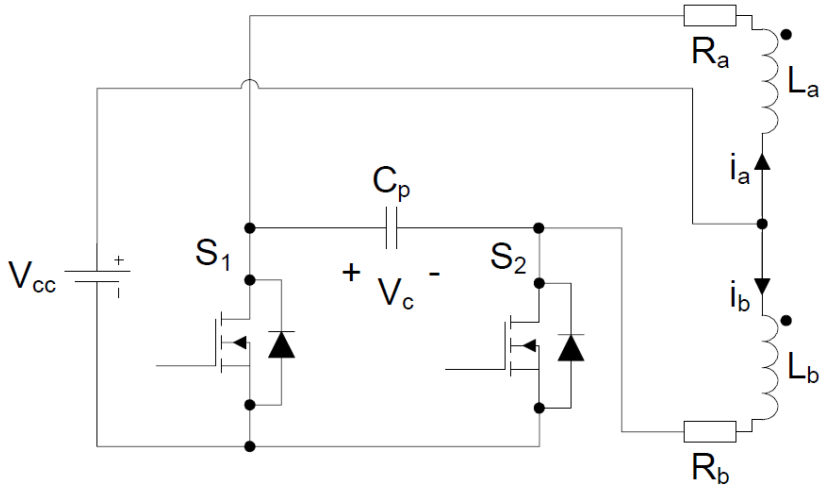


Figure 1–35 A compact push-pull current-fed parallel resonant converter [84]

TET coil designs using ferrites and amorphous material were investigated by Matsuki *et al.* (1993), Nishimura *et al.* (1994) and Zhao *et al.* (1998) [85-87]. Matsuki *et al.* investigated amorphous TET coils of 81mm and 60mm on the primary and secondary respectively, and found the best operating frequency to be between 100 and 200kHz [85]. Nishimura *et al.* presented detailed models and designs for a TET transformer with a ferrite core on the primary and an amorphous core on the secondary [86]. Zhao *et al.* suggested using a combination of ferrite and amorphous cores to allow for a balance between good power transmission and flexible shape suited for implantation [87].

In 2011, Artan *et al.* showed that a four layer secondary coil design without ferrite slows down temperature rise by 3.6 times compared with a single layer coil [88]. As shown in Figure 1–36, the temperature rise of four layers is clearly the lowest when compared to the other numbers of layers. The TET system in this thesis uses dual layers on the primary and a single layer on the secondary, and no attempt has been made to modify this design as it is outside the scope of the thesis.

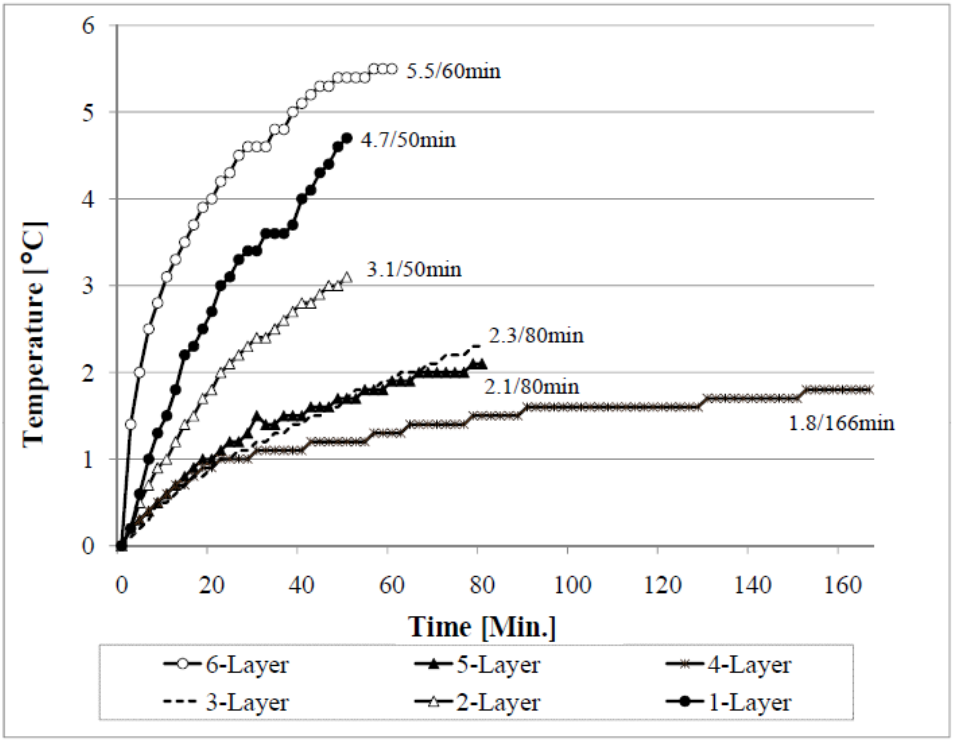


Figure 1–36 Skin temperature rise with time, when constant power is applied to the primary [88]

In 2012, Waters *et al.* presented a wireless power system, also called a 'free-range resonant electrical delivery' (FREE-D), capable of transmitting 16W with 50% efficiency over a large distance (~1m). This can be accomplished by employing five sets of coils of varying sizes as shown in Table 1–4 [67]. Figure 1–37 shows the implanted FREE-D coils while Figure 1–38 shows a room filled with FREE-D transmitters, giving greater freedom of movement for the patient.

Table 1–4 Resonator sizes for FREE-D Experimental Configuration [67]

Resonator Description	Diameter (cm)
Drive Resonator	31
TX Resonator	59
Relay Resonator	59
RX Vest Resonator	28
RX Implantable Resonator	9.5

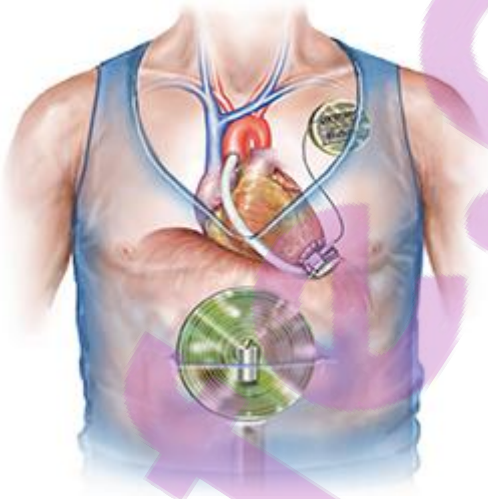


Figure 1–37 A tether-free Left Ventricular Assist Device (LVAD) [89]

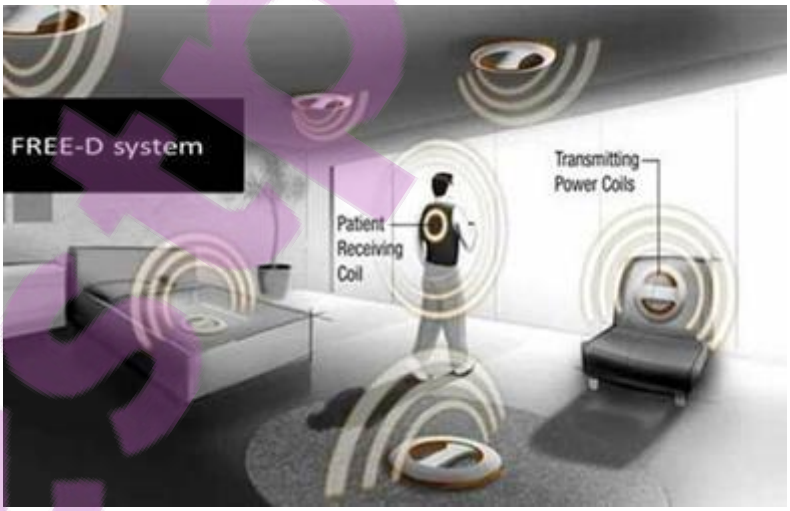


Figure 1–38 The FREE-D system [89].

1.4. The Objectives and Scope of this Thesis

The objective of this thesis is to design power controllers to improve operation of TET systems for powering heart pumps. The focus is on improving the coil magnetic coupling

tolerance, the input voltage range of the power source and the output power range. The thesis focuses on the design and implementation of power flow controllers to extend the operational ranges, as previously described. Here, extending the TET coil magnetic coupling tolerance corresponds to maximising the coil separation and the lateral or angular misalignments for which rated power is maintained. To extend the input voltage and output power ranges would involve power peak tracking as will be discussed later. Overall, the power flow controllers can be variable frequency or ZVS follower on the primary side, and variable resonant shorting period on the secondary side.

Chapter 2 provides a theoretical base for the analysis of power converters to support the work in other chapters within this thesis. It introduced the important concept of frequency stability and the issues arising from system frequency bifurcation. If unaccounted for, bifurcation can produce frequency jumps and a sharp drop in power flow when a simple controller is used. The chapter reveals the dynamic process of waveform change by examining the transient waveforms and trends during transition between ZVS operating points in the presence of frequency bifurcation. ZVS is determined accurately by the stroboscopic mapping method, while ac impedance analysis can approximate the location ZVS points and system power peak. The maximum power analysis is used throughout the thesis for the purpose of power flow controller design.

Chapter 3 proposes a novel primary power flow controller to maintain a constant voltage level for the heart pump operation. Existing controllers designed by Dissanayake *et al.* [34] and Si *et al.* [35] have used additional parallel switches and resonant capacitors to vary the effective resonant capacitance. The system ZVS frequency will be changed and with a simple ZVS control, the system operating frequency will match the ZVS frequency via a quick ZVS detecting resonant tank feedback loop. In comparison, the additional switching devices and resonant capacitors in the existing system are eliminated in the proposed novel primary controller; this means about 25% savings on the circuit size.

Chapter 4 proposes a primary power flow controller with an automatic ZVS range. It is always of interest to discover ways of increasing the coil coupling tolerance given a particular TET coil geometry and size. By detecting and processing the primary side resonant shorting period and the secondary side heart pump load voltage level, the TET coil coupling tolerance can be improved by allowing an automatic ZVS range; this gives

more power flow when required at lower coupling levels by tracking the system close to the lower ZVS branch.

Chapter 5 proposes a ZVS follower to maintain middle ZVS and peak power operation. While using a simple ZVS controller, the system will jump to a different operating frequency under bifurcation and thus significantly compromise the system power transfer capability. The chapter proposes a ZVS follower through two equally valid methods to maintain middle ZVS operation on bifurcation to keep high power transfer; this allows rated power delivery to a heart pump at a lower input voltage, larger coil separation and higher efficiency.

Chapter 6 proposes two drive options for a current doubler synchronous rectifier to improve end-to-end efficiency by around 1.35% (~200mW) at 10W delivery. By removing the drive options, the controller drives the low side switches of the synchronous rectifier separately to allow power flow control by variable resonant shorting period. Since the secondary side follows the frequency of the primary, fast resonant voltage detection is required to produce timely triggers to be processed by a FPGA controller.

Finally, Chapter 7 draws general conclusions and summarises the key work in this thesis in the development of primary and secondary power flow controllers, as well as a synchronous rectifier to further reduce the power losses and extend the operational range of TET systems. Research results from this thesis are published in two journal and two conference papers. Future work includes testing power flow controllers with real heart pumps, PCB miniaturisation and further sheep trials.

Chapter 2

Dynamic Bifurcation Phenomena Study of Wireless Power Transfer System

2.1. Introduction

Power transfer through an IPT system is heavily dependent upon the system's operating frequency. Efficient operations with low harmonics are usually highly favourable characteristics, and techniques such as zero voltage switching can help achieved these performance measures. However, some system parameters – such as primary to secondary coil coupling – are highly variable, and under some circumstances there can be multiple frequencies that satisfy the ZVS criteria, but deliver differing amounts of power. The phenomenon is referred to as frequency bifurcation, and can cause frequency jumps and sharp drops in the power transfer capability of IPT systems [90]. A current-fed parallel-parallel tuned circuit can generate a high resonant current with a very low input current corresponding to the load, therefore it has been used for primary side inverter throughout the thesis and has been chosen for study in this chapter. This chapter provides an analysis of a parallel-parallel tuned IPT system with a view to determining its bifurcation properties. This understanding will allow performance predictions over the range of coupling and loading conditions and the design of controller strategies to meet the power transfer capability needs. This chapter applies two different methods to revealing the dynamic behaviour of operating frequency in a bifurcated system, and thus enabling more robust variable or fixed frequency power flow controllers. The bifurcation phenomena have been observed in previous literature in inductive power transfer systems [28, 72, 91-94]. In this research a current-fed push-pull converter which is widely used in IPT systems is studied. It is found that by increasing the coupling level between primary and secondary resonant networks, the system zero voltage switching frequency bifurcates from one point to three operating points. By simply following the zero crossings of the resonant voltage, the system goes to a stable ZVS operating point upon bifurcation. The

dynamic process of ZVS point transition is investigated by forcing the switching frequency.

2.2. System ZVS Frequencies and Peak Power

2.2.1. AC Impedance Analysis

AC impedance analysis is a valuable way of identifying peak power at ZVS so that an effective soft switching control algorithm can be derived. If the harmonics generated by the inverter are ignored; through ac impedance analysis, the system approximate zero voltage switching frequencies can be found.

Throughout this thesis the parallel-parallel tuned topology is used (as shown in Figure 2–1). The bifurcation and the peak power characteristics of this topology are derived by ac impedance analysis. The open circuit voltage (V_{oc}) and reflected voltage (V_r) are given by (2.1) and (2.2), where I_p is the primary coil current, ω is the system operating frequency and M is the mutual inductance. The total secondary impedance (Z_s) is given by (2.3). The operating frequency throughout this thesis ranges between 130kHz to 270kHz, this range was selected to minimise timing inaccuracies during switching and to give a higher efficiency compared to the MHz frequency range.

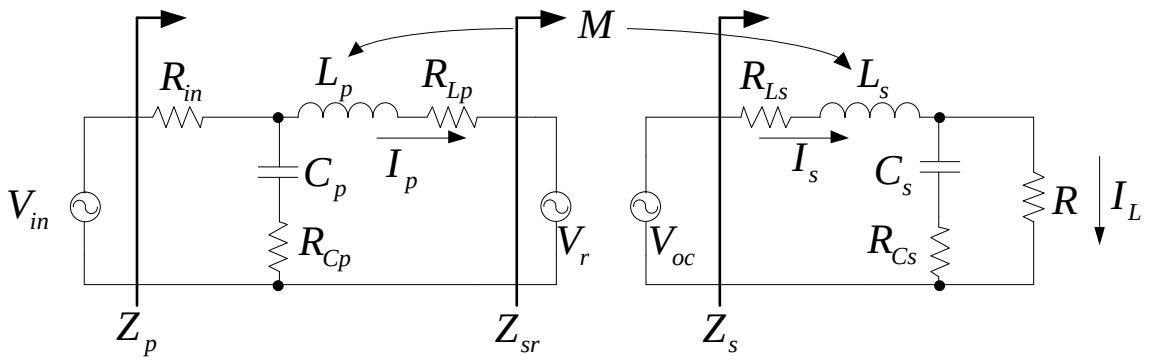


Figure 2–1 Parallel-parallel tuned

$$V_{oc} = j\omega M I_p \tag{2.1}$$

$$V_r = -j\omega M I_s \tag{2.2}$$

$$Z_s = R_{Ls} + j\omega L_s + \left(\frac{1}{j\omega C_s} + R_{Cs} \right) || R \tag{2.3}$$

By substituting (2.1) and (2.2), the secondary resonant coil current (I_s) and the reflected impedance to the primary (Z_{sr}) are given by (2.4) and (2.5) respectively.

$$I_s = \frac{V_{oc}}{Z_s} = \frac{j\omega M I_p}{Z_s} \tag{2.4}$$

$$Z_{sr} = \frac{V_r}{I_p} = -\frac{j\omega M I_s}{I_p} \tag{2.5}$$

Substituting (2.4) in (2.5) gives (2.6).

$$Z_{sr} = \frac{M^2\omega^2}{Z_s} \tag{2.6}$$

The total input primary impedance (Z_p) is given by (2.7), and the approximate ZVS frequencies using ac impedance approach can be found by solving (2.8), which forces the imaginary part of the input primary impedance to be zero. This effectively finds all possible frequencies where the input primary impedance phase angle equates to zero.

$$Z_p = R_{in} + \left(\frac{1}{j\omega C_p} + R_{Cp} \right) \| \left(j\omega L_p + R_{Lp} + Z_{sr} \right) \tag{2.7}$$

$$\mathrm{Im}\left(Z_p \right) = 0 \tag{2.8}$$

2.2.2. Peak Power Analysis

The total input current (I_{in}) from source is given by (2.9), while the current through the primary resonant coil is a share of this current given by (2.10). Similarly, the load current (I_L) is a share of the secondary resonant coil current given by (2.11).

$$I_{in} = \frac{V_{in}}{Z_p} \tag{2.9}$$

$$I_p = \frac{I_{in}\left(\frac{1}{j\omega C_p} + R_{Cp} \right)}{\frac{1}{j\omega C_p} + R_{Cp} + j\omega L_p + R_{Lp} + Z_{sr}} \tag{2.10}$$

$$I_L = I_s \frac{\frac{1}{j\omega C_s} + R_{Cs}}{\frac{1}{j\omega C_s} + R_{Cs} + R} \tag{2.11}$$

By combining (2.3), (2.4), (2.6), (2.7), (2.9) and (2.10) in (2.11), the complex conjugate of the resulting load current expression is used in (2.12) to obtain the load power (P_L) expression. Then, the peak power point can be found by equating the derivative of load power to zero as shown in (2.13). The system efficiency (η) can be found by (2.14). The resulting bifurcation and load power equations are derived using Mathcad Prime 2.0. The resulting equations are too long to present here. They are included in the attached CD for reference.

$$P_L = \mathrm{Re}\left(V_L I_L^*\right) \tag{2.12}$$

$$\frac{dP_L}{d\omega} = 0 \tag{2.13}$$

$$\eta = \frac{P_L}{P_{in}} \tag{2.14}$$

Eqn. (2.8) and (2.13) are applied to the parallel-parallel tuned system shown in Table 2–1. MATLAB is used to calculate the corresponding frequency points for a range of coupling coefficients, and the results are presented in Figure 2–2. The system begins with a single ZVS frequency and then bifurcates to three ZVS frequencies with the increase of the coupling coefficient, whereas the system has a single load power peak throughout the coupling level range. The peak power frequency is slightly offset below the single ZVS branch before ZVS bifurcation and equals the middle ZVS branch (determined by ac impedance analysis) upon bifurcation. A three dimensional contour plot of the power flow magnitude with respect to variations in frequency and coupling coefficient is shown in Figure 2–3, which clearly shows a single peak characteristic throughout the magnitude contour. More accurate analysis using the stroboscopic mapping method, which will be discussed later, can show that the peak power frequency is slightly below the accurate middle ZVS branch after bifurcation, but that the difference is negligible.

It can be derived that for a parallel-parallel tuned system there is a single maximum output power capability point for all loading conditions and coupling levels. This

characteristic is useful for controller design in Chapter 5 to maintain middle ZVS operation during ZVS bifurcation to keep high power transfer.

Table 2–1 System parameters for parallel-parallel tuned system

V_{in}	31.1 V	R_{Lp}	73.1 mΩ
L_p	11.3 μH	R_{Ls}	26.7 mΩ
L_s	3.31 μH	R_{Cp}	12 mΩ
C_p	47 nF	R_{Cs}	7 mΩ
C_s	168 nF	R	49.35 Ω

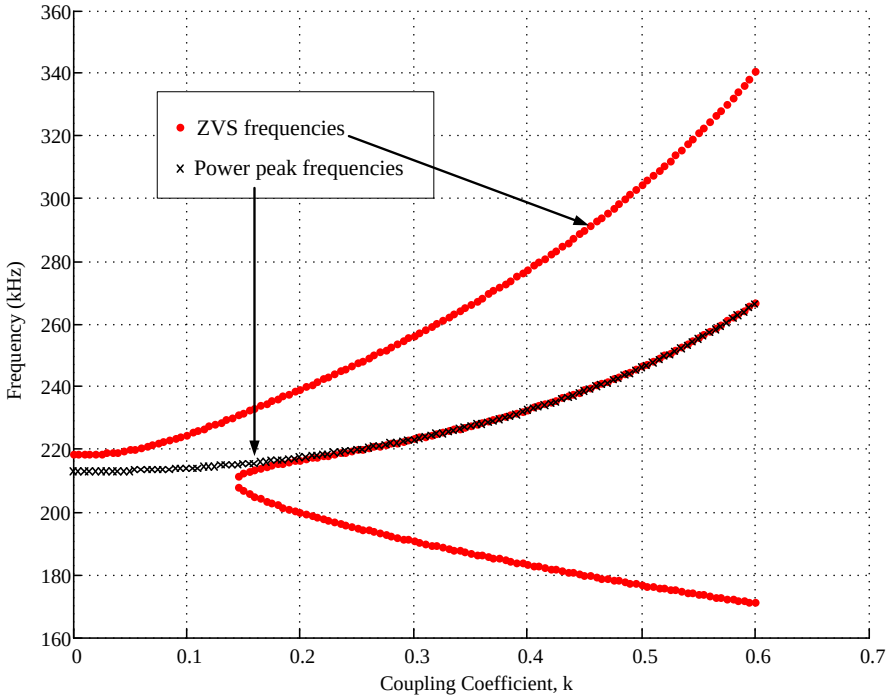


Figure 2–2 ZVS bifurcation and frequencies corresponding to system maximum power

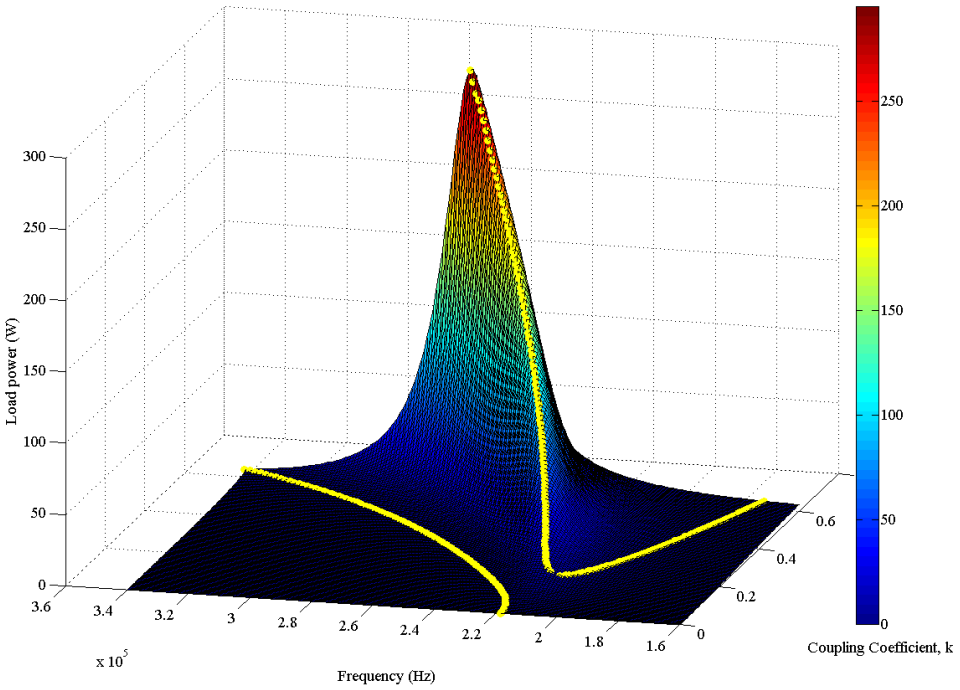


Figure 2–3 Load power curve with respect to frequency and coupling coefficient, where ZVS points are indicated by yellow lines

2.2.3. Stroboscopic Mapping Method

The stroboscopic mapping method is applied here to find the exact ZVS frequencies of the system by solving the full set of system state equations. Stroboscopic mapping method samples the circuit every switching period, so at steady state, a periodic system would have a fixed point repeating upon each sampling. ZVS points can be found by solving a fixed point equation that has the period as a variable. A comparison of this method and the impedance analysis is presented in Table 2–2. Further information can be found in work by Tang *et al.*[71].

Table 2–2 Comparing stroboscopic mapping method and ac impedance analysis

	Stroboscopic mapping method	AC impedance analysis
Pros	Exact ZVS frequencies	Reveals system peak power capability
Cons	Not for power capability analysis	Approximate ZVS frequencies

Figure 2–4 shows a system consisting of a current-fed push-pull parallel tuned converter with ideal switches and an inductively coupled parallel tuned secondary with an ac load. The system has two circuit operational modes which are shown in Table 2–3, and the two modes are presented in Figure 2–5 and Figure 2–6 respectively. Eqn (2.15) and (2.16) show the system state variables included in the analysis, and the system state equations

are shown in (2.17) and (2.18) for Mode 1 and 2 respectively, with the delta symbol represented by (2.19). Eqn (2.17) and (2.18) are then expressed as "A" matrices in (2.20) and (2.21) respectively. The system "B" matrices are given by (2.22) and (2.23) for Mode 1 and 2 respectively. The system selection matrix to extract the primary resonant capacitor voltage to find ZVS points is given in (2.24).

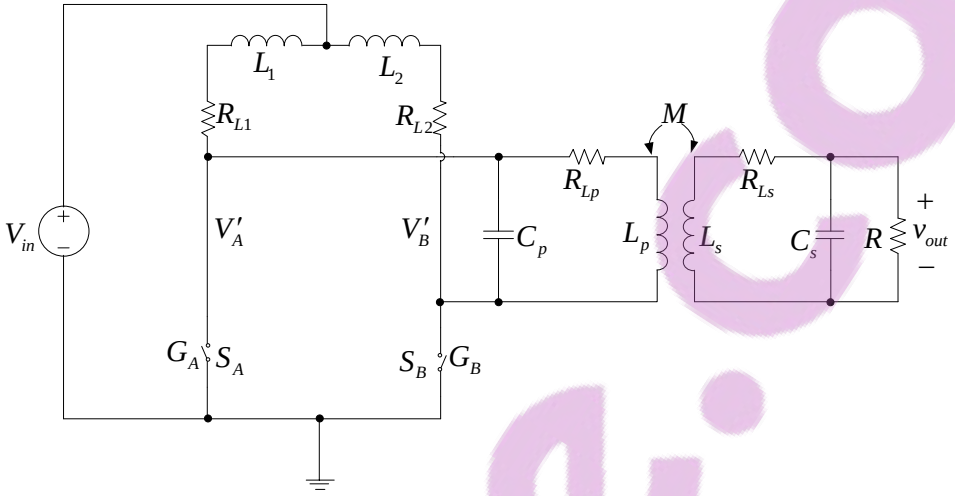


Figure 2–4 Push-pull converter with ideal switch and ac load

Table 2–3 System circuit operational modes

	S_A	S_B
Mode 1	ON	OFF
Mode 2	OFF	ON

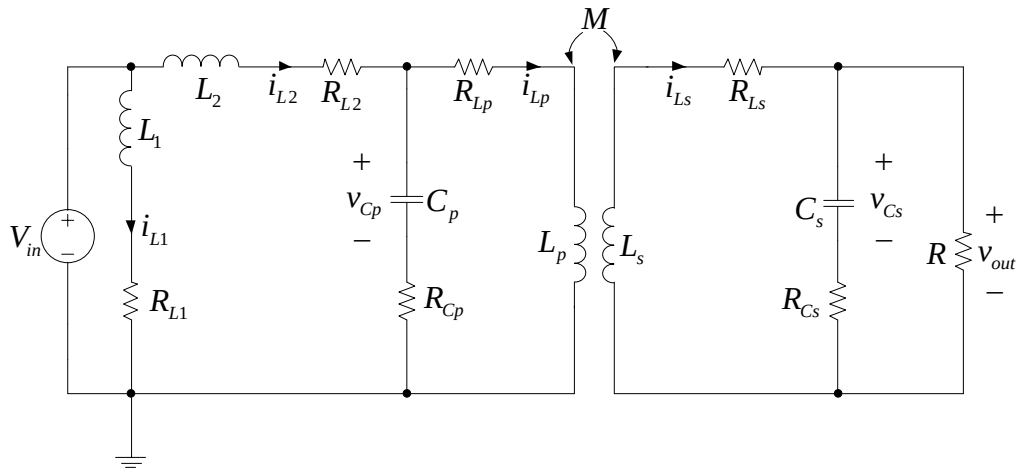


Figure 2–5 Push-pull converter with S_A ON and S_B OFF (Mode 1)

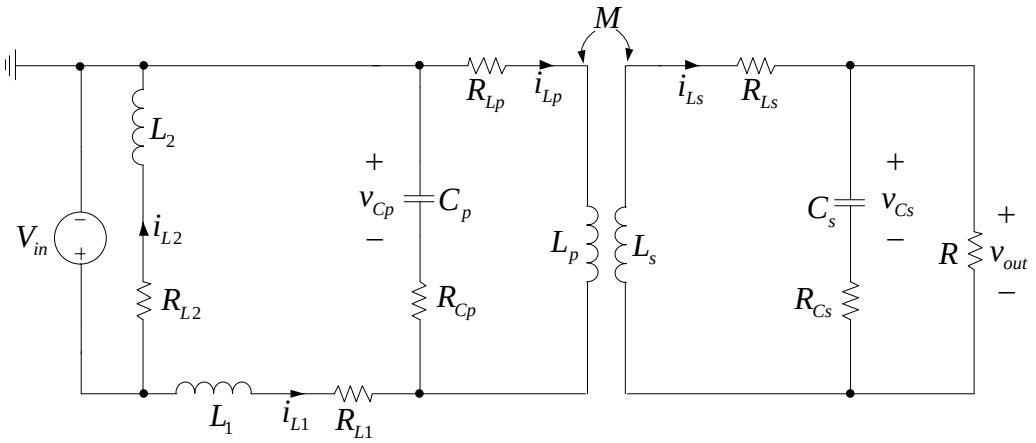


Figure 2–6 Push-pull converter with S_A OFF and S_B ON (Mode 2)

$$x_1 = \begin{bmatrix} i_{L2} & v_{Cp} & i_{Lp} & i_{Ls} & v_{out} \end{bmatrix}^T \tag{2.15}$$

$$x_2 = \begin{bmatrix} i_{L1} & v_{Cp} & i_{Lp} & i_{Ls} & v_{out} \end{bmatrix}^T \tag{2.16}$$

$$\begin{aligned}
\frac{di_{L2}}{dt} &= -\frac{R_{L2}}{L_2} i_{L2} - \frac{1}{L_2} v_{Cp} + 0 i_{Lp} + 0 i_{Ls} + 0 v_{out} + \frac{1}{L_2} V_{in} \\
\frac{dv_{Cp}}{dt} &= \frac{1}{C_p} i_{L2} + 0 v_{Cp} - \frac{1}{C_p} i_{Lp} + 0 i_{Ls} + 0 v_{out} \\
\frac{di_{Lp}}{dt} &= 0 i_{L2} - \frac{L_s}{\Delta} v_{Cp} + \frac{L_s R_{Lp}}{\Delta} i_{Lp} + \frac{M R_{Ls}}{\Delta} i_{Ls} + \frac{M}{\Delta} v_{out} \\
\frac{di_{Ls}}{dt} &= 0 i_{L2} - \frac{M}{\Delta} v_{Cp} + \frac{M R_{Lp}}{\Delta} i_{Lp} + \frac{L_p R_{Ls}}{\Delta} i_{Ls} + \frac{L_p}{\Delta} v_{out} \\
\frac{dv_{out}}{dt} &= 0 i_{L2} + 0 v_{Cp} + 0 i_{Lp} + \frac{1}{C_s} i_{Ls} - \frac{1}{RC_s} v_{out}
\end{aligned} \tag{2.17}$$

$$\begin{aligned}
\frac{di_{L1}}{dt} &= -\frac{R_{L1}}{L_1} i_{L1} + \frac{1}{L_1} v_{Cp} + 0 i_{Lp} + 0 i_{Ls} + 0 v_{out} + \frac{1}{L_1} V_{in} \\
\frac{dv_{Cp}}{dt} &= -\frac{1}{C_p} i_{L1} + 0 v_{Cp} - \frac{1}{C_p} i_{Lp} + 0 i_{Ls} + 0 v_{out} \\
\frac{di_{Lp}}{dt} &= 0 i_{L1} - \frac{L_s}{\triangle} v_{Cp} + \frac{L_s R_{Lp}}{\triangle} i_{Lp} + \frac{M R_{Ls}}{\triangle} i_{Ls} + \frac{M}{\triangle} v_{out} \\
\frac{di_{Ls}}{dt} &= 0 i_{L1} - \frac{M}{\triangle} v_{Cp} + \frac{M R_{Lp}}{\triangle} i_{Lp} + \frac{L_p R_{Ls}}{\triangle} i_{Ls} + \frac{L_p}{\triangle} v_{out} \\
\frac{dv_{out}}{dt} &= 0 i_{L1} + 0 v_{Cp} + 0 i_{Lp} + \frac{1}{C_s} i_{Ls} - \frac{1}{RC_s} v_{out}
\end{aligned} \tag{2.18}$$

$$\triangle = M^2 - L_p L_s \tag{2.19}$$

$$A_1 = \begin{bmatrix}
-\frac{R_{L2}}{L_2} & -\frac{1}{L_2} & 0 & 0 & 0 \\
\frac{1}{C_p} & 0 & -\frac{1}{C_p} & 0 & 0 \\
0 & -\frac{L_s}{\triangle} & \frac{L_s R_{Lp}}{\triangle} & \frac{M R_{Ls}}{\triangle} & \frac{M}{\triangle} \\
0 & -\frac{M}{\triangle} & \frac{M R_{Lp}}{\triangle} & \frac{L_p R_{Ls}}{\triangle} & \frac{L_p}{\triangle} \\
0 & 0 & 0 & \frac{1}{C_s} & -\frac{1}{RC_s}
\end{bmatrix} \tag{2.20}$$

$$A_2 = \begin{bmatrix}
-\frac{R_{L1}}{L_1} & \frac{1}{L_1} & 0 & 0 & 0 \\
-\frac{1}{C_p} & 0 & -\frac{1}{C_p} & 0 & 0 \\
0 & -\frac{L_s}{\triangle} & \frac{L_s R_{Lp}}{\triangle} & \frac{M R_{Ls}}{\triangle} & \frac{M}{\triangle} \\
0 & -\frac{M}{\triangle} & \frac{M R_{Lp}}{\triangle} & \frac{L_p R_{Ls}}{\triangle} & \frac{L_p}{\triangle} \\
0 & 0 & 0 & \frac{1}{C_s} & -\frac{1}{RC_s}
\end{bmatrix} \tag{2.21}$$

$$B_1 = \begin{bmatrix} \frac{1}{L_2} & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{2.22}$$

$$B_2 = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{2.23}$$

$$Y = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \end{bmatrix} \tag{2.24}$$

The system under study has the circuit parameters listed in Table 2–4. By applying the stroboscopic mapping method, the zero crossings of (2.25) gives the period of zero voltage switching points, which is converted to zero voltage switching frequencies by inverting the period shown by (2.26). The resulting ZVS frequency bifurcation curve with respect to variable coupling coefficient is plotted in Figure 2–7. There is one zero voltage switching point near the nominal frequency (f_0) at low coupling. As the coupling level increases, the system bifurcates to three zero voltage switching frequencies.

Table 2–4 System parameters for dynamic bifurcation study

V_{in}	10 V	L_p	11.3 µH
f_0	200 kHz	R_{Lp}	73.1 mΩ
L_1	1 mH	L_s	3.31 µH
L_2	1 mH	R_{Ls}	26.7 mΩ
R_{L1}	0.46 Ω	C_s	191.32 nF
R_{L2}	0.46 Ω	R	49.348 Ω
C_p	56.04 nF		

$$f_{x^*} = Y\left(I - e^{\frac{A_2 t}{2}} e^{\frac{A_1 t}{2}}\right)^{-1}\left(e^{\frac{A_2 t}{2}}\left(e^{\frac{A_1 t}{2}} - I\right)A_1^{-1}B_1 V_{in} + \left(e^{\frac{A_2 t}{2}} - I\right)A_2^{-1}B_2 V_{in}\right) \tag{2.25}$$

$$f_{zvs} = \frac{1}{t} \quad \text{where } f_{x^*}(t) = 0 \tag{2.26}$$

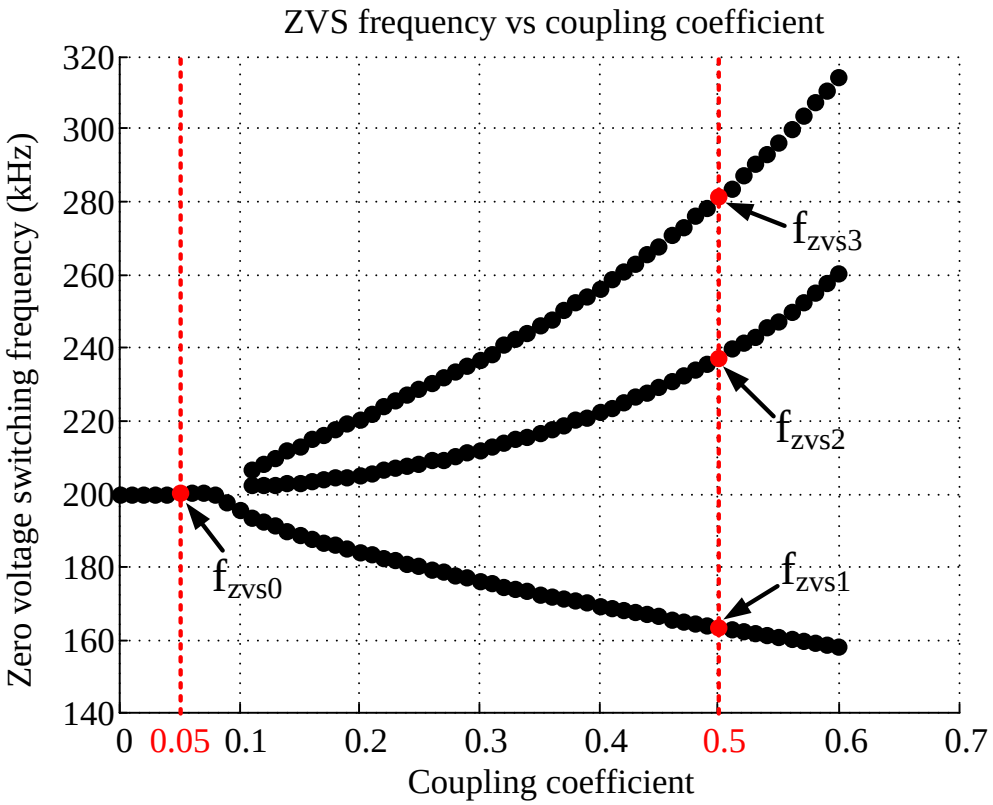


Figure 2–7 Bifurcation of system ZVS frequencies with increased coupling coefficients calculated using the stroboscopic mapping method

2.3. Operation via ZVS Detection

To investigate the frequency jump upon bifurcation, a simple ZVS detection method as shown by Figure 2–8 generate gate driving signals from primary resonant waveforms. The method applies a small hysteresis window about zero to reduce noise interference and attain zero crossings in the resonant tank voltage, V'_{AB}, which is the differential voltage of V'_A and V'_B. Then a start-up module is required to ensure the existence of ZVS in the system by shorting both switches simultaneously for a short duration on initial power up. This then produces square waves that drive the two low-side switches of the push-pull converter.

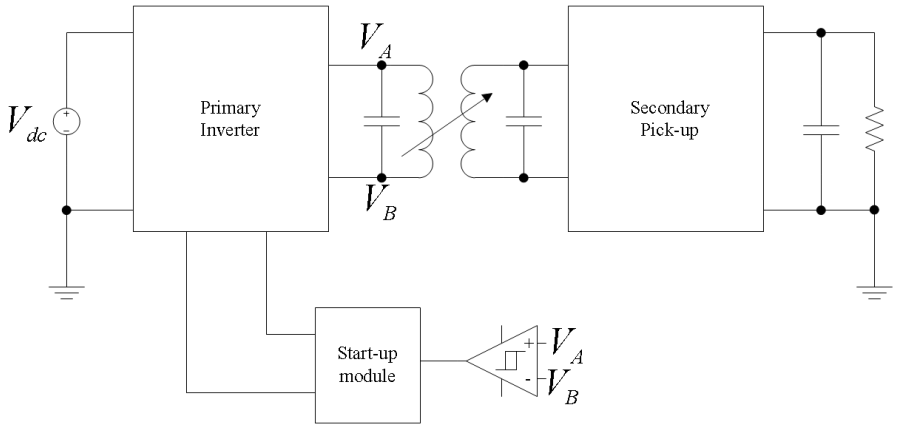


Figure 2–8 A simple ZVS detection method

After bifurcation, the upper and lower ZVS branches are stable points, while the middle branch is unstable. The TET coils used in this thesis have a magnetic coupling range between k=0.05 to k=0.5. When the system starts off at low coupling below k=0.05, the system will stabilise at the single ZVS point, f_{zvs0}. With a sudden coupling level increase, to k=0.5 for instance, it was observed that the system would stabilise at a higher ZVS frequency f_{zvs3} on Figure 2–7. The middle frequency point, f_{zvs2} is unstable as the zero voltage crossing detection of the waveform (Figure 2–13) pushes the operating frequency upwards toward f_{zvs3}. This is because the additional zero crossing within a half cycle for f_{zvs2} would toggle the gate drive square wave earlier giving a higher operating frequency. This process iterates quickly, ending with a stabilised system at operating point f_{zvs3}. The system may change to the lower ZVS branch if coupling were lowered to k=0.1 and then increased to k=0.5, this is due to the increased uncertainties near k=0.1.

In comparison, when the system started with k=0.5, it would stabilise at f_{zvs1} instead. This is because during start-up the system oscillates at a frequency lower than nominal [95]. The system will be attracted to operate at f_{zvs1}. The system may switch to operating at the upper ZVS branch if coupling is decreased to k=0.05 then increased to k=0.5.

In general, transition in operation between the upper and lower ZVS branches may occur around k=0.1, which is a particular area between non-bifurcated and bifurcated operation. After bifurcation, with a simple ZVS controller the system cannot stabilise at the middle ZVS frequency $f_{zvs2,}$ .and as a result the maximum power transfer capability of the system is compromised.

2.4. Waveform Investigation between ZVS Transition

Forcing the system operating frequency allows the steady state circuit waveforms during a dynamic transition to be examined by stepping the frequency manually. Figure 2–7 shows the system starting off at f_{zvs0} at k=0.05, and bifurcating after k≥0.11. It also shows three bifurcated ZVS points, f_{zvs1}, f_{zvs2} and f_{zvs3} at k=0.5. Figure 2–9 shows a typical ZVS waveform at operating point f_{zvs0}, V'_B is the voltage across switch, S_B, and G_A is the gate drive voltage for switch S_A. Figure 2–10 shows operating point f_{zvs3} with ZVS operation. Figure 2–11 and Figure 2–12 show a steady decline in operating frequency, here resonant tank waveforms show the system is slow switching with a negative voltage region at the end of the half cycle. The system reaches a special ZVS operating point, f_{zvs2} in Figure 2–13, where the resonant voltage starts and ends with zero crossings, but there is one more zero crossing in between. The system operating frequency continues to drop from Figure 2–14 to Figure 2–18; the system is operating with fast switching with a negative voltage region at the start of each half cycle. In Figure 2–19, the system ZVS stabilises at f_{zvs1}. These figures show the dynamic change of the resonant waveforms as the system stabilises towards its ZVS points. Details on the simulations for dynamic ZVS transition can be found in Appendix A.

Understanding these dynamic changes between ZVS points helped when designing smart ZVS followers that maintain the system power transfer capability and extend the operating range. This will be detailed in Chapter 5.

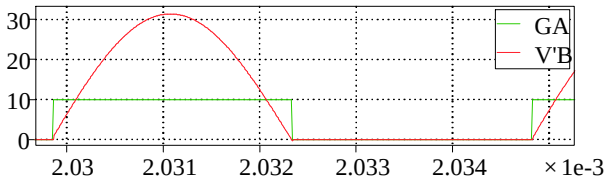


Figure 2–9 k=0.05, fsw=201 kHz (fzvs0)

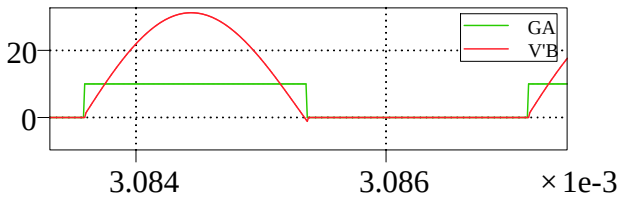


Figure 2–10 k=0.5, fsw=281.81 kHz (fzvs3)

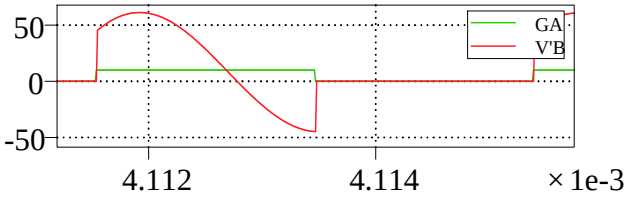


Figure 2–11 k=0.5, fsw=260 kHz

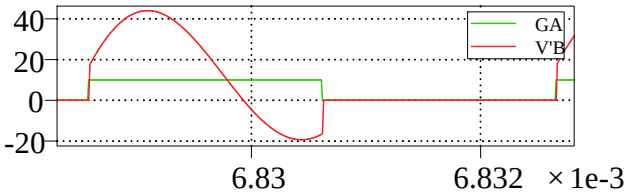


Figure 2–12 k=0.5, fsw=245 kHz

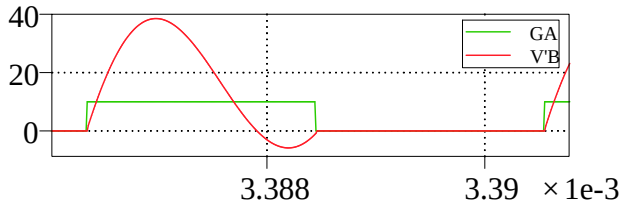


Figure 2–13 k=0.5, fsw=238.01 kHz (fzvs2)

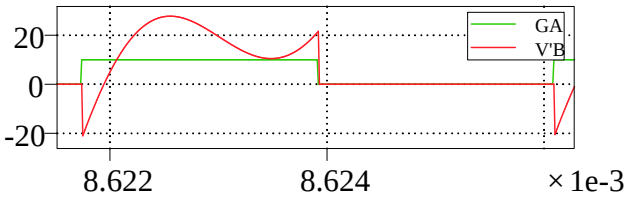


Figure 2–14 k=0.5, fsw=230 kHz

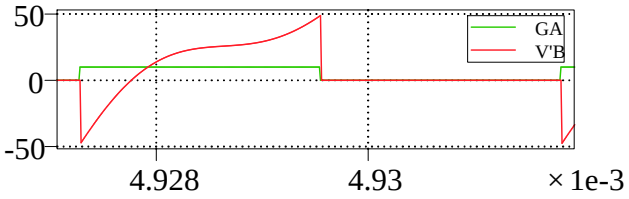


Figure 2–15 k=0.5, fsw=220 kHz

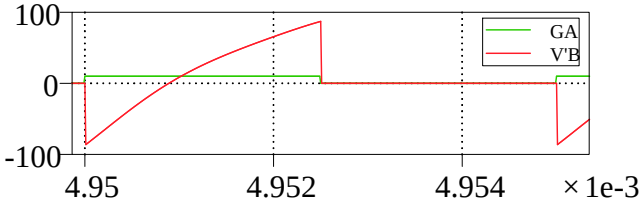


Figure 2–16 k=0.5, fsw=200 kHz

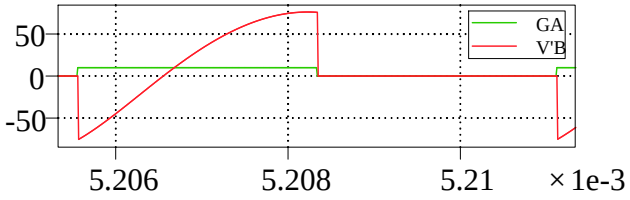


Figure 2–17 k=0.5, fsw=180 kHz

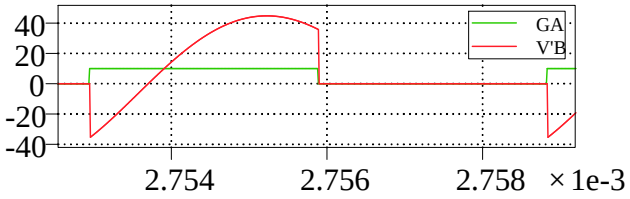


Figure 2–18 k=0.5, fsw=170 kHz

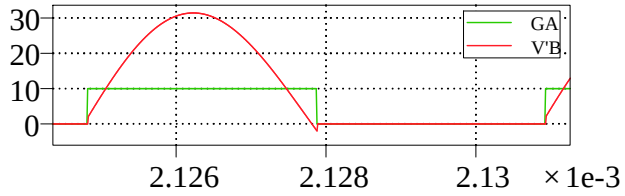


Figure 2–19 k=0.5, fsw=163.78 kHz (fzvs1)

2.5. Conclusions

The parallel-parallel current-fed push-pull converter has shown bifurcation phenomena as the magnetic coupling level between the primary and secondary coils increases, with the upper and lower ZVS points being stable and the middle one unstable. The investigation was done using approximate ac impedance analysis and accurate stroboscopic mapping modelling methods. Through forced frequency operation, the dynamic processes of the system waveform transition between ZVS points are revealed. Under bifurcation, the system tends toward the stable ZVS frequencies and away from the unstable middle ZVS frequency, which causes a significant drop in power transfer capability.

Chapter 3

Variable Frequency Primary Side Power Flow Controller with Pre-defined Upper Boundary

3.1. Introduction

A power flow controller can be developed at the primary side of an IPT system to regulate the power flow to a heart pump at the secondary side. The controller should maintain the output voltage at a constant level despite the presence of variations in magnetic coupling level and load resistance. Patient movement or tissue regrowth after implantation can cause direct distance, lateral or angular displacements between the TET coils. Variations in coil displacements will change the magnetic coupling and affect the system power transfer capability. The equivalent load resistance may change when blood flow and pressure vary under different patient physiological states, which also requires the controller to regulate the power flow.

Implanted heart pumps currently in use are powered by percutaneous drivelines, which are a major source of infection [21]. Wireless power transfer [96-98] for heart pump applications is known as transcutaneous energy transfer (TET), which can deliver power without the percutaneous driveline and its associated risks. As previously mentioned (in Chapter 1), Si *et al.* have proposed a variable resonant frequency method for power regulation [35] by changing the effective capacitance of the primary through switching in and out parallel capacitors to the primary MOSFETs. Dissanayake *et al.* [34] successfully implemented this frequency control in a TET system for powering heart pumps. This approach requires the system to have more switching devices and resonant capacitors.

Thrimawithana *et al.* [99-103] have proposed and analysed a split capacitor push-pull parallel resonant converter (SC-PPRC) in three different operational modes – namely buck, normal and boost modes. The SC-PPRC changes its frequency and duty cycle simultaneously to achieve the ZVS condition at a range of operational frequencies, and

the SC-PPRC can regulate power flow by varying the switching frequency directly. The boost version of SC-PPRC is so named because, as the operating frequency reduces, the peak resonant voltage increases.

In this study, a new frequency controller operating solely via a slow feedback loop is proposed for TET systems to deliver rated power for implanted heart pumps. The switching frequency regulation range was chosen to ensure a monotonic relationship between frequency and power flow; this allows the use of simple proportional and integral control to vary the system switching frequency. The switching frequency range is set below the system's lowest resonant tank zero voltage switching frequency, leading to resonant tank shorting (but no instant resonant capacitor shorting), and ZVS operation during MOSFET commutation without the need of fast detection circuitry. This controller also offers the advantage of reduced switching components and capacitors compared to the variable frequency circuit of Dissanayake *et al.* [34], and leads to a saving of about 25% in physical space as shown by Figure 3–1. The systems of Thrimawithana *et al.* operate in open-loop without feedback and output regulation. The system of Dissanayake *et al.* requires feedback from the primary resonant waveform which is oscillating at approximately 180kHz to derive gate driving signals. Here, the proposed system only need to feed back the dc output voltage and is therefore a slow feedback system.

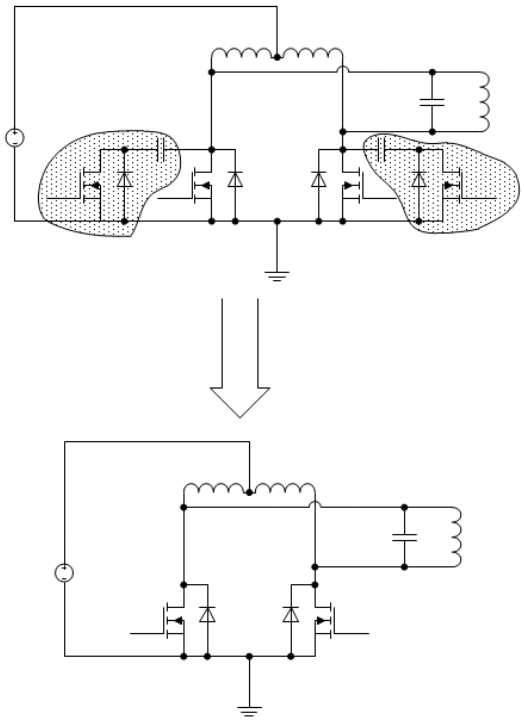


Figure 3–1 Space saving on primary side

3.2. System Overview

Figure 3–2 shows the proposed TET system with a proportional and integral (PI) controller. The system includes a push-pull parallel tuned resonant converter to invert a dc input voltage into a high frequency current flowing through a primary coil. A secondary pickup coil (with a quality factor Q of about 165) is coupled to the primary coil (with a quality factor Q of about 205) by magnetic induction. Then the pickup coil is parallel tuned and the induced voltage rectified to output a dc voltage to drive the load. The quality factors here are unloaded Q_u of the coils given by (3.1), where the resistance is the equivalent series resistance of the coil (ESR).

$$Q_u = \frac{\omega L}{\mathrm{R}_{esr}} \tag{3.1}$$

The load voltage is detected and sent back to the controller via a radio frequency (RF) channel, which makes use of the already available RF channel used for physiological sensors in an implantable heart pump application. The proposed controller compares the received feedback information with a pre-set reference V_{ref}, and the difference is regulated by the PI controller to generate a dc signal, which is fed into a voltage controlled oscillator (VCO) to generate gate drive signals G'_A and G'_B (inversion of G'_A) at a certain frequency.

The controller can operate in two separate gate drive modes by a manual selection switch: the basic mode and enhanced mode. In the basic mode, G'_A and G'_B are used to drive the two MOSFETs directly at 50% duty cycle after a gate drive circuit. One of the body diodes of the two MOSFETs would be conducting if the resonant tank needed to be shorted, as will be discussed later. The basic mode is based solely on a slow feedback PI loop, and does not require any fast detection, which simplifies the speed and timing requirement of the feedback channel and its components. Alternatively, in the enhanced mode, both MOSFETs would be ON during resonant tank shorting periods to reduce the voltage drop of the body diodes so as to improve the power efficiency. However, the enhanced mode requires an additional logic circuit that would require fast detection for resonant tank voltage as shown in Figure 3–2.

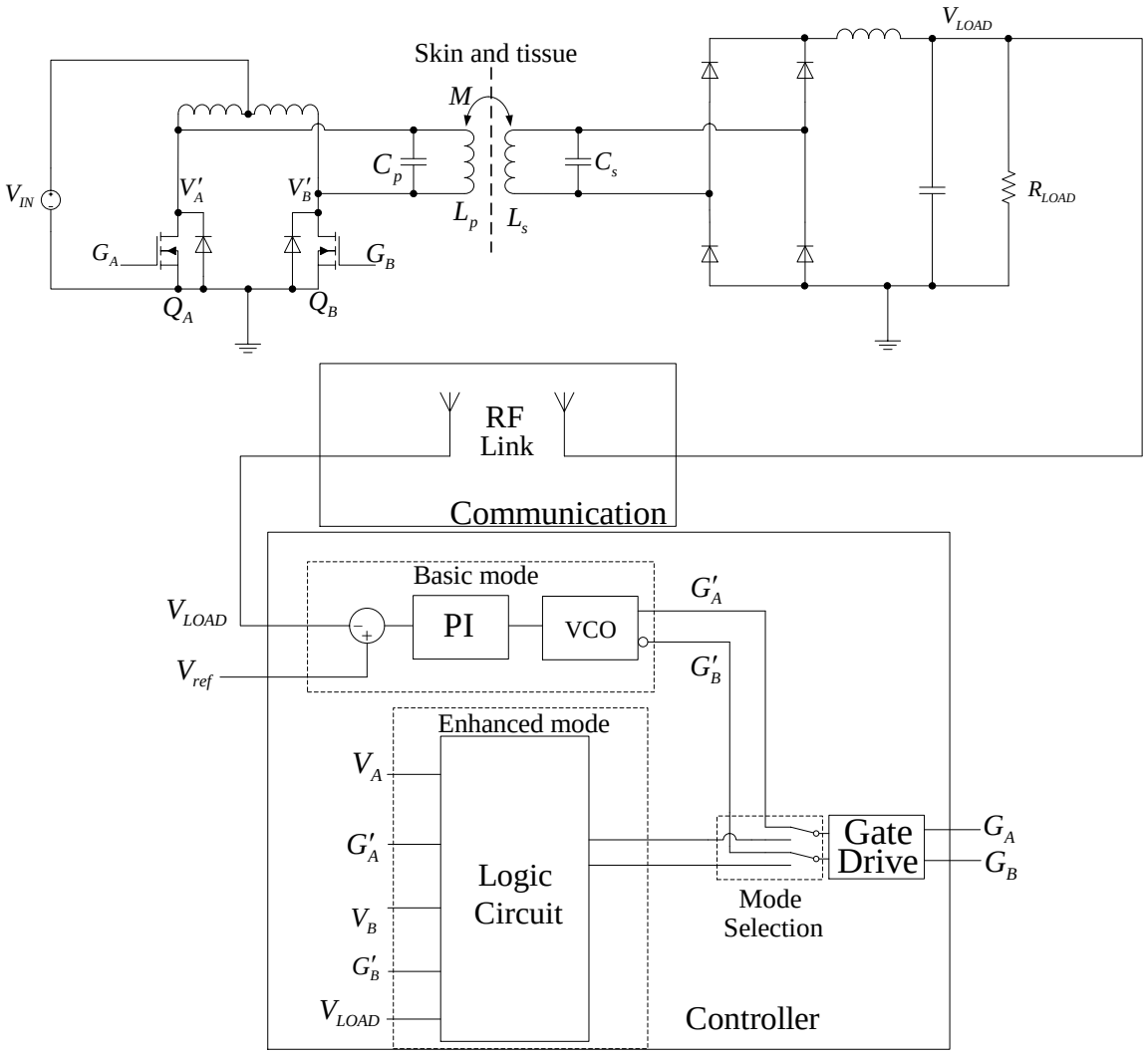


Figure 3–2 System overview

Figure 3–3 illustrates the ideal circuit waveforms of the proposed system. V_{AB} is the differential resonant tank waveform measured across the resonant capacitor; V_A and V_B are comparator results of MOSFET drain to source voltages (V'_A and V'_B) with respect to ground. The primary MOSFETs Q_A and Q_B can be driven either by the basic mode, G'_A and G'_B, which are simply the VCO outputs or by the enhanced mode, G_A and G_B.

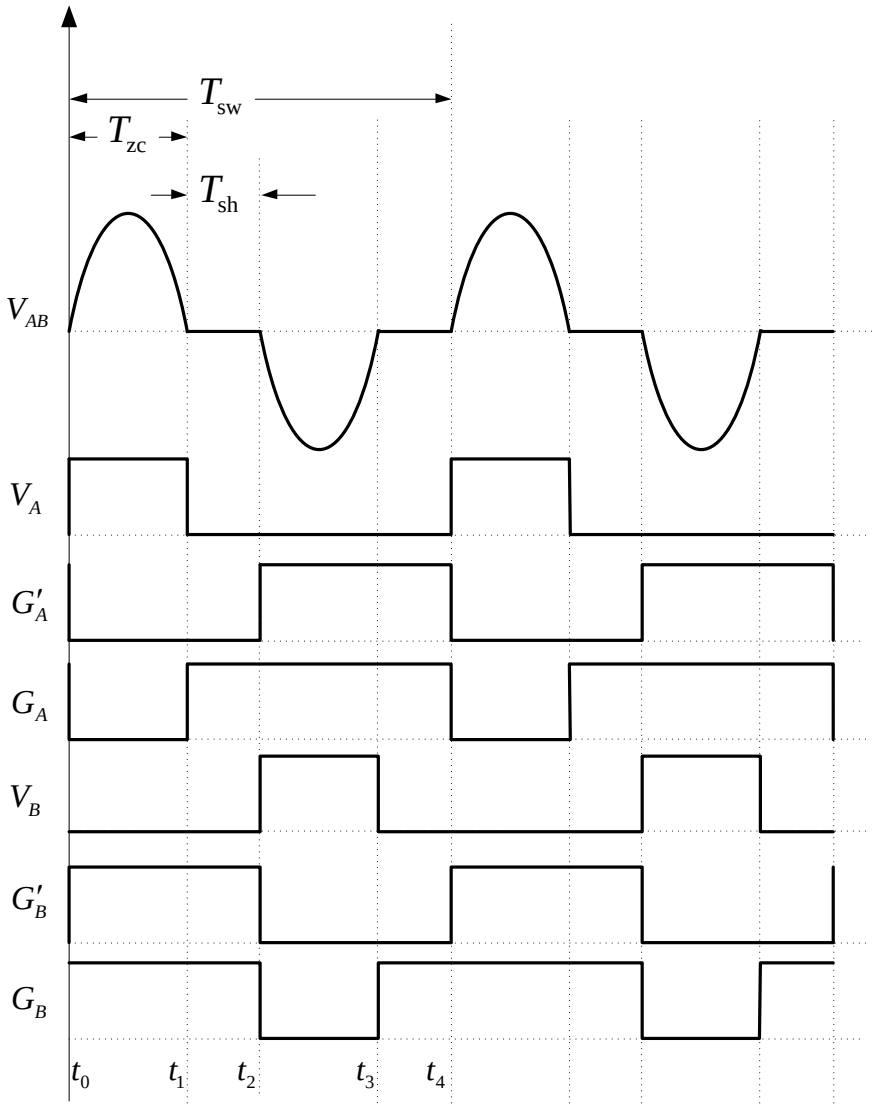


Figure 3–3 Primary control system ideal waveforms

In the basic gate driving mode, the MOSFET body diodes will take turns to conduct during consecutive resonant tank shorting periods (T_{sh}); note that T_{sh} occurs twice every switching period (T_{sw}), T_{zc} is the zero crossing period, which is the duration in between two T_{sh}. In enhanced gate drive mode, the MOSFETs' body diodes will cease to conduct as both MOSFETs are ON simultaneously during all T_{sh}. The circuit operation and current flow for basic mode and enhanced mode are shown in Figure 3–4 and Figure 3–5 respectively.

Instant capacitor shorting must be avoided to prevent damage to the capacitor and switching components. It will occur whenever MOSFETs are switched ON where there is a voltage present across the resonant capacitor leading to an unwanted high shorting current.

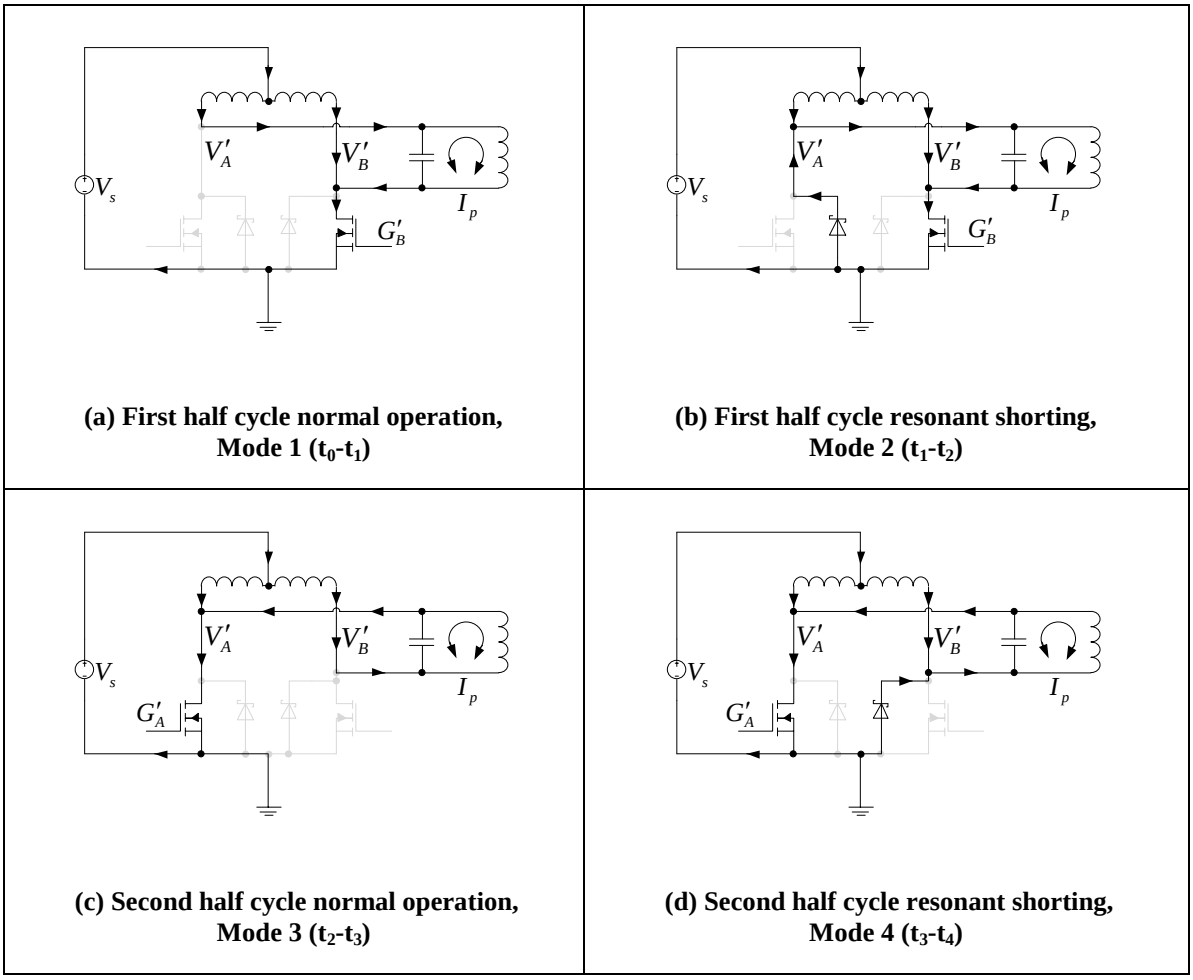
Instant capacitor shorting must not be confused with resonant tank shorting in the proposed controller. Resonant tank shorting occurs when MOSFETs are driven with a system switching frequency (f_{sw}) that is below the lowest system ZVS frequency, which means the resonant tank will resonate and then be shorted for a short period by a current loop formed by the two MOSFETs including their body diodes, if basic mode control is employed.

3.3. Determination of Switching Frequency Regulation Range

3.3.1. Finding System ZVS Frequency

It is necessary to solve (2.8) to find the zero voltage switching frequency (f_{zvs}) points of the system, in order to determine an operating frequency range that avoids instant capacitor shorting. At a f_{zvs} point, the circuit inductive and capacitive elements cancel each other, making the impedance purely resistive. The number of f_{zvs} points as well as their actual values are influenced by system parameters; for TET, important parameters are the load resistance and coupling levels. Under certain conditions, the system will have more than one zero voltage switching frequency, causing it to bifurcate. Similar bifurcation phenomena have also been found and studied in resonant converters in other wireless power transfer systems [71, 72, 91, 95, 104].

Figure 3–6 ignores all equivalent series resistances (ESR) of inductances and capacitances for simplicity. By employing the same approach discussed in Section 2.2.1 – equating the complex components of Z_p to zero and finding the phase plot zero crossings – (3.2) can be solved to give the approximate system f_{zvs} points. Stroboscopic mapping method can be used to attain a more accurate ZVS bifurcation plot [71]. The resistance, R in (3.2) is the effective load resistance seen by the resonant tank. For a full bridge rectifier, the relationship between R and the load resistance is given by (3.3).



(a) First half cycle normal operation, Mode 1 (t_0-t_1)

(b) First half cycle resonant shorting, Mode 2 (t_1-t_2)

(c) Second half cycle normal operation, Mode 3 (t_2-t_3)

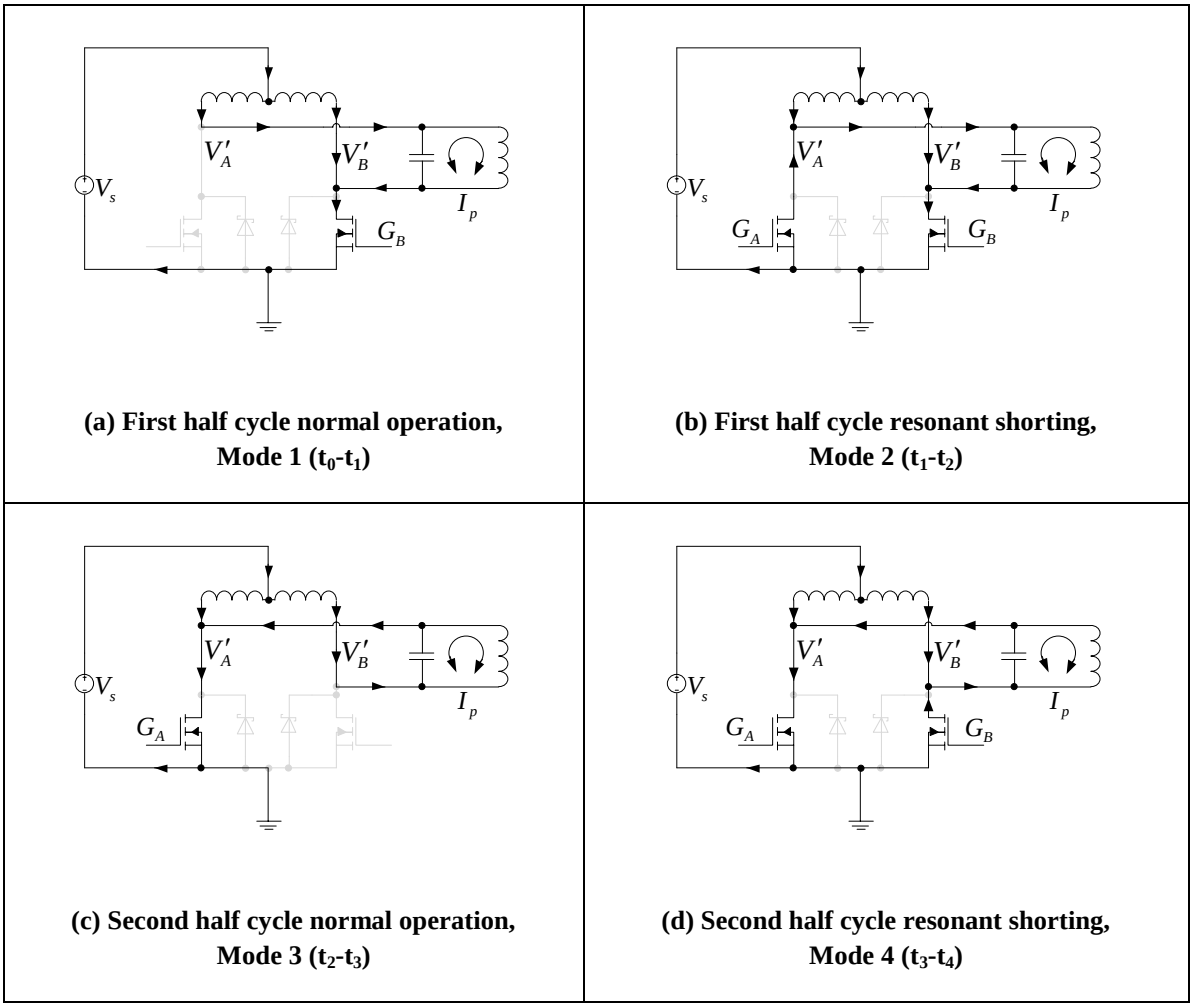
(d) Second half cycle resonant shorting, Mode 4 (t_3-t_4)

Figure 3–4 Basic mode circuit operation and current flow during entire operation cycle. The resonant tank contains resonating voltage during Mode 1(t_0-t_1) and Mode 3 (t_2-t_3), and resonant tank shorting occurs in Mode 2 (t_1-t_2) and Mode 4 (t_3-t_4) with a body diode closing the resonant shorting loop.

$$\omega^6 C_p C_s^2 R^2 \left(L_p L_s - M^2\right)^2 - \omega^4 \left(L_p L_s - M^2\right)\left[L_p C_p C_s R^2 + C_s R^2 \left(L_p C_p + L_s C_s\right) - C_p \left(L_p L_s - M^2\right)\right]$$
$$-\omega^2 \left[L_s \left(L_p L_s - M^2\right) - L_p R^2 \left(L_p C_p + L_s C_s\right) - C_s R^2 \left(L_p L_s - M^2\right)\right] - L_p R^2 = 0 \quad (3.2)$$

$$R = \frac{\pi^2}{8} R_{LOAD} \quad (3.3)$$

There are two graphical approaches to find f_{zvs}. Firstly and more conveniently LTspice can frequency sweep the circuit in Figure 3–6 to give phase plots of Z_p. The induced voltages from primary to secondary and vice versa need not be included during LTspice simulations as they are integral part of L_p and L_s. To represent the system more accurately, primary and secondary ESR of capacitances and inductances are included. Secondly, MATLAB can plot f_{zvs} bifurcation trends while stepping load resistance or coupling coefficients.



(a) First half cycle normal operation, Mode 1 (t_0-t_1)

(b) First half cycle resonant shorting, Mode 2 (t_1-t_2)

(c) Second half cycle normal operation, Mode 3 (t_2-t_3)

(d) Second half cycle resonant shorting, Mode 4 (t_3-t_4)

Figure 3–5 Enhanced mode circuit operation and current flow during entire operation cycle. The resonant tank contains resonating voltage during Mode 1(t_0-t_1) and Mode 3 (t_2-t_3), and resonant tank shorting occurs in Mode 2 (t_1-t_2) and Mode 4 (t_3-t_4) with both MOSFETs conducting to close the resonant shorting loop.

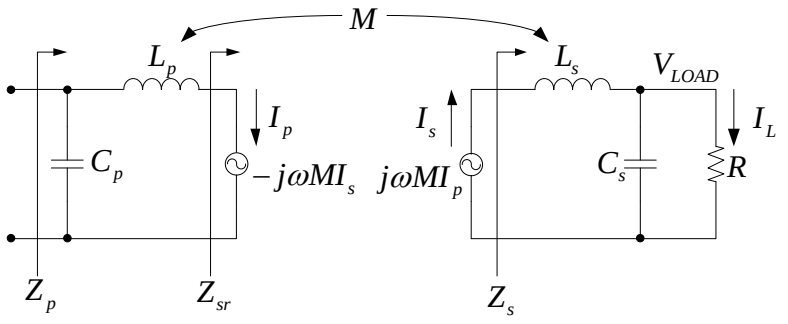


Figure 3–6 Circuit used to find system impedance phase angle

To differentiate between non-bifurcated and bifurcated system operating conditions, Figure 3–7 shows a single phase plot zero crossing, meaning one f_{zvs} point, while Figure 3–8 shows three phase plot zero crossings indicating f_{zvs} bifurcation with three f_{zvs} points.

3.3.2. Switching Frequency Regulation Range

Instant capacitor shorting is to be avoided. It occurs at negative resonant tank impedance phase angles, and thus the system must be constrained to operate in a f_{sw} regulation range with positive phase angles. The system can operate either in non-bifurcated or in bifurcated conditions. Figure 3–7 shows the load power, phase angle and impedance magnitude plot for a non-bifurcated condition. The phase angle is positive when f_{sw} is below f_{zvs} and is negative when f_{sw} is above f_{zvs}. During a bifurcated condition as shown by Figure 3–8, there are three f_{zvs} points, with positive phase angles when f_{sw} falls below f_{zvs1} or in between f_{zvs2} and f_{zvs3}. The frequency range between f_{zvs2} and f_{zvs3} may be utilised in theory since it has positive phase angles and will avoid instant capacitor shorting, but this frequency range is variable under different loading and coupling conditions, and it is difficult to track its bounds, operating inside that range was avoided. Therefore, in both non-bifurcated and bifurcated conditions, the f_{sw} regulation range must be less than or equal to the lowest f_{zvs}.

The PI action operates on a monotonic and positive load power over frequency slope. Under steady state operation and ignoring the effect of harmonics, the primary resonant tank is driven by a sinusoidal voltage source, this means for impedance analysis, the primary side resonant capacitance can be ignored making the resonant tank 3^{rd} order; a frequency sweep in LTspice gives Figure 3–7 and Figure 3–8, which shows there is only one peak for the load power while two peaks emerge in impedance magnitude upon bifurcation. With the load power peak greater than f_{zvs1}, the load power over frequency slope remains positive and monotonic, so the upper frequency boundary should remain at f_{zvs1}. Here, the magnitude of the load power peaks are indicative only – actual peaks should be acquired through physical measurements.

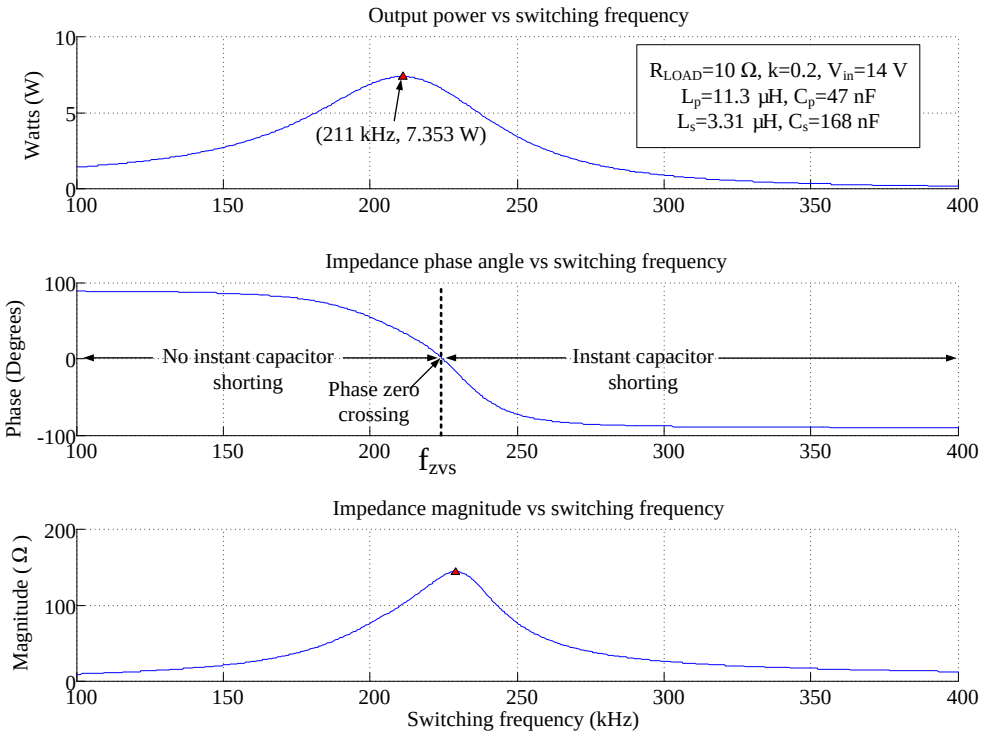


Figure 3–7 Output power, phase and magnitude plot of a non-bifurcated system

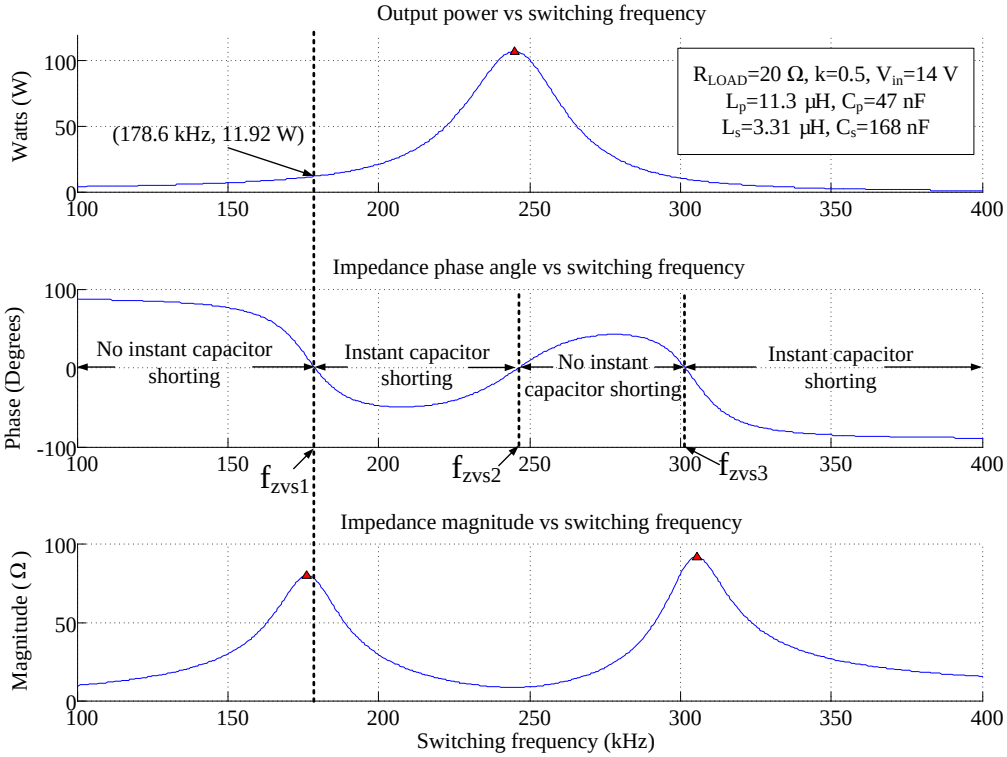


Figure 3–8 Output power, phase and magnitude plot of a bifurcated system

The lower boundary of the f_{sw} regulation range will be affected by a resonant tank voltage boosting effect in the converter as f_{sw} range decreases. Despite the differences between

the proposed controller and SC-PPRC, the analysis done by Thrimawithana *et al.* [102, 103] for boost mode SC-PPRC can be used to explain the boosting effect. Varying f_{sw} has two effects on power flow. The dominating effect in the proposed controller is frequency tuning and detuning as f_{sw} moves toward and away from f_{zvs1}; the lesser effect is change in resonant tank peak voltage (V_{pk}) and resonant tank RMS voltage (V_{rms}) with f_{sw}. An increase in the switching period (T_{sw}) will lead to an increase in V_{rms} as shown in (3.4), leading to increased power transfer.

$$V_{\text{rms}} = \frac{1}{2}\pi V_{IN}\sqrt{\frac{T_{sw}}{T_{zc}}} \tag{3.4}$$

In addition, because f_{sw} reduces as T_{sw} increases, the system will become increasingly detuned with a dropping power flow. However V_{rms} will be increasing to raise the power flow, and these two power flow effects will superpose. There will be a crossover point when the magnitude boosting effect overrides the frequency tuning effect, and this point shall be the theoretical lower f_{sw} boundary to maintain the monotonic relationship between power flow and f_{sw}.

The quality factor (Q) of the system will affect the frequency regulation range. If Q is increased, it means the magnitude is more sensitive to changes in frequency, and then to maintain the same variation in magnitude, the frequency range would be narrower. Conversely, if Q is decreased, the frequency range would need to be wider.

3.3.3. Phase Plot Trends and Bifurcation Plots

At increased loading or coupling level, bifurcation results when the number of phase zero crossing points increases from one to three. A series of phase plots can be summarised within a bifurcation trend plot, which shows f_{zvs} points while a system parameter is being stepped, usually coupling level or load resistance. When the primary and secondary resonant tanks are tuned to pre-set nominal frequency (f_0) (given by (3.5) and (3.6)), with increased loading or coupling level leading to f_{zvs} bifurcation, two additional f_{zvs} emerge on either side of original f_{zvs}. These two points will depart from the original f_{zvs}, with one rising and the other falling in frequency. Figure 3–9 shows the bifurcation plot for the proposed system while stepping the coupling coefficient – coupling level increase spreads bifurcated f_{zvs} points apart with a decreasing lower ZVS branch. In this case the system parameters are not exactly tuned to the nominal frequency, and on bifurcation the two

additional f_{zvs} appear below the original f_{zvs}. When the primary and secondary resonant tanks are tuned to (3.7) and (3.8) respectively, the three possible ZVS branch locations upon bifurcation are expressed in (3.9).

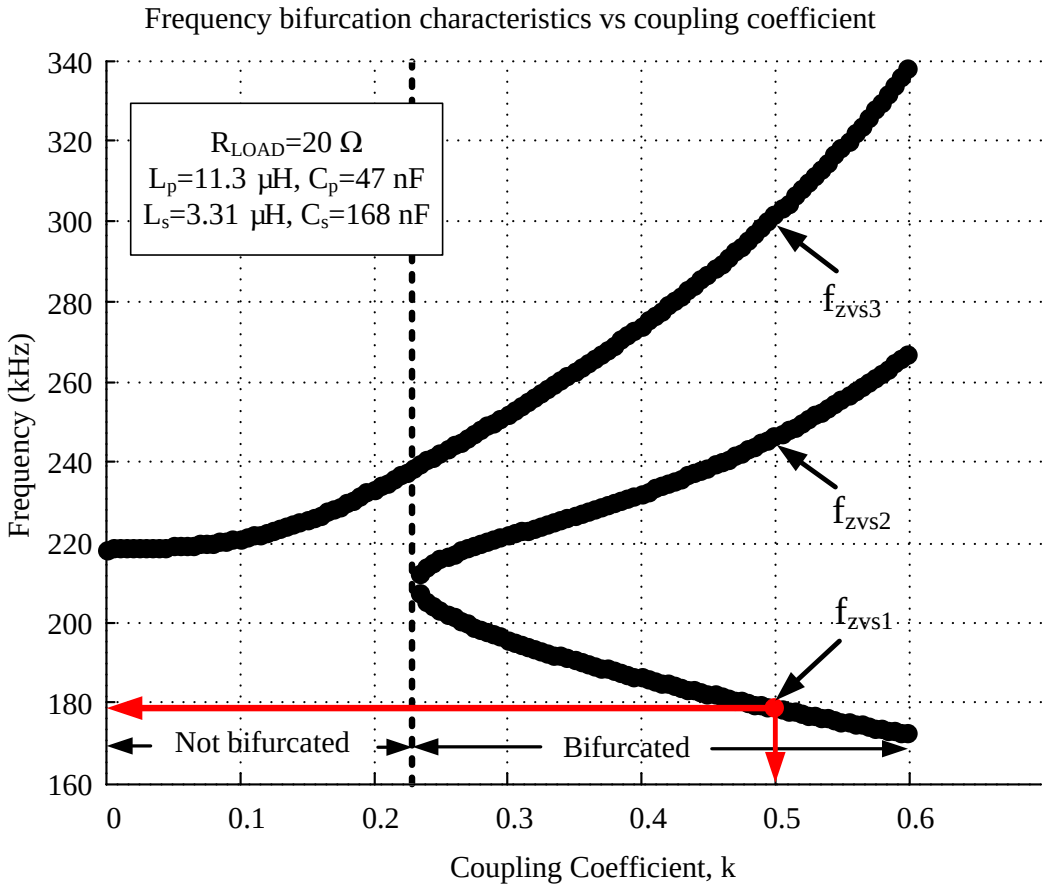


Figure 3–9 Switching frequency bifurcation plot with coupling coefficient

$$\omega_0 = 2\pi f_0 \tag{3.5}$$

$$\omega_0^2 = \frac{1}{L_p C_p} = \frac{1}{L_s C_s} \tag{3.6}$$

$$\omega_p^2 = \frac{1}{L_p C_p} \tag{3.7}$$

$$\omega_s^2 = \frac{1}{L_s C_s} \tag{3.8}$$

$$\begin{cases} \omega_p = \omega_s = \omega_0 & \text{two additional } f_{zvs} \text{ appear on either side of original } f_{zvs} \\ \omega_p > \omega_s & \text{two additional } f_{zvs} \text{ appear below the original } f_{zvs} \\ \omega_p < \omega_s & \text{two additional } f_{zvs} \text{ appear above the original } f_{zvs} \end{cases} \quad (3.9)$$

3.4. Controller Design

3.4.1. Finding the Switching Frequency Regulation Range

The highest coupling level and highest load resistance need to be considered to find the switching frequency regulation range, as this will give the worst case scenario giving the lowest expected ZVS point on bifurcation. The system will be constrained to work below this worst case ZVS point and above the switching frequency when magnitude boosting effect overrides frequency tuning effect.

The practical TET coils used for primary and secondary are encased in silicone with the same diameter of 50mm, but the primary is double layered and the secondary is single layered. The maximum coupling coefficient is 0.5 when the TET coils are flat against each other without lateral displacement. Such a best coupling condition is used to find the upper frequency boundary of the controller. The nominal load of the heart pump is equivalent to 10Ω, which translates to a loaded quality factor of 5.63 and 1.41 at primary (Q_p) and secondary (Q_s) circuits respectively. The parallel-tuned loaded quality factors are represented in (3.10) and (3.11) respectively. To find Q_p, one need to first find the reflected inductance and resistances, then find the net inductances and resistances. The resistance of Q_s is the effective load resistance seen by the resonant tank.

$$Q_p = \frac{\omega L_{net}}{R_{net}} \quad (3.10)$$

$$Q_s = \frac{R_L}{\omega L_s} \quad (3.11)$$

The thesis also investigates a load variation up to 20Ω in order to study a severe bifurcated situation. Figure 3–8 shows the load power, phase and magnitude sweep of the system with a coupling coefficient of 0.5 and a load resistance of 20Ω. Other system parameters are L_p (11.3 µH), C_p (47nF), L_s (3.31 µH) and C_s (168nF). The inductances and capacitances are selected so that the primary and secondary resonate at a nominal frequency. The equivalent mutual inductance at the highest coupling level is M (3.06 µH).

By applying (3.2), the six roots are ±178.60, ±245.85 and ±302.07. However, only positive frequencies are practically possible, so the system ZVS points are 178.60kHz (f_{zvs1}), 245.85kHz (f_{zvs2}) and 302.07kHz (f_{zvs3}), which are shown in Figure 3–9. The lowest ZVS point being 178.60kHz or f_{zvs1} is set as the upper f_{sw} boundary. As shown by Figure 3–8, at f_{zvs1} the maximum load power potential (11.92W) is greater than the rated 10W power, and the frequency controller then regulates the excess power by detuning and decreasing the switching frequency. When coupling decreases, frequency then increases to regain the previously detuned power flow.

As a practical verification of the calculated upper frequency boundary for power flow regulation, let the proposed controller run in open loop with a desirable dc input voltage (V_{IN}), and the highest expected coupling level and load resistance. Then, start at a switching frequency lower than the theoretical f_{zvs1} and tune the f_{sw} upwards toward a ZVS point by avoiding instant capacitor shorting. This practical ZVS point can be used as the upper frequency boundary. The location of theoretical f_{zvs1} approximates the practical; the process used to attain the theoretical calculations assumes the resonant tank to be fed with perfect sinusoidal waveforms of different frequencies, whereas practical waveforms are distorted by differing load resistance, coupling level, practical component drifts, parasitic elements, the resonant tank shorting period and its associated magnitude boosting effect. These factors can offset the practical results from the theoretical and change the location of f_{zvs1}.

When the coupling is weak and the system is not bifurcated, for example with a coupling coefficient of 0.2 and load of 10Ω as shown by Figure 3–7. From (3.2) the six roots are -212.19±j31.84, 212.19±j31.84, ±225.08. Clearly only 225.08kHz is a valid frequency; this frequency is the one and only unique f_{zvs} point for the system to operate under. Note that this f_{zvs} is 46kHz higher than the upper boundary operating frequency corresponding to the closest coupling and bifurcated situation. With these parameters, the system fails to regulate load power at 10W as its maximum power potential is only 7.35W. This means the power flow controller has insufficient power to regulate with through frequency tuning, so this particular operational point is outside the frequency regulation range. In order to supply rated power, the system parameters must be re-designed, which can include coil size, make and geometry, operating frequency and so forth.

When accounting for component variations and other factors, a frequency margin is needed in practical design to ensure the system can work properly. This may affect the system's full power capability and the power efficiency slightly.

The lower f_{sw} boundary can be found empirically by operating the controller in open loop. The f_{sw} should be decreased away from the fully tuned state. The f_{sw} boundary will be when output voltage reaches a minimum and begin to rise. The lower boundary need not be at its theoretical minimum and can be set sufficiently low to allow enough room to regulate power flow downwards. In addition, as frequency lowers the magnitude boosting effects cause higher voltage rating requirements for primary MOSFETs.

3.4.2. PI Controller Parameters

The PI controller achieves regulation when V_{LOAD} equals V_{ref}. Important parameters that influence this process include the f_{sw} regulation range, V_{IN}, coupling level and the load resistance. To maximise the regulated coil separation range, the upper frequency boundary (f_{zvs1}) is first determined according to prior analysis, then under close loop, the TET coils are pushed flat against each other for the highest coupling level, then V_{IN} is increased so that PI action starts to regulate V_{LOAD} to V_{ref} by decreasing the frequency downwards. Stop increasing V_{IN} just before V_{LOAD} starts to increase beyond V_{ref}. This condition shows the signs of failing regulation and can be set as the lower boundary. This procedure is simplified in Figure 3–10 and ensures that the system is capable of regulating voltage down to V_{ref} under highest coupling level, and as the coupling level drops by separating the TET coils, PI action will increase f_{sw} to deliver more power, until the system reaches f_{zvs1} and the separation distance becomes too great to maintain V_{ref} at the load.

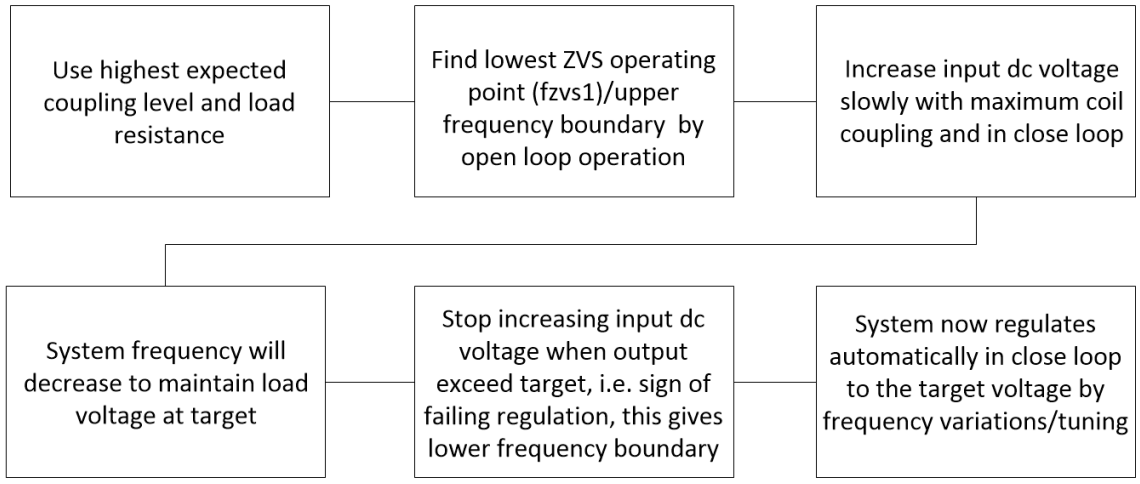


Figure 3–10 Steps to obtain the frequency regulation range

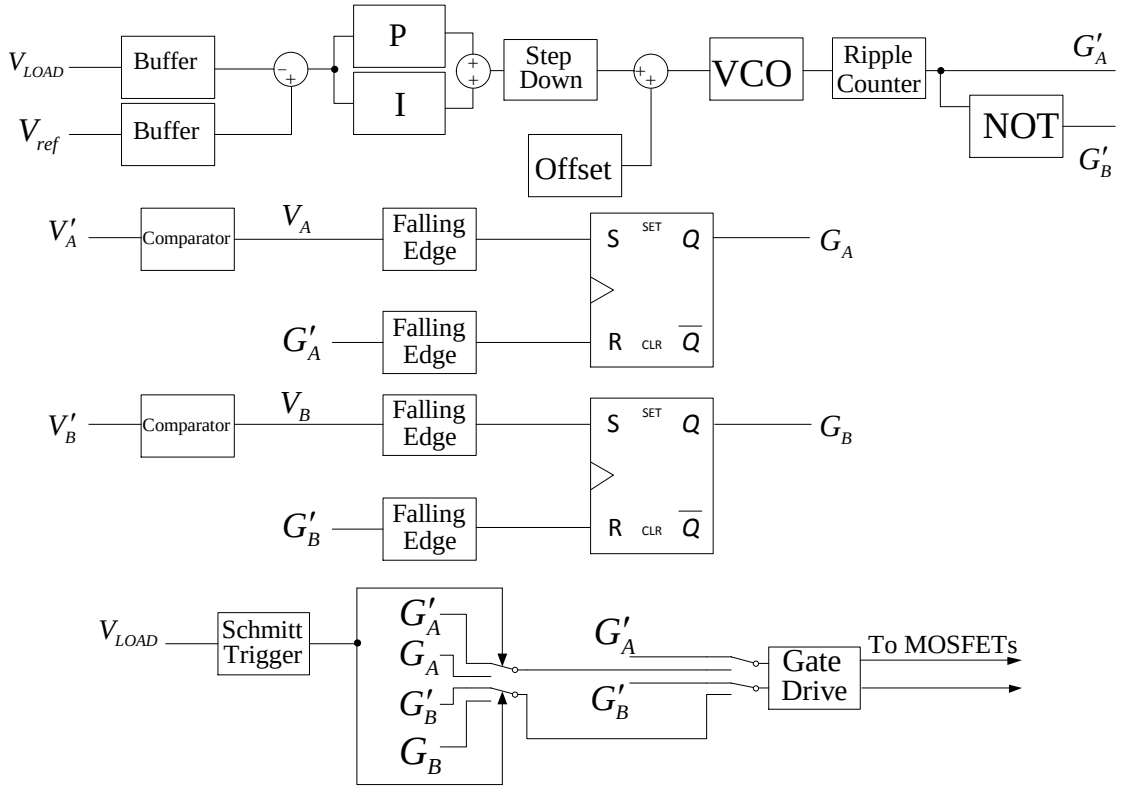


Figure 3–11 Controller details

3.4.3. Controller Hardware Design

The new controller as shown in Figure 3–11 has a PI to vary frequency and regulate the output power flow. This controller was built with discrete analogue components using OPAMPs, VCO and NAND gates. The OPAMPs achieve the needed buffering, differencing, summing, offsetting, proportional gain and integral gain functions of the PI controller; the PI output is stepped down through a potentiometer and an offset voltage is

added to complete the necessary frequency range level shifting. The resulting dc voltage level is processed by a VCO into a square wave, which is not 50% duty cycle, so a ripple counter can be used to halve the frequency of the VCO output in order to produce a 50% duty cycle waveform. NAND gates are used to realise the required NOT gate function in order to produce the complement of the VCO output resulting in G'_A and G'_B, which are two complementary 50% duty cycle basic mode gate driving signals. To generate MOSFET overlap conducting enhanced mode gate drive signals, G_A and G_B, the falling edge of V_A is used to set a SR latch while a falling edge of G'_A resets that SR latch producing G_A. Similarly a falling edge of V_B sets a second SR latch while a falling edge of G'_B resets the second SR latch producing G_B. The enhanced mode waveforms will step in after V_{LOAD} is above a threshold as it relies on the readiness of basic mode waveforms, G'_A and G'_B, as well as the comparator waveforms V_A and V_B. This design has used only discrete components to realise all the necessary elements of the power flow controller. However microcontrollers or FPGA can also be used to realise the controller. The output dc inductor normally conducts continuously to smooth the load current, while discontinuous operation reduces the smoothness of output voltage.

3.5. Simulation and Experimental Results

PLECS has been used to simulate the proposed controller and its PI action used to regulate the output voltage to 10V. The system switching frequency regulation range has been calculated according to the previous analysis and set to 140kHz to 180.26kHz. The simulated V_{IN} range for which regulation is achievable is between 23V and 28V for a load of 10Ω and a 0.2 coupling coefficient.

Similarly, a simulation study was undertaken using PLECS under different coupling and load variations. In all cases the calculated f_{sw} regulation range was used and V_{IN} set at 25V, the coupling regulation range was between 0.19 to 0.23 for a load of 10Ω, while the simulated load regulation range between 7Ω and 50Ω for a 0.2 coupling coefficient. If the f_{sw} regulation range is to increase by lowering the f_{sw} lower boundary, the simulated V_{IN}, coupling and load regulation ranges would also increase, leading to a larger f_{sw} regulation range and increased controller regulation capability. Note that the simulated regulation ranges are useful for guiding system design; they may not be exactly the same as the actual system operating ranges. Further details of this PLECS simulation can be found in Appendix B.

Practical TET systems require a regulated power of typically 10W at the heart pump; the power flow controller must overcome variations in TET coil separation and misalignment due to patient movement, which corresponds to variations in coupling level between primary and secondary. A 10Ω load is used to model a working heart pump approximately. The practical switching frequency regulation range is between 149.3kHz to 182.2 kHz. The proposed controller has demonstrated good power regulation of 10W to the load with a TET coil separation ranging from 4 mm to 10mm. Note that the minimum distance of 4mm in fact corresponds to the best coupling situation with the two coils touching – the distance is caused by the silicone casing. The 10mm distance is the lowest coupling level for maintaining the rated power delivery. Normally the system operates in a non-bifurcated condition; however when the TET coils are less than about 5mm from each other, the system may bifurcate. Under both non-bifurcated and bifurcated conditions the practical system continues to work well below the f_{zvs1} within its f_{sw} regulation range, and avoids instant capacitor shorting.

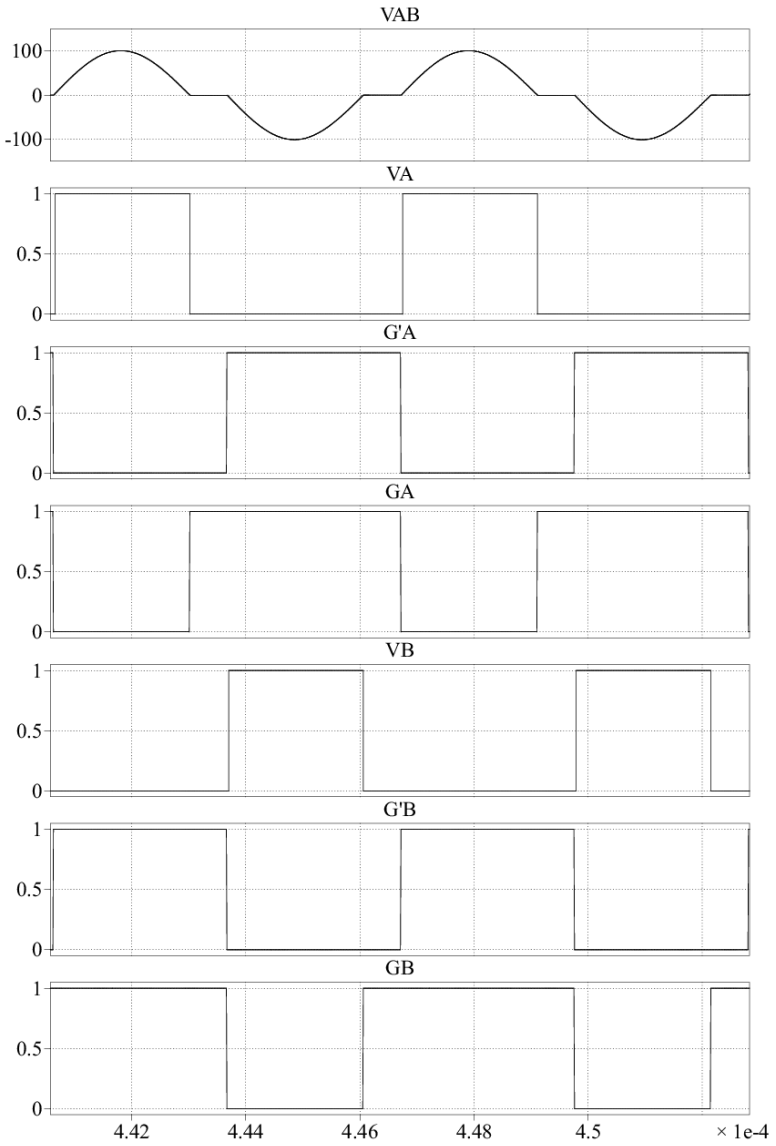


Figure 3–12 Simulation waveforms

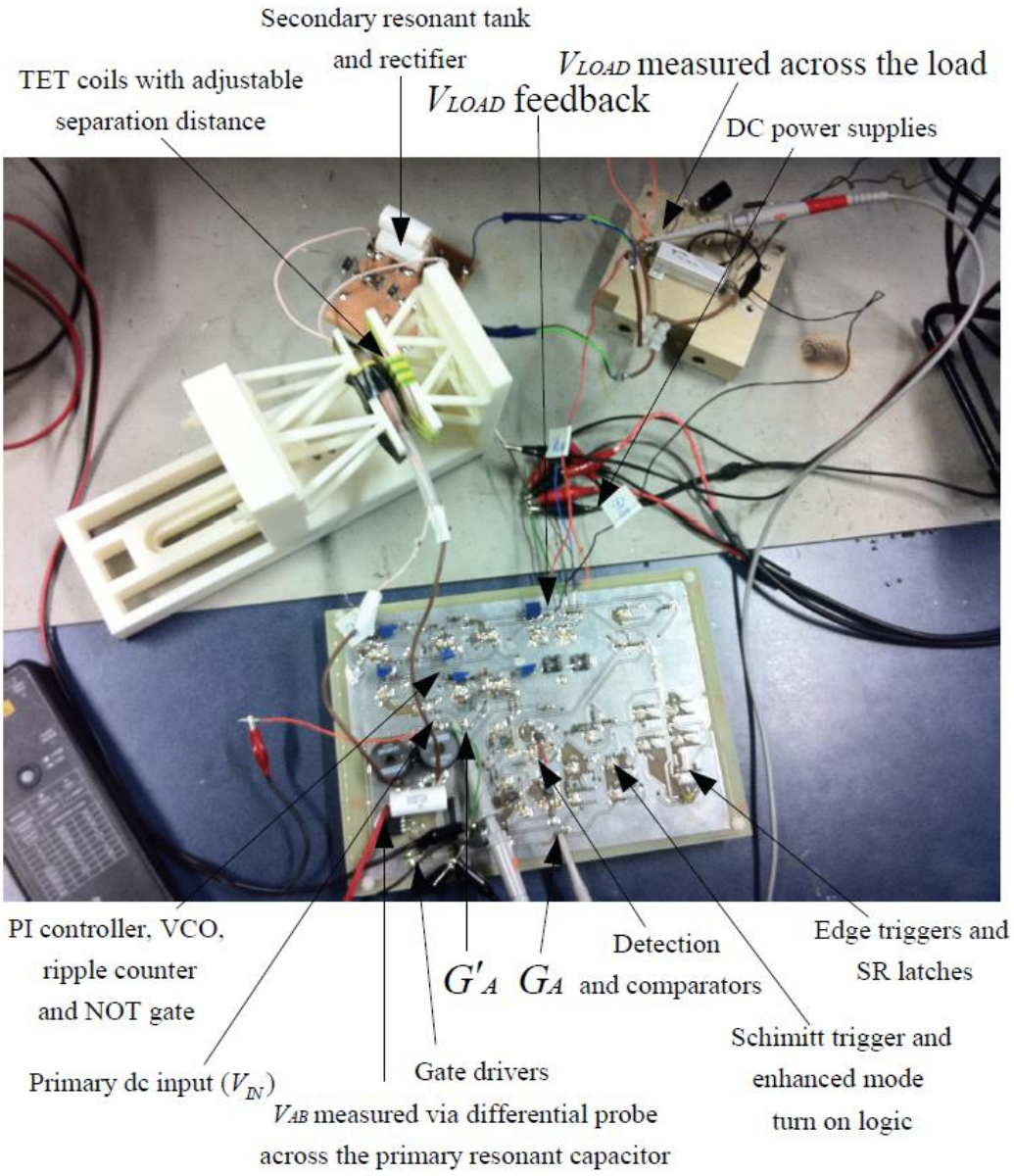


Figure 3–13 Practical measurement setup

The PLECS simulation circuit waveforms are shown in Figure 3–12, the practical measurement setup is shown in Figure 3–13, and the practical circuit waveforms of three different TET coil separation distances are shown in Figure 3–14, Figure 3–15 and Figure 3–16 under an input dc voltage of 14V. Note that in all cases the system was able to maintain 10V at the load side. It is clear that the practical measurement waveforms correspond well to the simulation circuit waveforms and to the ideal circuit waveforms illustrated in Figure 3–3. In all three practical circuit waveform figures, the top waveform is the differential resonant tank voltage, V_{AB}, the second waveform is the VCO output or basic mode gate driving waveform, G'_A. The next waveform is the enhanced mode gate driving waveforms, G_A and the last waveform is the load voltage, V_{LOAD}. The circuit

currently operates in enhanced mode. Operation under basic gate driving mode will give similar results, but due to body diode conduction during resonant tank shorting period, the efficiency drops slightly.

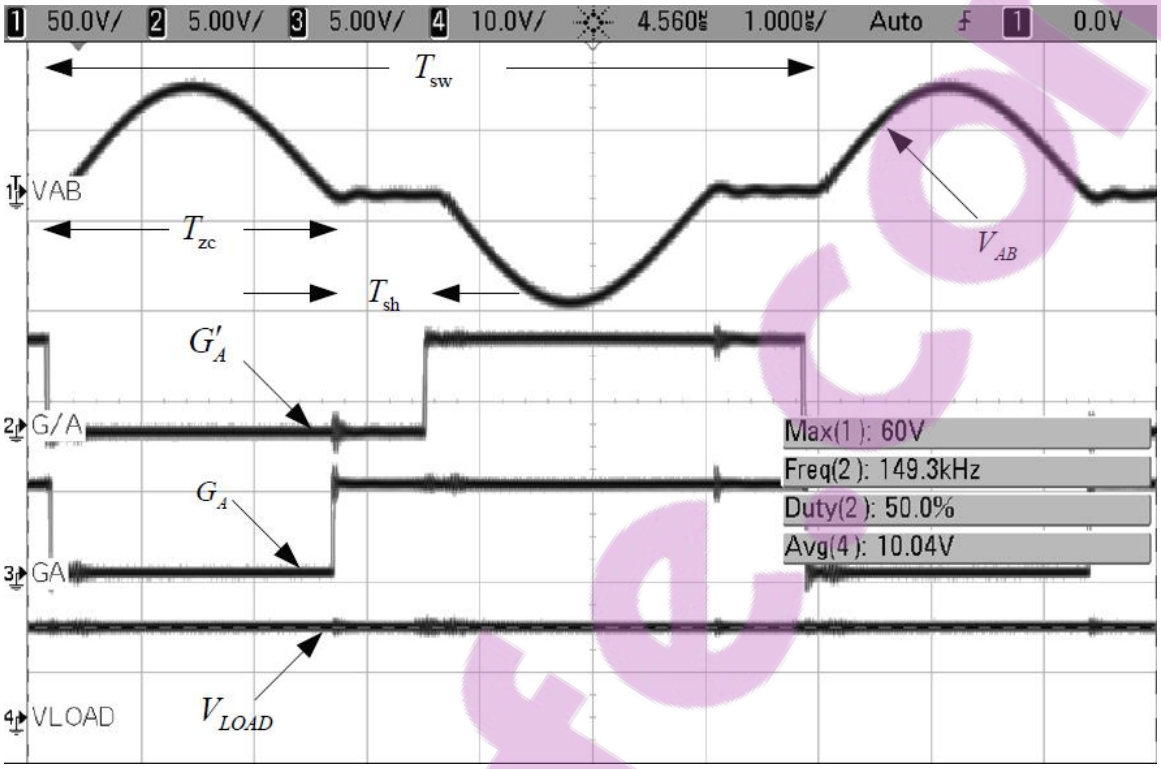


Figure 3–14 Practical circuit waveforms, TET coil separation of 4mm

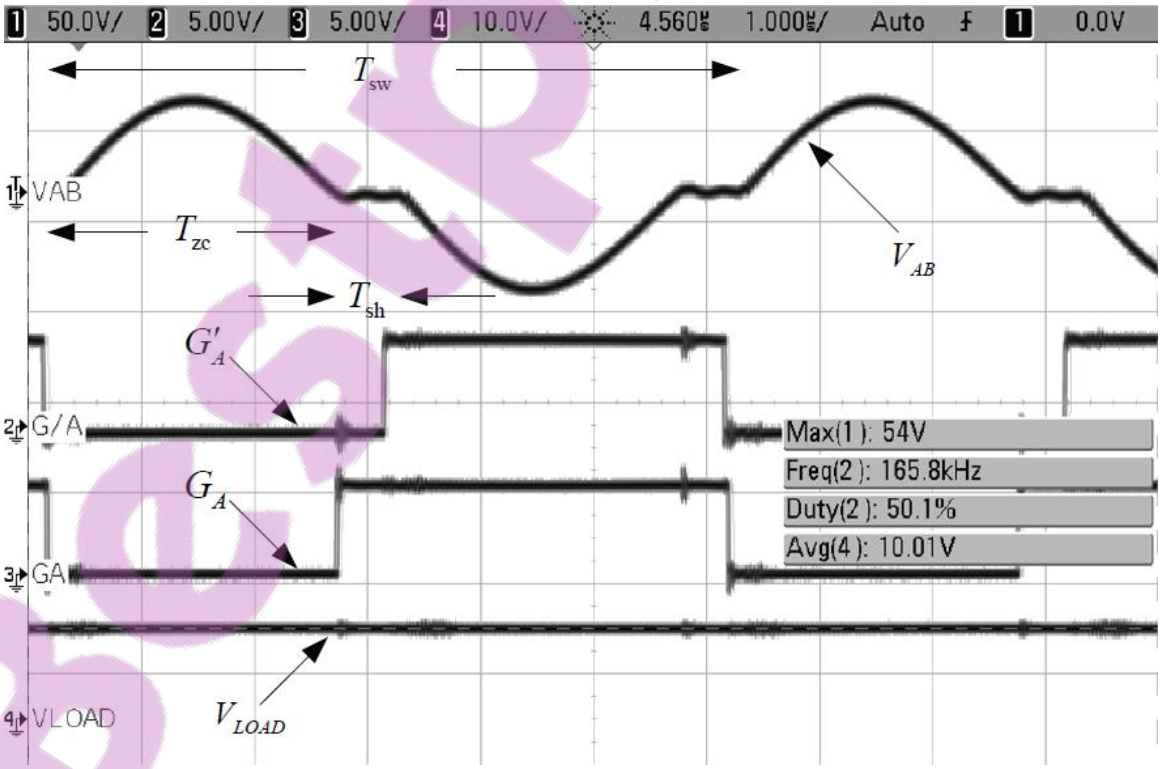


Figure 3–15 Practical circuit waveforms, TET coil separation of 7mm

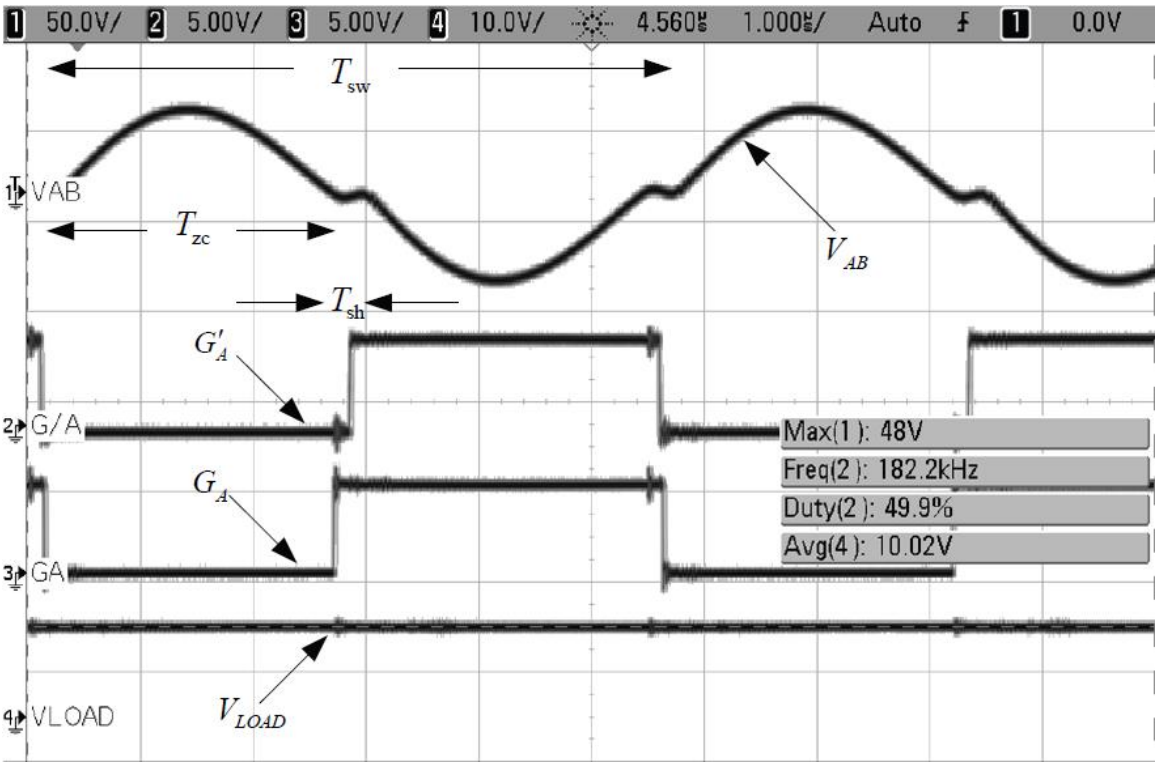


Figure 3–16 Practical circuit waveforms, TET coil separation of 10mm

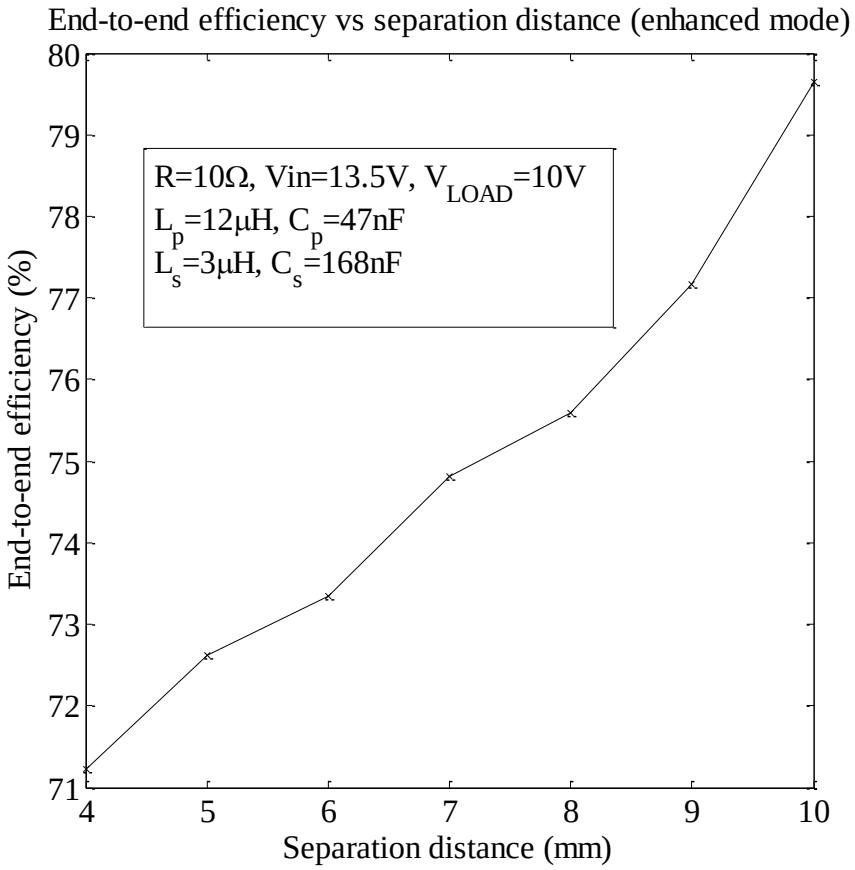


Figure 3–17 End-to-end efficiency vs. separation distance (enhanced mode)

The basic mode achieved an end-to-end efficiency of 77.97% compared to 79.65% for the enhanced mode when delivering 10W at TET coil separation of 10mm. Figure 3–17 shows the end-to-end efficiencies for enhanced mode operation under different direct separation distances, where the system is operating with close loop feedback to regulate V_{LOAD} at 10V. Here only the regulated separation range of up to 10mm is shown – larger separation is irrelevant as load regulation would fail. When TET coils are closer, frequency is lower to detune the excess power, which introduces more resonant shorting period. This is associated with increased coil current and losses. Therefore, efficiency would be lower at lesser coil separation, and as coil separation increases, frequency will increase to tune more power flow to compensate for the lesser magnetic coupling. This means less resonant shorting period, coil current and losses – efficiency would improve. This positive relationship between efficiency and coil separation would not continue indefinitely – load regulation fails with coil separation greater than 10mm, which means lower output power and efficiency. Figure 3–18 shows end-to-end efficiencies for enhanced mode under different V_{LOAD} by operating the system in open loop and varying the operating frequency. These efficiencies do not include controller power losses as the controller components are fed by separate ±15V and ±5V supplies. The end-to-end efficiency with controller loss is estimated to be above 70%.

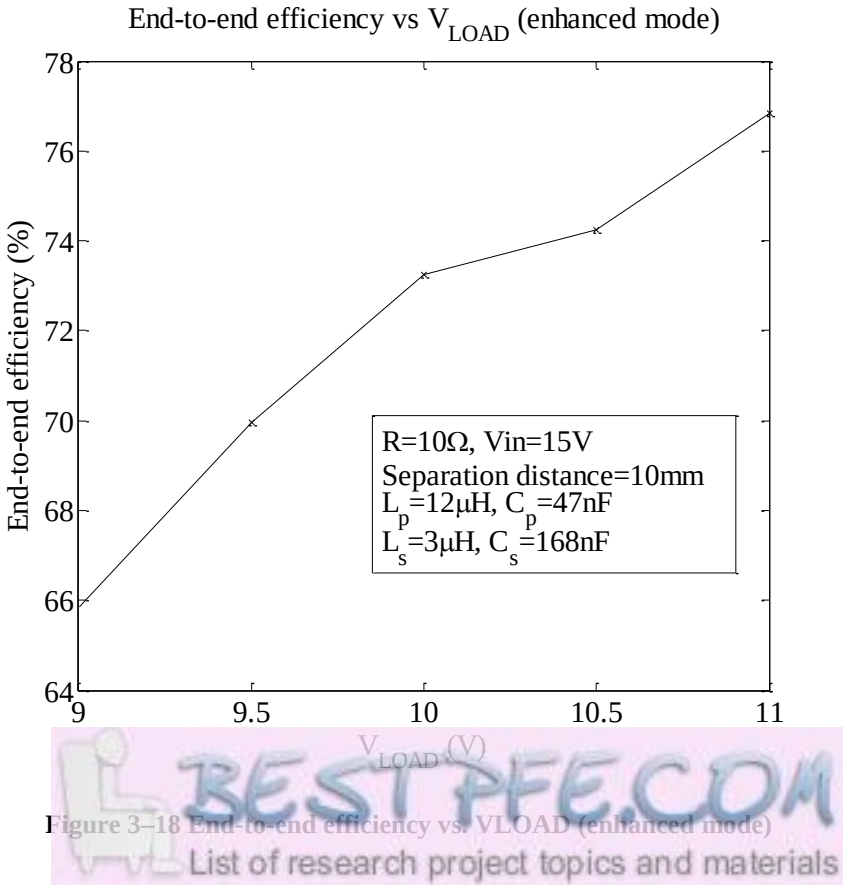


Figure 3–18 End-to-end efficiency vs. VLOAD (enhanced mode)

A demonstration system based on the proposed power flow controller has been made as shown in Figure 3–19, and it transfers wireless power from the primary to the secondary via a plastic human figure. The power received is used to drive a marine bilge pump to extract and pump blood coloured water from a fish tank around the human figure, imitating a human blood circulation system. The water is pumped through a series of transparent pipes and plastic tubes. The water eventually returns to the fish tank forming a complete circulation loop.

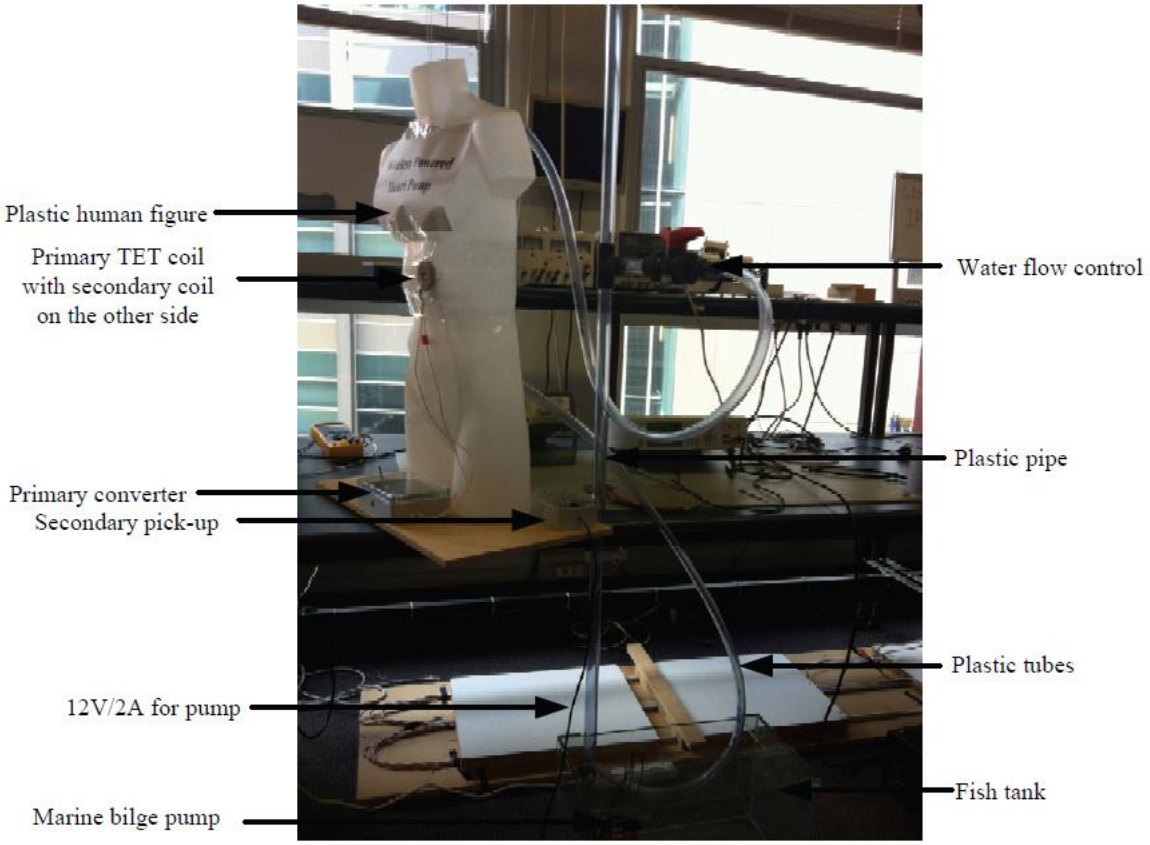


Figure 3–19 Demonstration system

3.6. Conclusions

A new power flow control method based on resonant tank shorting by slightly slow switching and shorting period detection has been proposed and developed for heart pump applications. The system has been analysed to determine the switching frequency regulation range to avoid instant capacitor shorting during operation. The system has reduced total switching component counts compared to the existing frequency controllers; leading to about 25% physical space savings, lower production costs and improved

reliability. The realised power flow controller has demonstrated 10W power regulation for up to a maximum coil separation of 10mm.

Chapter 4

Improved Primary Variable Frequency Power Flow Controller with Shorting Period Detection

4.1. Introduction

A basic primary power flow controller was developed to regulate heart pump load voltage level at the desired reference level, in Chapter 3 of this thesis. The controller worked well in regulating the output voltage but the coil separation range is very limited. The system operates below a fixed upper frequency boundary, which is found to be the lowest ZVS frequency under the closest magnetic coupling. The frequency gap between the upper frequency boundary and the lower ZVS branch increases with reduced coupling level. This means that by limiting operation below the upper frequency boundary, the system is not utilising the extra power transfer potential it would otherwise have if it could track the lower ZVS branch. A new controller is proposed here to extend the coil separation regulation range of the basic primary power flow controller by tracking the lower ZVS branch instead of being limited at the upper frequency boundary.

4.2. System Overview

Figure 4–1 shows a system overview of the proposed power flow control. The primary consists of a current-fed push-pull converter with parallel tuned resonant tank; the secondary is also parallel tuned with a current doubler rectifier. The primary and secondary circuits are designed to achieve inductively coupled transcutaneous energy transfer (TET). The output voltage is low pass filtered to reduce ripples before driving the heart pump load. The output voltage is fed back via RF link to the PSoC 5 microcontroller to be processed by an analogue to digital converter (ADC). The resulting digital format is compared with an internal desired target voltage reference. The operating frequency of the power converter is controlled via PWM to allow the output voltage to track the reference. A shorting period detection circuit will detect the voltage across each

MOSFET and process it as a resonant tank shorting period which is then converted by another ADC into a voltage reading. The frequency control module will drive the system between the lower ZVS branch and the lower frequency boundary. The system is detuned at high coupling by decrementing switching frequency toward the lower frequency boundary, and the system tracks towards the lower ZVS branch as the coupling level declines to tap into more power transfer potential. This will improve the system operating range – mainly reflected in the coil separation regulation range, which is the range of coil separation for which the controller can maintain the load voltage at rated level. The use of a current doubler rectifier instead of a normal full bridge rectifier has also contributed to extending the coil separation regulation range. This is because for the same ac input current from the parallel tuned power pickup, the current doubler doubles the dc output current, so the system dc output voltage can be increased significantly. With the same equivalent dc load, the current doubler also provides four times the effective ac resistance of full bridge rectifier at the resonant tank due to the impedance conversion related to the current and voltage change.

The frequency control module produces a control signal to the PWM module which then produces two 50% complementary signals. This further passes through a gate driver to drive the primary MOSFETs in the main circuit.

Figure 4–2 shows the resonant tank shorting period (V_{sh}) detection circuit. First the voltages across primary MOSFETs are fed to two difference amplifiers – V'_A is fed to the positive terminal of one difference amplifier and to the negative terminal of the other difference amplifier; V'_B is fed to the remaining terminal of each difference amplifier. The signals are then passed to two Schmitt triggers to generate digital square wave signals for the NOR gate. The NOR gate output is low pass filtered and fed to the microcontroller ADC to be transformed into V_{sh}, which is a variable representing the shorting period of the resonant tank waveform.

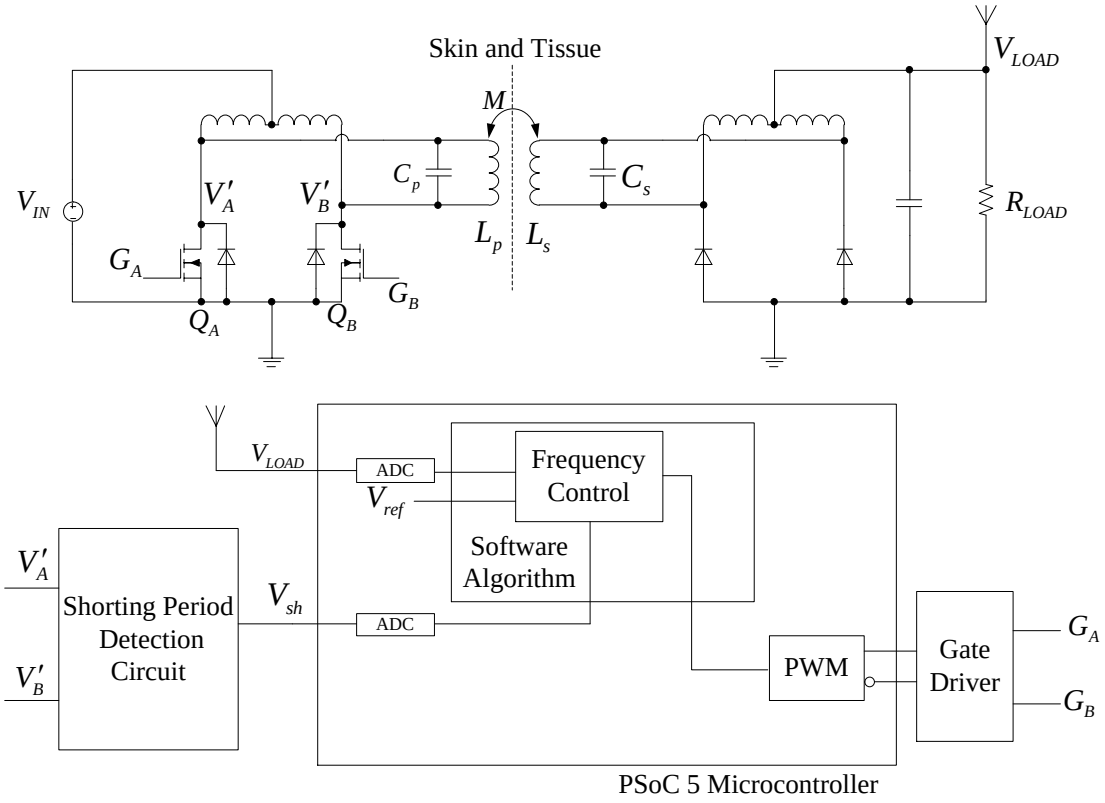


Figure 4–1 System overview of the proposed primary power flow control

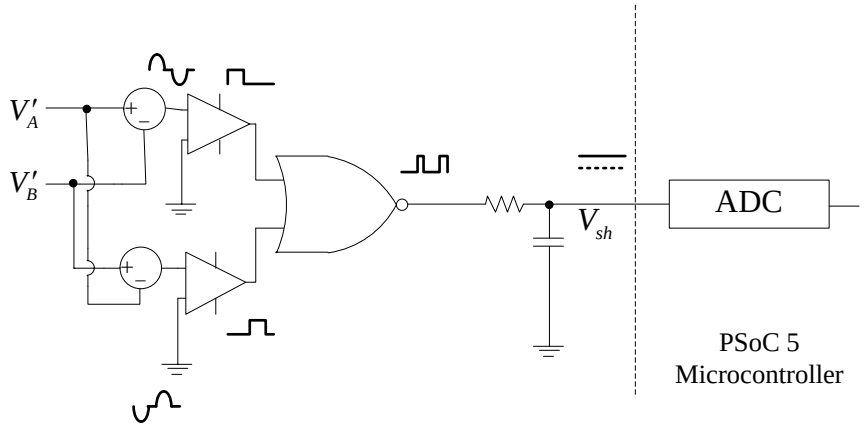


Figure 4–2 Shorting period detection circuit

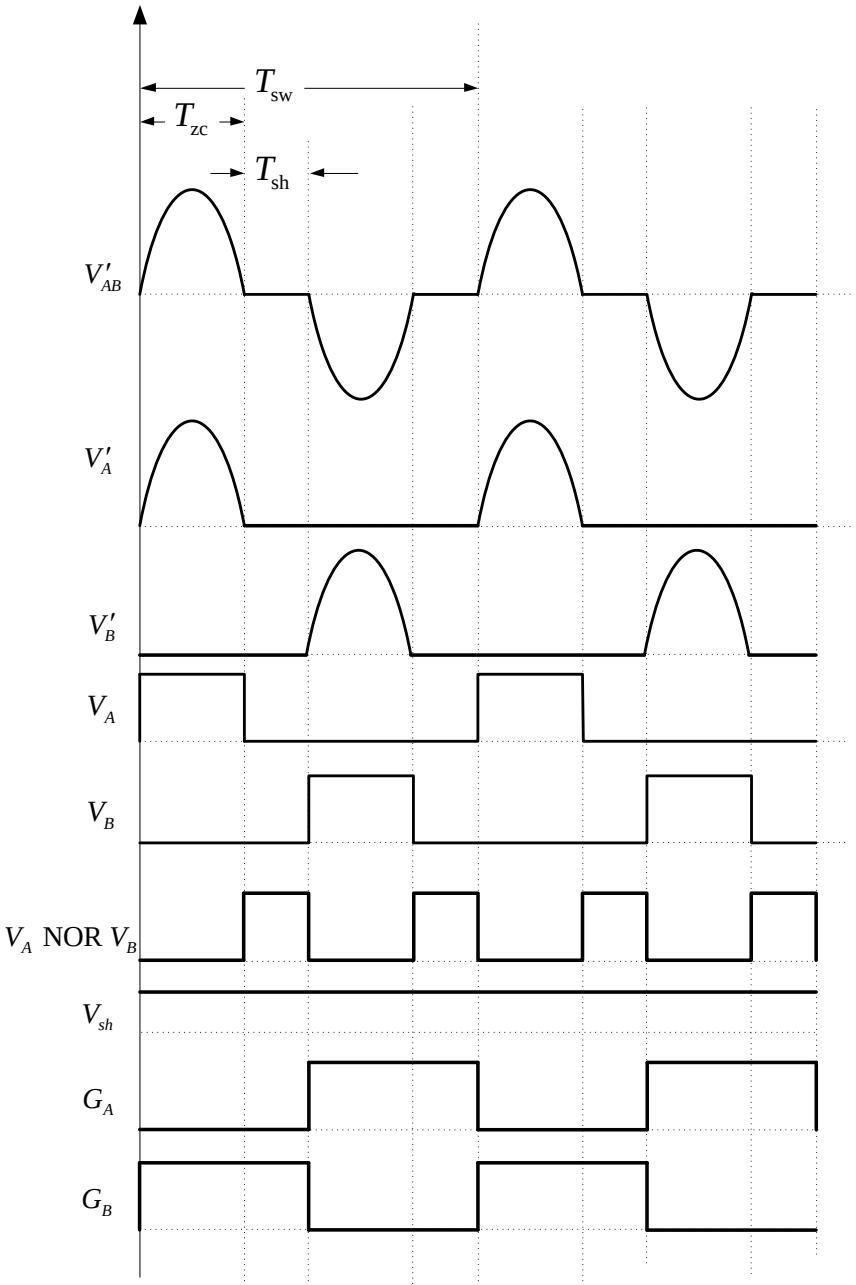


Figure 4–3 Theoretical waveforms

Typical theoretical waveforms of the system are shown in Figure 4–3. V'_{AB} shows the differential waveform across the resonant tank capacitor; V'_A and V'_B are drain to source voltages of MOSFET Q_A and Q_B respectively. V_A and V_B represent the non-zero region of V'_A and V'_B respectively. The resonant shorting period is represented by the NOR gate of V_A and V_B; this waveform is then converted to V_{sh} through low pass filtering. The

controller regulates output power by controlling the switching frequency of the gate driver outputs, G_A and G_B.

4.3. Operating Principle of the Proposed Controller

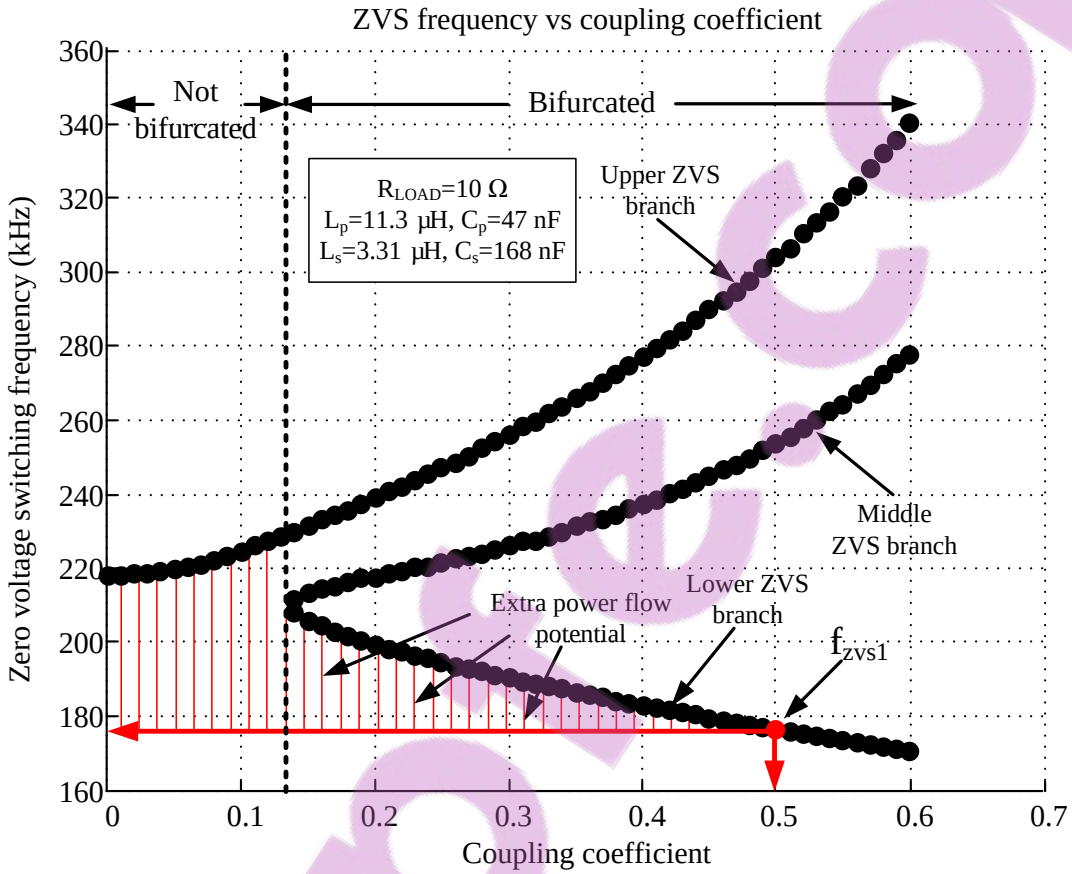


Figure 4–4 Frequency bifurcation stepping coupling coefficient

As shown in Figure 4–4, at the closest magnetic coupling of 0.5 the zero voltage switching frequency is 176.7kHz. As the magnetic coupling decreases, the lower ZVS branch rises, which means that a larger possible region of operation without instant capacitor shorting becomes available, giving extra power flow potential. The system also makes use of frequencies below f_{zvs1} down to a lower frequency boundary where regulation can no longer be maintained, as discussed in the previous chapter.

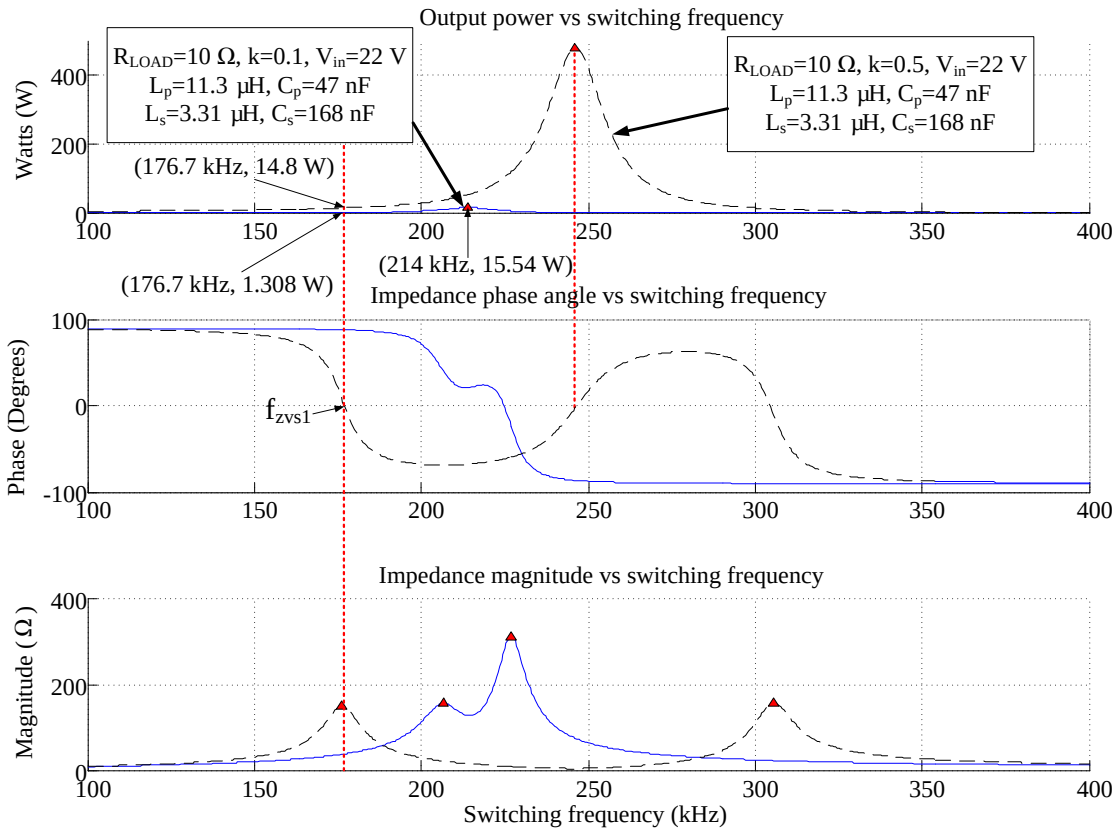


Figure 4–5 Extra power flow

Figure 4–5 plots the output power, impedance phase and magnitude graphs for the current system operated with two coupling levels. If the harmonics are ignored, it can be shown through ac impedance analysis that the power flow peak increases with magnetic coupling. The location of the peak on the switching frequency axis follows the middle impedance phase angle zero crossing upon bifurcation, which has a frequency offset when compared to the exact middle ZVS branch. The basic controller presented in Chapter 3 is bounded by an upper frequency set by f_{zvs1}. With the system upper frequency bounded, its maximum power is 14.8W for k=0.5 and only 1.308W for k=0.1. By comparison, once the upper frequency boundary is removed, maximum power can be as high as 15.54W at k=0.1 by allowing switching frequency to increase to 214kHz, while the maximum power for k=0.5 remains at 14.8W, as the system must still remain below the lower ZVS branch to avoid instant capacitor shorting.

4.4. Controller Design

An algorithm was designed to control the system to operate above the lower frequency boundary, below the single ZVS branch when not bifurcated and below the lower ZVS

branch upon bifurcation. The inputs to the algorithm are load voltage (V_{LOAD}) and the resonant tank shorting period (V_{sh}), which indicates closeness to the ZVS branch. During system operation, these inputs are converged toward their references: the load voltage reference (V_{ref}) and resonant tank shorting period reference (V_{sh_ref}). The system switching frequency (f_{sw}) is modified according to a series of logical conditions.

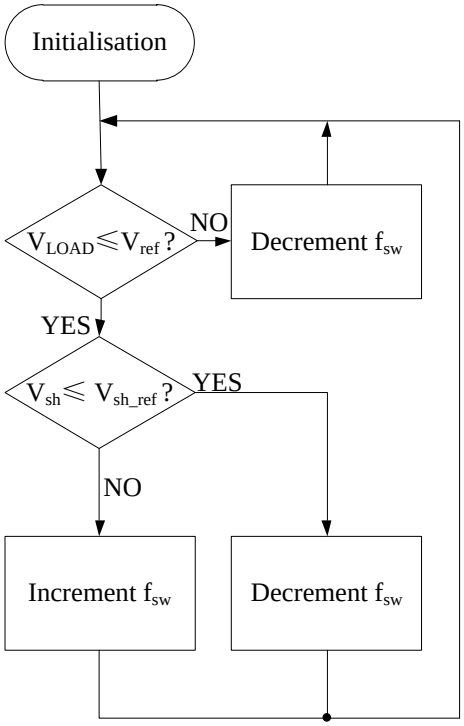


Figure 4–6 Software algorithm to set the switching frequency

As shown in Figure 4–6, when the software algorithm initialises; if $V_{LOAD}>V_{ref}$, f_{sw} decrements and waits for the next iteration, this condition detunes the system until load power reaches rated level. If $V_{LOAD}\leq V_{ref,}$ the algorithm then converges V_{sh} towards V_{sh_ref}. If $V_{sh}\leq V_{sh\_ref}$, the system is too close to the ZVS branch f_{sw} decrements, otherwise it is too far from the ZVS branch then f_{sw} increments. The software algorithm first ensures that load voltage stays within the rated level and then ensures that the system operates as close to the lower ZVS branch as possible. The dc inductance for the current doubler should sufficiently filter dc voltage ripple, handle rated dc current and is of minimal size.

4.5. Simulation and Experimental Results

The simulation waveforms in Figure 4–7 correspond well to the theoretical waveforms in Figure 4–3. Figure 4–8 shows that during start-up, the shorting period, load voltage and switching frequency ramps up. The controller algorithm repeats every count_max

simulation iteration, giving time for the power electronic system to respond. During each run, f_{sw} continues to increment at a rate of Δf to converge V_{LOAD} to V_{ref} (10V); f_{sw} is free to rise as long as $V_{sh}>V_{sh\_ref}$. Figure 4–8 shows V_{sh} settling down to above its pre-set V_{sh_ref} at 0.1, which means the system has reached V_{ref} before V_{sh_ref}, suggesting desired power level has been reached and the system still has room to move towards ZVS branch. In comparison, if V_{sh_ref} is reached before V_{ref}, then f_{sw} will not rise further, which means load power is below rated and the system is currently operating outside regulation range. In steady state, changes in f_{sw} cause ripples in V_{sh} and V_{LOAD} waveforms, which can be reduced by reducing Δf. Upon changes to the coupling level, the system will then converge V_{LOAD} and V_{sh} towards their references through f_{sw} variations in order to maintain load power regulation. Further details on this simulation can be found in Appendix C.

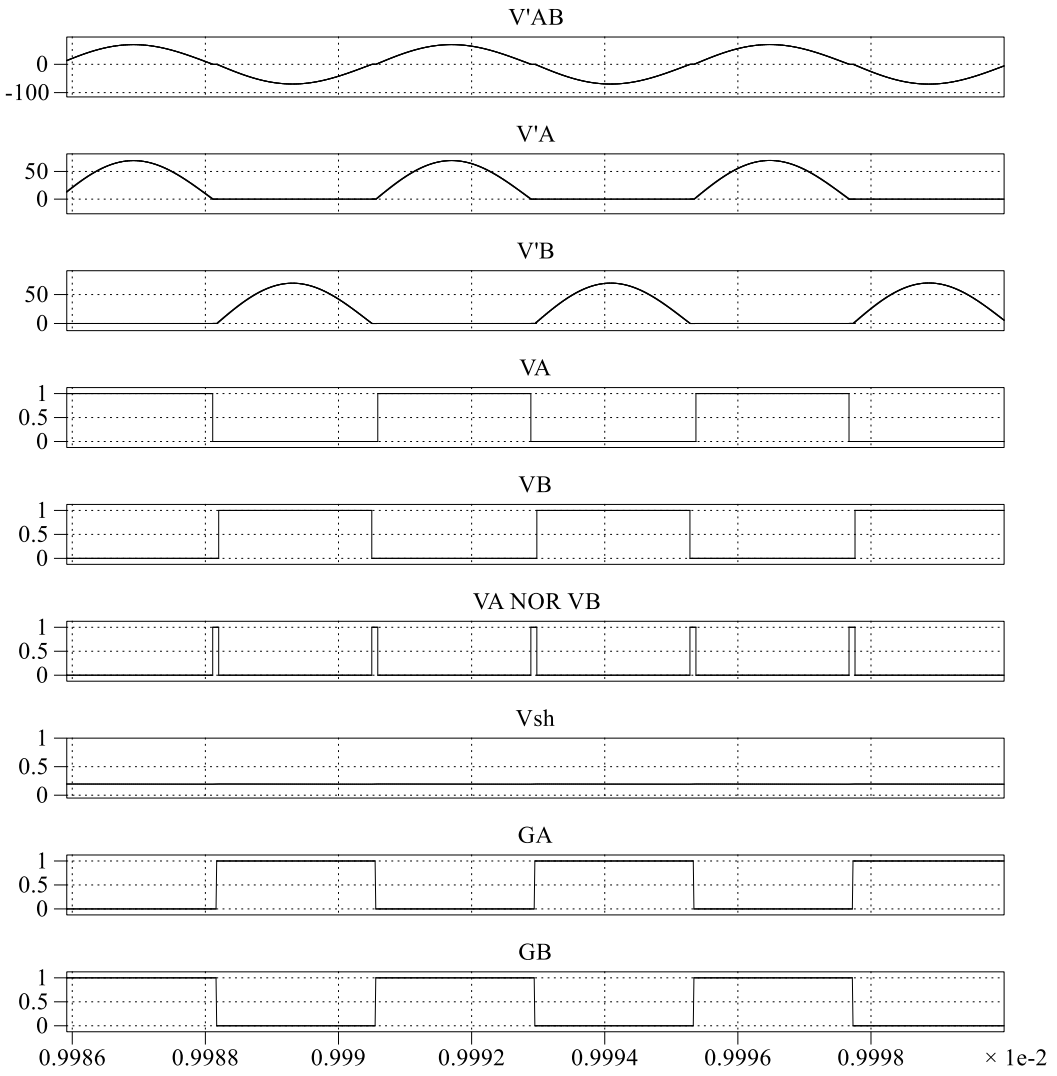


Figure 4–7 Simulation waveforms

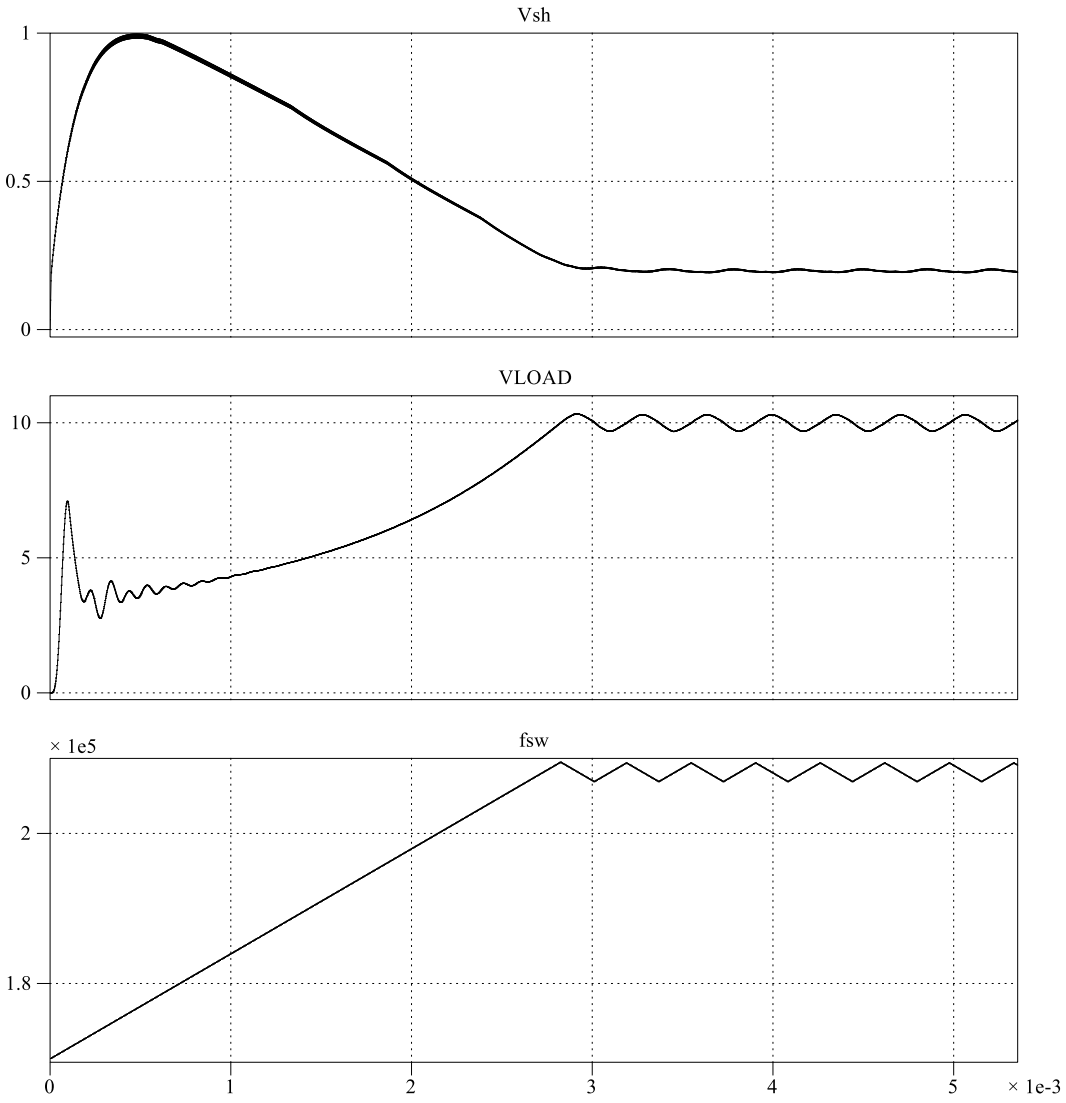


Figure 4–8 Simulated control actions

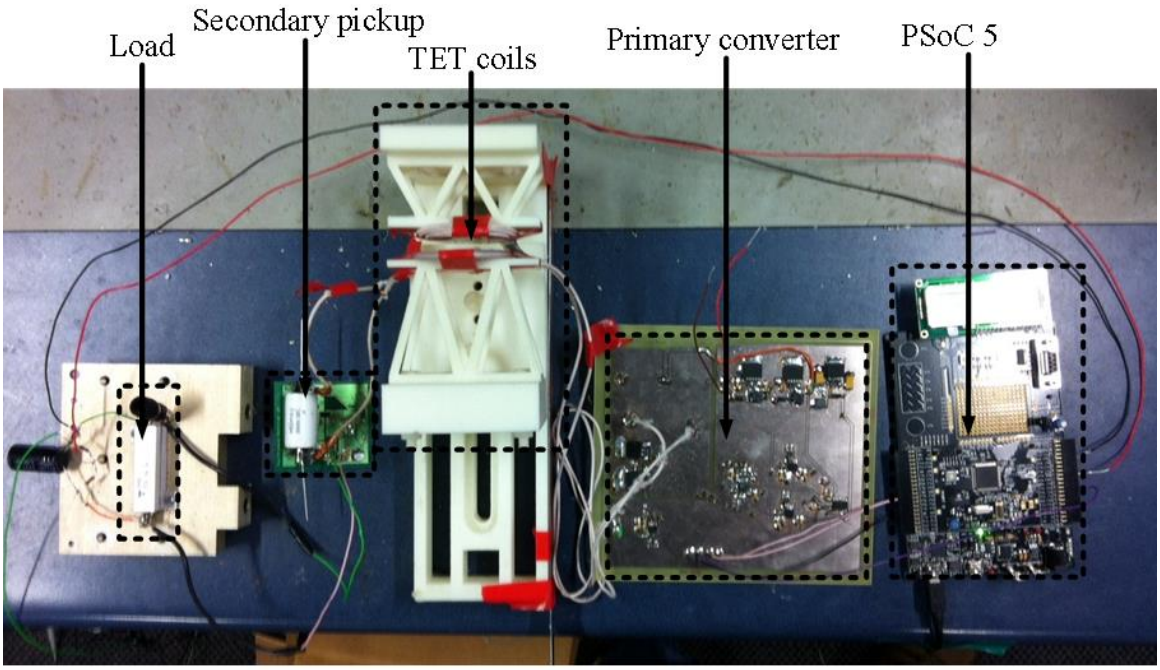


Figure 4–9 Experimental setup

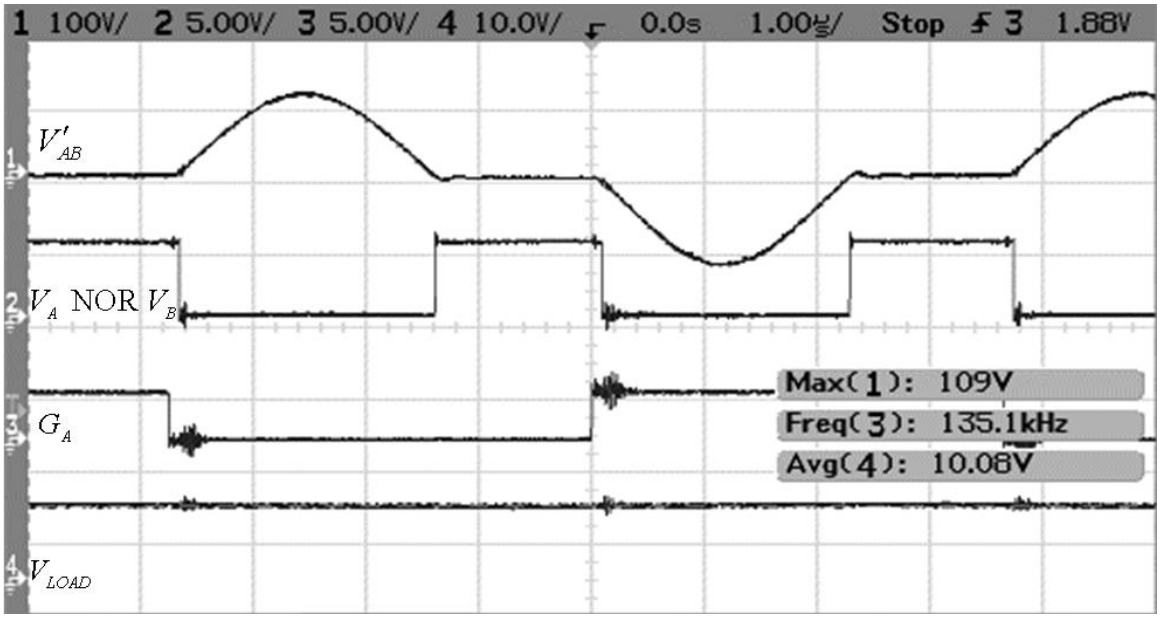


Figure 4–10 Experimental waveforms for 0mm coil separation

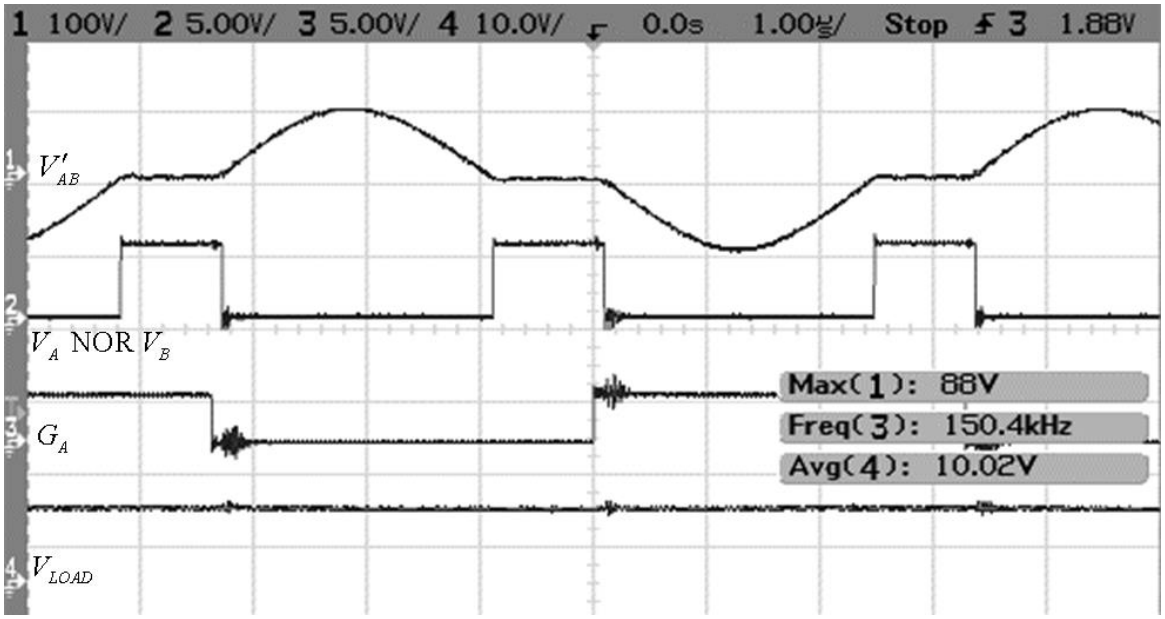


Figure 4–11 Experimental waveforms for 1mm coil separation

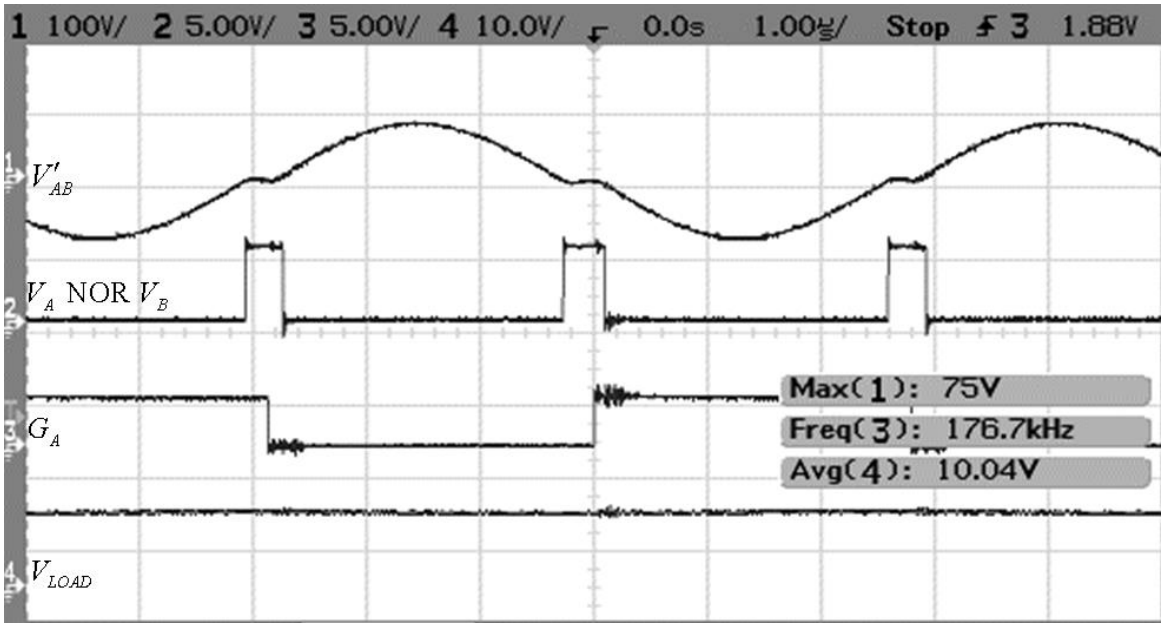


Figure 4–12 Experimental waveforms for 3mm coil separation

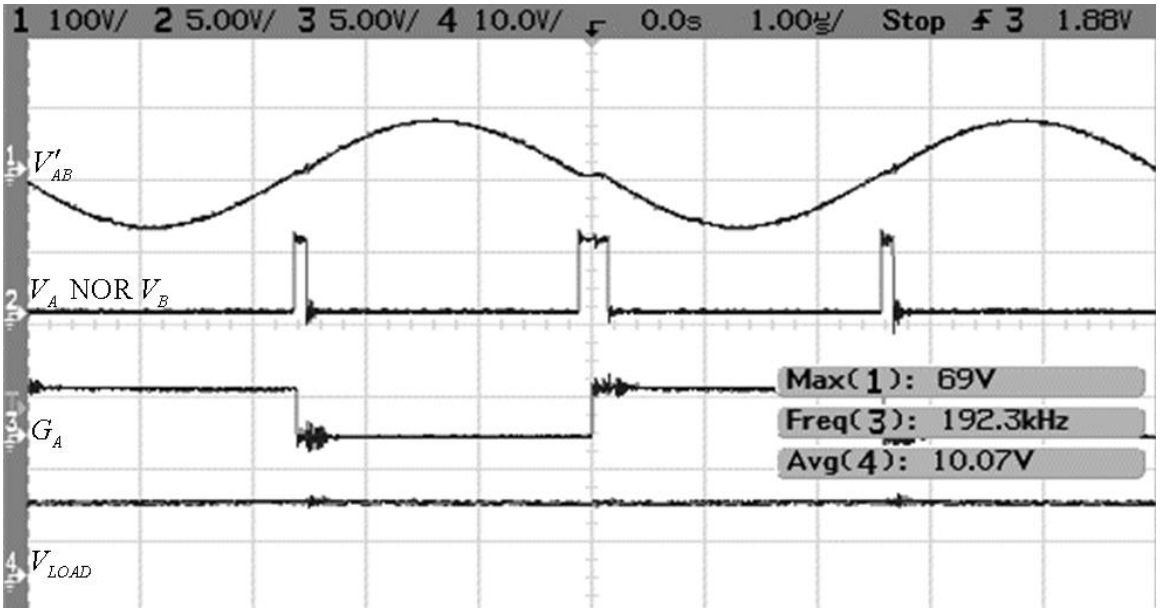


Figure 4–13 Experimental waveforms for 9mm coil separation

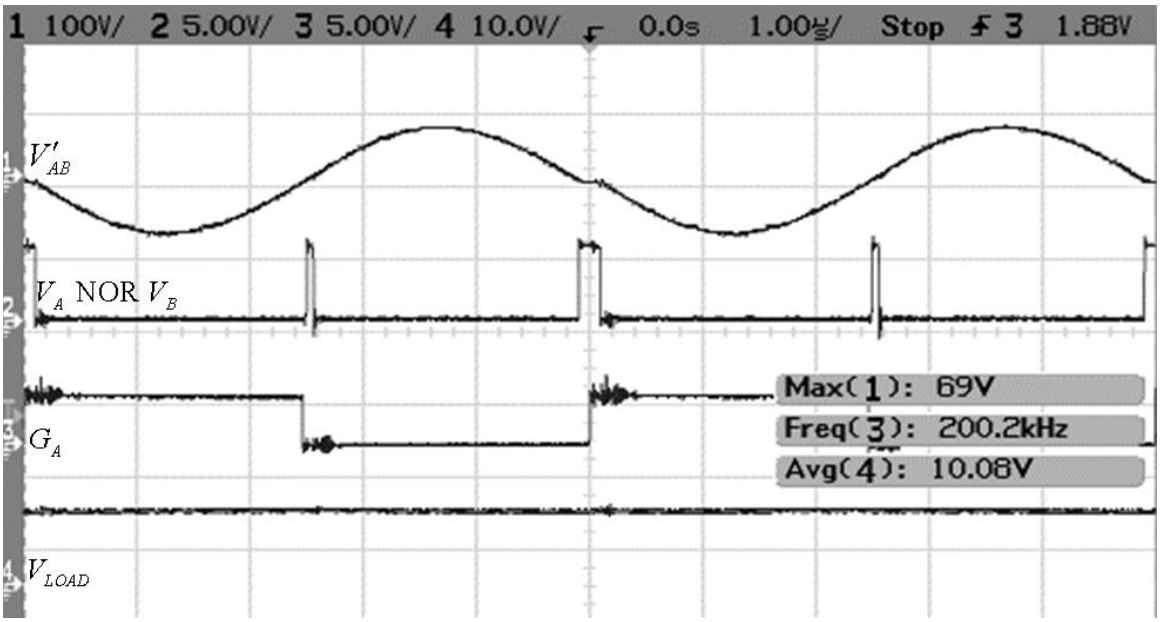


Figure 4–14 Experimental waveforms for 14mm coil separation

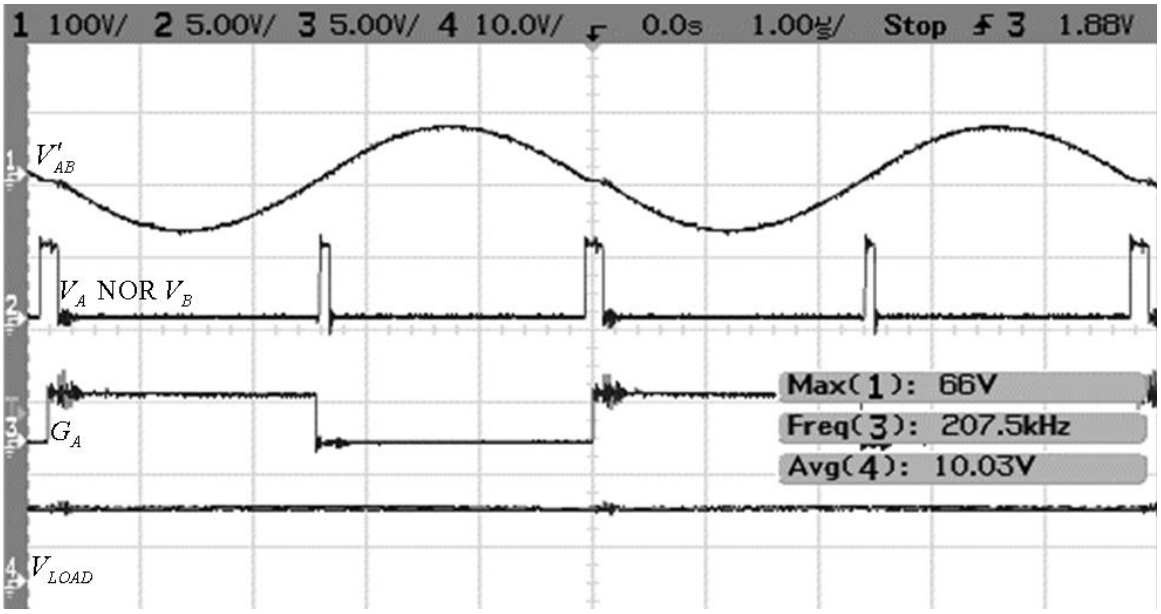


Figure 4–15 Experimental waveforms for 19mm coil separation

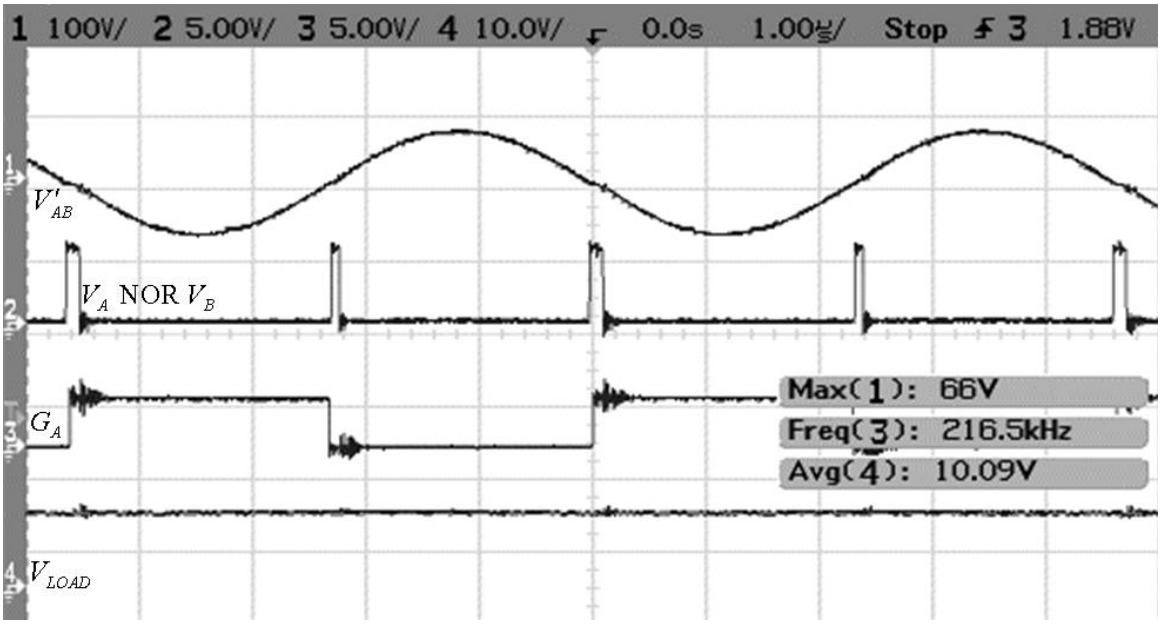


Figure 4–16 Experimental waveforms for 24mm coil separation

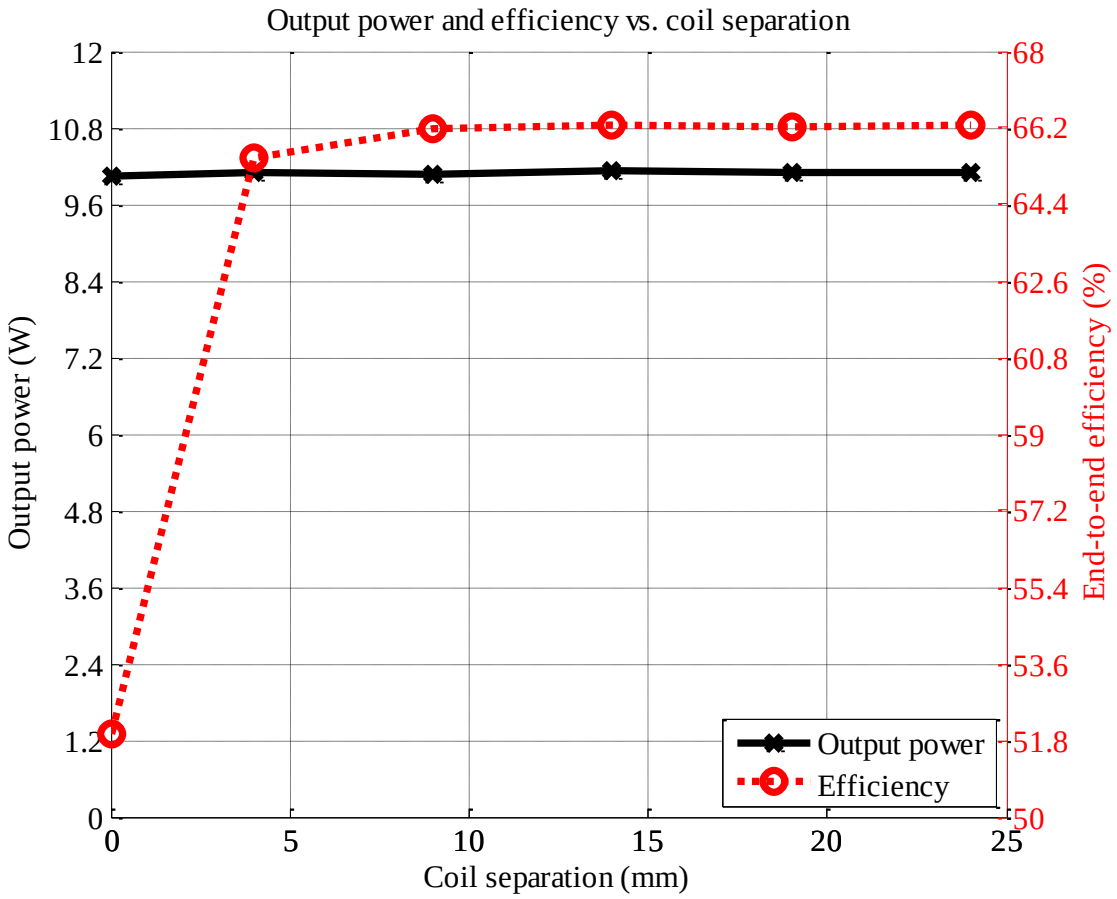


Figure 4–17 For a coil separation of 0 to 24mm, the controller is able to regulate the output power at the rated 10W with the corresponding efficiencies shown.

The circuit experimental setup is shown in Figure 4–9. It consists of a primary converter, TET coils, secondary pickup, load and a PSoC 5 microcontroller. Further details on PSoC 5 implementation of this controller can be found in Appendix D. The experimental waveforms for a range of coil separations are shown from Figure 4–10 to Figure 4–16. The top waveform is the resonant voltage, while the next waveform is the square wave representing the resonant shorting period. The third waveform is a gate drive signal while the last is the load voltage, which is regulated at the rated 10V. It is clear that the experimental waveforms correspond well to the theoretical and simulation waveforms.

The measurements in Figure 4–17 were collected by varying the direct distance separation without angular or lateral displacements. Figure 4–17 shows a stable 10W regulation at load from 0 to 24mm coil separation range. It also presents the end-to-end efficiencies within this regulated coil separation range. Efficiency is lower (52%) at 0mm separation and becomes static at around 66% after 4mm. The lower efficiency at 0mm separation or closest coupling level is due to the larger circulating resonant shorting

current through the MOSFETs and its body diodes. With further coil separation, frequency increases, the resonant shorting current decreases and therefore efficiency improves. This explains the positive slope between efficiency and coil separation for the 0 to 4mm coil separation range. A rough loss distribution of a push-pull converter has been analysed in work by Chen *et al.* [80] and ways of improving system efficiency include using more efficient Litz wires, more suitable switching devices for the designed voltage/current and frequency level. A more efficient system would produce less heat and a less efficient system would produce more heat. Heat analysis has been modelled and performed on live sheep by Dissanayake *et al.* [81], heat conduction for implanted coil and component can be contained by the use of silicon layers and titanium casing.

A further decrease in coupling level will trigger several events simultaneously. Firstly, efficiency improves as the resonant shorting period continues to be minimised. Secondly, efficiency improves as the system moves closer to its peak capability point; this is due to a rising trend in the lower ZVS branch as coil separation increases (coupling level reduces). Lastly, efficiency decreases as the coupling level decreases. The relatively static efficiency for coil separation between 4mm to 24mm is a result of complex interactions between these events. If the coil separation were to increase beyond the maximum regulated range of 24mm, the rated power could no longer be sustained, causing a sharp drop in the end-to-end efficiency.

4.6. Conclusions

An improved power flow controller was proposed and developed to extend the regulated coil separation range significantly. The controllers require detection of the resonant shorting period via a fast feedback loop from the primary resonant tank. The shorting period and the load voltage level are processed to generate a variable system operating frequency to achieve the desired output power regulation. An algorithm is designed to track the lower ZVS branch instead of being fixed to operate below an upper frequency boundary. Having a floating frequency boundary gives a significant boost in power flow potential, which improves the input voltage range, output power range and the coil magnetic coupling tolerance.

Chapter 5

Maintaining Middle ZVS Operation of TET System under Bifurcation

5.1. Introduction

Transcutaneous energy transfer can deliver wireless power into the body, eliminating the risks associated with having a percutaneous driveline breaking the skin [37]. Soft switched resonant converters are often used in TET systems to reduce power losses and EMI (Electromagnetic Interference). Among various resonant topologies, current-fed parallel-parallel tuned circuits are the most popular because high resonant current can be generated with a very low input current corresponding to the load, and there are only two low side driven switches without the need of high side drive circuitry.

At light load and loose magnetic field coupling, the system has only one ZVS (Zero Voltage Switching) operating point. When frequency bifurcation occurs there will be three ZVS points [71, 91, 95, 105]. If a simple controller is used to follow ZVS operation, the system will move away from the middle ZVS point, causing significant loss in power transfer capability, as reported by Boys *et al.* [90]. This is because a current-fed push pull converter with parallel tuned primary and secondary contains a single power peak corresponding to the middle ZVS point.

To visualize the effect of bifurcation on system ZVS operation, Figure 5–1(a) shows a system without ZVS bifurcation: the system will always converge toward the single stable ZVS operating point. Figure 5–1(b) however portrays a system with ZVS bifurcation – the system has two stable ZVS points with an unstable middle ZVS point that has a tendency to jump to either one of the stable points.

Chapter 2 introduces the idea of the peak power capability of the system; Chapter 3, Chapter 4 and other work in [34, 63, 105-107] have proposed power flow controllers for load power regulation of TET systems; but they were not designed to track the middle

ZVS to maintain the system peak power capability [105]. Waters *et al.* have suggested adaptive frequency tuning, and implemented dynamic impedance matching to ensure maximum power transfer [67, 108], but the design employs different converter topology using multiple coils with large diameters.

This chapter presents a ZVS follower to track the single ZVS before bifurcation, and to maintain middle ZVS operation after bifurcation, so as to obtain the maximum power transfer potential of the system. This enables the rated 10W power to be transferred wirelessly to a heart pump via a lower input voltage, a greater coil separation and an improved end-to-end efficiency.

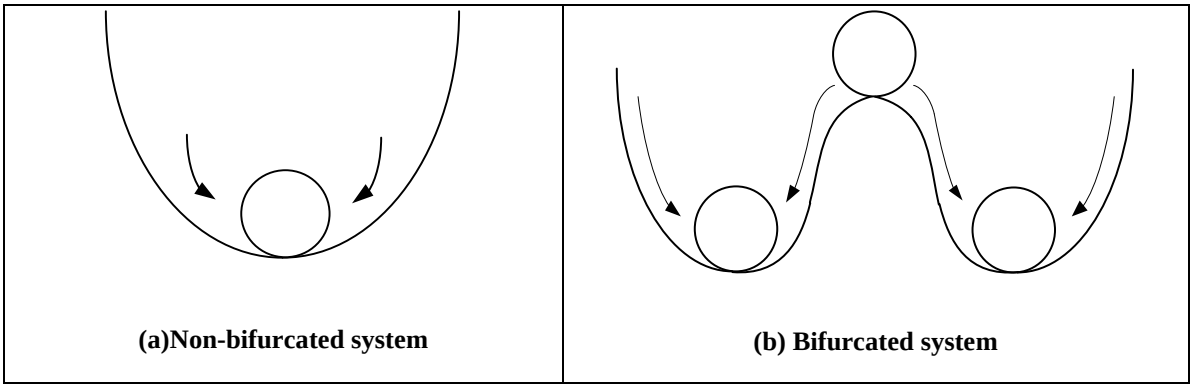


Figure 5–1 Analogy for non-bifurcated and bifurcated systems

5.2. Primary Side ZVS Follower with Blocking Diode

The ZVS follower proposed is designed to sense the presence of instant capacitor shorting and resonant tank shorting, and to vary the system switching frequency to converge to the single ZVS branch before bifurcation occurs, and to the middle ZVS branch after bifurcation. The system overview is shown in Figure 5–2, the primary side is a current-fed parallel tuned push-pull converter driven by a dc input, V_{IN}. Blocking diodes are added in series with each MOSFET, to stop reverse current flow and instant capacitor shorting when converging towards ZVS operation. The secondary is parallel tuned with a passive current doubler rectifier and a resistive load, R_{LOAD}. V'_A and V'_B are the drain to source voltages of Q_A and Q_B respectively. The inverse of V'_B and gate drive signal G_A are processed by a feedback signal processing module to output two dc voltages, V_{diode} and $V_{direction}$. These two dc signals are passed through analogue to digital converter (ADC) modules. The CompactRIO controller then uses them to determine the frequency of two complementary pulses with 50% duty cycle. Finally, a gate driver is used to drive the two low-side primary MOSFETs properly.

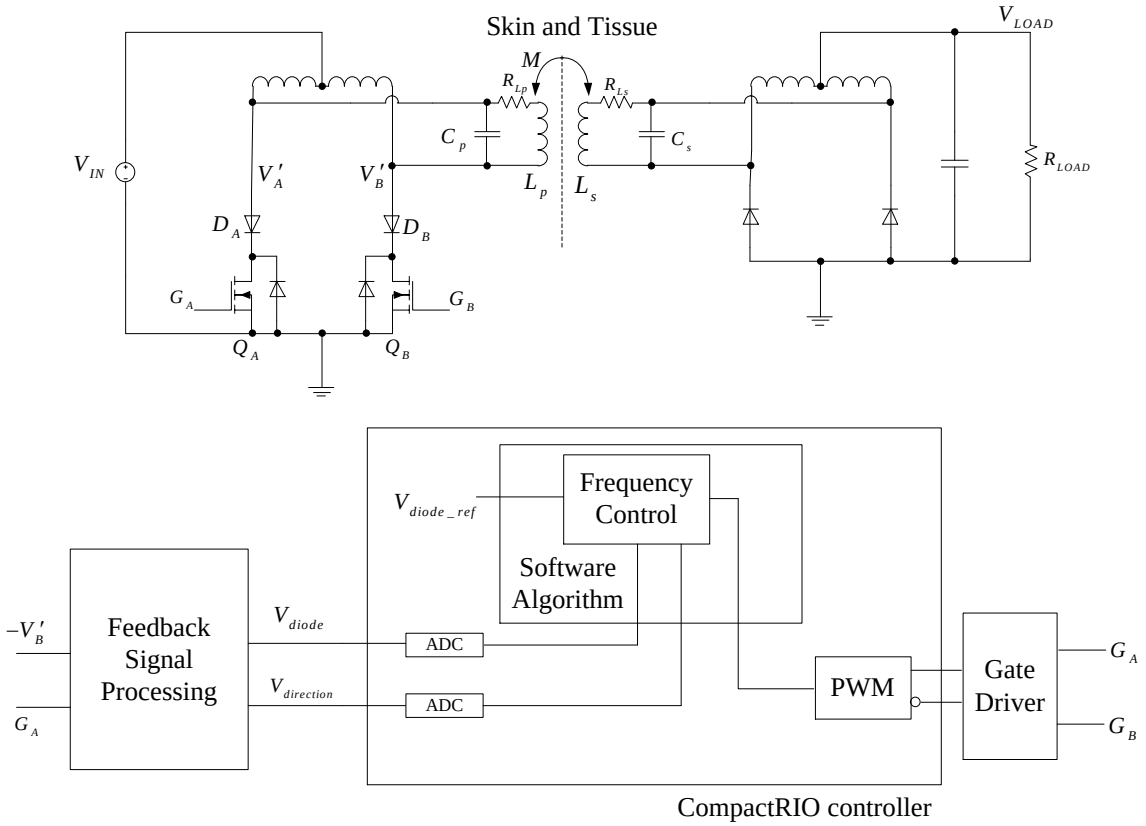


Figure 5–2 System overview of proposed ZVS tracker that operates at near peak power flow potential

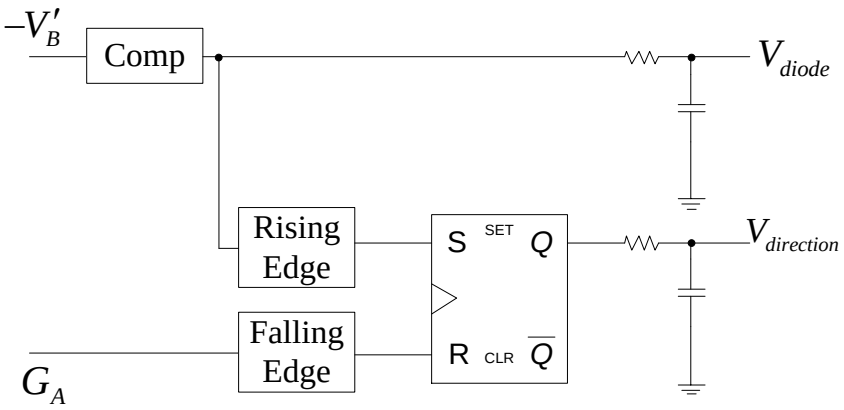


Figure 5–3 Feedback signal processing details

The details of the feedback signal processing module is shown in Figure 5–3. An inverse of V'_B is compared to ground to generate a pulse proportional in width to the negative region of V'_B; the pulse is low pass filtered to generate V_{diode}, which reflects the error to ZVS operation. The rising edge of the pulse sets an SR latch while the falling edge of G_A resets the latch; the output of the SR latch is low pass filtered to generate $V_{direction}$, which determines the direction for proportional and integral action to increase or decrease the PI

output. The intention of the low pass filtering is to ensure V_{diode} and $V_{direction}$ are converted to dc signals, therefore a low cut-off frequency of 1kHz has been used to attain the RC values.

5.2.1. Circuit Operation Theory

The blocking diodes stop reverse current flow, and prevent any shorting current through MOSFETs, their body diodes and the resonant tank. The voltage across resonant capacitor cannot change instantly due to limited dv/dt. One side of the resonant capacitor will be grounded on commutation; the instant change in voltage will be transferred to the other side, and the overall differential capacitor voltage remains unchanged. When the system operates at ZVS, the next half cycle starts from zero volts. In comparison, without ZVS, the residual voltage at the end of each half cycle will become the starting voltage in the next half cycle.

A relationship between the resonant tank ac peak voltage and the dc input voltage is shown in (5.1), where θ is the negative region of V'_B. The cosθ term is a result of adding blocking diodes to the primary converter; it increases the primary resonant tank peak as system departs from ZVS frequency.

$$\hat{V}'_{AB} = \frac{\pi V_{IN}}{\cos\theta} \tag{5.1}$$

5.2.1.1. Locating Peak Power Capability Point

Figure 5–4 shows system ZVS frequency bifurcating with the increased coupling level. It is known through ac impedance analysis that the system peak power occurs below the single ZVS branch before bifurcation and near the middle ZVS branch upon bifurcation. By designing the system ZVS frequency to bifurcate at a relatively low coupling level, the controller maximises the ratio of the bifurcated region to non-bifurcated region and gives more access to the middle ZVS branch to maximise power when the system tends to bifurcate.

In Figure 5–4, the shaded regions are fast switching area, while the clear regions are slow switching area, and the dots represent ZVS operating points. In the non-bifurcated region there is one ZVS point, and in the bifurcated region there are three possible ZVS points for any coupling level. At the interface between non-bifurcated and bifurcated regions,

there is a critical coupling level where there would be two ZVS points, but this is not shown here due to insufficient resolution in coupling steps. The blue ZVS points represent the desired operating points to maintain ZVS operation and maximise power transfer.

The direction of 'one' is assigned when the system is switching fast with a negative impedance phase angle and a direction of 'zero' is assigned when the system is switching slow with a positive impedance phase angle. V'_B has no negative region when system operates at a ZVS frequency, but the negative region will be present when the system operates at non-ZVS. Figure 5–5 shows a system operating with ZVS: V_{diode} stays low since V'_B has no negative region. In turn the set trigger for SR will be absent, and $V_{direction}$ will remain low. The reset trigger will always be present as it depends on gate drive signal G_A. The negative region appears at the start of V'_B half period when the system is switching fast as shown in Figure 5–6, and appears at the end of V'_B half period when the system is switching slow as shown in Figure 5–7.

When switching fast, the resulting SR latch waveform is a square wave close to 50% duty cycle as SR is set at the start of the half period. When switching slow the resulting SR latch waveform is a pulse proportional in width to the negative region in V'_B.

A special case SR output occurs when accounting for trigger hysteresis in comparator, logic and switching component delays as shown in Figure 5–8. The reset trigger has occurred before the set trigger. While V_{diode} remains unaffected, the SR output stays high much longer and will impact on the direction indicator $V_{direction}$ for the controller.

After accepting the dc values of V_{diode} and $V_{direction}$, the CompactRIO controller regulates V_{diode} toward its reference to converge the system towards ZVS operation. The dc average of $V_{direction}$ is compared to a set of thresholds to determine the correct movement direction for the system switching frequency.

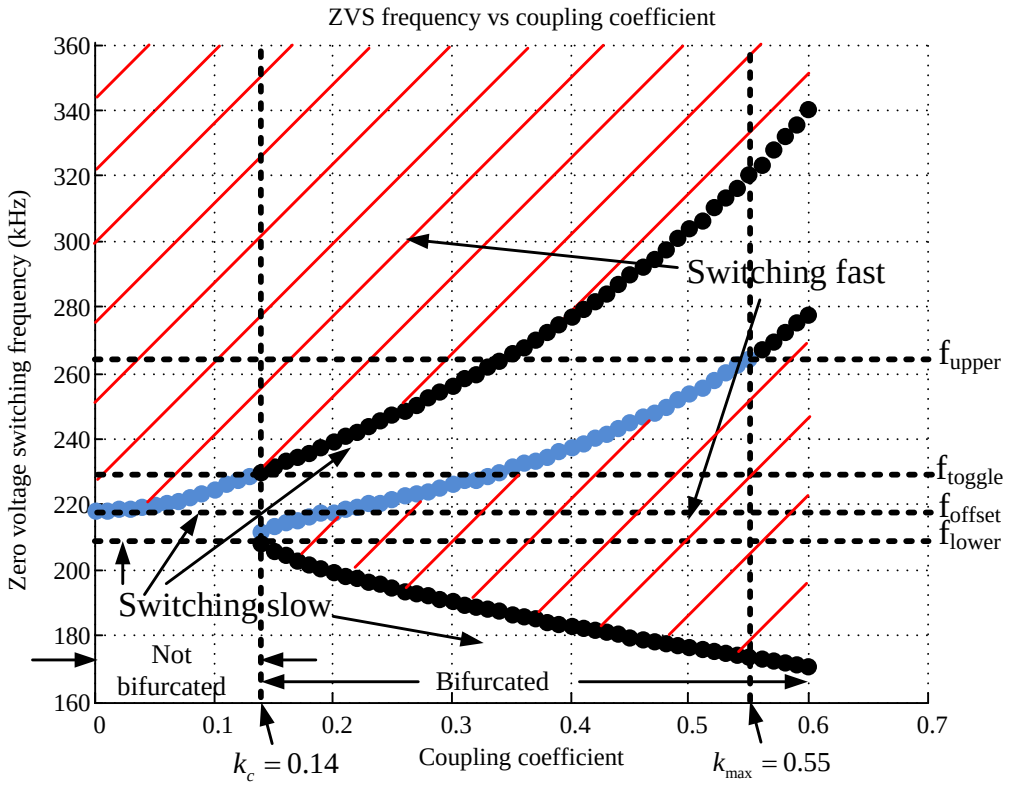


Figure 5–4 Bifurcation plot of ZVS frequency with coupling variations

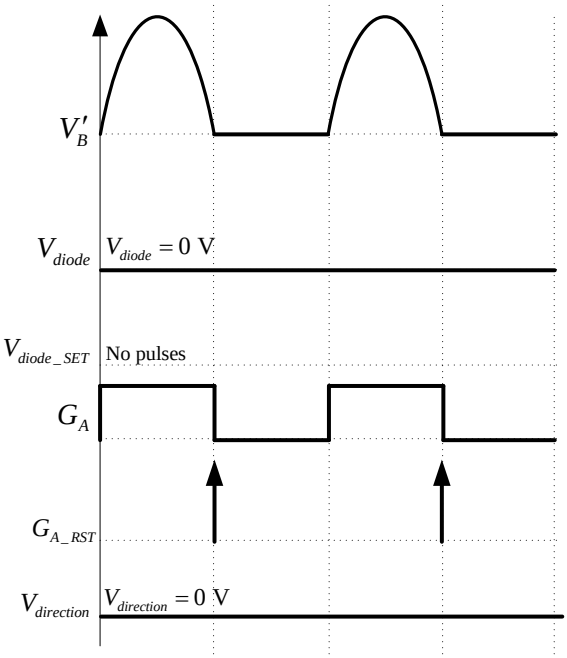


Figure 5–5 Switching with ZVS operating at zero resonant tank impedance phase angle

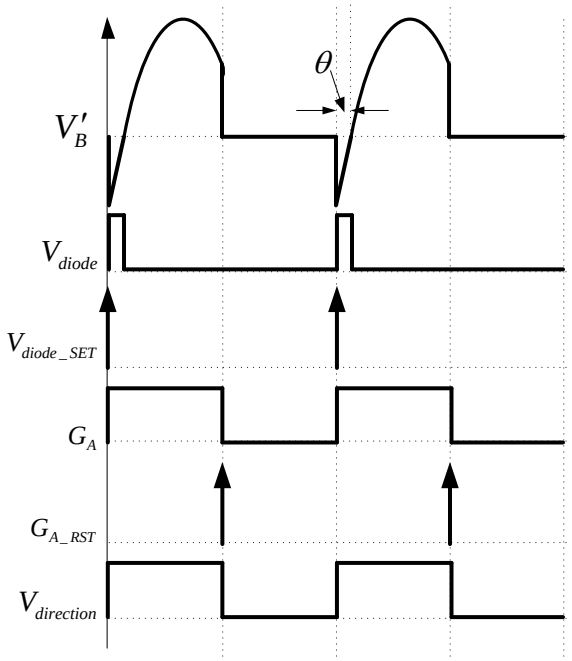


Figure 5–6 Fast switching with a negative resonant tank impedance phase angle

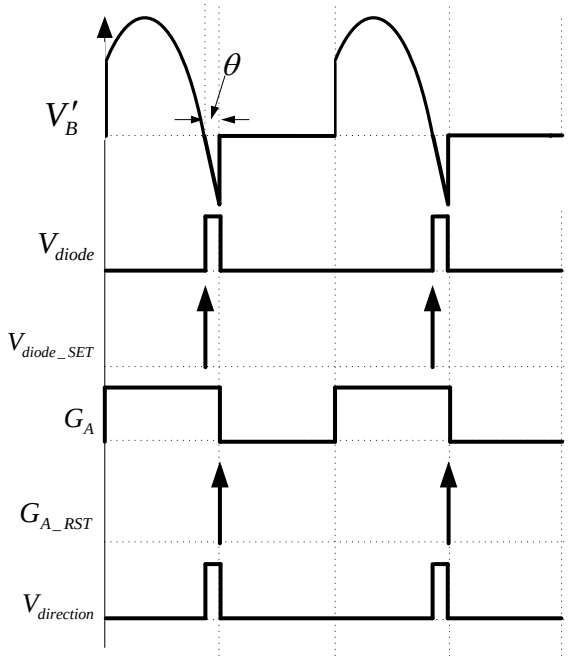


Figure 5–7 Slow switching with a positive resonant tank impedance phase angle

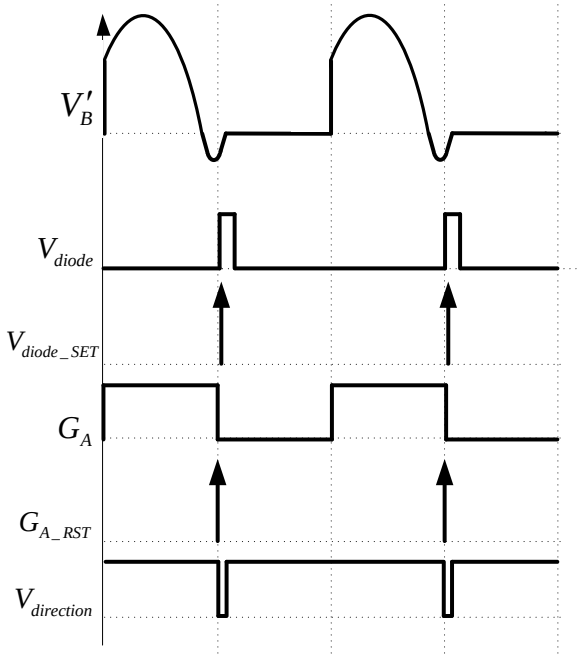


Figure 5–8 A special case control waveform due to comparator triggering hysteresis, logic and switching component delays.

5.2.2. Controller Design

As shown in Figure 5–4, before bifurcation, fast switching and slow switching are above and below the single ZVS branch respectively, and this is swapped after bifurcation with fast switching and slow switching below and above the middle ZVS branch respectively. To overcome the contradicting movement directions, a 'toggle' variable is introduced to reverse tracking direction by negating the signs of PI gains, in order to track toward the target ZVS branches. In the bifurcated region a direction of one and zero correspond to incrementing and decrementing switching frequency respectively, and the toggle would be set to one in the non-bifurcated region, so that a direction of one and zero now correspond to decrementing and incrementing switching frequency respectively.

To set the toggle, the system switching frequency must be kept at the lower frequency boundary (f_{lower}) for a set wait time, and the toggle can be reset either by remaining at f_{lower} for another wait time or by reaching the toggle frequency (f_{toggle}).

5.2.2.1. Start-up Sequence

The coupling range of the TET system ranges from 0 to 0.55 (k_{max}) for the current coil design. At start-up, the controller starts at the PI offset frequency (f_{offset}) with the toggle as zero. When starting coupling level is lower than the critical coupling (k_c), the system

switching frequency decreases and saturates at f_{lower} for the set wait time. This sets the toggle and the system reverses direction and stabilises at the single ZVS branch. When starting coupling level is between k_c and 0.2, the switching frequency will decrease toward the middle ZVS branch. When the starting coupling level is between 0.2 and k_{max}, the switching frequency will increase towards the middle ZVS branch.

5.2.2.2. Normal Operation

After start-up, by decreasing coil separation (or increasing coupling level) from a very large separation, the system will settle at the single ZVS branch after setting the toggle. As coil separation decreases further, the toggle is reset after frequency reaches f_{toggle}, which is located at the boundary of the non-bifurcated and bifurcated regions. Further reduction in coil separation will force the system to track the middle ZVS branch for peak power.

The toggle is allowed to change from one to zero and zero to one to allow for a special case at critical coupling. The system saturates at f_{lower} and sets the toggle at critical coupling level, and further coupling increases enters the fast switching bifurcated region. PI action forces frequency downwards and system will continue to saturate at f_{lower}. By changing toggle back to zero after another wait time, the system would resume normal tracking process.

5.2.2.3. Control Algorithm

Figure 5–9 shows the logic behind the frequency controller. The system first determines the state of the toggle, then V_{diode} is regulated towards its reference through proportional and integral action. The error between V_{diode} and its reference is used to calculate the proportional term and the integral term, which is a continuous summation of all previous integral terms. The integral term is then limited by a suitable upper and lower boundary to prevent unexpected PI behaviour due to unlimited ramping of the integral term. The proportional and integral terms are then added, and the rate of change of this sum is limited to prevent sharp variations in switching frequency. The PI output is added to an offset, which puts the switching frequency in the correct range with suitable variations. The switching frequency is then limited by an upper and lower boundary to avoid unexpected operation beyond the set range. While the system frequency is saturated at f_{lower}, the integral term is forced to be constant.

The movement direction is determined by the value of $V_{direction}$, which is compared with a set of boundaries that includes normal situations and the special case. In the absence of $V_{direction}$ or V'_B negative region as shown by Figure 5–5, a direction of zero is assigned. Since the system is at ZVS, the integral term and switching frequency are forced to be constant. The slow switching $V_{direction}$ gives a direction of zero while the fast switching $V_{direction}$ gives a direction of one. The special case when $V_{direction}$ is greater than direction_lower_correction is given a direction zero as it is slow switched.

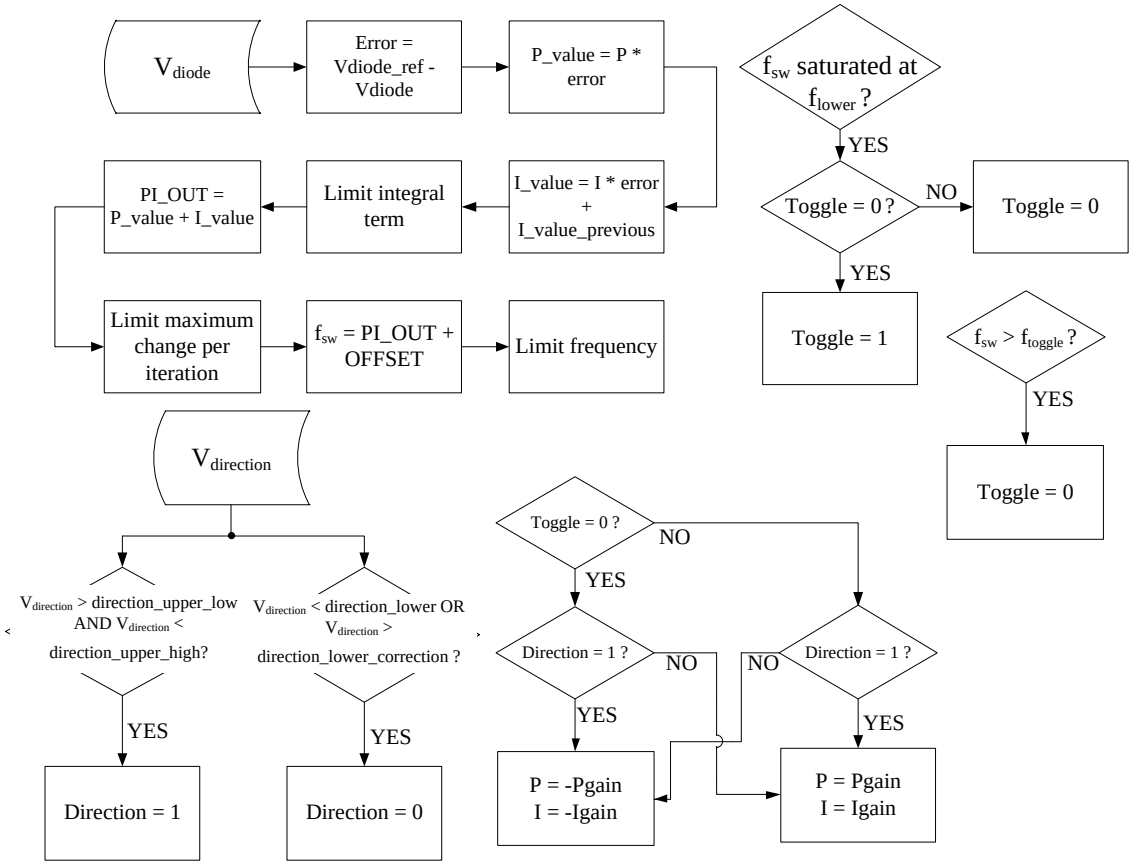


Figure 5–9 Logic flow for frequency controller through PI action

5.2.3. Simulation and Experimental Results

Figure 5–10 shows the simulated internal system waveforms for PI control with increasing coupling levels. The top plot titled V_{diode} shows the system tracking towards the 0.1V reference after each coupling level change. After simplifying the secondary by its ac load equivalent, the effective V_{LOAD} peak increases with the incrementing coupling level. The system switching frequency (f_{sw}) saturates twice at the lower boundary (210kHz). The first one set the toggle to one, which is reset when the frequency reaches 230kHz (f_{toggle}). The second occurred during $V_{direction}$ transit from low to high, but the

toggle was unaffected as it was less than the set wait time. Care must be taken to ensure wait time threshold is large enough to avoid false toggles. The bottom plot shows the proportional and integral terms. The proportional term is relatively static, since most changes in frequency are driven by the varying integral term, the sum of the two terms closely tracks the integral term.

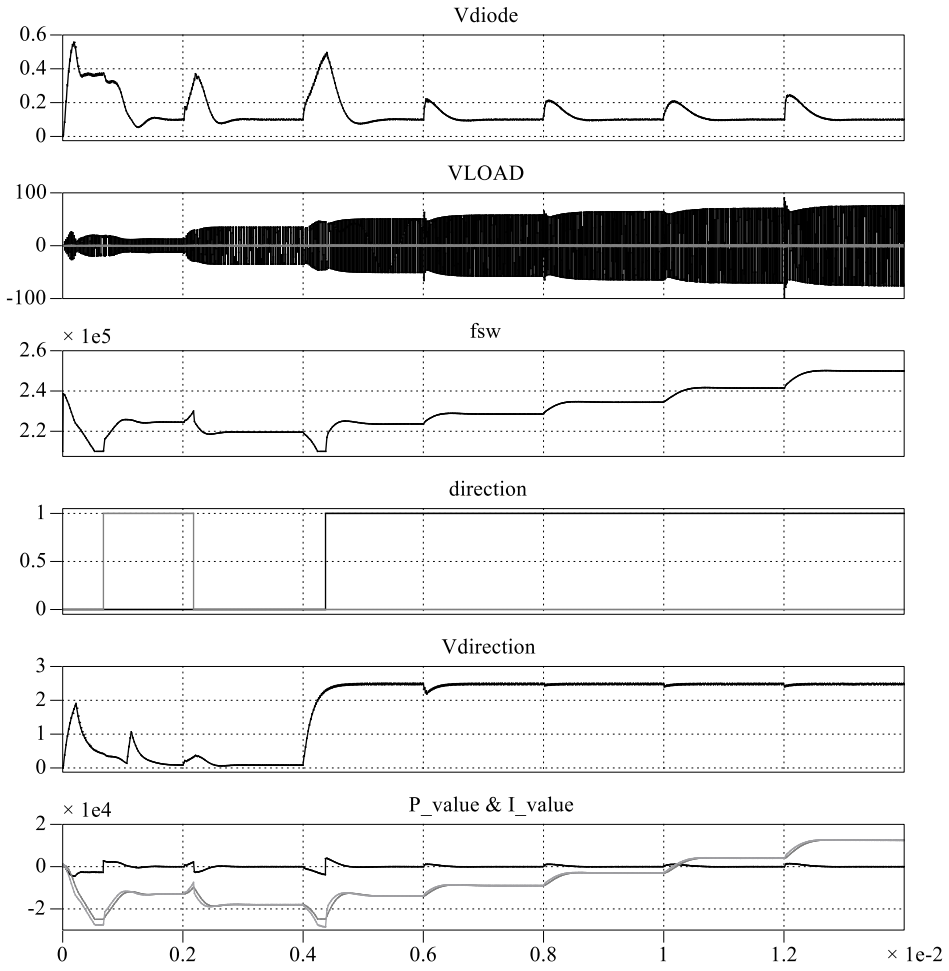


Figure 5–10 Simulated internal system waveforms for PI control with increasing coupling levels

Similarly, Figure 5–11 shows the case for simulated PI control by decreasing the coupling level. The system is able to track toward the V_{diode} reference and the effective V_{LOAD} peak decreases with the decrementing coupling level. Upon each coupling change, the direction is changed to one or zero depending on whether the middle ZVS branch is approached from below or above respectively. The final coupling of 0.1 has resulted in setting the toggle variable for the system to approach the non-bifurcated single ZVS branch.

Figure 5–12 and Figure 5–13 are simulation waveforms showing the system approaching the middle ZVS branch from below and above respectively. Further details on this PLECS simulation can be found in Appendix E.

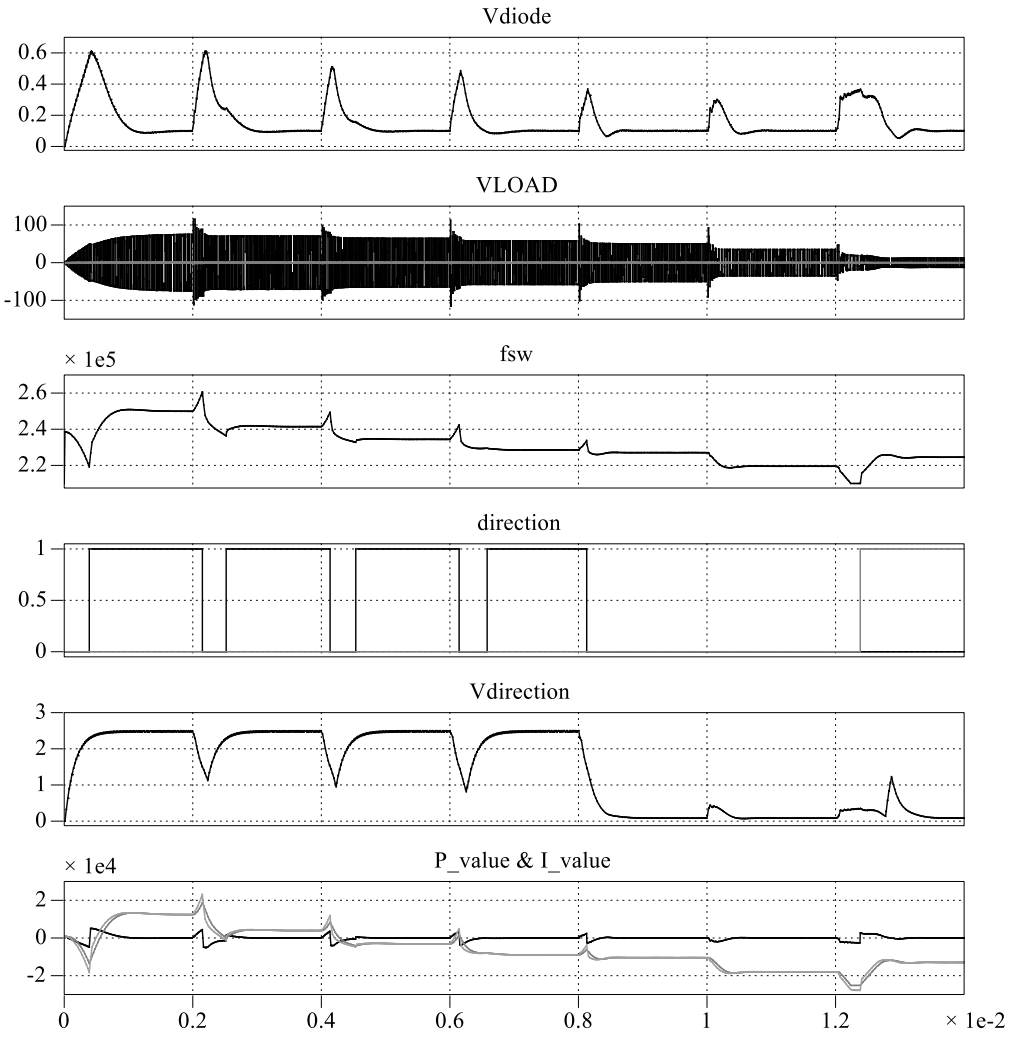


Figure 5–11 Simulated internal system waveforms for PI control with decreasing coupling levels

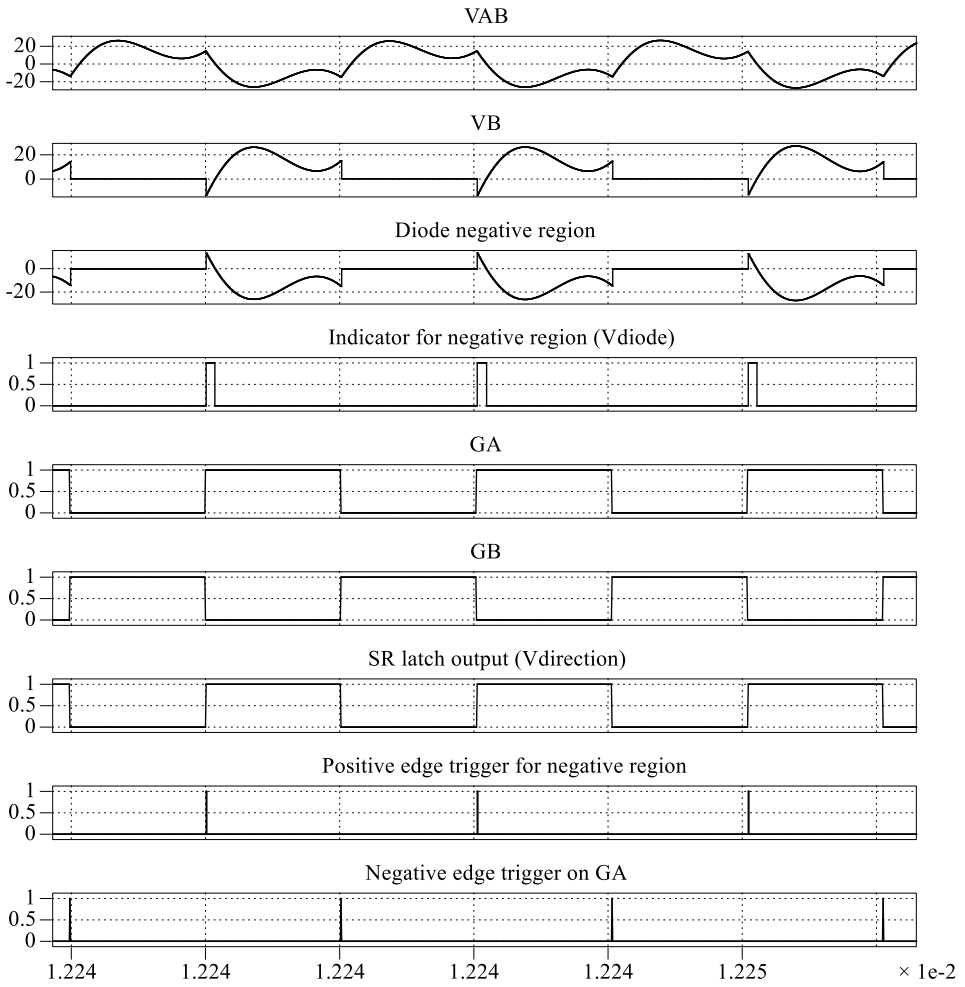


Figure 5–12 Simulation waveform with system approaching middle ZVS branch from below

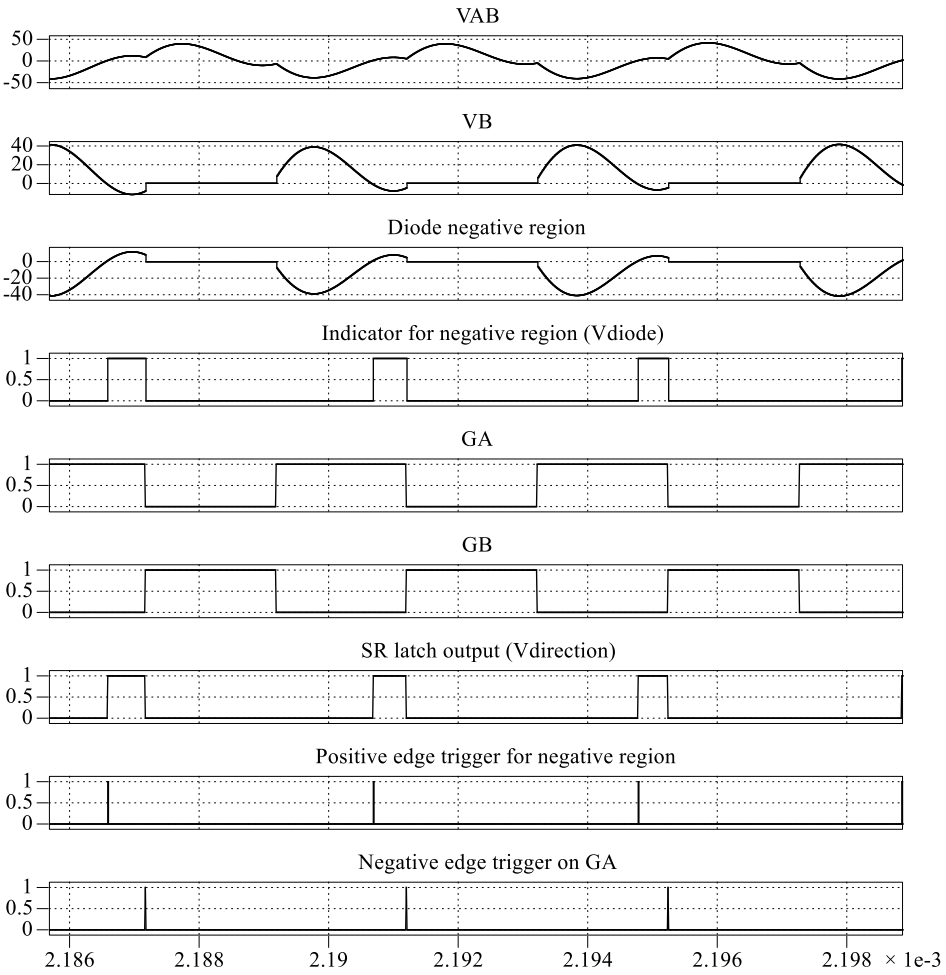


Figure 5–13 Simulation waveform with system approaching middle ZVS branch from above

Table 5–1 Practical system parameters

V_{IN}	8 V	L_p	11.3 μH
C_p	47 nF	R_{Lp}	73.1 mΩ
C_s	168 nF	L_s	3.31 μH
R_{LOAD}	10 Ω	R_{Ls}	26.7 mΩ

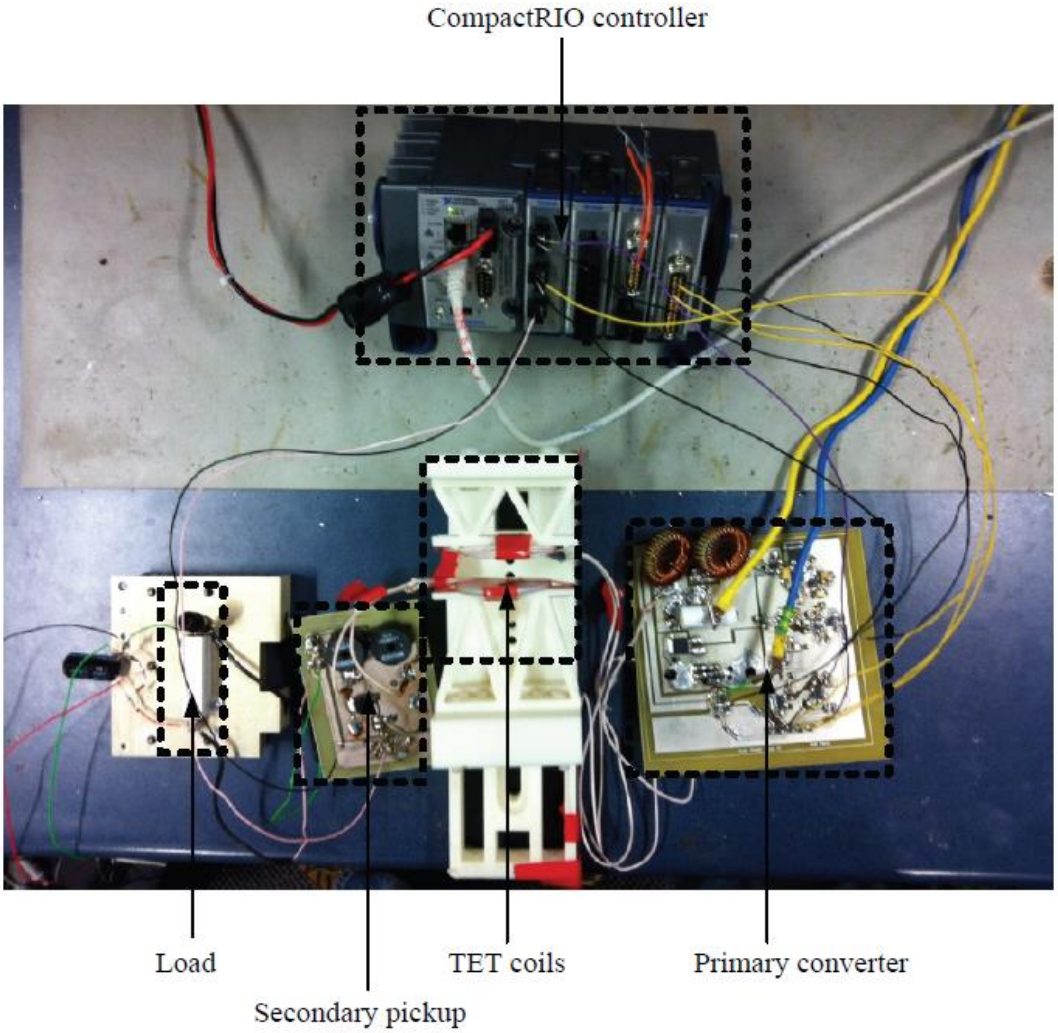


Figure 5–14 Experimental setup

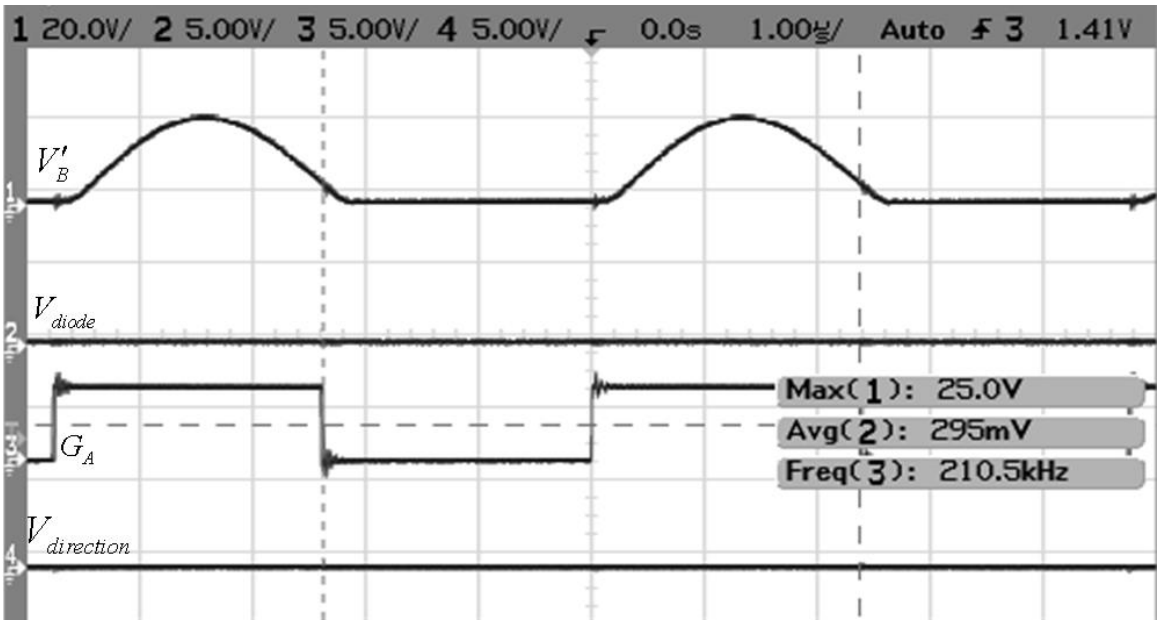


Figure 5–15 Practical circuit waveforms for operating with ZVS at critical coupling level (k_c).

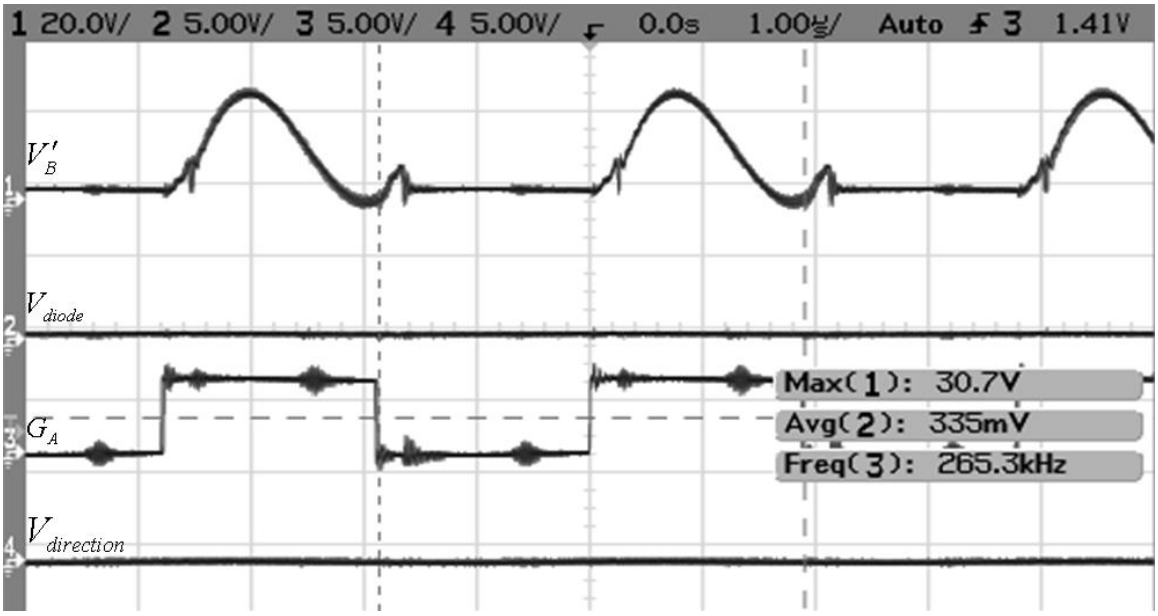


Figure 5–16 Practical circuit waveforms for operating with ZVS at maximum coupling level (k_{max}).

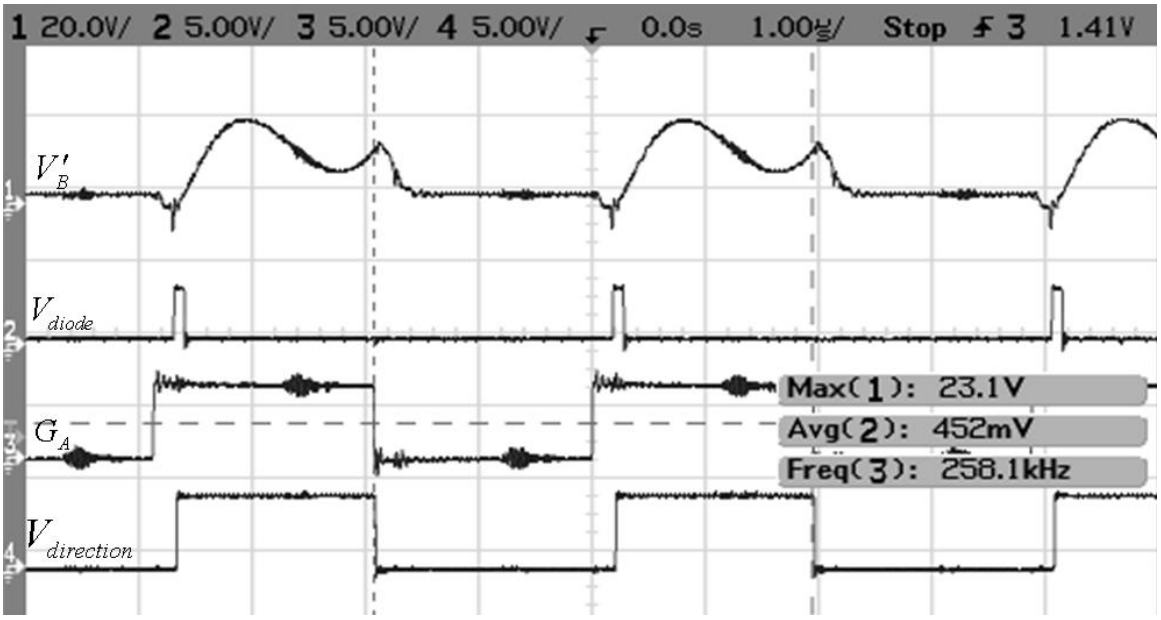


Figure 5–17 Practical circuit waveforms for approaching the middle ZVS branch from below.

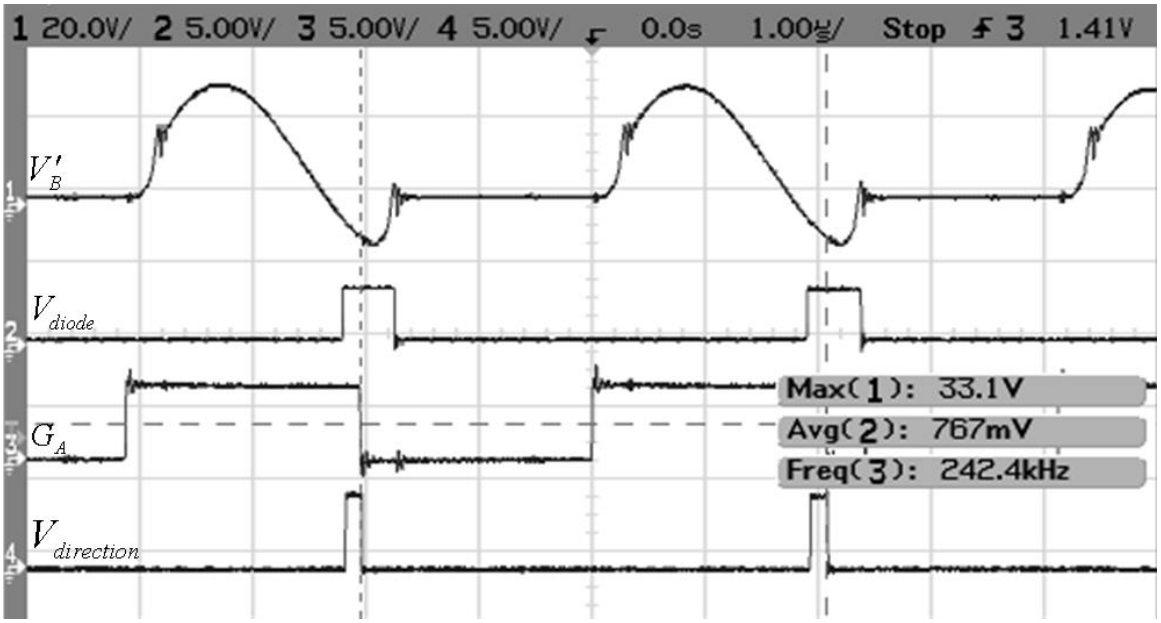


Figure 5–18 Practical circuit waveforms for approaching the middle ZVS branch from above.

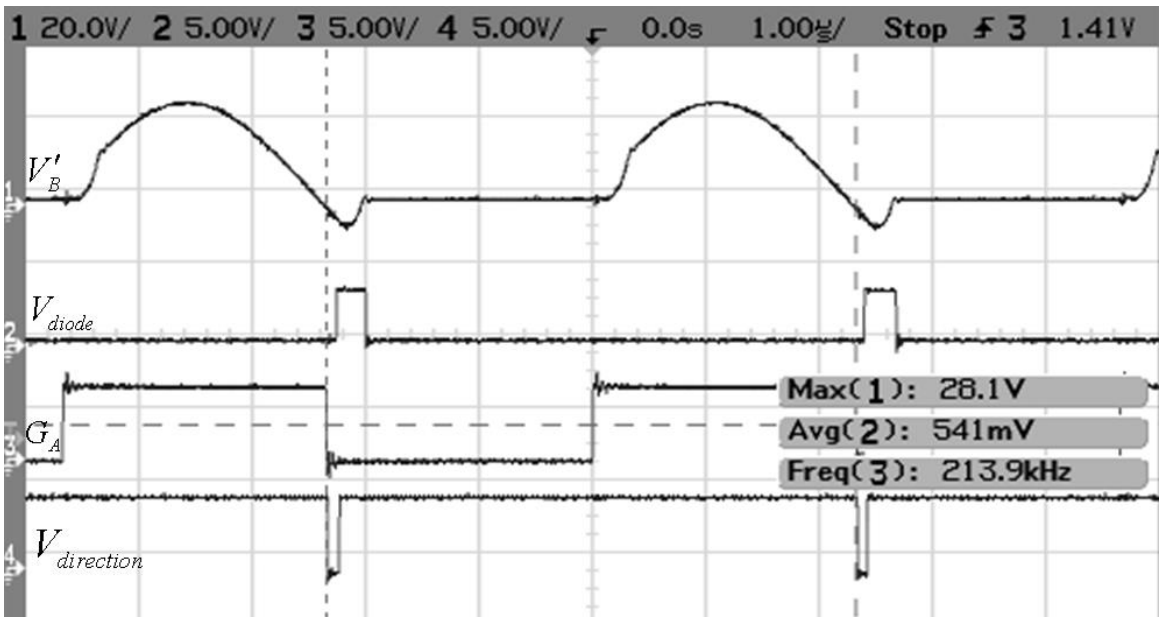


Figure 5–19 Practical circuit waveforms for special case control waveform due to comparator triggering hysteresis, logic and switching component delays.

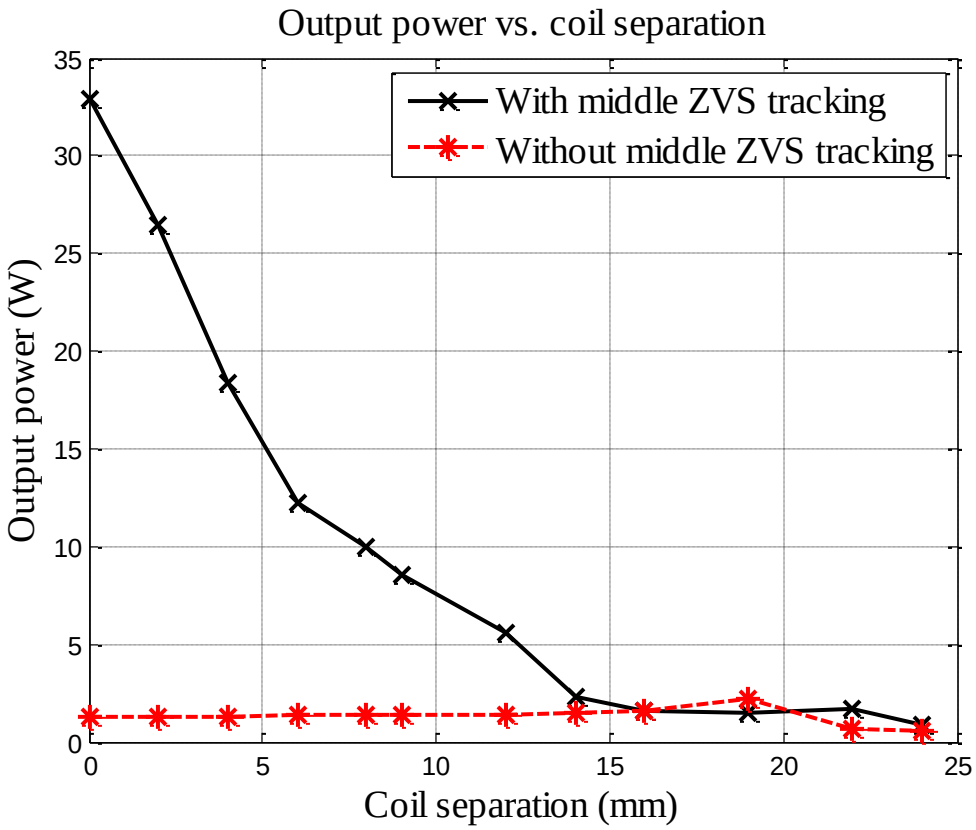


Figure 5–20 System output power vs. coil separation

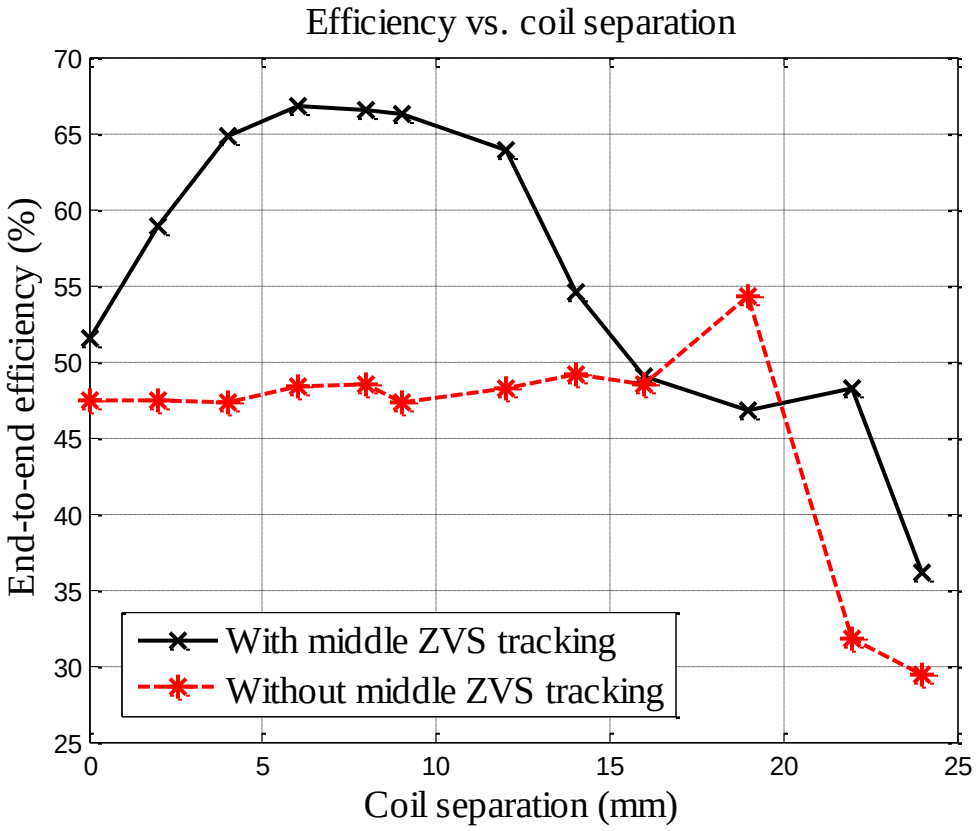


Figure 5–21 System end-to-end efficiency vs coil separation

Table 5–1 shows the practical parameters used to construct the system. The ESR of the primary (R_{Lp}) and secondary (R_{Ls}) coils are measured values, small variations of the chosen parameters in Table 5–1 is allowed while large variations may change the bifurcation curve and the maximum power tracking positions. Figure 5–14 shows the experimental setup. The system has a primary converter to transfer power across a pair of TET coils with an adjustable air gap; the secondary contains a rectifier, and the heart pump is modelled by a resistive 10 Ω load. The digital programming of the ZVS follower is implemented inside a CompactRIO controller, which adjusts the operating frequency according to feedback conditions from the primary converter. Further details on this CompactRIO controller implementation can be found in Appendix F. Figure 5–15 and Figure 5–16 show practical waveforms with the system operating with ZVS at critical and maximum coupling levels respectively. Figure 5–17 and Figure 5–18 show practical waveforms with the system approaching the middle ZVS branch from below and above respectively. Figure 5–19 shows the effect of comparator hysteresis, logic and switching component delays on $V_{direction}$. This is a special case and sets the direction to zero.

The output power and end-to-end efficiency are plotted in Figure 5–20 and Figure 5–21 when running the system with and without middle ZVS tracking. When operating without middle ZVS tracking, the system operates instead at the lower ZVS branch with less power potential. Power drops with coil separation along the middle ZVS curve while increasing slowly along the lower ZVS curve. A maximum power transfer of 32.9W occurs at closest coupling level (0mm coil separation). In a similar way, Figure 5–21 shows end-to-end efficiency with and without middle ZVS tracking. With increased coil separation and middle ZVS tracking, the efficiency increases then drops away after reaching a maximum. A maximum efficiency of 66.7% is achieved when delivering 12.3W at a coil separation of 6mm.

Figure 5–20 and Figure 5–21 also show that operating at the middle ZVS branch, the system is able to deliver the rated 10W power to the heart pump with an 8mm coil separation and a 66.5% end-to-end efficiency.

It has been found that to deliver 10W via the lower ZVS branch would require a higher input voltage of 20V and the closest coupling level (0mm coil separation). The higher input voltage results in larger resonant tank voltage and track current, which increases coil losses and lowers the end-to-end efficiency to 59%.

5.2.4. Discussion

The practical system has used two different V_{diode} references for proportional and integral control, depending on the state of the toggle variable. When toggle is set to one, reference is 0.2V, and when toggle is set to zero, reference is 0.1V, which ensures a smoother transition between non-bifurcated and bifurcated regions.

At steady state, since V_{diode} represents closeness to exact ZVS operation, having a V_{diode} reference means the proportional and integral action will ramp toward and stabilise at the set reference level. The system therefore may have a small frequency offset from exact ZVS operation. In addition, when approaching ZVS operation from below the middle ZVS branch, the system may oscillate near ZVS as direction keeps changing between one and zero.

5.3. Primary Side Control without Blocking Diodes

The previous maximum power tracking control is based on detection of negative voltages in V'_B, which is due to the two blocking diodes, D_A and D_B, shown in Figure 5–2. These two diodes can be removed, as shown in Figure 5–22. The primary side is a current-fed parallel tuned push-pull converter driven by a dc input, V_{IN}. The secondary is parallel tuned with a passive current doubler rectifier and a resistive load, R_{LOAD}. V'_A and V'_B are the drain to source voltages of MOSFETs Q_A and Q_B respectively. The MOSFETs are driven by two complementary 50% duty cycled square waveforms. A current transformer is added between the sources of the primary MOSFETs to detect shorting current giving V_{CT+} and V_{CT-}. The feedback signal processing module inputs are V'_A, V'_B, V_{CT+},V_{CT-} and G_A and the outputs, V_{Res_shrt} and V_{CT} indicate the presence of a resonant shorting period and instant capacitor shorting respectively. These two dc signals are processed by analogue to digital converter (ADC) modules within the CompactRIO controller, and then a frequency control software algorithm is applied to determine the system switching frequency. A gate driver is used to properly drive the two low-side primary MOSFETs. Note this method is based on detecting shorting current which was prevented by the previous method that had blocking diodes, therefore this method will not work when shorting current goes beyond the ratings of the switching devices.

The details of the feedback signal processing module is shown in Figure 5–23. The differential of V'_B and V'_A is compared to ground with hysteresis and then low pass filtered to give V_{Res_shrt}, which shows the presence of a resonant shorting period.

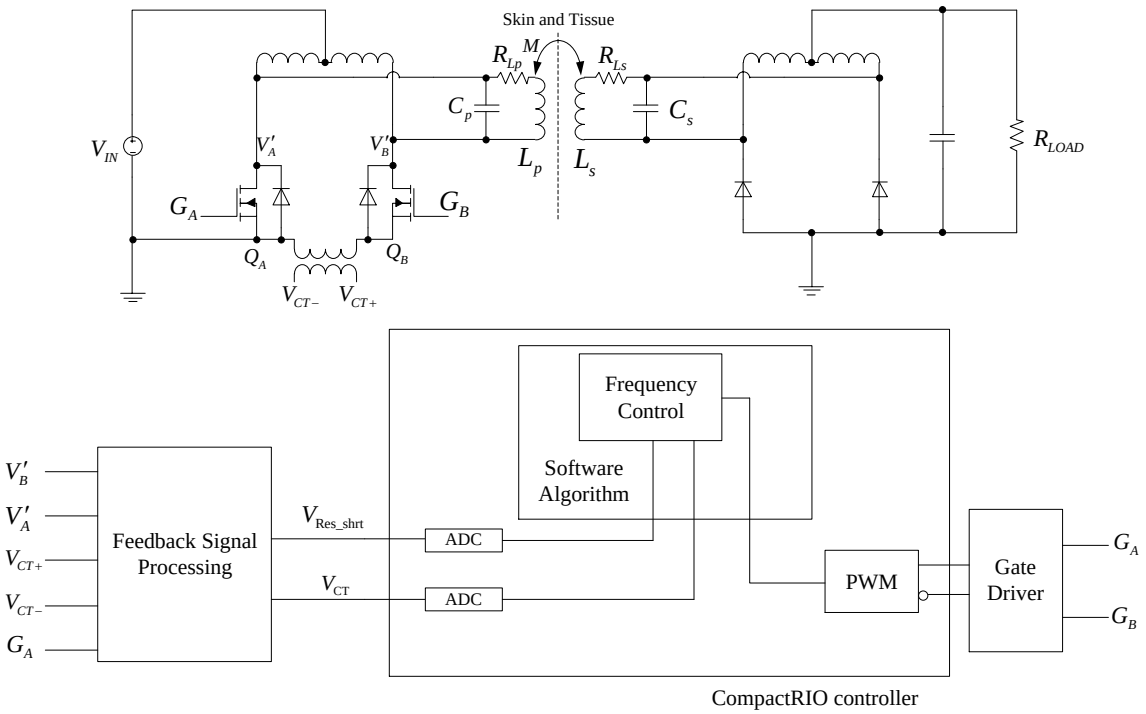


Figure 5–22 System overview of the proposed ZVS tracker that operates at near peak power flow potential

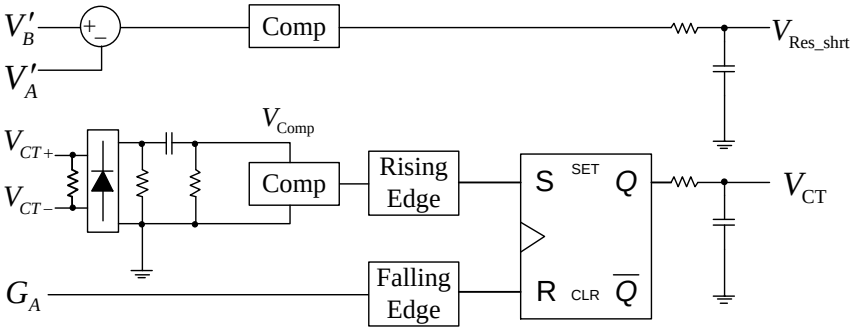


Figure 5–23 Feedback signal processing details

The current transformer output signals, V_{CT+} and V_{CT-} are full bridge rectified and high pass filtered to flip the negative polarities to the positive and then remove dc offset. This leaves only voltage spikes during instant capacitor shorting or resonant shorting (V_{Comp}). The voltage spikes are compared to ground with hysteresis and the rising edge of the resulting waveform is used to set a SR latch while the falling edge of G_A resets the latch. The SR latch output is low pass filtered to generate V_{CT}, which shows the presence of instant capacitor shorting or resonant shorting. The controller avoids the indication of

resonant shorting from V_{CT} as it can be in contradiction with instant capacitor shorting as will be clarified later. Together V_{Res_shrt} and V_{CT} determine when to stop frequency variations after reaching ZVS and when to change the direction for frequency movement.

5.3.1. Circuit Operation Theory

The relationship between the resonant tank ac peak voltage and the dc input voltage at full ZVS operation is shown in (5.2).

$$\hat{V}'_{AB} = \pi V_{IN} \tag{5.2}$$

The system ZVS frequency bifurcation caused by coupling variation is shown in Figure 5–24. Compared to Figure 5–4, the curve removed the offset frequency. The controller proposed here is not PI and does not require an offset frequency.

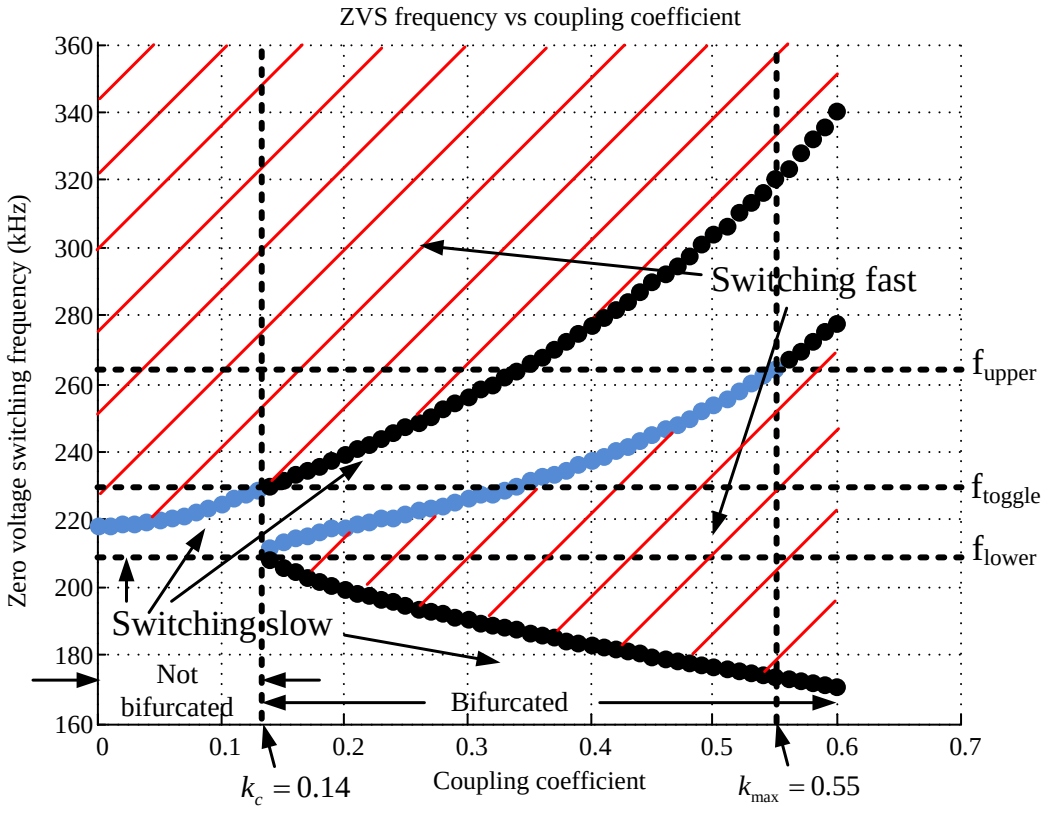


Figure 5–24 Bifurcation plot of ZVS frequency with coupling variations

Direction will be assigned as ‘one’ when the system is switching fast with a negative impedance phase angle and will be assigned as ‘zero’ when the system is switching slow with a positive impedance phase angle.

Figure 5–25 shows a system operating with ZVS. There is no shorting current through the current transformer so the SR latch will never be set and V_{CT} will remain low. The reset trigger will always be present as it depends on gate drive signal G_A.

The system is switching fast in Figure 5–26; the instant capacitor shorting current flows through the current transformer, and this shows up as regular voltage pulses in V_{Comp} and is compared to ground with hysteresis. The resulting waveform sets SR on its rising edge and the falling edge of G_A resets SR to produce V_{CT}.

The system is switching slow in Figure 5–27. The resonant shorting current flows through the current transformer resulting in regular voltage pulses in V_{Comp}. In comparison to fast switching, the pulses have a smaller magnitude and occur slightly earlier relative to G_A. This produces a square wave V_{CT}. Figure 5–28 shows an alternative ideal waveform during slow switching. Note that the resulting V_{CT} is very similar to that of Figure 5–26, which will cause conflicting logic and should be avoided.

By using the dc values of V_{Res_shrt} and V_{CT}, the CompactRIO controller determines whether the system is operating under ZVS to stop further frequency variations. In addition, it would determine when to increment or decrement frequency.

5.3.2. Controller Design

A ‘toggle’ variable is required to distinguish the difference of frequency direction in non-bifurcated and bifurcated regions. The value of toggle will be swapped between one or zero after saturating at either the lower frequency boundary (f_{lower}) or the upper frequency boundary (f_{upper}) for every set wait time. In addition, the toggle will be reset when system frequency exceeds toggle frequency (f_{toggle}) in the presence of resonant shorting. Toggle frequency is pre-set at the interface between non-bifurcated and bifurcated regions.

5.3.2.1. Start-up Sequence

The coupling level can range from 0 to 0.55 (k_{max}) for the current TET coil design. At start-up, the controller starts at f_{toggle} with toggle as zero. When starting coupling level is lower than the critical coupling (k_c), the system is switching fast and will increment to f_{upper} and set toggle after wait time. The frequency then ramps down to stabilise at the single ZVS branch. When starting coupling level is between k_c and 0.35, the switching frequency will decrease toward the middle ZVS branch. When the starting coupling level

is between 0.35 and k_{max}, the switching frequency will increase towards the middle ZVS branch.

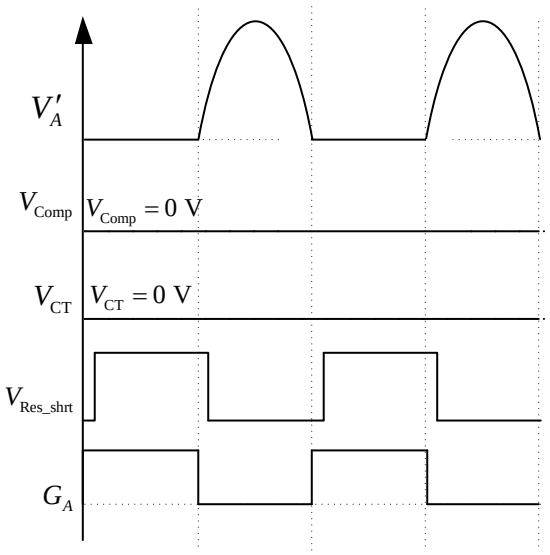


Figure 5–25 Switching with ZVS operating at zero resonant tank impedance phase angle

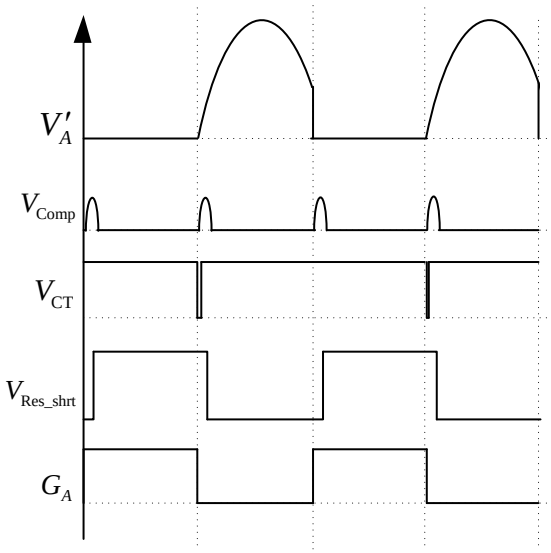


Figure 5–26 Fast switching with a negative resonant tank impedance phase angle

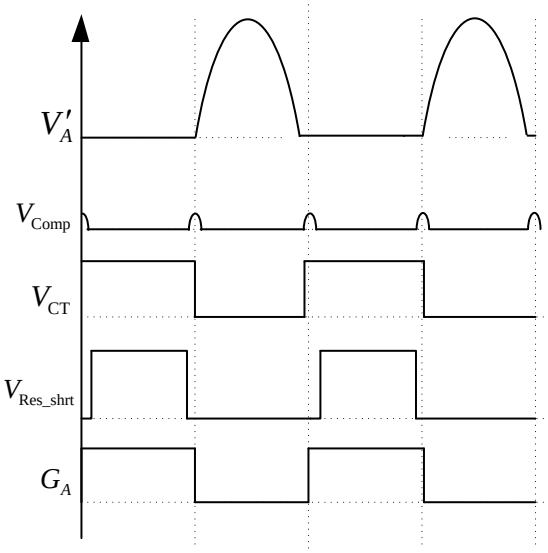


Figure 5–27 Slow switching with a positive resonant tank impedance phase angle

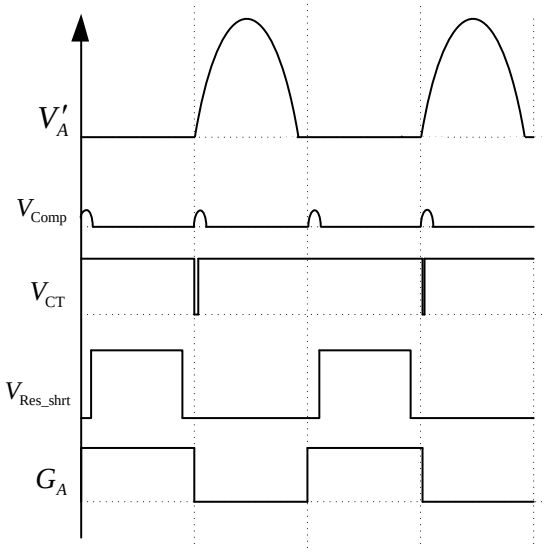


Figure 5–28 An alternative slow switching system response

5.3.2.2. Normal Operation

After start-up, by decreasing coil separation (or increasing coupling level) from a very large separation, the system frequency will ramp to and saturate at f_{upper} to set toggle, and then stabilise at the single ZVS branch. As coil separation decreases further, direction will become one and toggle will be reset by saturating at $f_{lower.}$ Further reduction in coil separation will force the system to track the middle ZVS branch for peak power.

Alternatively, starting at the closest coupling level and by increasing coil separation (or decreasing coupling level), the system tracks the middle ZVS branch. As coil separation

increases, the system will cross the upper ZVS branch and will ramp to and saturate at f_{upper} to set toggle, and then stabilise at the single ZVS branch.

5.3.2.3. Controller Logic

Figure 5–29 shows the logic behind the frequency controller. The system first determines the state of toggle; then the frequency is incremented or decremented according to the value of toggle and direction.

There are three states for the direction variable: zero, one or two. With toggle as zero, a direction of zero means ‘decrement frequency’ while a one means ‘increment frequency’. Once toggle is set the movement direction reverses. When the direction is two, the system stops frequency variations as it has reached a satisfactory ZVS operation.

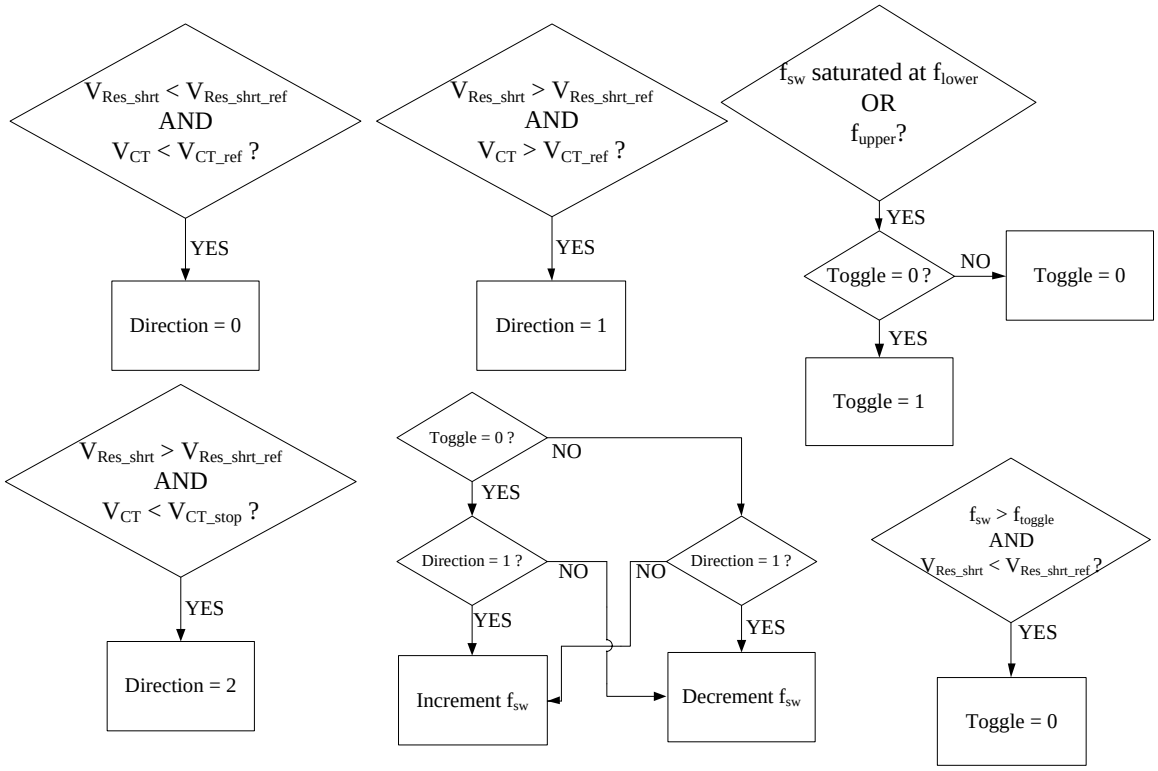


Figure 5–29 Logic flow for ZVS follower

The references for V_{CT} and V_{Res_shrt} are set slightly lower than their corresponding dc averages from Figure 5–26. The movement direction is determined by the value of V_{Res_shrt} and V_{CT} by comparing to their references. For direction to be assigned to zero, the system needs to be slow switching and to have a resonant shorting period, so V_{Res_shrt} and V_{CT} should be less than their references. For direction to be assigned to one, the

system must have instant capacitor shorting, and V_{CT} and V_{Res_shrt} should be greater than their references.

Figure 5–25 shows the waveforms when direction should be two, and neither resonant shorting nor instant capacitor shorting exist, so V_{Res_shrt} should be greater than its reference. V_{CT} should be less than V_{CT_stop}, which is set close to 0.1 V.

It is desirable to avoid the conflicting alternative slow switching waveform from Figure 5–28, which has a V_{CT} greater than its reference and a V_{Res_shrt} less than its reference. This does not alter the direction as it does not satisfy any of the pre-existing logic conditions.

5.3.3. Simulation and Experimental Results

Figure 5–30 shows the simulated system internal waveforms with increasing coupling levels. The system switching frequency (f_{sw}) first tracks the single ZVS branch, and then tracks the middle ZVS branch. The middle plot shows the direction changing for the system to ramp towards the target ZVS operation. The simulation was performed using the effective ac load, so the bottom plot shows an increasing effective V_{LOAD} peak with an increasing coupling level.

Similarly, Figure 5–31 shows the case for simulated internal system waveforms by decreasing the coupling level. The switching frequency and the effective V_{LOAD} peak decrease with the decrementing coupling level. The direction is changed to track system frequency towards the desired ZVS branches. Here the effective V_{LOAD} at the resonant tank is plotted in Figure 5–30 and Figure 5–31 to simplify and speed up the simulation process.

Figure 5–32 and Figure 5–33 are simulation waveforms showing the system approaching the middle ZVS branch from below and above respectively. Further details on this PLECS simulation can be found in Appendix G.

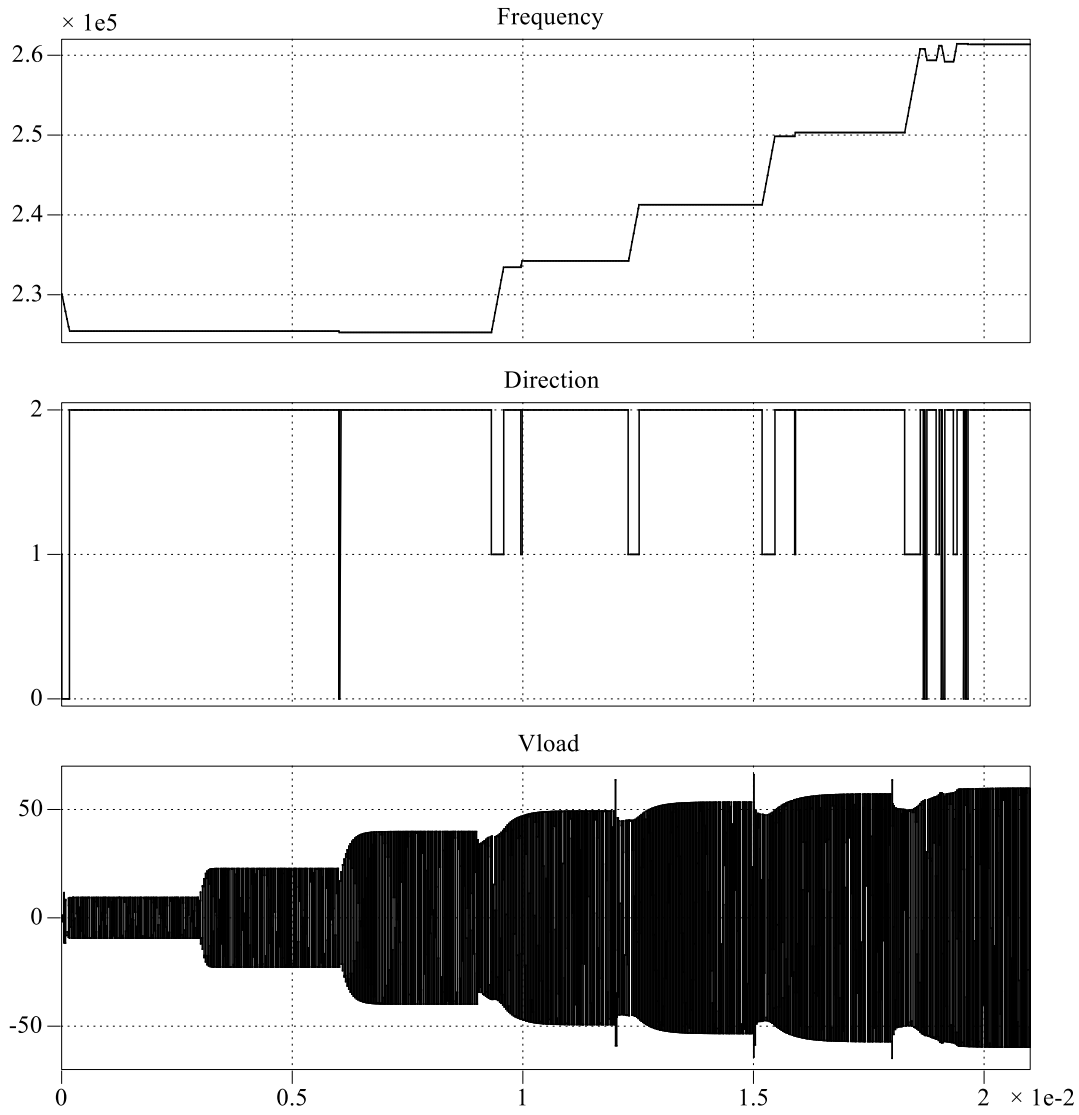


Figure 5–30 Simulated system internal waveforms with increasing coupling levels

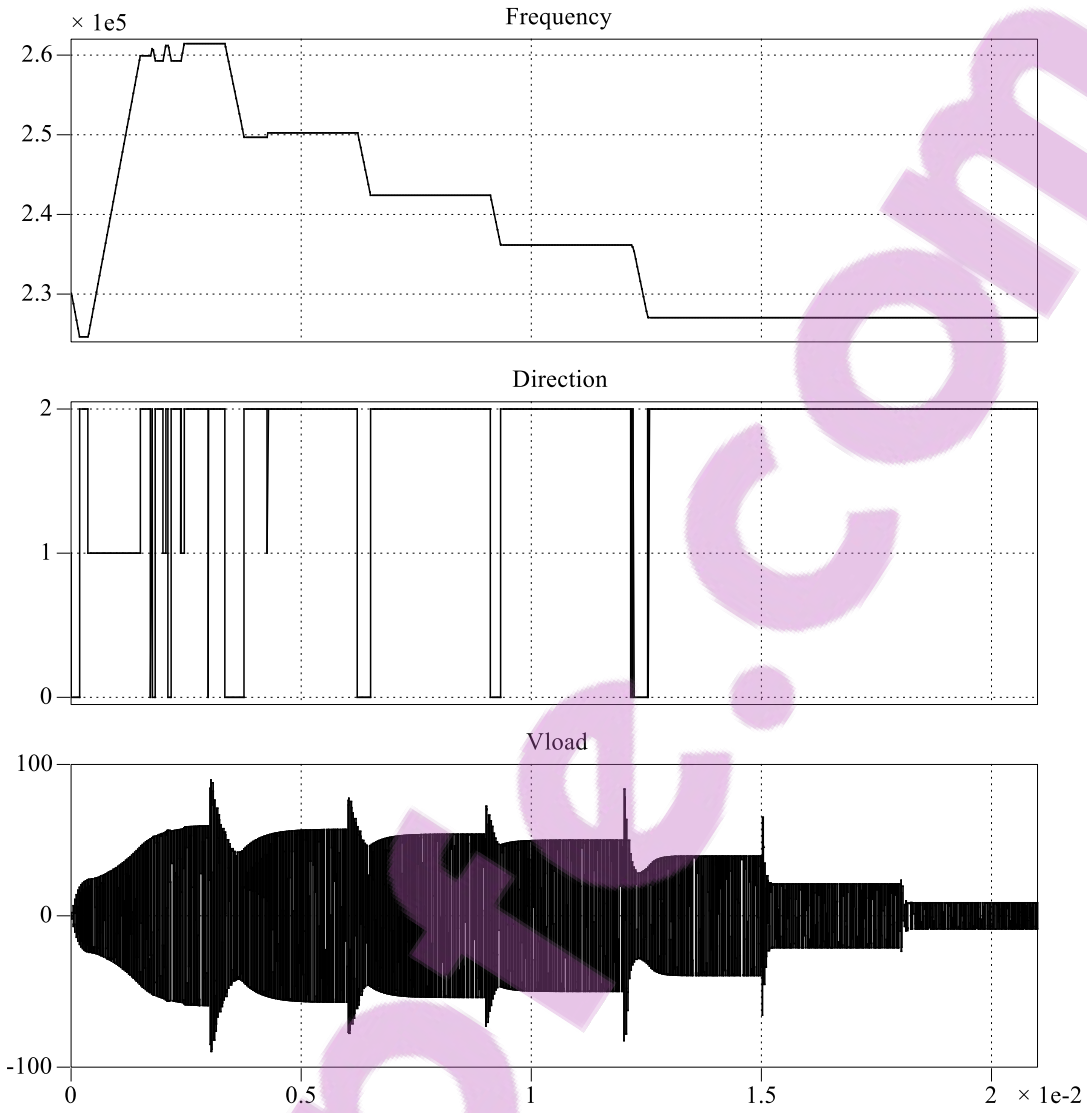


Figure 5–31 Simulated system internal waveforms with decreasing coupling levels

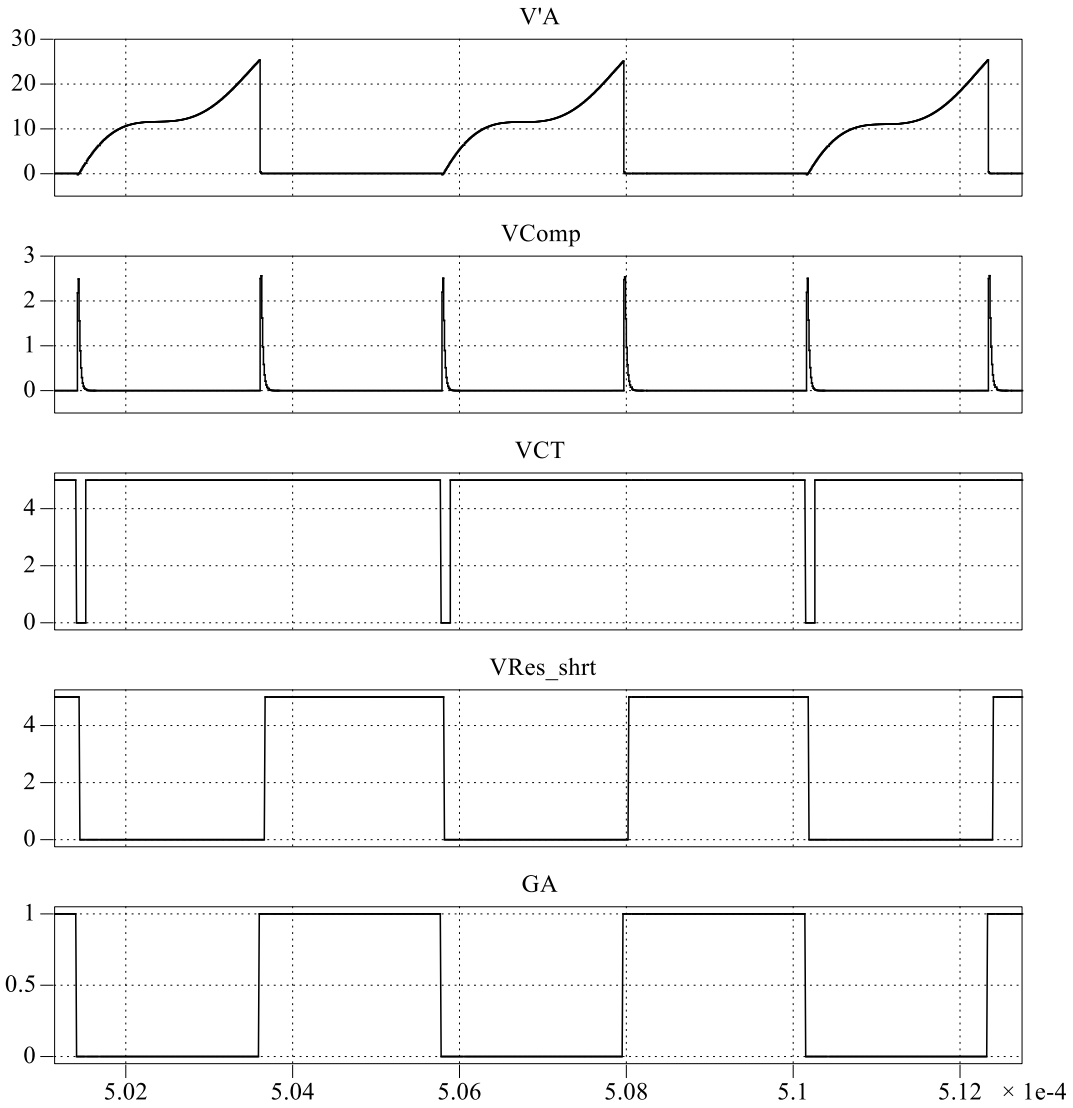


Figure 5–32 Simulation waveform with system approaching middle ZVS branch from below

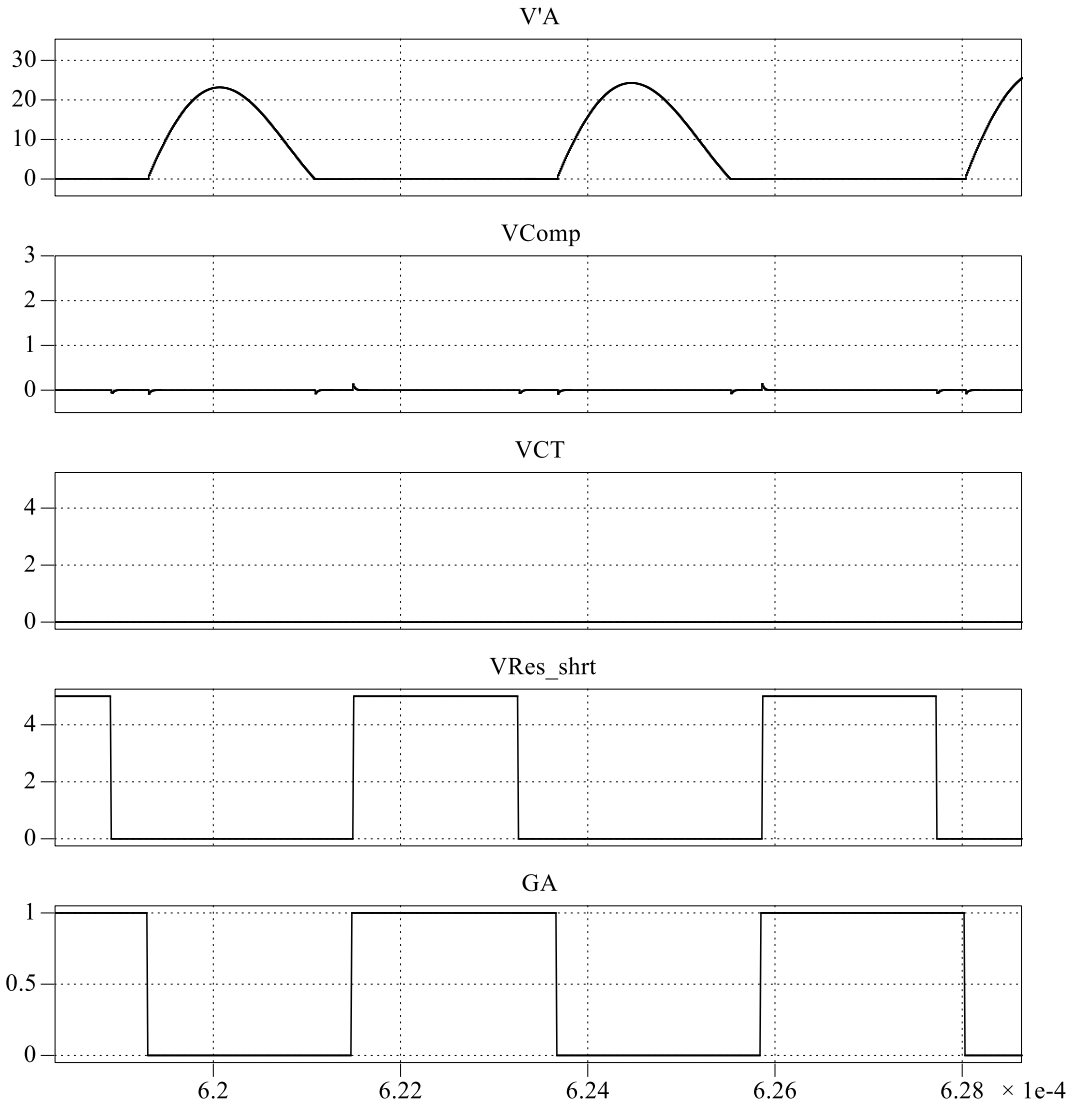


Figure 5–33 Simulation waveform with system approaching middle ZVS branch from above

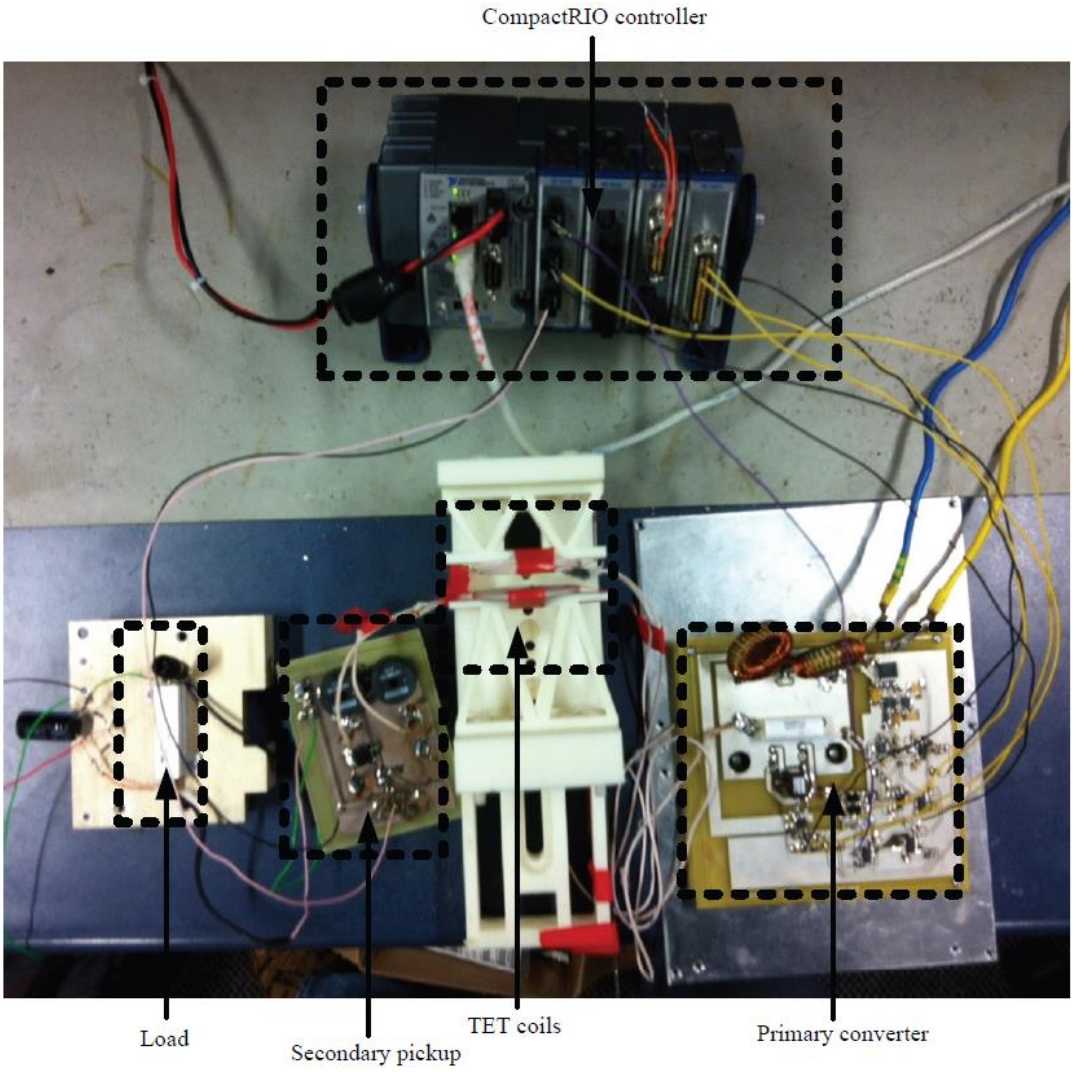


Figure 5–34 Experimental setup

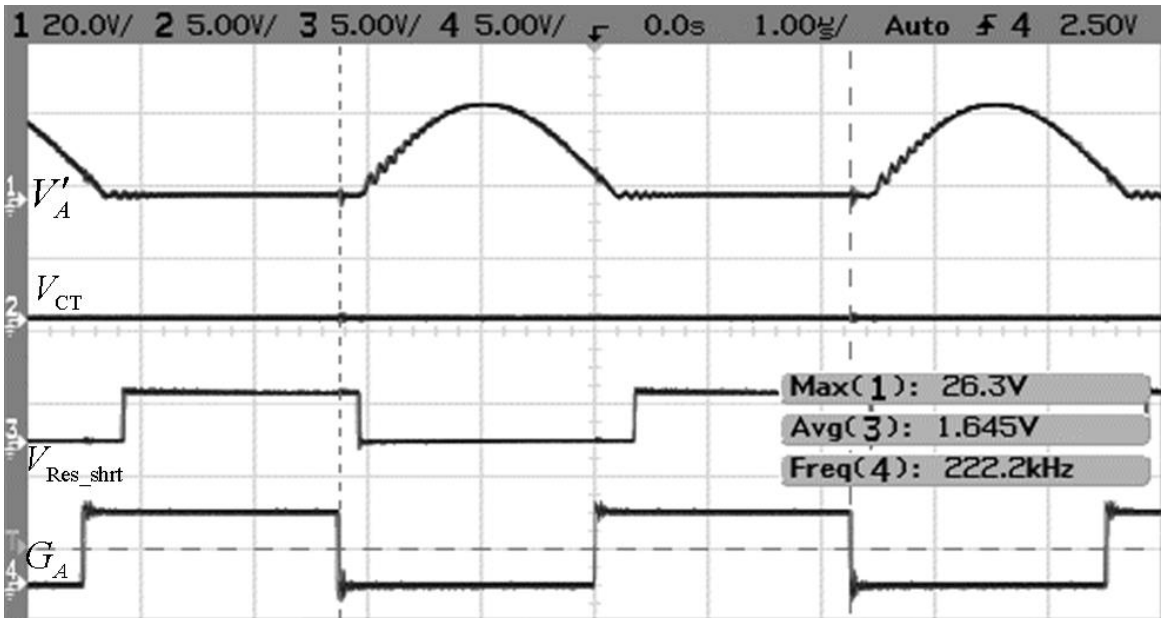


Figure 5–35 Practical circuit waveforms for operating with ZVS at critical coupling level (k_c).

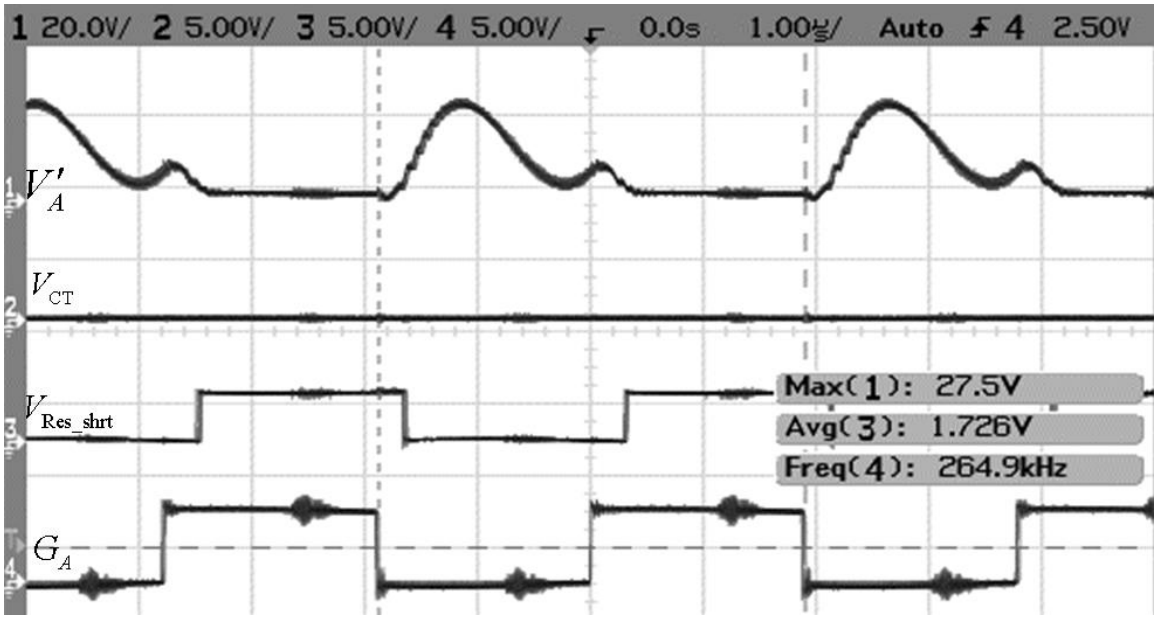


Figure 5–36 Practical circuit waveforms for operating with ZVS at maximum coupling level (k_{max}).

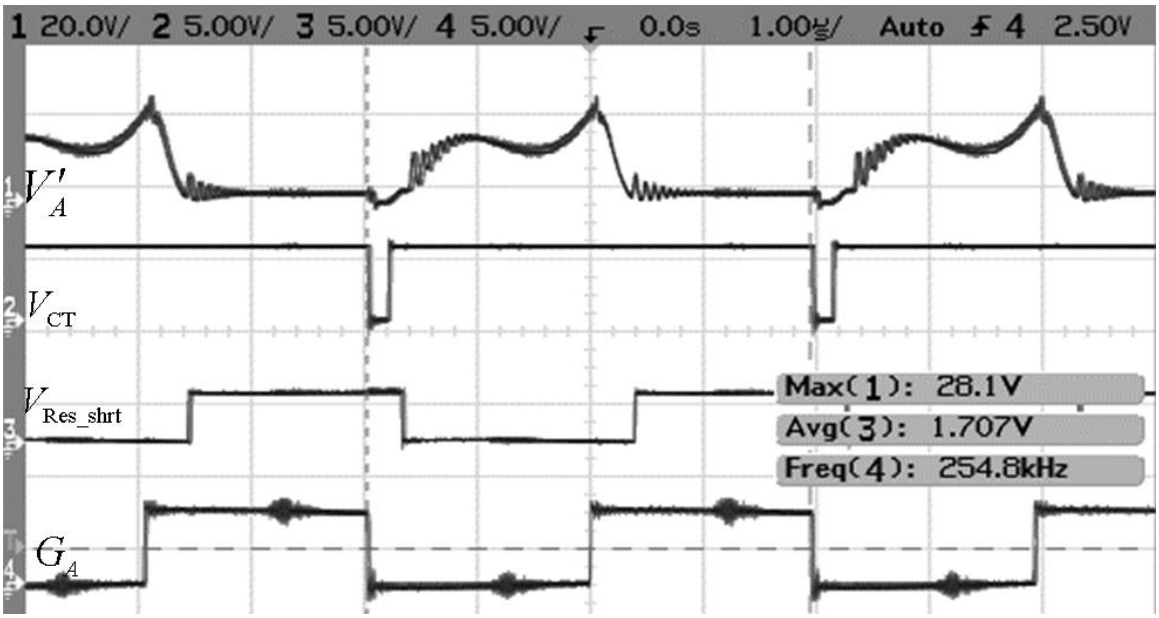


Figure 5–37 Practical circuit waveforms for approaching the middle ZVS branch from below.

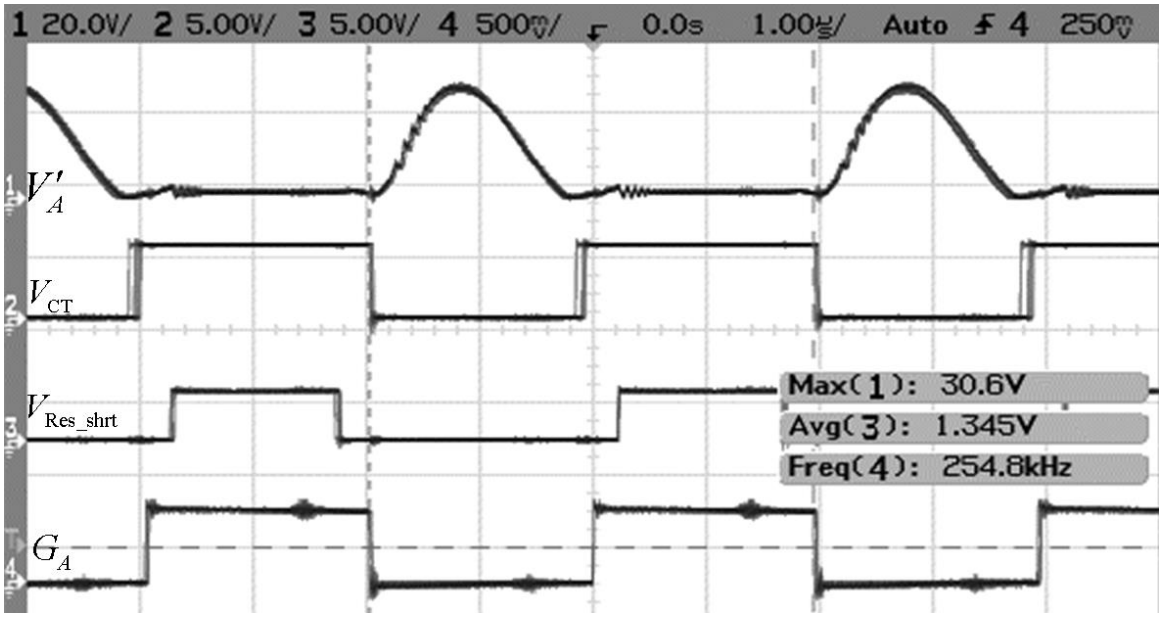


Figure 5–38 Practical circuit waveforms for approaching the middle ZVS branch from above.

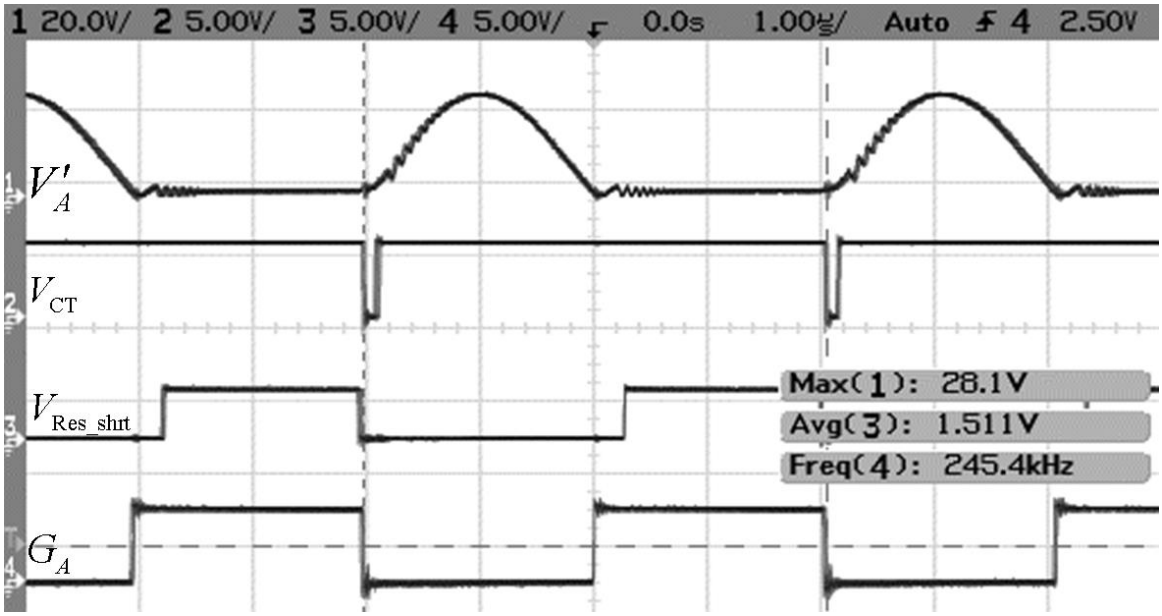


Figure 5–39 Practical circuit waveforms for the alternative slow switching system response.

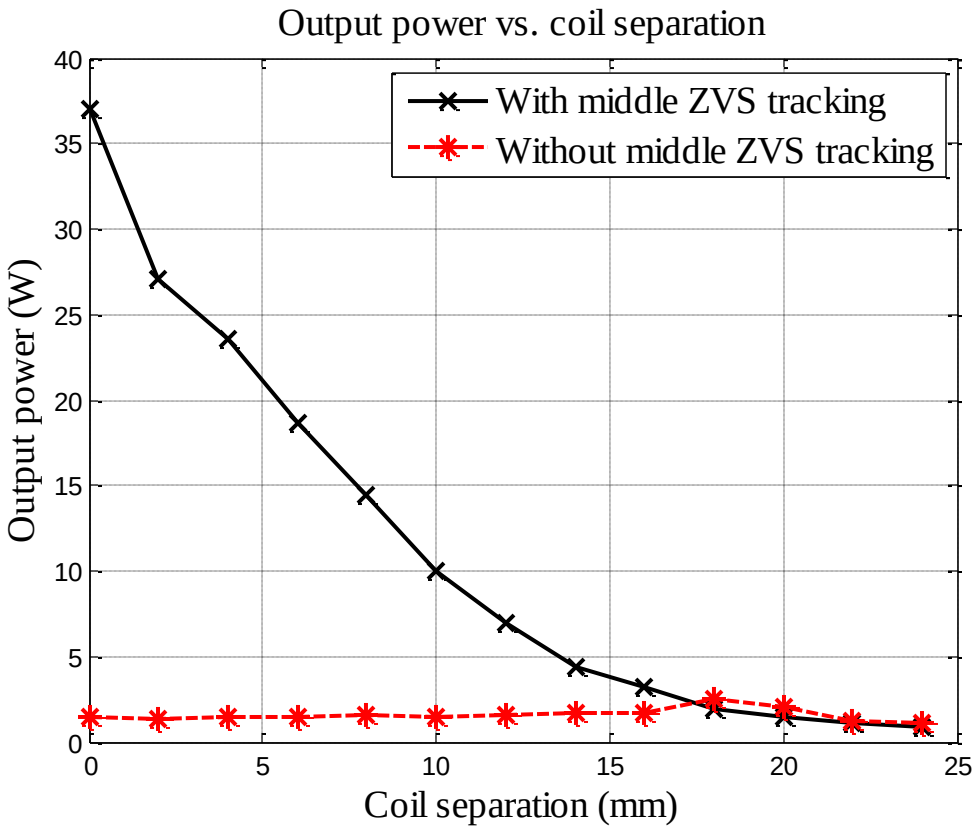


Figure 5–40 System output power vs. coil separation

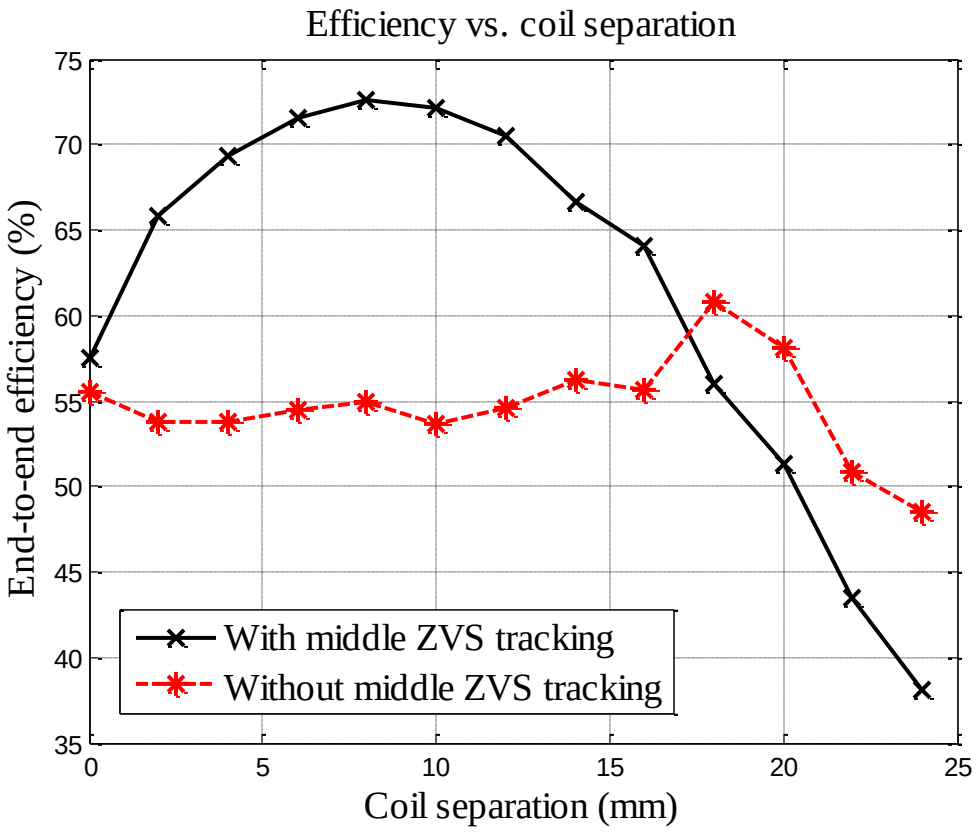


Figure 5–41 System end-to-end efficiency vs. coil separation

Table 5–1 has been used again as practical parameters to construct this system. Figure 5–34 shows the experimental setup consisting of the primary converter, TET coils, secondary pickup, load and a CompactRIO based controller to implement the ZVS follower. Further details on this CompactRIO controller implementation can be found in Appendix H. Figure 5–35 and Figure 5–36 show practical waveforms with the system operating with ZVS at critical and maximum coupling levels respectively. Figure 5–37 and Figure 5–38 show practical waveforms with the system approaching the middle ZVS branch from below and above respectively. Figure 5–39 shows the alternative slow switching situation, which is avoided as it is in conflict with the fast switched V_{CT} waveforms in Figure 5–37.

The output power and end-to-end efficiency are plotted in Figure 5–40 and Figure 5–41, when running the system with and without middle ZVS tracking. When operating without middle ZVS tracking, the system operates instead at the lower ZVS branch with less power potential. Power drops with coil separation along the middle ZVS curve while increasing slowly along the lower ZVS curve. A maximum power transfer of 36.98W occurs at the closest coupling level (0mm coil separation). Figure 5–41 shows end-to-end efficiency with and without middle ZVS tracking. The efficiency increases then drops away after reaching a maximum. A maximum efficiency of 72.6% is achieved when delivering 14.4W at a coil separation of 8mm.

Figure 5–40 and Figure 5–41 also show that by tracking the power peak and operating at the middle ZVS branch, the system is able to deliver the rated 10W power to the heart pump with a 10mm coil separation and a 72.2% end-to-end efficiency.

It has been found that to deliver 10W via the lower ZVS branch would require a higher input voltage of 20.6V at the closest coupling level, and a higher input voltage results in larger resonant tank voltage and track current, which increases coil losses and lowers the end-to-end efficiency to 60.3%.

Because it is difficult to model the practical circuit accurately, there are differences between the simulated and practical circuit transformer output and this therefore impacts on the appearance of V_{Comp}. The frequency of the practical circuit settles down and does not have the variations displayed in Figure 5–30 at closest coupling. Neither does the direction change as often in the practical circuit.

5.4. Conclusions

Two ZVS followers have been proposed to track the non-bifurcated ZVS operating points and the bifurcated middle ZVS points of TET systems based on current-fed parallel-parallel tuned resonant converters so as to maintain ZVS operation and maximum power transfer potential in a wide range. A practical TET system with blocking diodes was constructed and is capable of transferring a maximum power of 32.9W at closest coupling level and a highest efficiency of 66.7% when delivering 12.3W at 6mm coil separation. Another TET system without blocking diodes was capable of transferring a maximum power of 36.98W at closest coupling level, and a highest efficiency of 72.6% when delivering 14.4W at 8mm coil separation. The ZVS followers are able to deliver the rated 10W power required to drive a 10Ω heart pump load at a lower input voltage, larger coil separation and an improved efficiency compared with simple ZVS controllers which cannot track the middle ZVS branch when the system is bifurcated.

Chapter 6

Synchronous Rectification Combined with Secondary Power Flow Control

6.1. Introduction

The previous work presented for this thesis considers power flow control at the primary side of IPT/TET systems. This chapter will present push-pull current doubler synchronous rectifiers for secondary power pickup circuits. Two gate drive options are investigated as a means to lower the system power losses. They help to increase the maximum system power transfer capability, or in improving the operation range at a fixed output power. Apart from synchronous rectification, the power switch gates are also controlled separately for variable resonant shorting periods to enable output voltage regulation.

6.2. Synchronous Rectifier

Transcutaneous energy transfer offers a means of transmitting power across the skin from an exterior primary side circuitry to an implanted secondary side circuitry without using a percutaneous driveline penetrating the skin [37]. Eliminating this percutaneous driveline could significantly reduce the risk of infection [109]. In a TET system, apart from supplying the required power to drive the heart hump, one important challenge is to reduce the power loss at the implanted pickup circuit, so as to reduce the heat generation and associated temperature rise. Lower power losses would also improve the system operational range. Because heart pumps are driven by a dc voltage, a rectifier is needed at the power pickup, which is a source of power loss. Synchronous rectifiers can be used to replace diode rectifiers to reduce the conduction losses of diodes, but complicated control circuits are often required. The zero crossings of the ac voltage were detected and a special ZVS circuit was designed to drive a push-pull synchronous rectifier [110], but the circuit was too complicated and power loss caused by the additional circuits was high. Miura *et al.* [78, 79] also researched push-pull synchronous rectifiers for TET systems

using PLL control, and again the system was complicated and overhead power loss became high. In this chapter, a simple autonomous synchronous rectifier based on push-pull current doubler topology is introduced, and two drive options are proposed to lower the power loss of the implanted circuitry. The first drive option is fully self-sustained, using passive components without the need of any auxiliary power supply and gate driver; while the second option uses a buffering circuit to improve the gate drive waveforms.

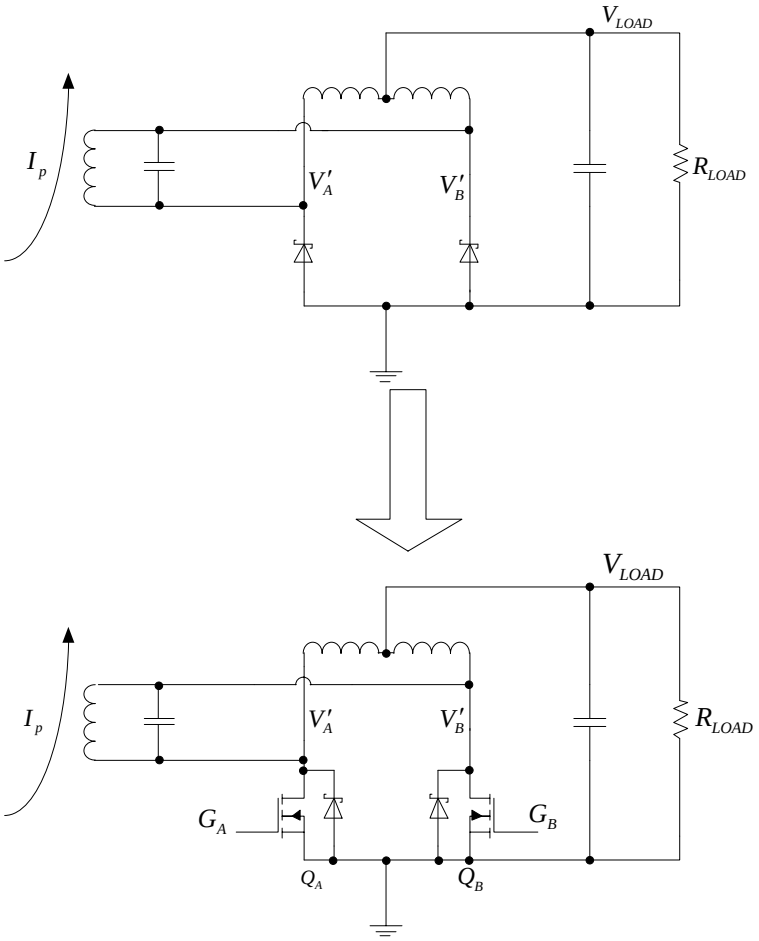


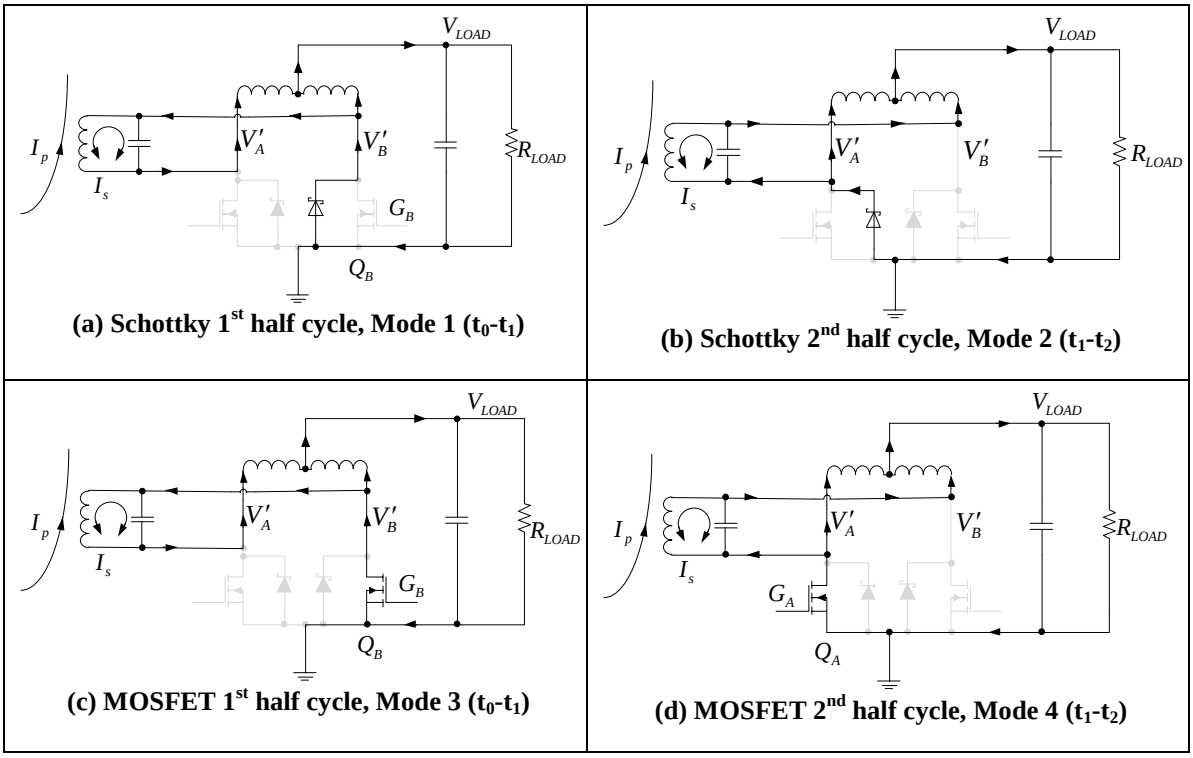
Figure 6–1 Proposed main synchronous rectifier circuit

6.2.1. Proposed Circuit and Operating Principle

Figure 6–1 shows the main circuit of the proposed push-pull synchronous rectifier with the two passive Schottky diodes replaced with two active MOSFETs Q_A and Q_B. Two additional Schottky diodes are placed in parallel with the MOSFET to short out MOSFET body diodes, in order to lower losses on startup and other MOSFET non-conduction periods. Because the proposed push-pull synchronous rectifier contains only low side MOSFETs, high side gate drives are not necessary. Such a synchronous rectifier is named a ‘current doubler’ because the heart pump load current is doubled, when compared with

the average current through each MOSFET. This is made possible by the current addition of the two dc inductors at the positive terminal of the load.

Figure 6–2 shows the circuit operation from startup to normal operation. On startup (Mode 1 and 2) the parallel Schottky diodes operate alternatively to increase the heart pump load voltage. Once the load voltage reaches a sufficient level for the drive options, the gate drive circuit then begins to operate the MOSFETs and the circuit now operates as a synchronous rectifier with commutating MOSFETs (Mode 3 and 4).



(a) Schottky 1st half cycle, Mode 1 (t_0-t_1)

(b) Schottky 2nd half cycle, Mode 2 (t_1-t_2)

(c) MOSFET 1st half cycle, Mode 3 (t_0-t_1)

(d) MOSFET 2nd half cycle, Mode 4 (t_1-t_2)

Figure 6–2 Startup and steady state system operation; Schottky diodes ramp up load voltage in (a) and (b); and with sufficient voltage, the drive options enable synchronous rectification in (c) and (d).

Figure 6–3 and Figure 6–4 show two different drive options for the MOSFETs in order to make it a synchronous rectifier. Figure 6–3 shows the passive autonomous rectifier drive option using simple components like capacitor, resistor and Zener, whereas the autonomous rectifier with buffer circuit drive option in Figure 6–4 uses a gate driver to improve the output waveform. Both options employ the MOSFET drain to source voltages (V'_A and V'_B) as the inputs and derive the gate drive signals from them. The passive autonomous rectifier feeds V'_A to a resistor and Zener to limit the voltage to the Zener voltage; a speed up capacitor is in parallel with the Zener resistance to give the right gate driving voltage G_B, and similar action is applied to obtain G_A from V'_B.

The autonomous rectifier with the buffer circuit feeds V'_A through a resistor and Zener to limit V'_A to the Zener voltage, and applies this voltage into a gate driver to generate G_B, a square wave for gate driving. Similar action is applied to obtain G_A from V'_B.

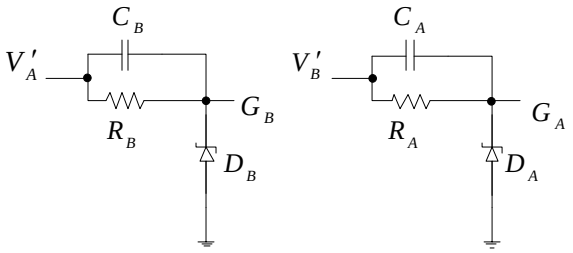


Figure 6–3 Passive autonomous rectifier drive option

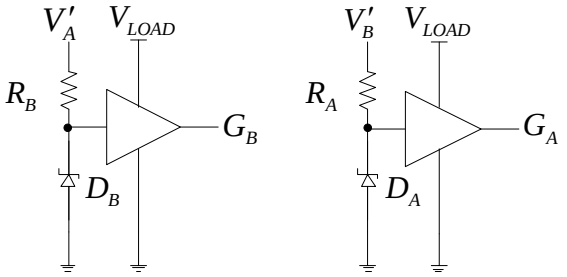


Figure 6–4 Autonomous rectifier with buffer circuit drive option

Figure 6–5 shows the theoretical waveforms for the passive autonomous synchronous rectifier. V'_A and V'_B are MOSFET drain to source voltages for MOSFETs Q_A and Q_B respectively. G_A and G_B are gate drive voltages for MOSFETs Q_A and Q_B respectively. During the first half cycle (Mode 3), G_B rises and falls with V'_A and is limited to the Zener voltage. G_B remains low with a low V'_A in the second half cycle (Mode 4). Similar detection approach and signal processing is applied to obtain G_A from V'_B.

The ideal gate drive waveforms are similar for the autonomous rectifier with buffer circuit synchronous rectifier as shown in Figure 6–6, but the gate driving waveforms are squarer.

The relationship between the resonant tank voltage peak and the heart pump load voltage is governed by (6.1), and (6.2) gives the equivalent resistance of the heart pump load seen by the secondary resonant tank.

$$\hat{v}_{ac} = \pi V_{LOAD} \tag{6.1}$$

$$R_{eq} = \frac{\pi^2}{2} R_{LOAD} \tag{6.2}$$

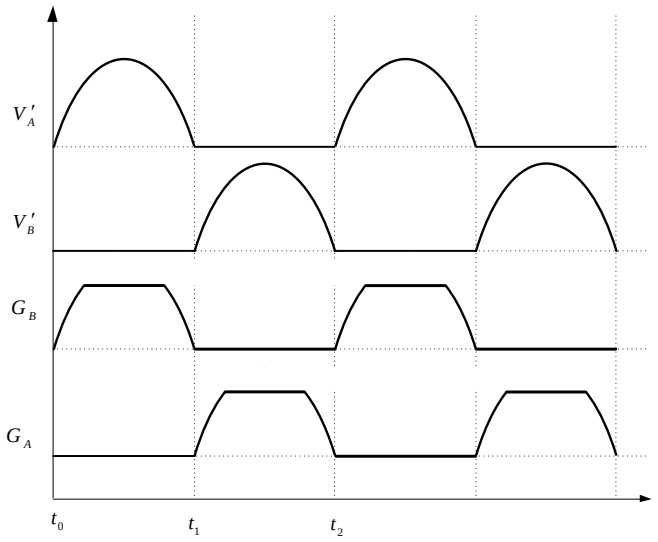


Figure 6–5 Theoretical passive autonomous synchronous rectifier waveforms

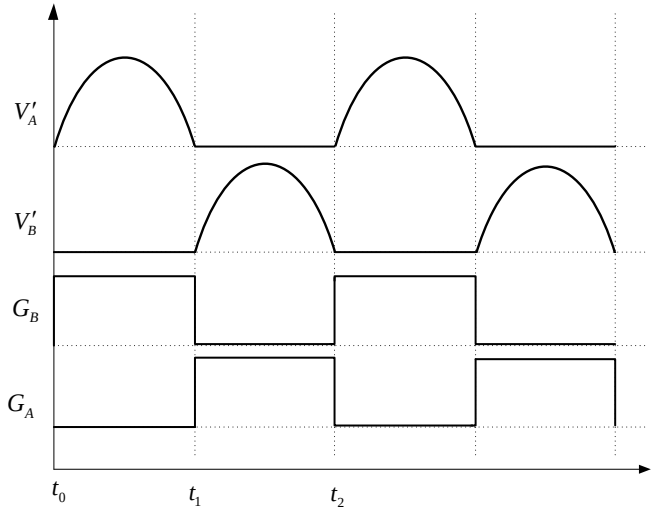


Figure 6–6 Ideal gate drive waveform for autonomous rectifier with buffer circuit

6.2.2. Circuit Design

Correct power rating components are selected for a 10V, 10Ω and 10W system. Here, a resistive load of 10Ω is used to model the practical operation of an implantable heart pump. To maximize efficiency, the synchronous MOSFETs are chosen to have a minimal total gate charge and ON-state resistance while withstanding the rated resonant voltage levels.

For the passive autonomous rectifier drive option, 10V Zener diodes are chosen to drive the MOSFETs properly. Zener saturation occurs when it is biased by at least 5mA (i_z), which depends on the difference between the ac peak given by (6.1) and the Zener voltage (V_z) as shown by (6.3). To improve the overall efficiency, the Zener bias resistor

(R_Z) is chosen to be high (~1.2kΩ) to reduce power dissipation, while sufficiently low to bias Zener correctly. This requires the speed-up capacitor to be about 1nF to avoid erroneous and unstable gate drive waveforms during startup and system operation.

$$\frac{\hat{v}_{ac} - V_z}{R_z} > i_z \tag{6.3}$$

For the autonomous rectifier with the buffer circuit, the same resistor and Zener setup is used before the gate driver. The ADP3624ARDZ gate driver was selected because it has a high switching speed and a high maximum single supply rating of 18V. The high maximum supply rating well exceeds the 10V rated load voltage and means the gate driver can be powered directly from the heart pump load voltage to remove the need of additional voltage regulators and their associated power losses.

The PCB board size was minimised to reduce noise through the use of surface mount components and tight component packing. Separate ground planes were used for signal and power in the autonomous rectifier with buffer circuit. The two ground planes were joined at the negative terminal of the heart pump load using a thicker track for the power ground and a thinner track for the signal ground. This attempts to avoid power ground currents affecting the signal ground and its components.

A 1nF commutation capacitance can be placed as close as possible to the drains of two MOSFETs to reduce switching noise and the commutation loop formed by the capacitor and the two MOSFETs. However it does not necessarily lead to better efficiency because of added power losses inside the commutation capacitor.

Table 6–1 System parameters

Primary coil inductance (L_p)	11.3 µH
Primary resonant capacitance (C_p)	47nF
Secondary coil inductance (L_s)	3.31 µH
Secondary resonant capacitance (C_s)	220nF
Load resistance (R_{LOAD})	10Ω
System switching frequency (f_{sw})	178 kHz
Coil separation	5mm

6.2.3. Simulation and Experimental Results

The primary side or exterior circuitry is a current-fed parallel tuned push-pull converter, which is essentially the same circuit as the current doubler synchronous rectifier, but with reversed operation. The end-to-end efficiency measurements are done with the primary resonating at zero voltage switching (ZVS) frequency.

Table 6–1 provides parameters used to construct the system. Figure 6–7 and Figure 6–8 show the simulation waveforms for the passive autonomous rectifier and the autonomous rectifier with buffer circuit respectively. Figure 6–9 shows the system experimental setup. It includes a primary converter, TET coils with adjustable coil separation distance, and then the synchronous rectifier and resistive load. Figure 6–10 and Figure 6–11 show the oscilloscope waveforms for the passive autonomous rectifier and autonomous rectifier with buffer circuit respectively. The simulation and experimental waveforms correspond well to each other.

The end-to-end power efficiency is measured when the coil separation is fixed at 5mm to keep the coupling coefficient constant. Under such a condition the ZVS frequency of the system is found to be 178kHz. Figure 6–12 shows the end-to-end efficiency against the output power delivered to the heart pump. These measurements are completed by incrementing the input voltage.

Figure 6–12 shows that the two proposed drive options have achieved similar end-to-end efficiency, and that they are higher than the passive Schottky current doubler for the entire 6.4-14.4W measured range, including the 10W rated power for heart pump operation where the improvement is about 1.3%.

Figure 6–12 also shows the end-to-end efficiency increases with the load power, P_L. This also increases the load current, ON state losses across commutating MOSFETs and ESR losses in dc inductors, resonant inductors and capacitors. However, the increase in load power (P_L) is higher than the increase in total power losses (P_{Loss}), so a higher overall end-to-end efficiency is achieved at higher power output according to the basic definition of end-to-end power efficiency of the system given by (6.4).

$$\eta = \frac{P_L}{P_L + P_{Loss}} \times 100 \tag{6.4}$$

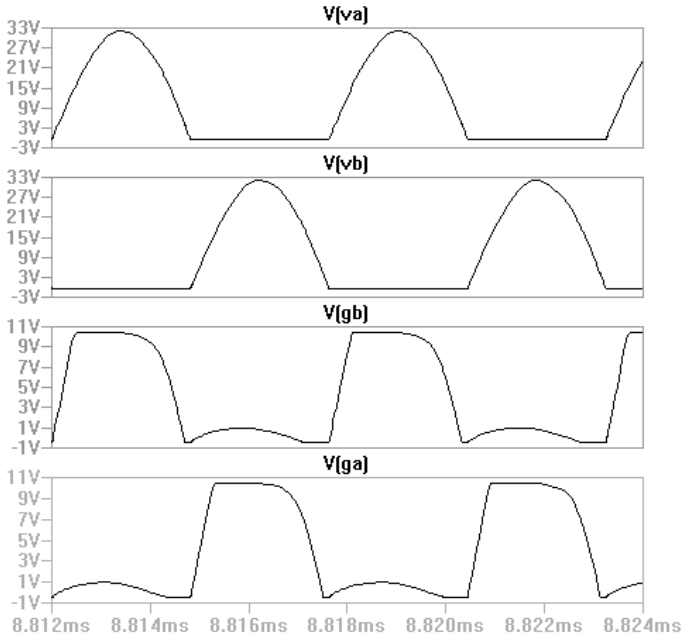


Figure 6–7 Simulation waveform for passive autonomous synchronous rectifier

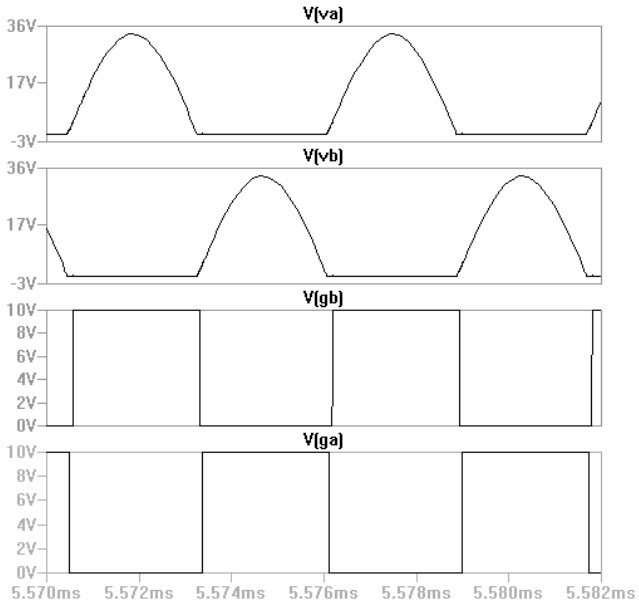


Figure 6–8 Simulation waveform for autonomous rectifier with buffer circuit

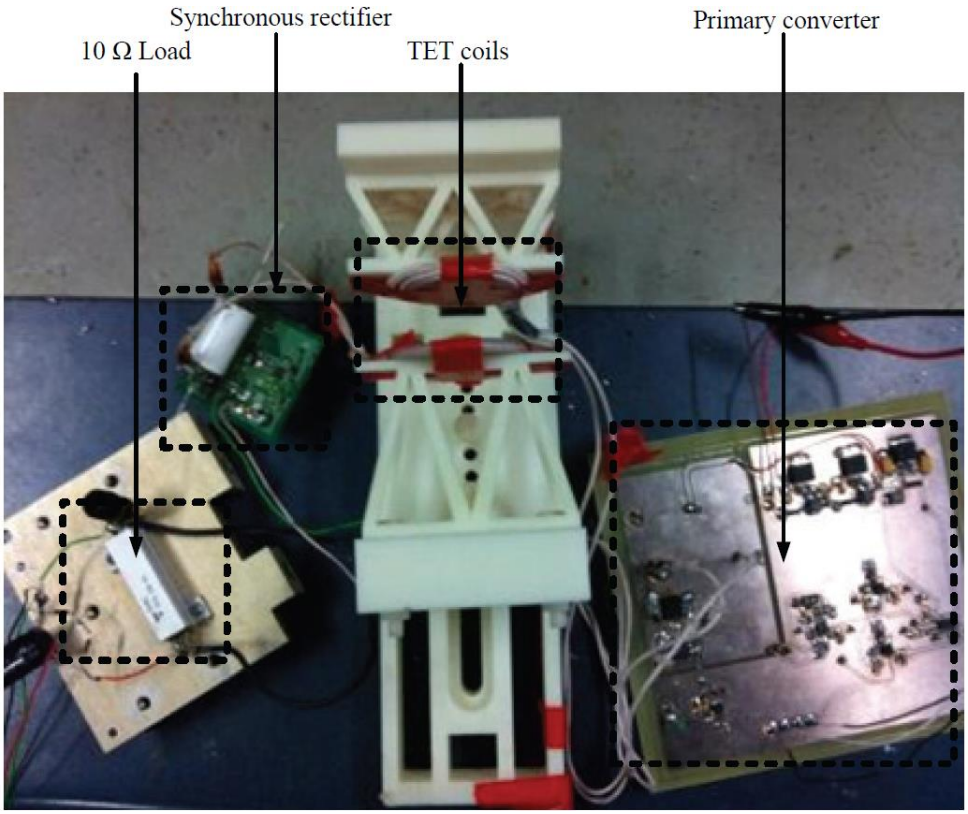


Figure 6–9 Experimental setup for synchronous rectifier

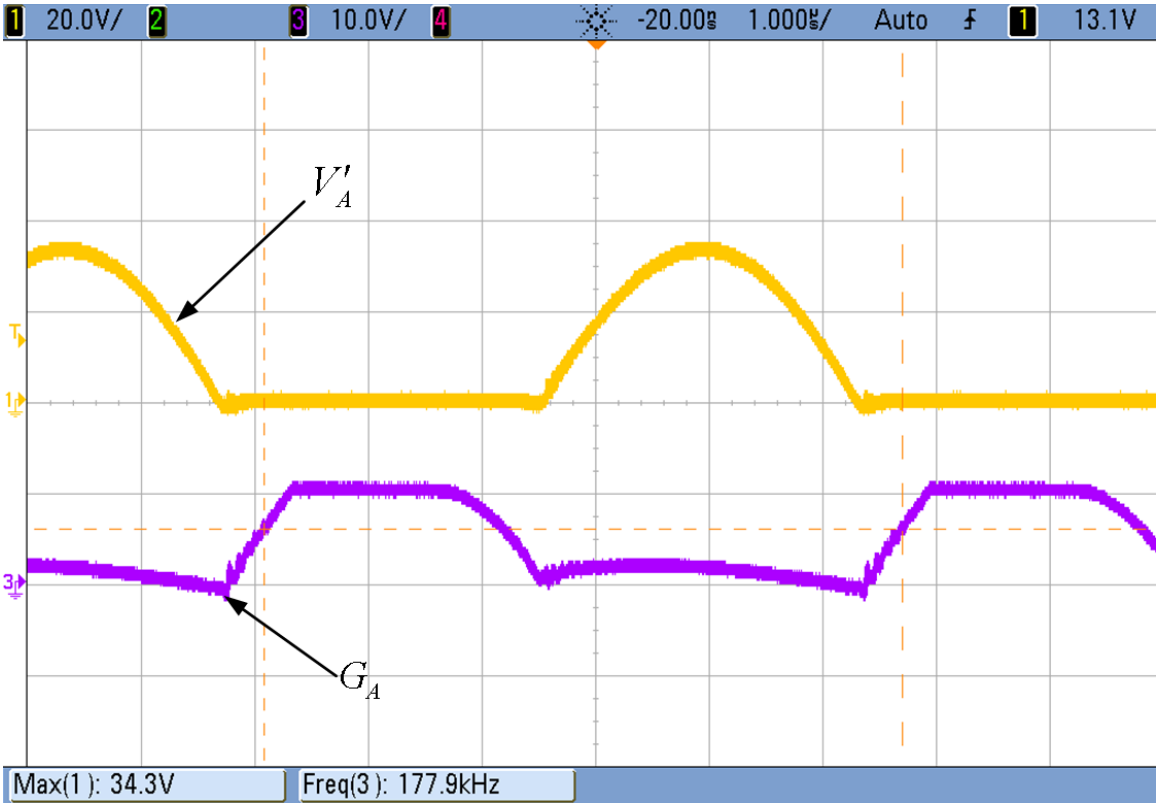


Figure 6–10 Oscilloscope waveforms for passive autonomous synchronous rectifier

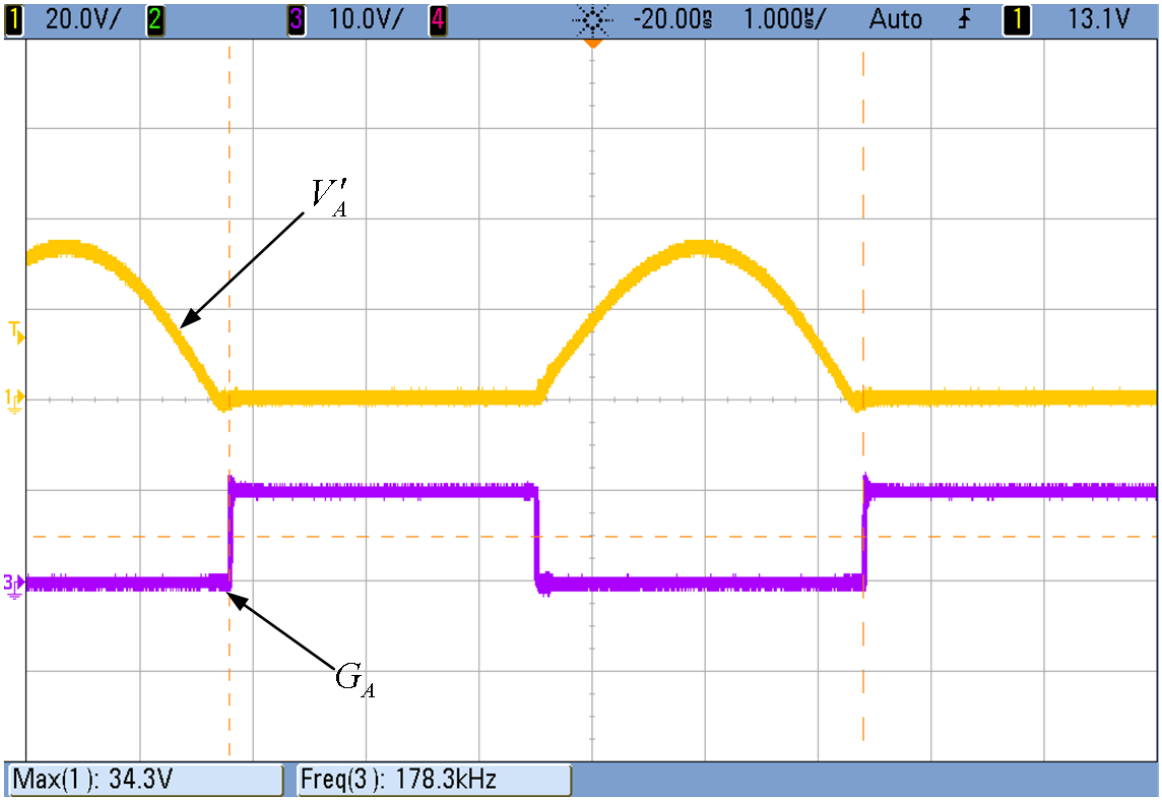


Figure 6–11 Oscilloscope waveforms for autonomous rectifier with buffer circuit

6.2.4. Discussion

The passive autonomous synchronous rectifier has the benefit of a simple circuit without any auxiliary power supply; it also achieves similar end-to-end efficiencies when compared with the autonomous rectifier with buffer circuit. However the passive autonomous synchronous rectifier may have frequency jittering and instability problems during startup and low resonant voltage operation. With fast startup processes and operation at a sufficiently high resonant voltage level, the system can reach a stable steady state correctly.

The autonomous rectifier with a buffer circuit exhibits a short delay time between commutations; this delay time is caused by a minimum input voltage to toggle the gate driver ON. During the delay time, both MOSFETs are off, and parallel Schottky diodes would conduct to keep continuous current flow.

The experiment was conducted with an air gap. Given that the permittivity of dry skin is not the same as that of air at the operating frequency [111], the corresponding efficiency result may be different. Therefore, further research with skin tissues will be needed for achieving practical transcutaneous energy transfer.

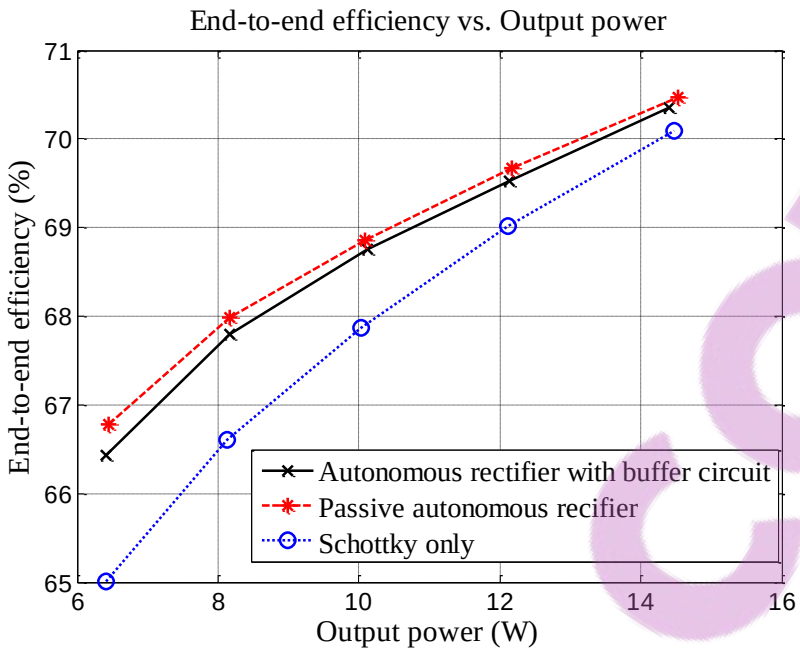


Figure 6–12 End-to-end efficiency vs. output power for 5mm coil separation

6.3. Synchronous Rectifier with Combined Power Flow Control

The basic primary power flow controller as discussed in Chapter 3, regulates load power by operating below an upper frequency boundary, which is set by the intersection of the lower ZVS branch and the closest coupling level. In comparison, the improved primary controller in Chapter 4 removes the upper frequency boundary to track the lower ZVS branch giving more power flow potential and significantly extending the regulated coil separation range.

However, the primary power flow controllers usually require a radio frequency (RF) link to communicate the secondary load voltage back to the primary for regulation purposes. This chapter proposes a secondary power flow controller which regulates the pickup output voltage directly, so there would be no need for a communication link between the primary and secondary. Here, the secondary operates as a synchronous rectifier combined with power flow control.

6.3.1. System Overview

The proposed secondary power flow controller is shown in Figure 6–13, V'_{AB} is the differential of MOSFET drain to source voltages V'_A and V'_B respectively. V'_{AB} is then compared with ground to give V_A. Similarly, V'_{BA} is found by differencing V'_B and V'_A respectively. Then, V_B is attained by comparing V'_{BA} to ground. V_{LOAD} is stepped down

to V'_{LOAD} and converted to 16 bits by the ADC. The step down ratio is selected to constrain V'_{LOAD} to be within ADC's input voltage limits.

A Field-Programmable Gate Array (FPGA) controller is designed, with three inputs and two outputs. The three inputs are V_A, V_B and V'_{LOAD} in 16 bits. The two outputs are square waveforms for driving the MOSFETs. An interface is designed in FPGA to extract the 16 bits representing V'_{LOAD} from the ADC. The control module will track V'_{LOAD} toward V_{ref} and produce a delay value. The delay module adjusts the amount of resonant shorting period according to the delay value. The system would reach rated power level when $V'_{LOAD}=V_{ref}$.

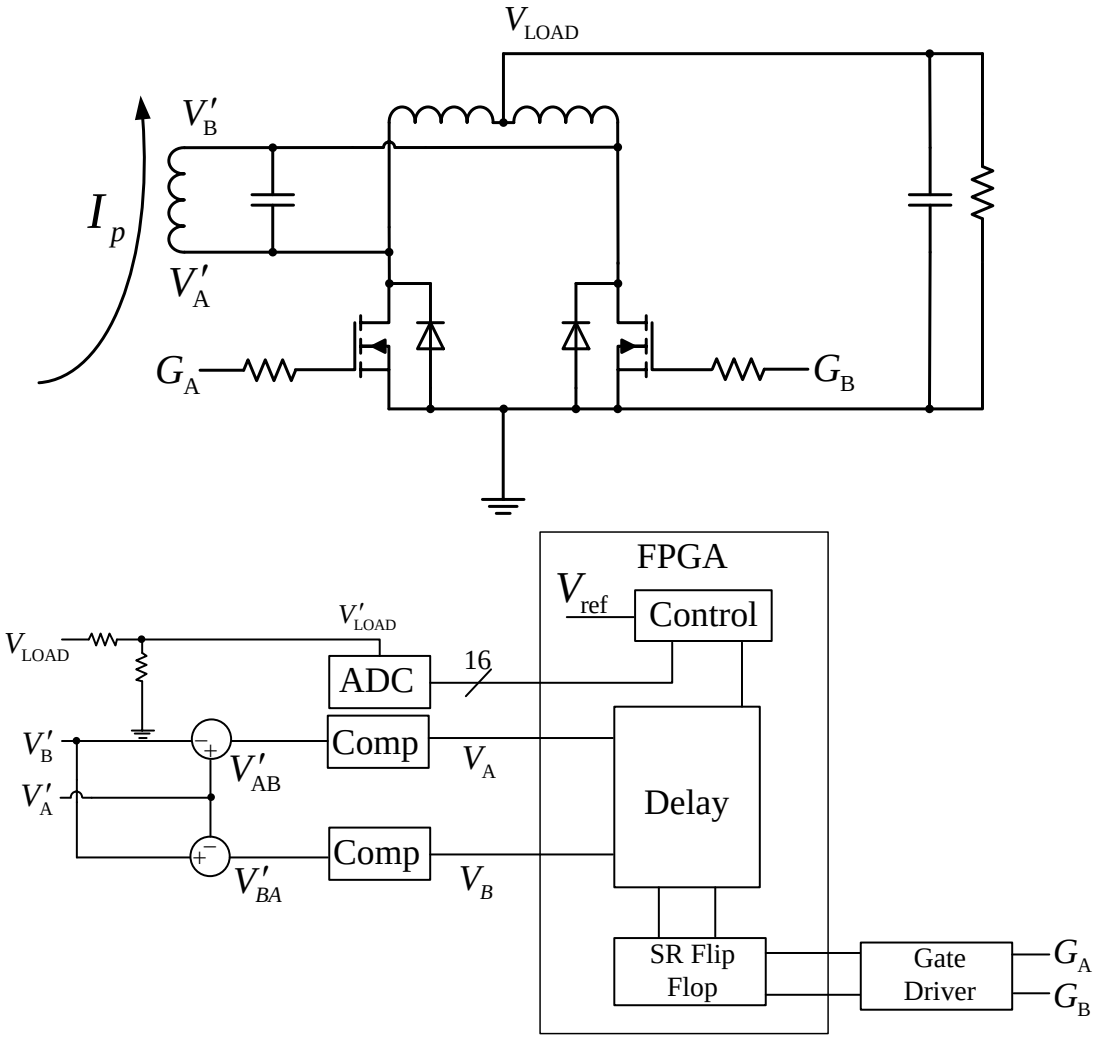


Figure 6–13 System overview of the proposed secondary power flow controller

In open loop operation, the output load voltage (V_{LOAD}) is positively proportional to the delay value and the resonant shorting period. The secondary does not have control over operational frequency; therefore for a given frequency, an increase in resonant shorting

period will reduce the zero crossing period (T_{zc}). From (3.3), this results in higher voltage and power levels.

6.3.2. Circuit Operation Theory

Figure 6–14 shows the theoretical circuit waveform for the proposed secondary power flow controller, and V_A and V_B are comparator results as described earlier, V_{A_SET} and V_{B_SET} are negative edge trigger signals from V_A and V_B respectively. V_{A_SET} and V_{B_SET} instruct the delay module to begin a delay counter, and after the delay time has elapsed, two new negative edge trigger signals are produced, $V_{A\_D\_SET}$ and $V_{B\_D\_SET}$. The four edge trigger signals are inputs to two SR flip flops. V_{A_SET} and $V_{B\_D\_SET}$ sets and resets the first SR flip flop respectively, while V_{B_SET} and $V_{A\_D\_SET}$ sets and resets the second SR flip flop respectively. The outputs of the first and second SR flip flops are the resulting gate drive signals G_A and G_B respectively.

6.3.3. Controller Design

The secondary must passively follow the primary by synchronising to the primary frequency and oscillation for correct operation. As the coupling level decreases, the control module will increase the delay value and resonant shorting period, which would counterbalance the weaker coupling level and converge load power back to the rated level. Since the MOSFET drain to source (V_{ds}) voltage rises with introduced delay, the maximum delay is limited to the maximum V_{ds} ratings of the secondary MOSFETs.

The controller use discrete components for differential amplifiers, comparators, ADC and the gate driver. The differential amplifiers have a gain less than one to step down the resonant tank voltage to be processed by the comparators. The comparator is designed to have a positive upper trigger point and a zero lower trigger point, which prevents mis-triggering by the noise from the resonant tank waveform. The gate driver attains the supply voltage directly from the output load voltage, while the positive and negative 5V power supplies are derived for the remaining components.

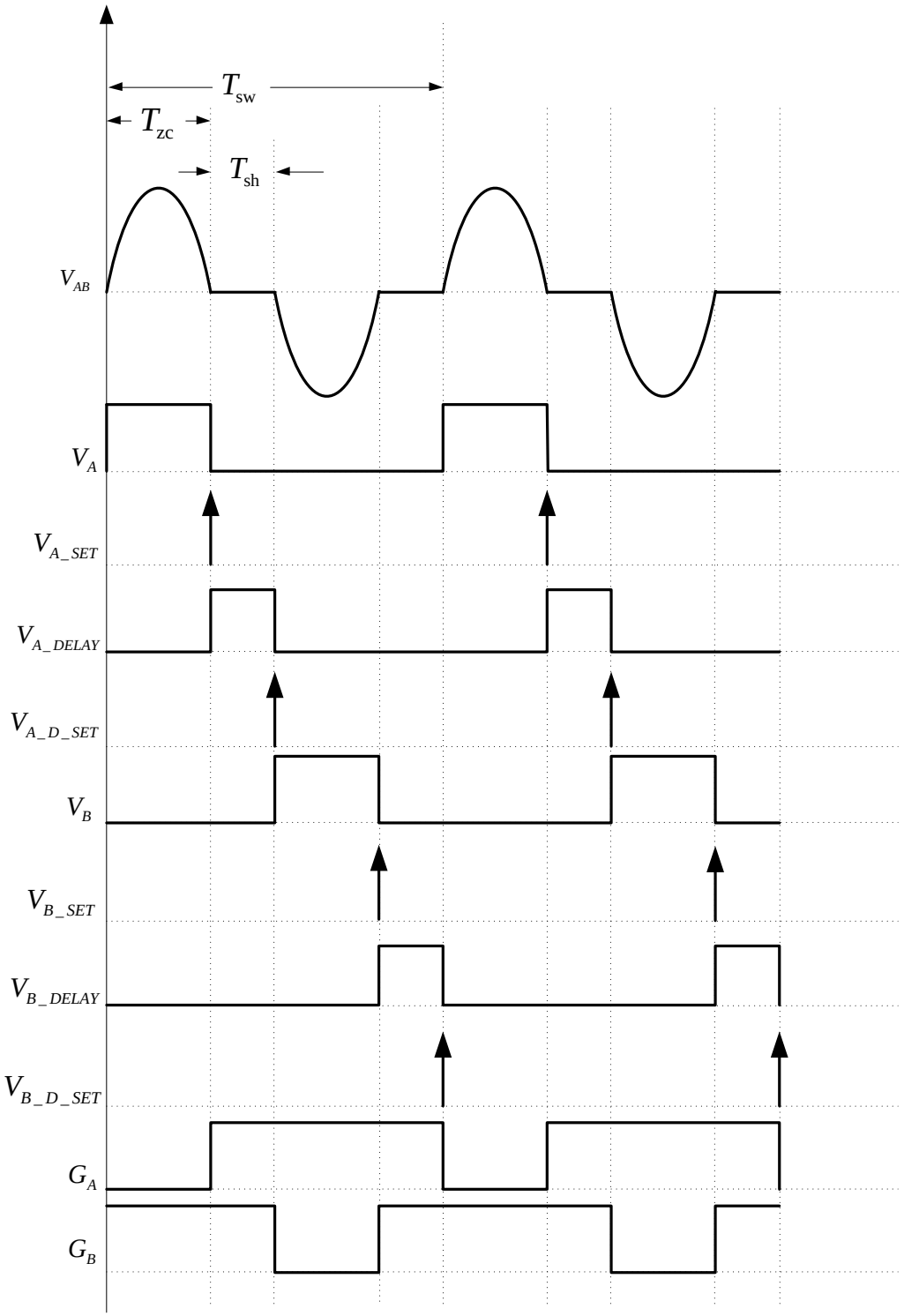


Figure 6–14 Theoretical circuit waveforms for secondary power flow controller

The control, delay and SR flip flop modules were written in Very-High-Speed Integrated Circuits Hardware Description Language (VHDL) and realised on the Altera DE2 board. Since the output power is sensitive to steps in delay value, the control module is coded to smooth the transition between adjacent delay values. This is similar to varying the duty cycle of a square wave over time, with the ON and OFF duration representing two

adjacent delay values. The duty cycle increases when the direction is upwards; the delay is set to the current delay when ON and the previous delay when OFF. The duty cycle decreases when the direction is downwards, and the delay is set to the previous delay when ON and the current delay when OFF. There will be a swap between previous delay and current delay values upon a direction change.

6.3.4. Simulation and Practical Results

Circuit simulation can be done using PLECS and ModelSim. These two methods are used to simulate the proposed control strategy: firstly through PLECS simulation the system uses a PI controller to attain the required delay by varying the resistance of the delay circuit. Two SR flip flops are set and reset to generate the required gate drive signals. Secondly the FPGA controller is simulated using ModelSim to ensure that the VHDL codes are operating correctly. Details of this PLECS simulation, ModelSim simulation and VHDL programming can be found in Appendices I, J and K respectively.

Figure 6–15 shows the PLECS simulation waveforms for the secondary power flow controller. Note that it corresponds well with the theoretical waveforms in Figure 6–14. Figure 6–16 shows the experimental setup. It shows a primary converter controlled by PSoC 5; a set of TET coils with adjustable separation distance, a secondary pickup with power flow control by the DE2 FPGA board and lastly the resistive load representing an implantable heart pump. The practical waveforms during operation of the secondary power flow controller are presented from Figure 6–17 to Figure 6–20 for the regulated coil separation range of 0 to 9mm.

The primary power flow controller presented in Chapter 4 can be operated together with this secondary power flow controller to extend the regulated coil separation range up to 27mm. The practical waveforms during combined operation of the primary and secondary power flow controllers are presented from Figure 6–21 to Figure 6–28.

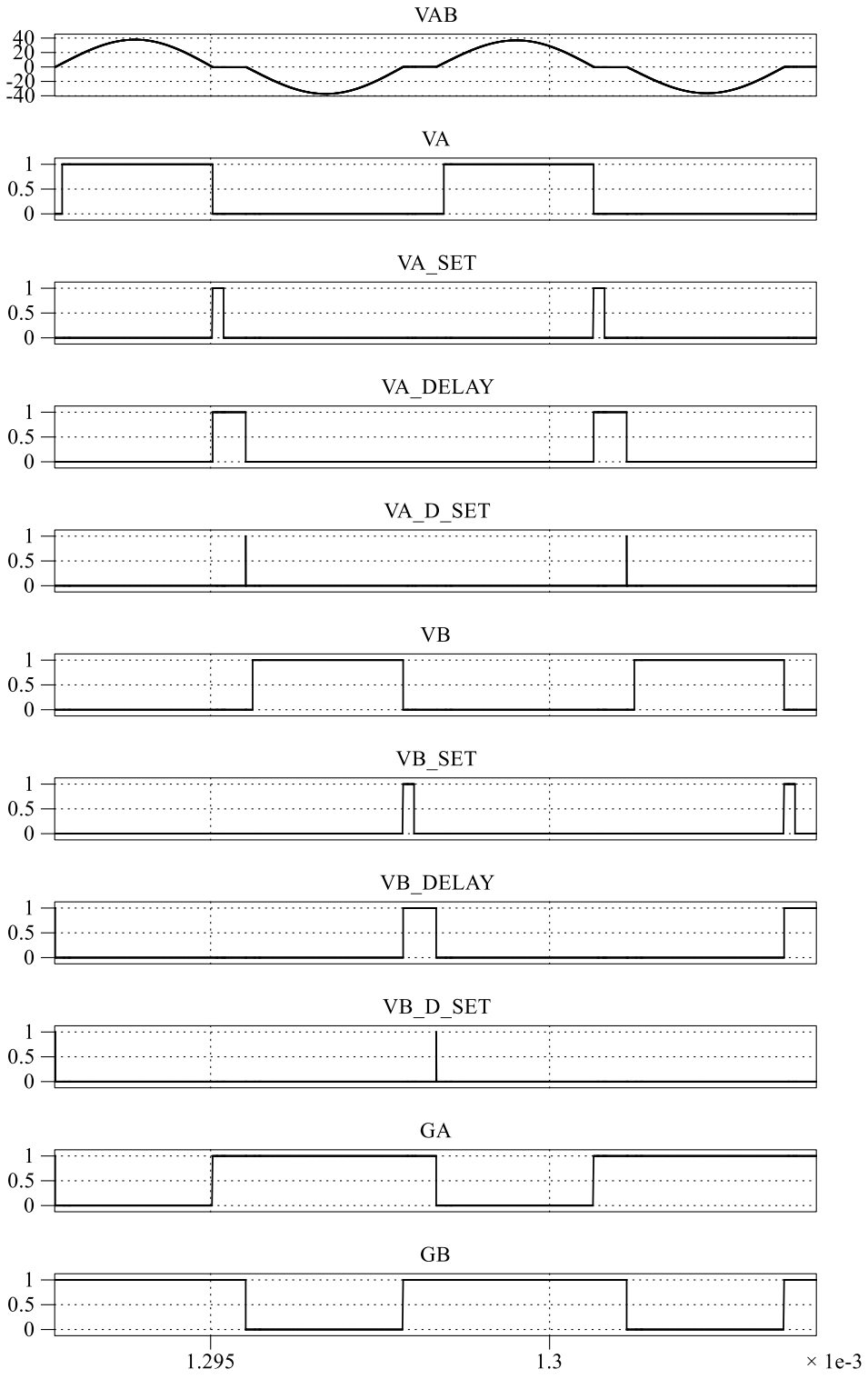


Figure 6–15 Simulation result for improved power flow controller

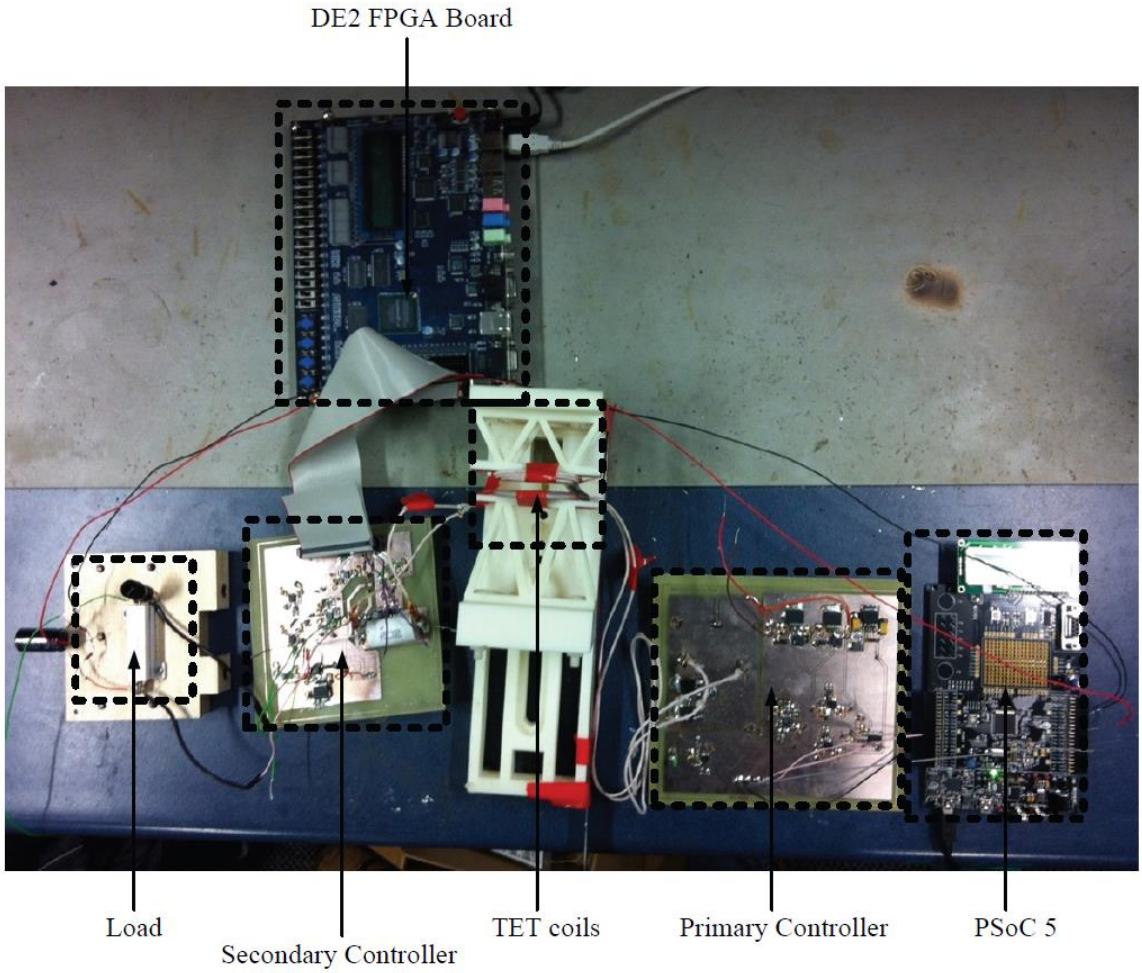


Figure 6–16 Experimental setup

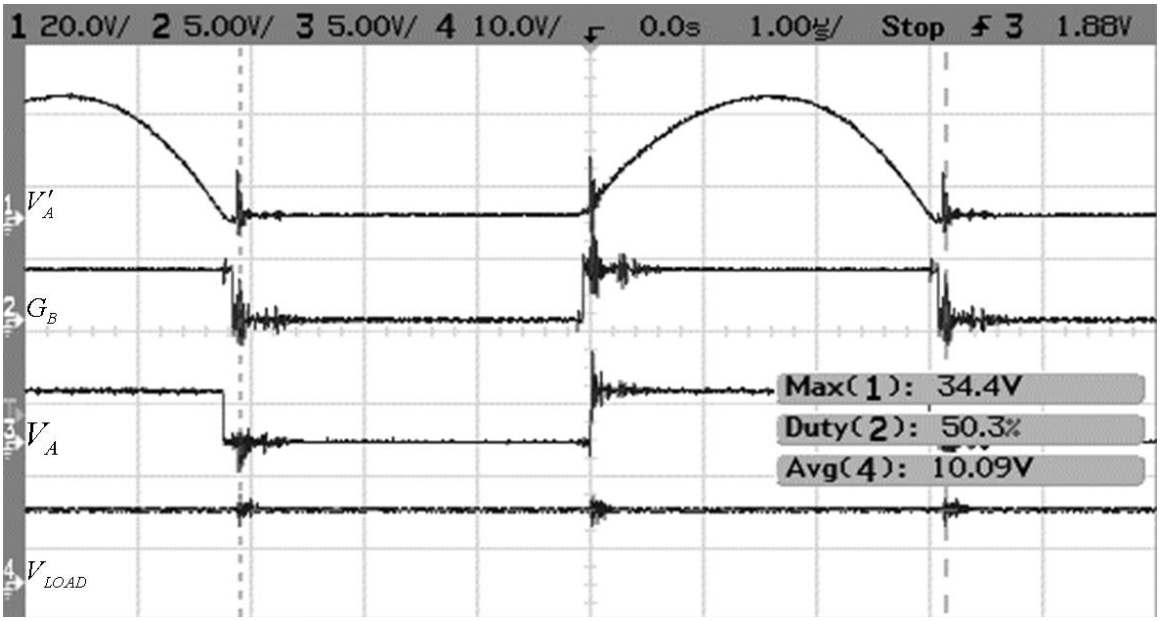


Figure 6–17 Experimental waveforms for 0mm coil separation (secondary controller)

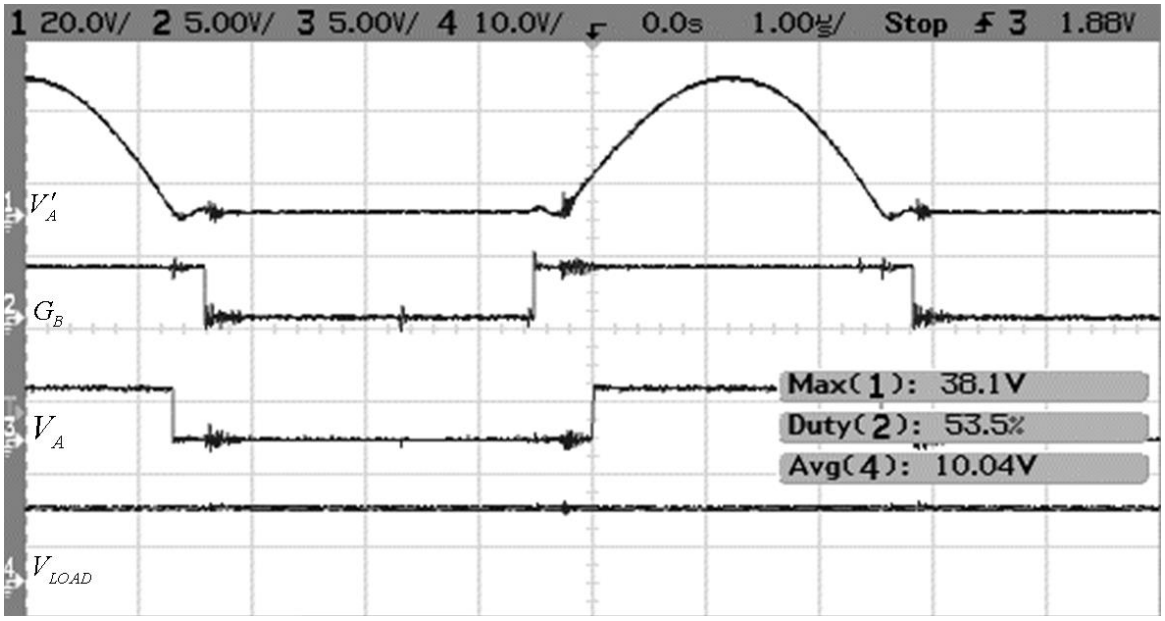


Figure 6–18 Experimental waveforms for 2mm coil separation (secondary controller)

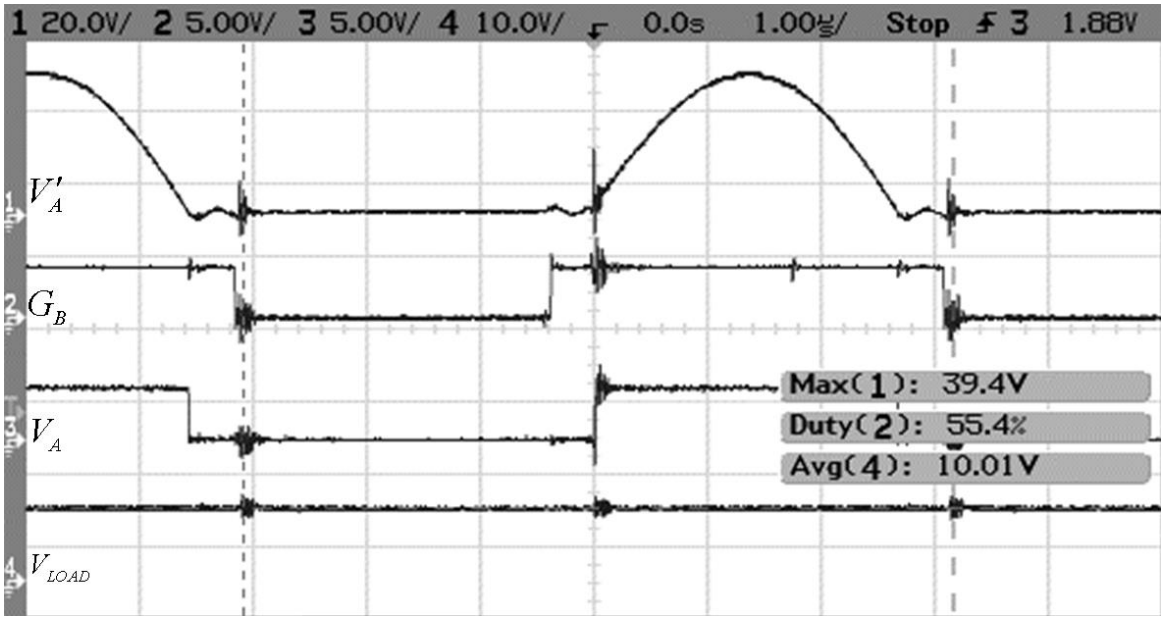


Figure 6–19 Experimental waveforms for 4mm coil separation (secondary controller)

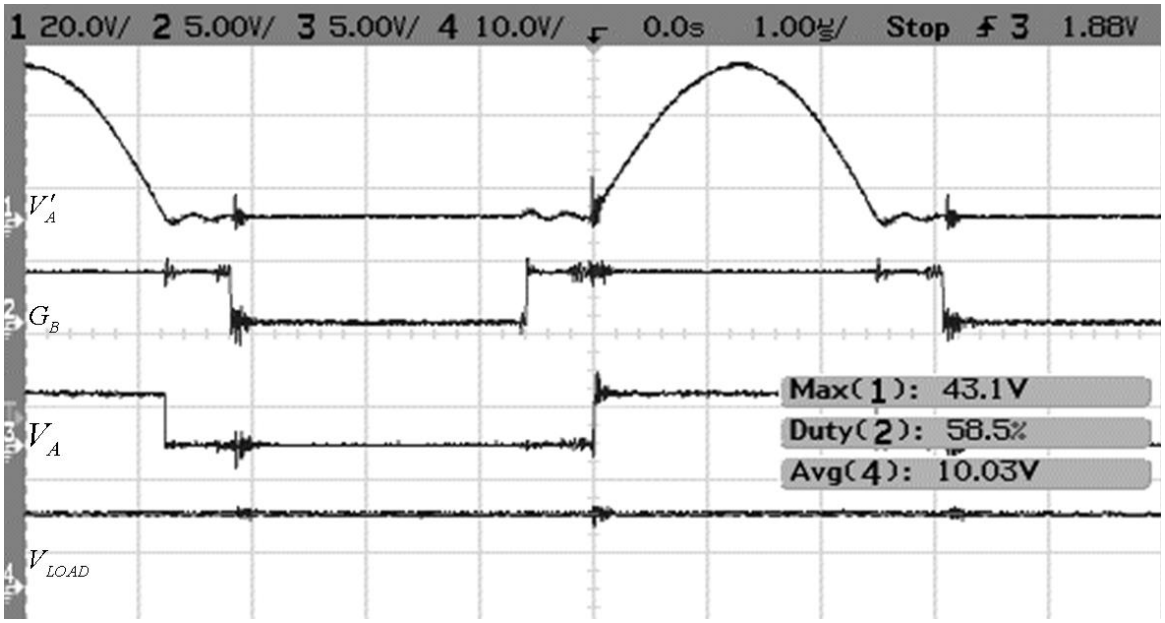


Figure 6–20 Experimental waveforms for 9mm coil separation (secondary controller)

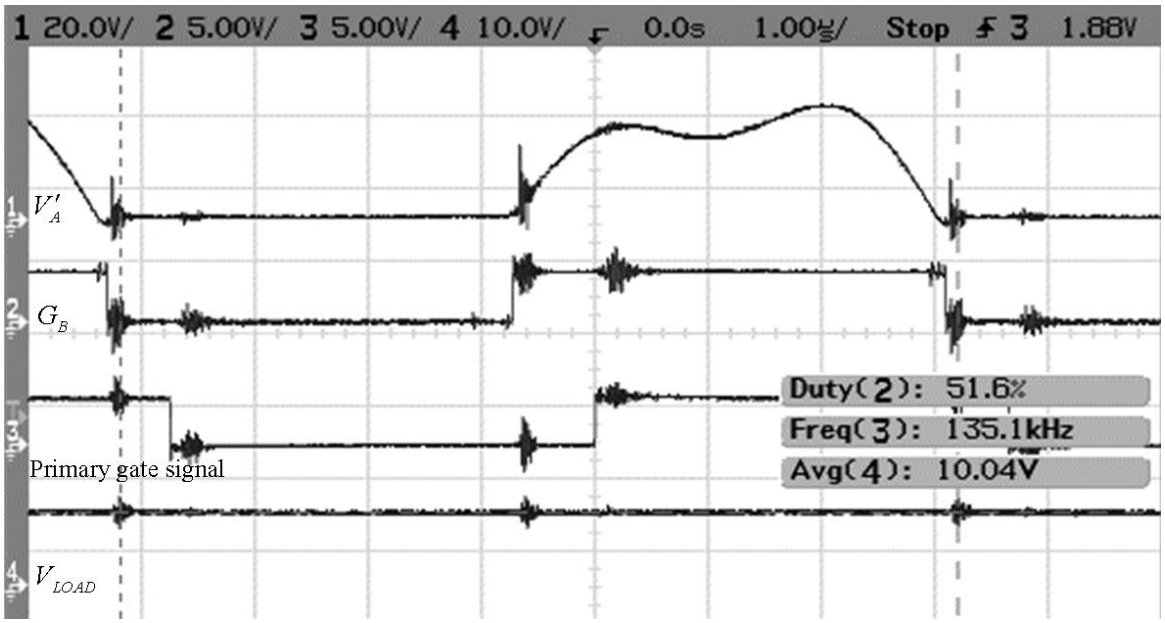


Figure 6–21 Experimental waveforms for 0mm coil separation (primary and secondary controllers)

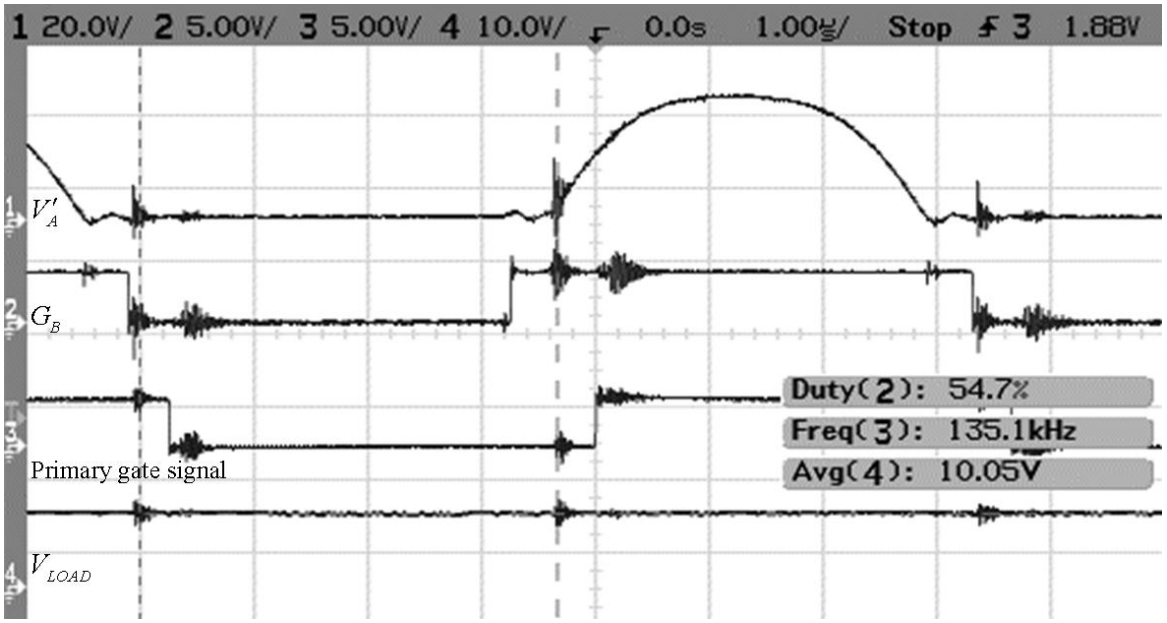


Figure 6–22 Experimental waveforms for 1mm coil separation (primary and secondary controllers)

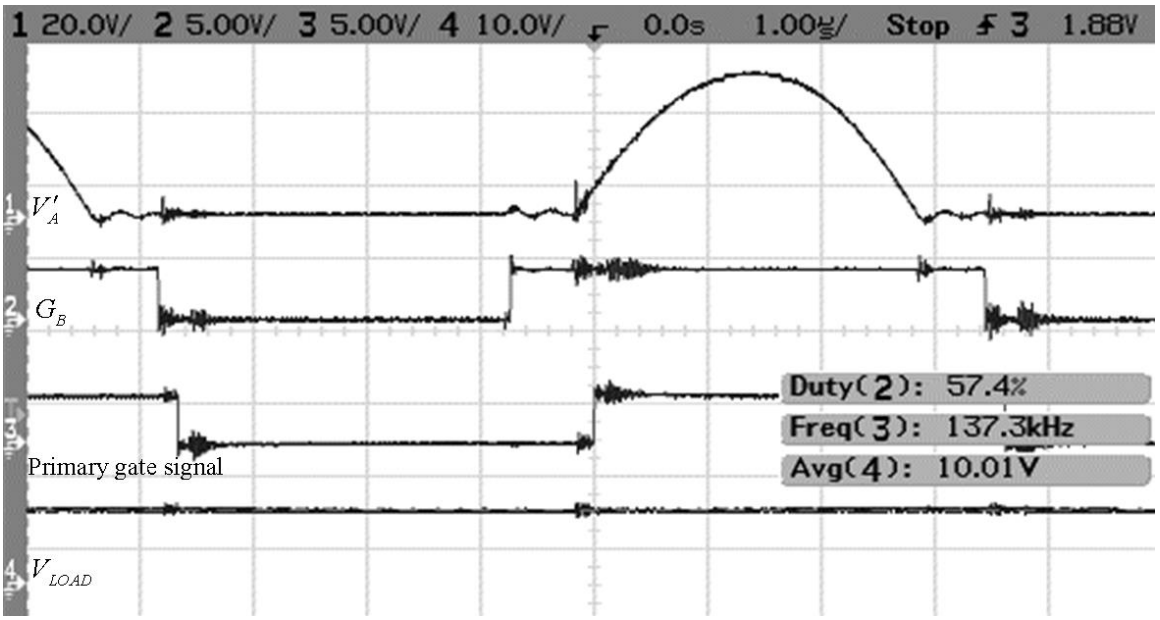


Figure 6–23 Experimental waveforms for 2mm coil separation (primary and secondary controllers)

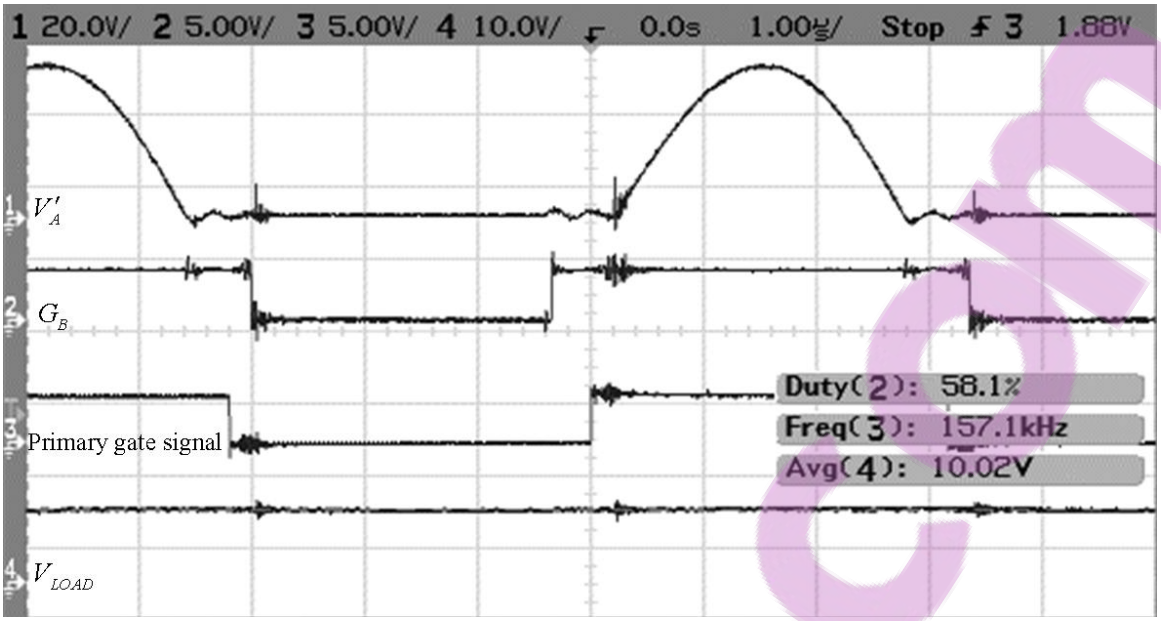


Figure 6–24 Experimental waveforms for 9mm coil separation (primary and secondary controllers)

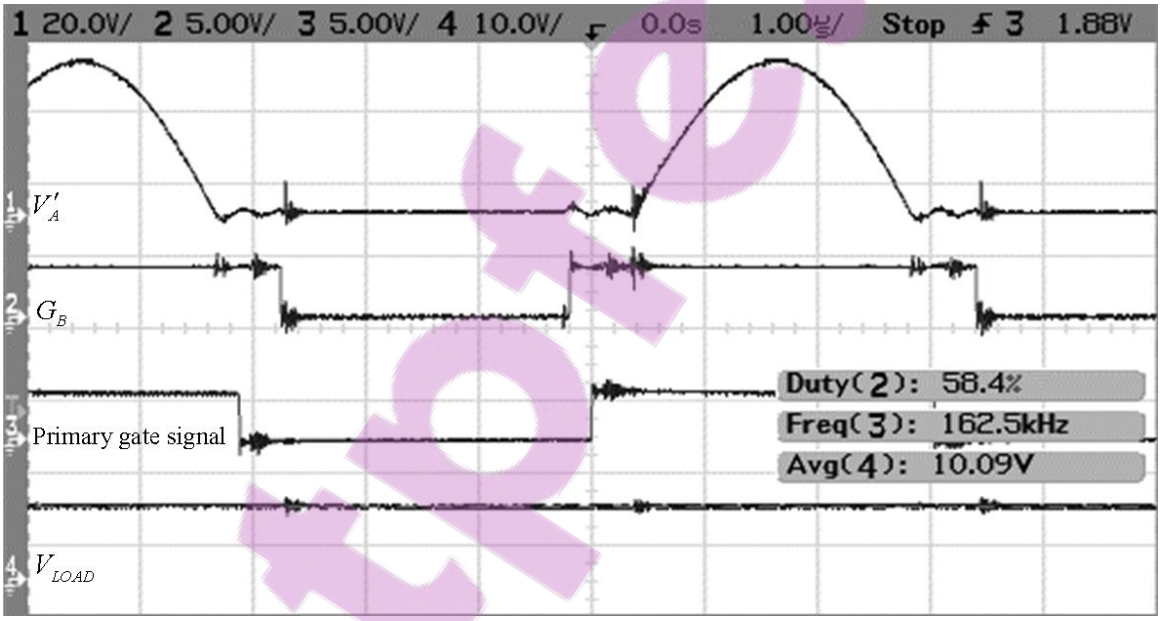


Figure 6–25 Experimental waveforms for 14mm coil separation (primary and secondary controllers)

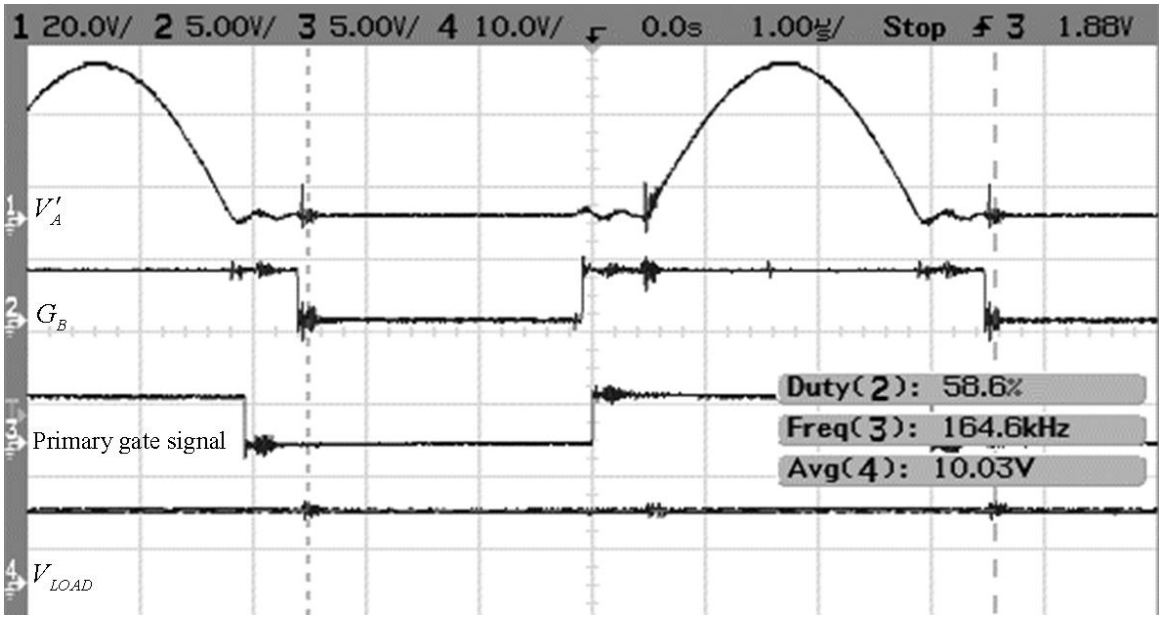


Figure 6–26 Experimental waveforms for 19mm coil separation (primary and secondary controllers)

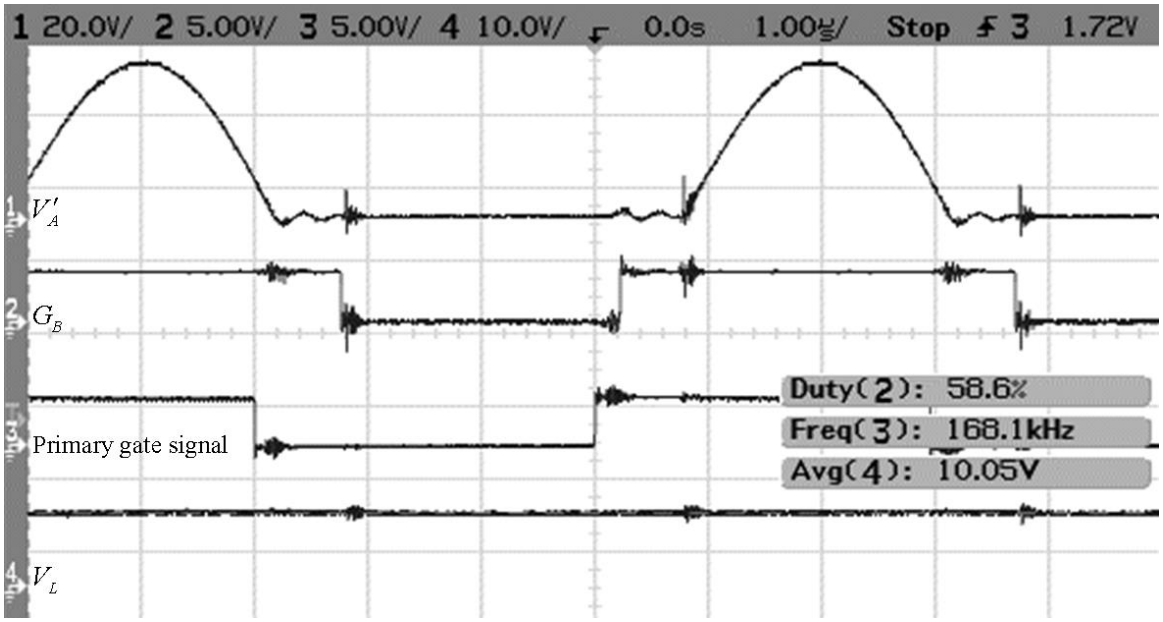


Figure 6–27 Experimental waveforms for 24mm coil separation (primary and secondary controllers)

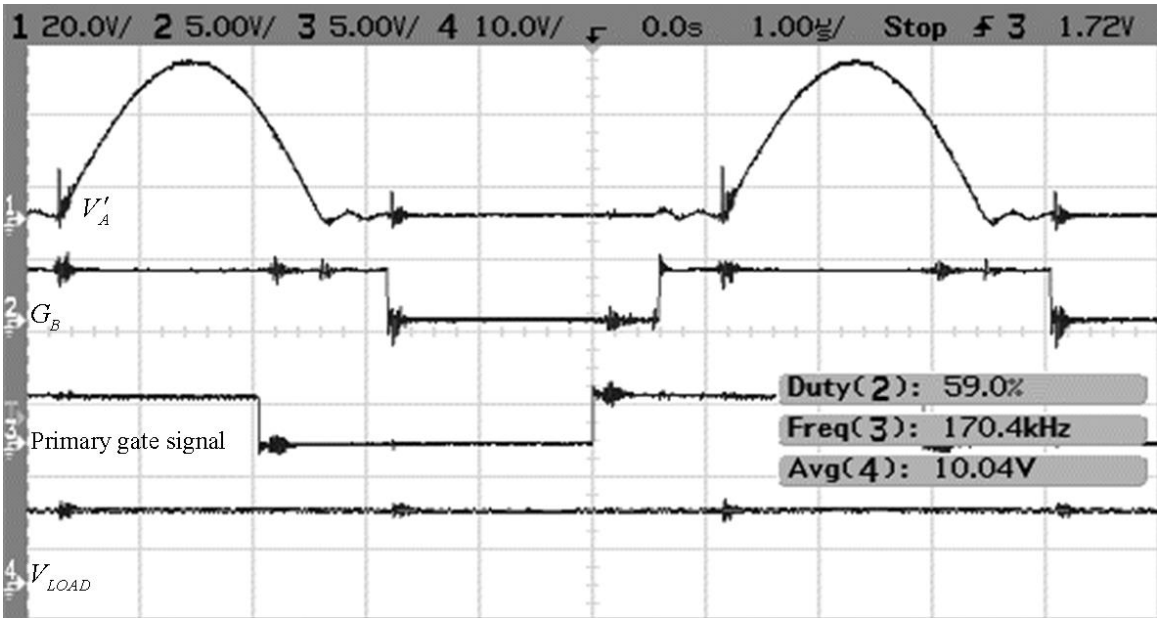


Figure 6–28 Experimental waveforms for 27mm coil separation (primary and secondary controllers)

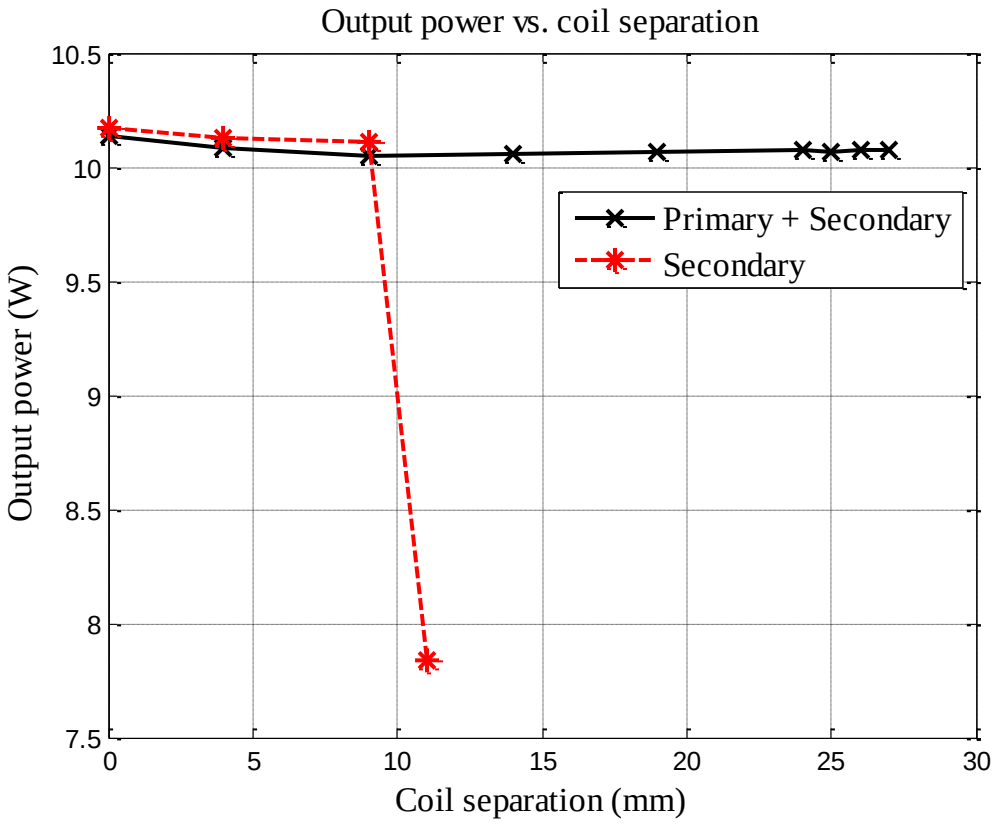


Figure 6–29 Output power vs. direct distance coil separation distance

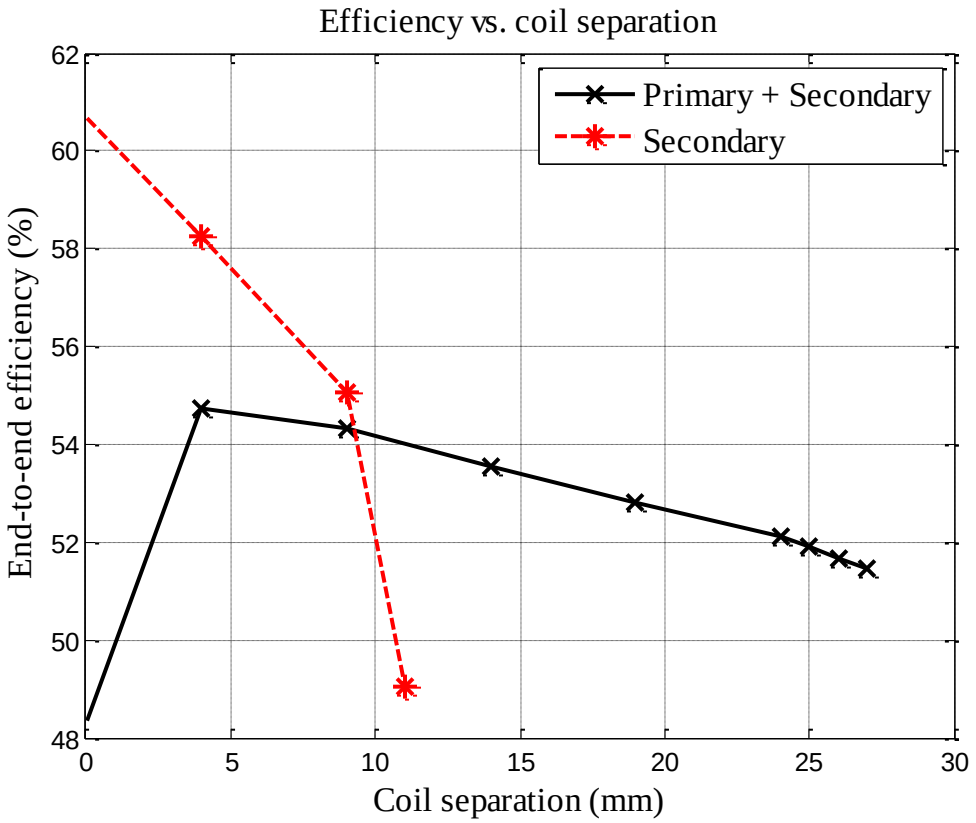


Figure 6–30 End-to-end efficiency vs. direct coil separation distance

With the primary operating frequency fixed, Figure 6–29 and Figure 6–30 show that the secondary regulates 10W load power for up to 9mm coil separation at 55.1% end-to-end efficiency, secondary only operation is shown by the red line. In collaboration, the primary and secondary can achieve a maximum of 27mm regulation range at 51.4% end-to-end efficiency. Collaborative operation is shown by the black line in Figure 6–29 and Figure 6–30. This means the proposed secondary controller and primary power flow controller of Chapter 4 is active simultaneously, with the primary controller operating, the system would now require communication between the primary and secondary. Overall, the collaborative efficiency has dropped compared to the primary controller of Chapter 4, this can be due to the introduced losses from the control actions of the secondary side.

Figure 6–30 shows that the secondary controller end-to-end efficiency drops with separation as resonant shorting period increases. The power losses are from increased circulating resonant current through MOSFETs and body diodes. The end-to-end efficiency for collaborative control rises, and then drops steadily. The initial rising trend in efficiency occurs when the detuned system tunes itself with increasing separation, and then efficiency slowly drops with reducing magnetic coupling. Note that more

experimental points could have been taken between 0-4mm in collaborative control to further clarify the rising trend, which should be a simple linear line with positive gradient. The rising trend is similar to the experimental results obtained from primary side power flow controllers discussed in Chapters 3 and 4. The regulation range is extended by 3mm when compared to the primary controller operating with a passive current doubler rectifier as discussed in Chapter 4.

6.4. Conclusions

This chapter has proposed and implemented an autonomous push-pull rectifier with passive or buffer circuit gate drives. The experimental results have demonstrated that the proposed synchronous rectifier can reduce the power losses of the implanted power pickup circuit and improve the overall end-to-end efficiency of the TET system for driving a 10W heart pump by 1.3% when compared with the counterpart passive rectifier using Schottky diodes.

The proposed push-pull current doubler synchronous rectifier with combined power flow achieves load regulation by variable resonant shorting period and variable resonant voltage magnitude. The circuit is designed with a combination of discrete components and FPGA control under VHDL coding. The controller regulates the load power directly from the secondary, and is able to extend the regulated coil separation range to 27mm together with the primary power flow control.

Chapter 7

Conclusions and Suggestion for Further Work

7.1. General Conclusions

Heart disease is a costly medical problem. The lack of heart donors necessitates the development of heart pumps such as left ventricular assist devices (LVAD). These heart assist devices are increasingly used as a bridge to recovery, a bridge to transplantation, and as a destination therapy. Existing heart pumps are powered through a percutaneous driveline, which can cause infection and for this reason should be eliminated. Transcutaneous energy transfer (TET) eliminates the percutaneous driveline and its associated infection risks. But existing TETs have very limited range of operation. This thesis has researched on various control methods to provide a large operation range with good magnetic coupling tolerance, input voltage, and output power regulation range.

A TET system relies on resonances to transfer power, but under a bifurcated condition the operating frequency of the system may jump suddenly, causing sharp variations in system output power, and this situation must be avoided. In Chapter 2, this bifurcation phenomenon of a current-fed push-pull converter is analysed first by zero voltage switching (ZVS) detection and then using forced frequency operation. The system ZVS points can be found accurately using the stroboscopic mapping method and are found to contain a single ZVS branch before bifurcation and three after bifurcation. Due to complicated dynamic waveform changes, the unstable middle ZVS branch may have an extra zero crossing within a half period. With simple ZVS detection, this extra zero crossing would cause the system to jump to a higher ZVS operating point. It was found by employing ac impedances analysis that a parallel-parallel tuned TET system has a single power peak capability point at all coupling and load conditions, and this characteristic is used in subsequent power flow controller design.

TET systems require power regulation to stabilise the output load voltage, and a novel variable frequency primary power flow controller with upper boundary is proposed in Chapter 3 to remove the additional switching components in the existing frequency controller. A PI controller was designed to vary the switching frequency, to regulate the output voltage to its reference. The relationship between the power flow and frequency is positively monotonic. Under the close loop PI control, the load power regulation is achieved by variable frequency operation against coil magnetic coupling variation. The system is controlled to operate below a fixed upper frequency boundary chosen based on the closest expected coupling level and highest load resistance. The system demonstrated 10W power regulation for up to a maximum coil separation of 10mm, and a maximum efficiency of 79.65%.

To improve the maximum magnetic coil coupling tolerance, a novel primary power flow controller with an automatic ZVS range and shorting period detection is proposed in Chapter 4. The controller keeps the system close to the lower ZVS branch by detecting the resonant shorting period. The frequency decreases when the load voltage exceeds its reference, or increases when the voltage is too low. The resonant shorting period of the converter is increased or decreased automatically during the regulation. The system has shown a 10W power regulation for a coil separation range of 0 to 24mm, while the end-to-end efficiency is 52% at 0mm separation, and becomes static at around 66% from 4mm to 24mm.

The frequency jump under system bifurcation can cause sharp drops in the power transfer capability. Two ZVS followers are proposed in Chapter 5 to maintain the middle ZVS branch operation after bifurcation. The controllers can deliver 10W rated power at a lower input voltage, a greater coil separation, and an improved end-to-end efficiency. A prototype wireless power transfer system was developed, and it has achieved an end-to-end efficiency of 72.2% while delivering 10W at a coil separation of 10mm.

To reduce the power losses in the pickup circuit which may cause tissue heating, two drive options for a current doubler synchronous rectifier are proposed in Chapter 6. One drive option is an autonomous technique while the other employs an active gate driver. The new synchronous rectifiers driven by the two gate drive options have higher end-to-end efficiencies than the passive Schottky rectifier, while comparable efficiencies are achieved between the two drive options.

Chapter 6 also proposes a power flow control method based on the synchronous rectifier. Without any RF or any other communication channels, the pickup output voltage regulation is achieved by varying the shorting period of the current doubler rectifier. The secondary power flow controller achieves 10W power regulation for up to 9mm coil separation at 55.1% end-to-end efficiency. While in collaboration with the primary power flow controller, the coil separation regulation range is extended to 27mm at 51.4% end-to-end efficiency.

7.2. Contributions Made by this Thesis

The main contributions of this research work include the following.

Development of a primary power flow control system based solely on slow feedback to regulate heart pump load voltage level. This removes the additional parallel switches and capacitors used in the existing controller, thereby reducing the system component count. This work has been published as a journal paper in IEEE Transactions on Biomedical Circuits and Systems [105].

A demonstration system based on the proposed technology, using the primary power flow control, has been developed using a marine bilge pump, water pipes, plastic tubes, a fish tank and a plastic human figure. Wireless power is transferred across the plastic layer of the human figure to drive the bilge pump. Water is extracted and pumped to circulate around the human figure and then back to the fish tank.

Two ZVS followers have been proposed to maintain middle ZVS branch operation after bifurcation to keep high power transfer capability. This is proposed because if simple ZVS detection is used, frequency jumps under bifurcation can cause sharp changes in output power. The system is parallel-parallel tuned with a single power peak characteristic at all coupling conditions. This work has been submitted to IET Power Electronics and is under review.

A current doubler synchronous rectifier and its controller have been proposed and developed, increasing the system end-to-end efficiency by 3% when compared with a passive Schottky diode rectifier. This work has been published as a conference paper in the 5th IEEE Conference on Industrial Electronics and Applications (ICIEA), 2010 [110].

Two simpler controller options for the current doubler synchronous rectifier have been proposed, and these have each demonstrated around 1.3% improvement in end-to-end efficiency when compared to the passive diode rectifier when delivering 10W. This work has been accepted as a conference paper for the International Conference on Industrial Technology (IEEE ICIT 2013).

7.3. Suggestions for Future Work

For future work, thorough investigation is needed into the capability of the power regulation in more realistic magnetic coupling and loading conditions. It is recommended that trials of the proposed TET system and its controllers be conducted on real heart pumps, using sheep.

On the technological side, in the future the required controller circuits will be able to be miniaturised by combining the essential microcontroller chips and using high density and multiple layer PCB design.

In addition to the peak power tracking controller designed within this thesis, a peak efficiency tracking controller can also be designed, then a method of switching between the two need to be formulated.

The Class-E converter for TET power flow control could be investigated to improve system operation range and efficiency. The Class-E converter is known for its single switch operation at high frequency and efficiency. However, its control range is very limited. It is worthwhile to study its suitability to wireless power supplies for heart pumps.

Appendices

Appendix A: PLECS simulation of dynamic bifurcation phenomena

The push-pull circuit requires existing currents through the primary dc inductors to ensure the existence of ZVS points upon start-up process. A set of logic conditions ensure that the two low side switches are turned on for a brief period of time during start-up to ensure the initial current in the dc inductors. Logic switches are used to change the system coupling level during the simulation by switching between different sets of mutually coupled coils. Then, the bifurcation phenomena can be simulated as a result of changing coupling level. The simulation circuit is presented in Figure A-1.

The following MATLAB code sets the initial conditions and the system parameters before simulation run for the system.

```
clear all;
format long;

tsim=11e-3;
%% Variable circuit parameters
k1=0.05;
k2=0.5;
k3=0.1;
k4=0.4;

R=10*pi^2/2;

Vin=10;
Vth_relay=0;

T1=3e-3;
T2=6e-3;
T3=9e-3;
%% Circuit components
w0=2*pi*200e3;
L1=1e-3;
L2=1e-3;
Lp=11.3e-6;
Ls=3.31e-6;
Cp=1/(w0^2*Lp);
Cs=1/(w0^2*Ls);
RL1=0.46;
RL2=0.46;
RLp=73.1e-3;
RLs=26.7e-3;
RCp=0;
```

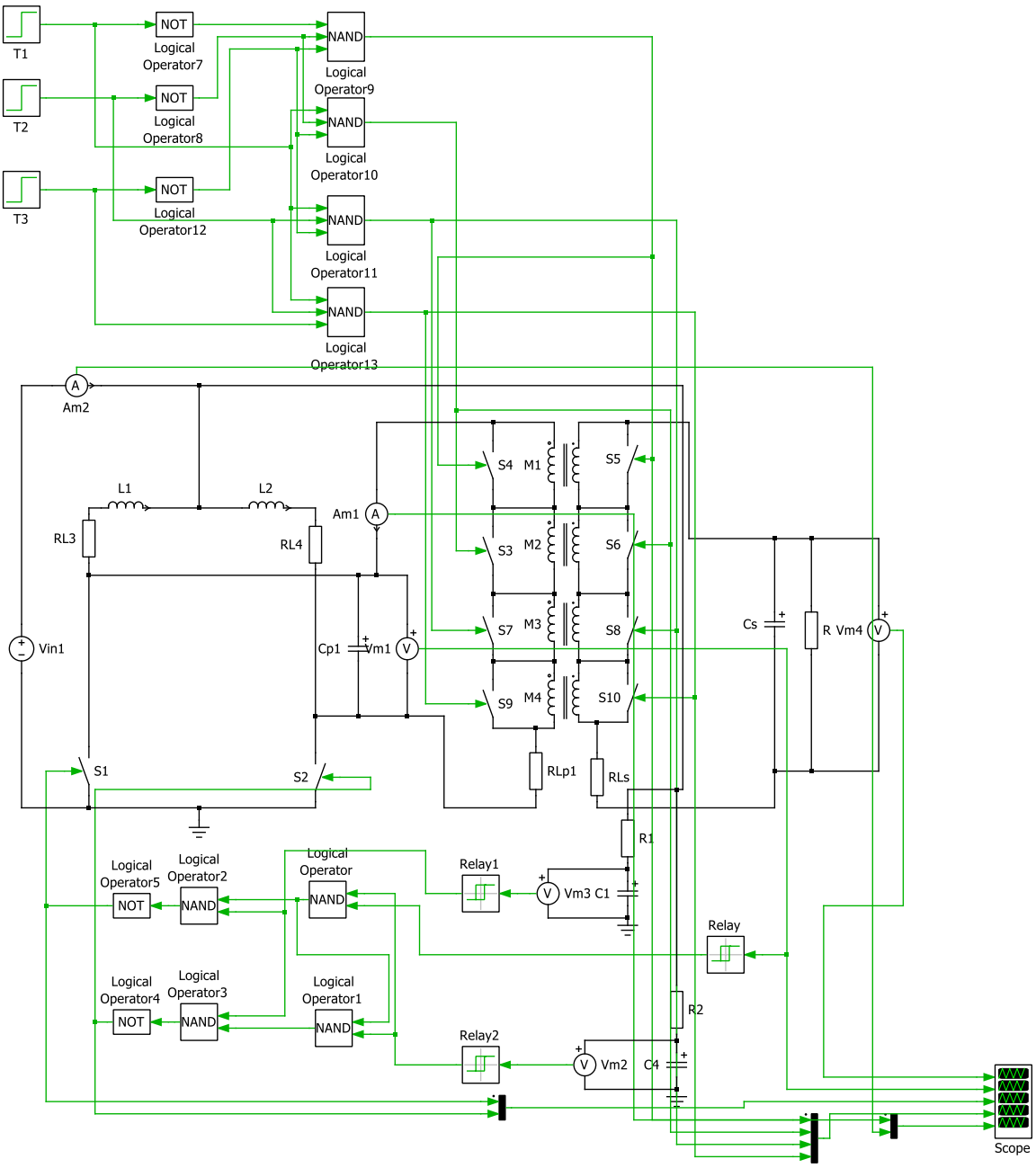


Figure A-1 PLECS schematic to simulate bifurcation phenomena using simple ZVS detection and variable magnetic coupling

```
RCs=0;
M1=k1*sqrt(Lp*Ls);
M2=k2*sqrt(Lp*Ls);
M3=k3*sqrt(Lp*Ls);
M4=k4*sqrt(Lp*Ls);
%% Switching devices
Vf_diode=0.01;
Ron_diode=0.01;
Ron_MOSFET=1e-6;
I0=0;
Vth=1e-6;

%% PLECS parameters
Ts=1e-8;
```

```
Tol_rel=1e-9;
Ref_fact=1;
Tol_abs=1e-9;
Tzc=1e-9;
```

The following PLECS circuit is used to capture snapshots of system transition between ZVS points. By driving the system under a fixed frequency, the system resonant tank waveform is captured to reveal its dynamic bifurcation response.

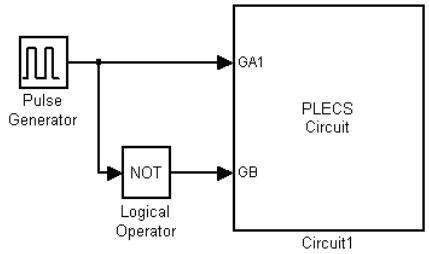


Figure A-2 PLECS circuit to drive the system with complementary 50% duty cycle pulses

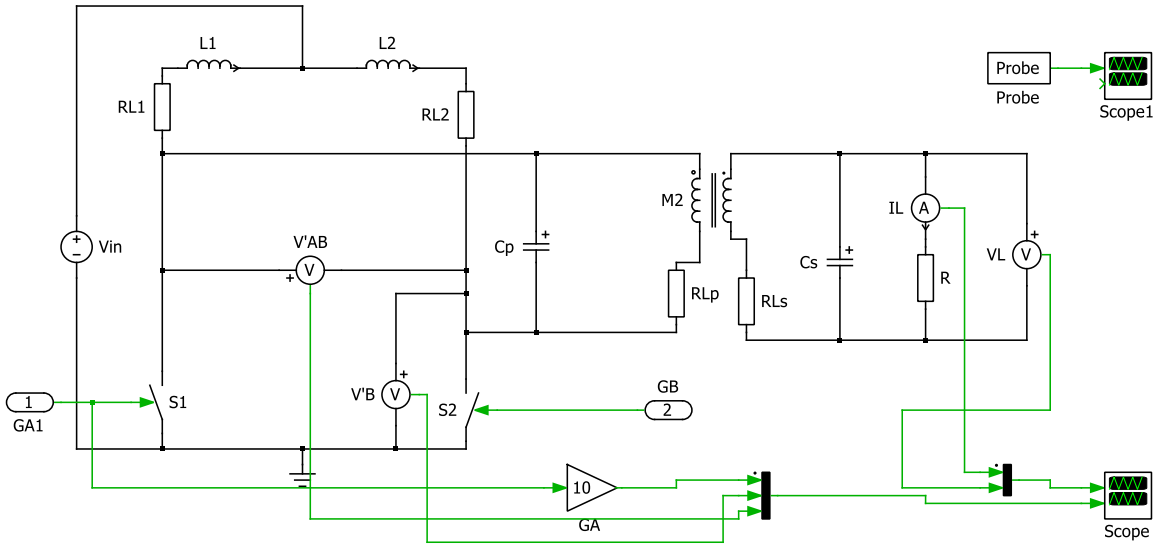


Figure A-3 PLECS circuit for current-fed push-pull primary and secondary with ac load

The following MATLAB code sets up initial conditions and system parameters for the above circuit.

```
clear all;
format long;

tsim=10e-3;
%% Variable circuit parameters
k=0.5;
fsw=163.7e3;

R=10*pi^2/2;
Tsw=1/fsw;
D=50;
Vin=10;
```

```
%% Circuit components
w0=2*pi*200e3;
L1=1e-3;
L2=1e-3;
Lp=11.3e-6;
Ls=3.31e-6;
Cp=1/(w0^2*Lp);
Cs=1/(w0^2*Ls);

RL1=0.46;
RL2=0.46;
RLp=73.1e-3;
RLs=26.7e-3;
RCp=0;
RCs=0;
M=k*sqrt(Lp*Ls);
%% Switching devices
Vf_diode=0.01;
Ron_diode=0.01;
Ron_MOSFET=1e-6;
I0=0;
Vth=1e-6;

%% PLECS parameters
Ts=1e-8;
Tol_rel=1e-9;
Ref_fact=1;
Tol_abs=1e-9;
Tzc=1e-9;
```

Appendix B: PLECS simulation for primary power flow control with pre-defined upper boundary

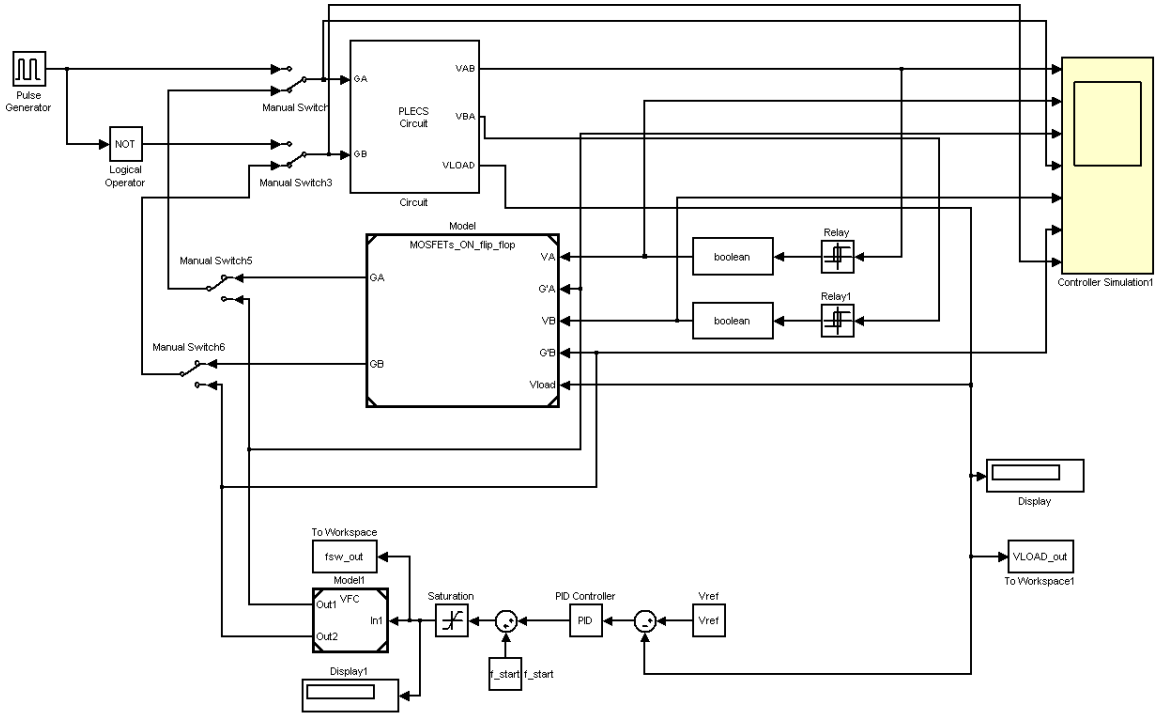


Figure B-1 PLECS simulation for primary power flow control with upper frequency boundary

The above schematic shows the overall system simulation for primary power flow control.

The following power electronic circuit is used during simulation.

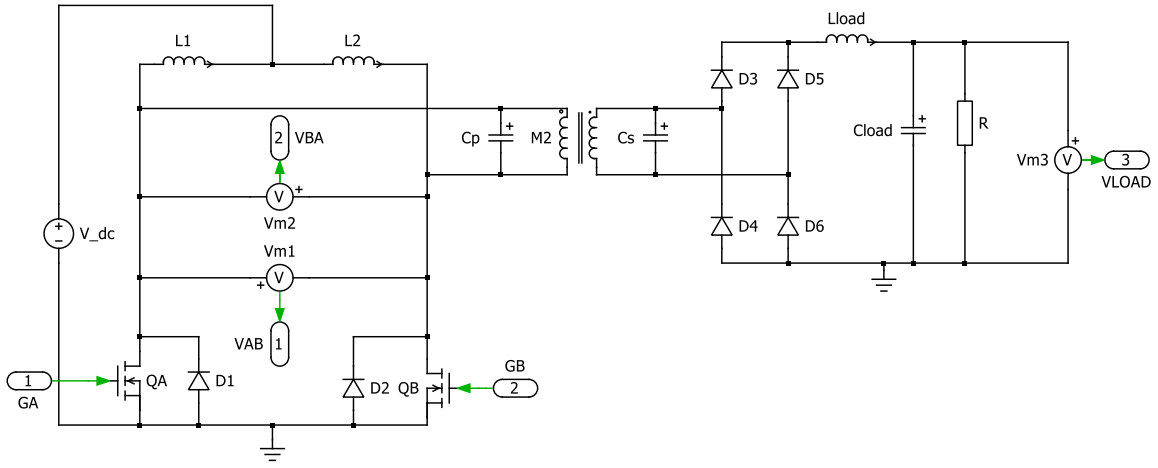


Figure B-2 PLECS circuit for current-fed push-pull primary and a secondary with full bridge rectifier

The following logic is used to derive the enhanced mode gate drive waveforms from the system waveforms, V_A, V_B, G'_A and G'_B. After sufficient load voltage (V_{LOAD}) is present,

the system will transit from basic gate drive waveforms, G'_A and G'_B to the enhanced mode gate drive waveforms, G_A and G_B.

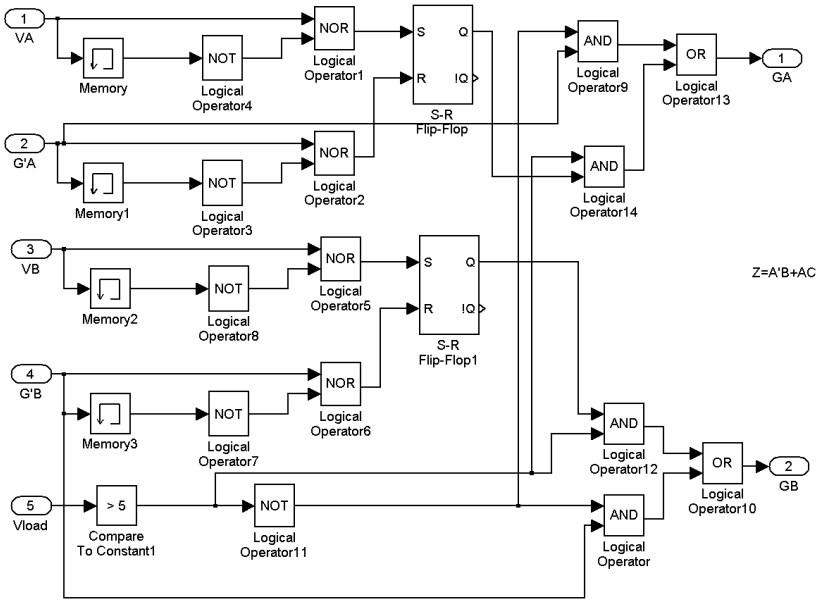


Figure B-3 PLECS controller details for enhanced mode operation

The following is a voltage controlled oscillator outputting two complementary square waveforms from a dc input.

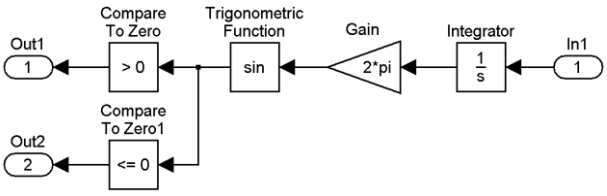


Figure B-4 Simulink realisation of a voltage controlled oscillator

The following MATLAB code is used to initialise the system with correct parameter values.

```
clear all;
format long;

tsim=4e-3;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
V_dc=25;
R=10;
k=0.23;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
RLOAD=R;
f0=200e3;
Lp=12e-6;
Ls=3e-6;
Cp=47e-9;
```

```
Cs=168e-9;

Lload=10e-6;
Cload=10e-6;
Vf_diode=0.01;
Ron_diode=0.01;
Ron_MOSFET=20e-3;
I0=0;
Vth=1e-6;

Ts=1e-8;
Tol_rel=1e-9;
Ref_fact=1;
Tol_abs=1e-9;
Tzc=1e-9;

L1=1e-3;
L2=1e-3;

D1=50;
D=50;
fsw=180e3;
Tsw=1/fsw;

Lp_dc=1e-3;
Ls_dc=30e-6;

w0=2*pi*f0;

M=k*sqrt(Lp*Ls);
f=find_fzvs(R,Lp,Ls,Cp,Cs,M);

Rldc1=0.419;
Rldc2=Rldc1;
Rlp=0.0671;
Rcp=0.012;
Rls=0.0271;
Rcs=0.007;
Rldc3=0.106;
Rcload=0.001;

Vdc=23;
Vref=10;

Kc=200;
Ti=1e-5;
Ki=Kc/Ti;

P=Kc; %proportional gain
I=Ki;

f_start=170e3;
f_upper=178.52e3;
f_lower=120e3;
```

Appendix C: PLECS simulation for primary controller with shorting period detection

The following main PLECS diagrams show the circuit being controlled by a software algorithm.

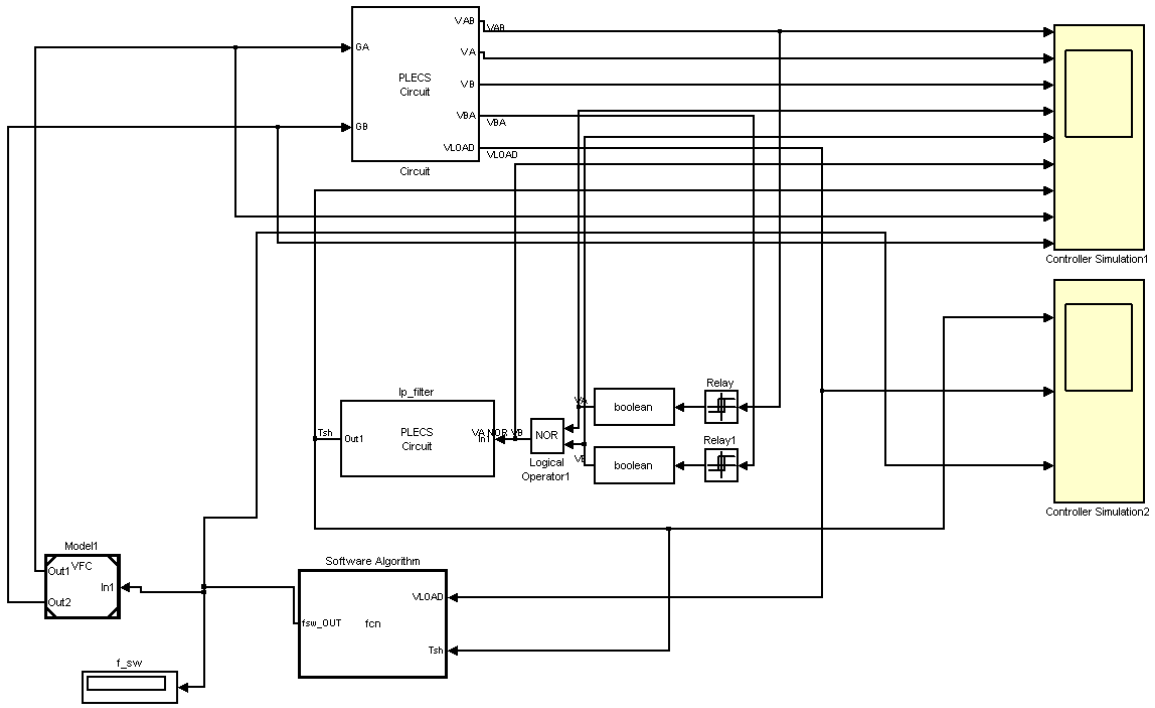


Figure C-1 PLECS schematic for the primary power flow controller with shorting period detection

The following diagram is the main power electronic circuit for the primary and secondary.

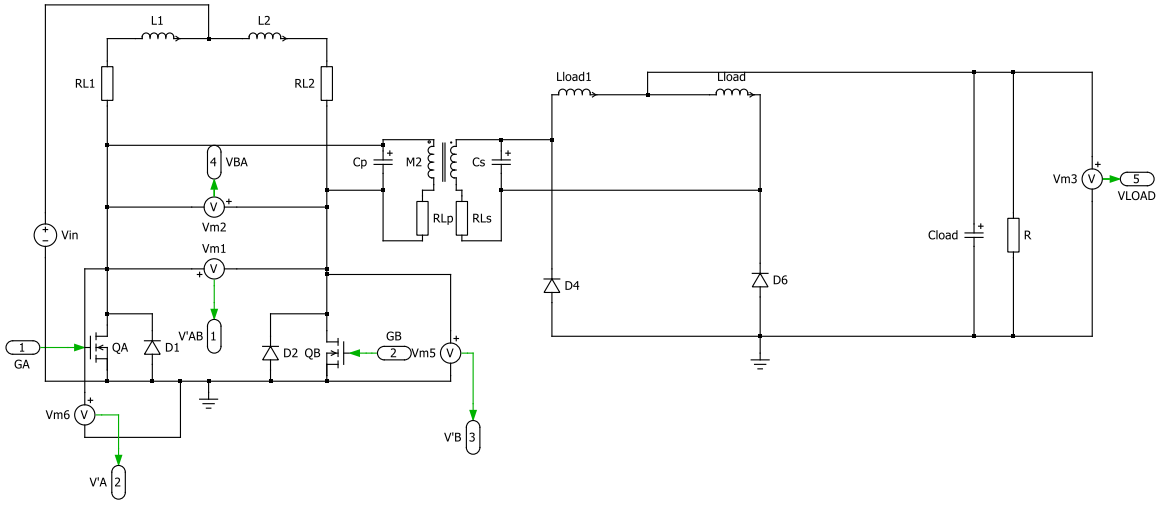


Figure C-2 PLECS circuit using a current-fed push pull primary and a secondary with current doubler rectifier

The following circuit is used to convert the resonant shorting pulse into a dc voltage for the software algorithm module.

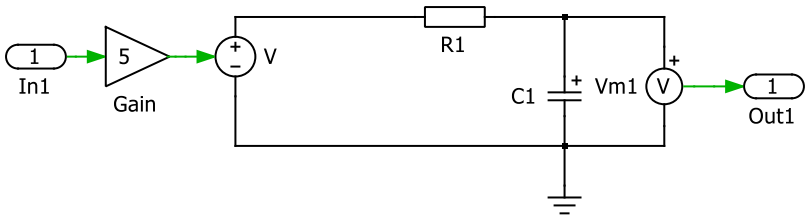


Figure C-3 PLECS circuit for converting square pulse shorting period into its dc average

The following embedded MATLAB code in PLECS is the central frequency controller that determines the output frequency from the load voltage and resonant shorting period inputs.

```
function fsw_OUT = fcn(VLOAD,Tsh)
%%-------------------------------------------------------------------------
---
%% Define variables
persistent fsw
persistent start_up
persistent count
count_max = 5e3;
Vref = 10;
Tsh_ref = 0.1;
delta = 100;
f_start = 170e3;
f_upper = 230e3;
f_lower = 140e3;
%%-------------------------------------------------------------------------
---
%% Initialisation
if isempty(start_up)
    fsw = f_start;
    count = 0;
    start_up = 1;
end
%%-------------------------------------------------------------------------
---
%% Frequency controller
if(count == count_max) %delay
    if (VLOAD <= Vref) % is VLOAD still below desired set target?
        if(Tsh <= Tsh_ref) % is shorting period below the set reference?
            fsw = fsw - delta; % then decrement switching frequency
        else
            fsw = fsw + delta; % otherwise increment switching frequency
        end
    else
       fsw = fsw - delta; % otherwise decrement switching frequency
    end
    count = 0; % clear count
else
    count = count + 1; % otherwise increment count value
end
```

```
%-------------------------------------------------------------------------
---
%% Limit output frequency
if (fsw > f_upper)
    fsw = f_upper;
elseif (fsw < f_lower)
    fsw = f_lower;
end

fsw_OUT = fsw; % assign fsw_OUT to fsw for output
```

The following MATLAB code is used to initialise the system with correct parameter values.

```
clear all;
format long;

tsim=10e-3;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Vin=22;
R=10;
k=0.1;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Lp=11.3e-6;
Ls=3.31e-6;

Cp=47e-9;
Cs=168e-9;

Lload=100e-6;
Cload=10e-6;

RL1=0.46;
RL2=0.46;
RLp=73.1e-3;
RLs=26.7e-3;

L1=1e-3;
L2=1e-3;

M=k*sqrt(Lp*Ls);

%% Switching devices
Vf_diode=0.01;
Ron_diode=0.01;
Ron_MOSFET=20e-3;
I0=0;
Vth=1e-6;

%% PLECS parameters
Ts=1e-8;
Tol_rel=1e-9;
Ref_fact=1;
Tol_abs=1e-9;
Tzc=1e-9;
```

Appendix D: PSoC 5 implementation of improved primary controller

The following shows modules used in PSoC 5 to realise the controller, two ADC modules to read the load voltage and the resonant shorting period. The PWM module is used to generate gate driving signals.

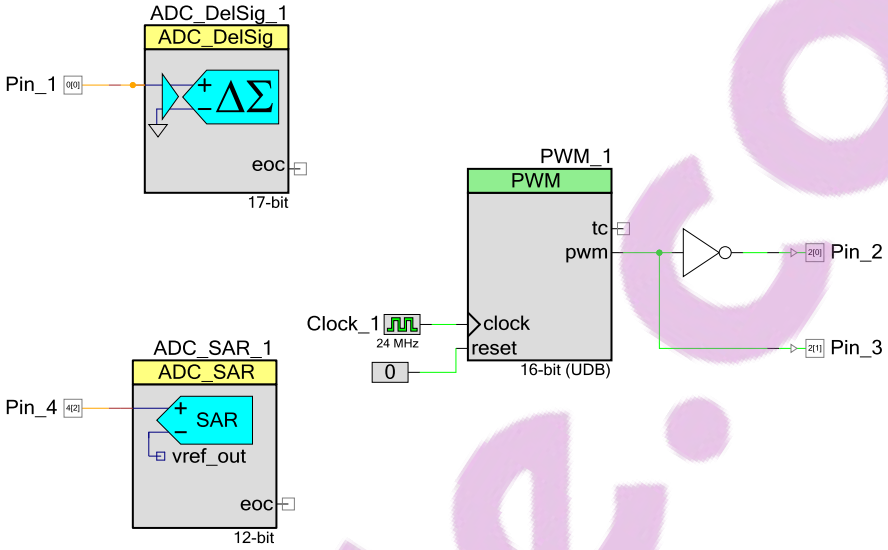


Figure D-1 PSoC 5 schematic for two ADC input and complementary 50% duty cycle pulse outputs

The following C code was written to control the frequency of the output PWM according the load voltage level and the resonant shorting period.

```
#include <device.h>

unsigned long feedback;
unsigned long Vsh;
unsigned long FCLOCK;

unsigned int REF;
unsigned int REFsh;

unsigned long PWM_freq_improved;

unsigned long PWM_freq_improved_upper;
unsigned long PWM_freq_improved_lower;

unsigned int PWM_Period;
unsigned int PWM_PulseWidth;

void main()
{

      ADC_DelSig_1_Start();
      ADC_DelSig_1_StartConvert();
      ADC_SAR_1_Start();
      ADC_SAR_1_StartConvert();
      PWM_1_Start();
```

```
      FCLOCK = 24000000;
      REF = 92000; //An equivalent of 10V reference for load voltage
2^17=131072 (max) representing 5V
      REFsh = 1000; //the shorting period reference

      PWM_freq_improved_upper = 230000; //improved mode
      PWM_freq_improved = 170000;
      PWM_freq_improved_lower = 135000;


      for(;;) //start a while loop
    {
//-------------------------------------------------------------------------
---
// This action gets the analog load voltage and converts into a digital
17 bits number 2^17=131072 (5V)
// However 5V represents 12V load voltage, so the actual 10V reference
need to be less.
            while(ADC_DelSig_1_IsEndConversion(1) == 0);
            feedback = ADC_DelSig_1_GetResult32(); //VLOAD feedback
//-------------------------------------------------------------------------
---
            while(ADC_SAR_1_IsEndConversion(1) == 0);
            Vsh = ADC_SAR_1_GetResult16(); //resonant shorting feedback
//-------------------------------------------------------------------------
---
      //Vsh is the shorting period represented as a voltage level
      //REFsh is the reference margin to prevent instant capacitor
shorting
      //error is the a difference, REF - feedback
      //REF is the reference voltage for comparison with feedback
      //feedback is the load voltage fed back to compare with reference
      //=========================================
      // whenever resonant shorting period is greater than a set margin
and when
      // the load voltage is less than desired, we increment the PWM
frequency by 1kHz.
if(feedback < REF){ // check whether the load voltage is less than
target reference or set point voltage
      if(Vsh < REFsh){ // check whether the resonant shorting period is
less than target reference or set point voltage
            PWM_freq_improved = PWM_freq_improved - 100; //decrement
switching frequency
      }
      else{
            PWM_freq_improved = PWM_freq_improved + 100; //else
increment switching frequency
      }
}
else{
      PWM_freq_improved = PWM_freq_improved - 100; //decrement switching
frequency
}
//=============================================================
//startup sequence
if(feedback > 80000){
      REFsh = 210; //210 for current doubler
}
else if (feedback < 50000){
      REFsh = 1000;
}
```

```
//-------------------------------------------------------------------------
---// Limit the PWM frequency to the system operating frequency
boundaries
// No upper boundary is really required as it is sensed by shorting
period
// but for protection purposes one is placed
        if(PWM_freq_improved >= PWM_freq_improved_upper){ //limit upper
fsw
            PWM_freq_improved = PWM_freq_improved_upper;
        }
        else if (PWM_freq_improved <= PWM_freq_improved_lower){ //limit
lower fsw
            PWM_freq_improved = PWM_freq_improved_lower;
        }
        else{
            ;
        }
//-------------------------------------------------------------------------
---
            PWM_Period = FCLOCK/PWM_freq_improved; //number of clock
cycle in relation to system clock
            PWM_PulseWidth = PWM_Period / 2;
            PWM_1_WritePeriod(PWM_Period);
            PWM_1_WriteCompare(PWM_PulseWidth);

//=========================================================================
===
            unsigned int i;
            for (i=1 ; i<1000 ; i++); //slowing the code down
//=========================================================================
===
      }
}
```

Appendix E PLECS simulation of middle ZVS follower with blocking diode

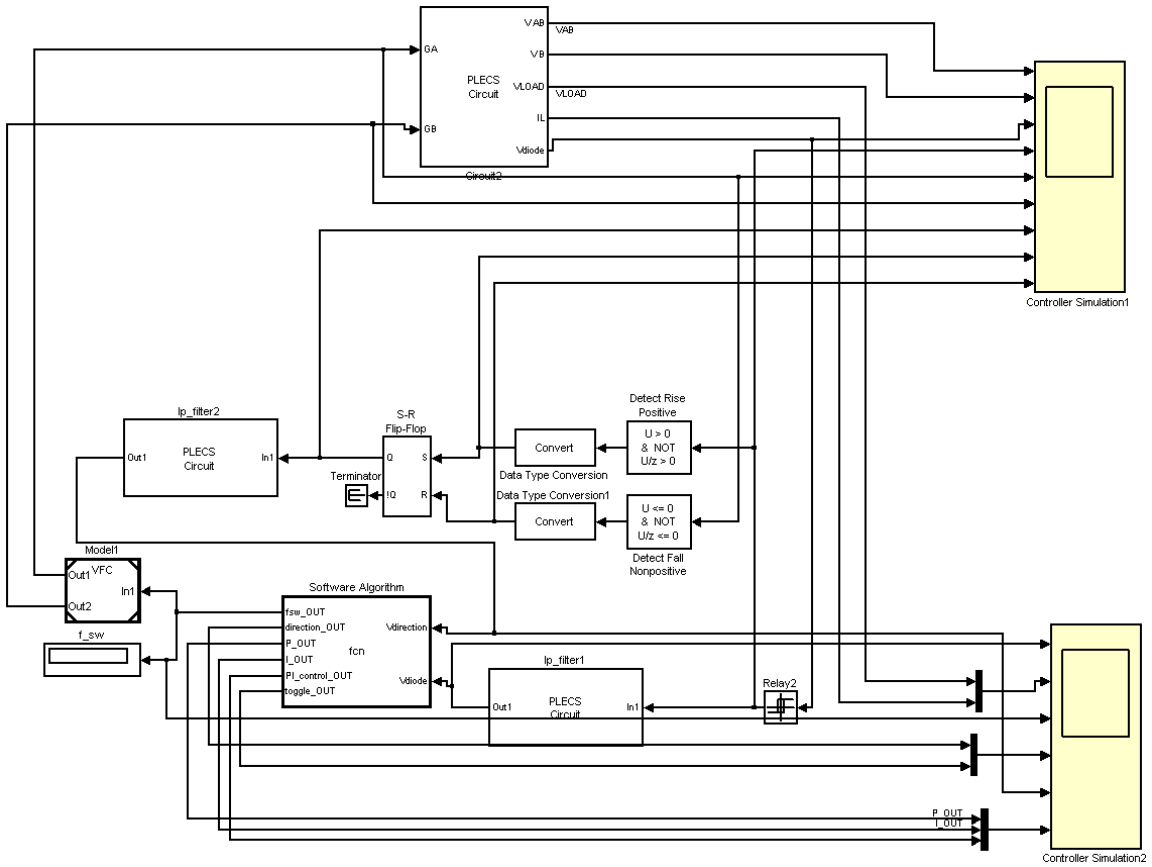


Figure E-1 PLECS schematic for middle ZVS operation with blocking diodes

The above shows the schematic diagram for simulating power tracking under PLECS.

Figure E-2 is the power electronic circuit to be controlled with a parallel tuned current-fed push-pull converter at the primary and a paralleled tuned secondary with an ac load.

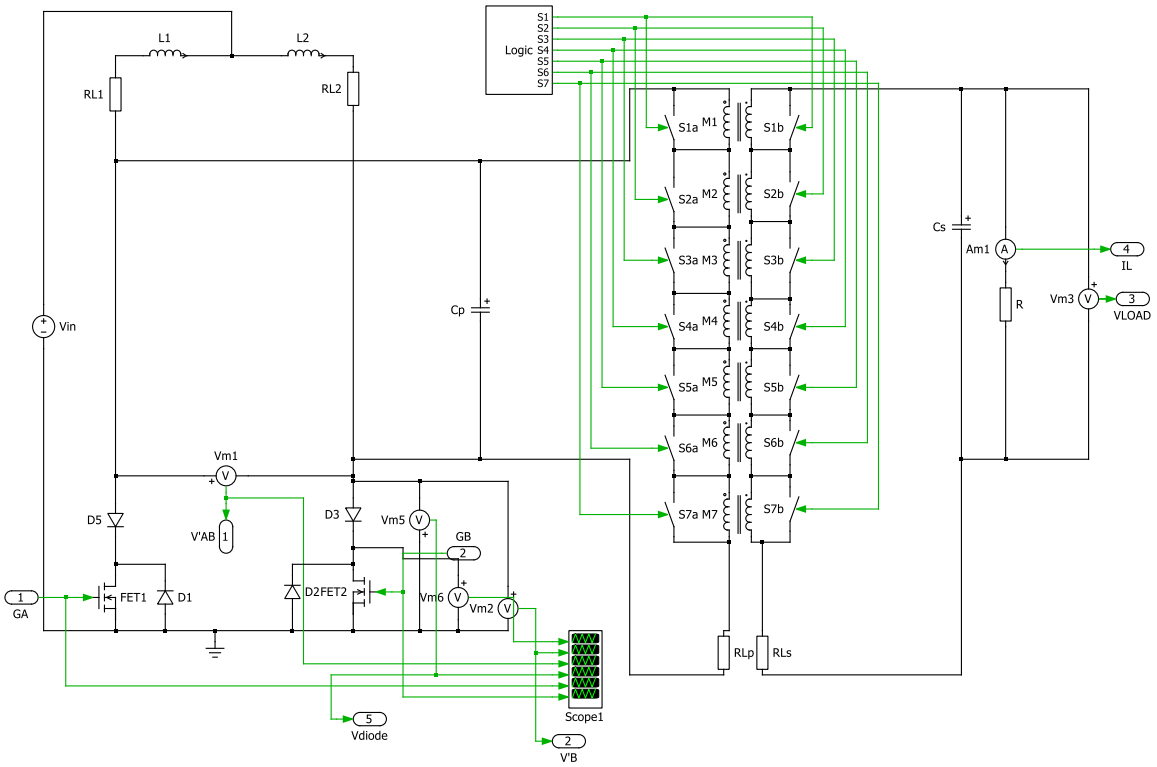


Figure E-2 PLECS circuit for primary and secondary with stepping coupling levels

Figure E-3 shows the logic used to switch between the different mutual inductors and coupling levels to simulate variations in direct distance coil separation.

The following function is embedded into the PLECS simulation to control frequency.

```
function [fsw_OUT, direction_OUT,P_OUT,I_OUT,PI_control_OUT,toggle_OUT]
= fcn(Vdirection,Vdiode)
%%-------------------------------------------------------------------------
----
%% Define variables
persistent fsw  %-- this may be the term that is different when it comes
to C programming
persistent count
persistent tog_cnt
persistent toggle
persistent start_up
persistent direction
persistent P_value_previous
persistent I_value_previous
persistent PI_OUT
persistent PI_OUT_LAST
persistent P
persistent I
%%-------------------------------------------------------------------------
----
%% Initialise variables
f_start = 210e3;
f_upper = 265e3;
Vdiode_ref = 0.1;
f_toggle = 230e3;
```

```
direction_upper = 2.3;
direction_lower = 1.5;
count_max = 200;
tog_cnt_max = 100000;
OFFSET = 237.5e3;
I_value_saturate = 100e3;
maxChange = 100;


Pgain = 10e3;
Igain = 50;
%%-------------------------------------------------------------------------
----
%% Initialise persistent variables
if isempty(start_up)
    fsw = f_start;
    count = 0;
    tog_cnt = 0;
    toggle = 0;
    start_up = 1;
    direction = 1;
    P_value_previous = 0;
    I_value_previous = 0;
    PI_OUT = 0;
    PI_OUT_LAST = 0;
    P = -Pgain;
    I = -Igain;
end
%%-------------------------------------------------------------------------
----
%% Track ZVS for non-bifurcated region
if(fsw == f_start)
    tog_cnt = tog_cnt + 1;
else
    tog_cnt = 0;
end
if(tog_cnt == tog_cnt_max)
    toggle = 1;
end
if (fsw > f_toggle)
    toggle = 0;
end
%%-------------------------------------------------------------------------
----
%% PI control
if (count == count_max) %delay
    if (toggle == 0)
        if(direction == 1)
            P = -Pgain;
            I = -Igain;
        elseif(direction == 0) %approaches middle ZVS branch from above
            P = Pgain;
            I = Igain;
        end
    elseif (toggle == 1)
        if(direction == 1)
            P = Pgain;
            I = Igain;
        elseif(direction == 0)
            P = -Pgain;
```

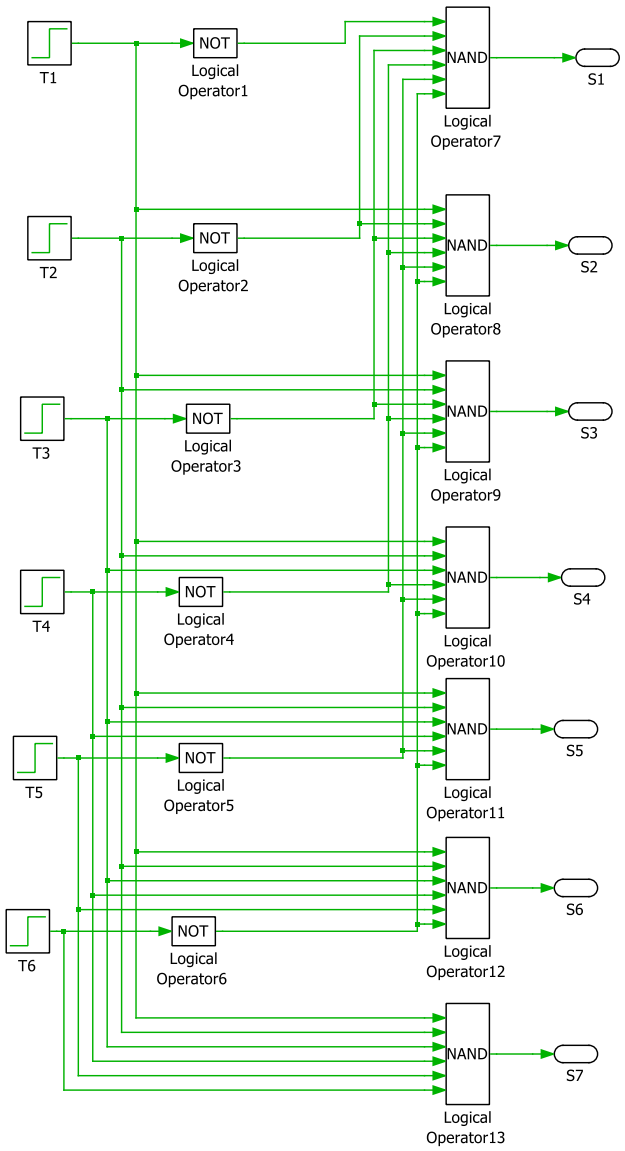


Figure E-3 The logic required to create a set of stepping coupling level in PLECS simulation

```
            I = -Igain;
        end
    end

    error = Vdiode_ref - Vdiode;

    P_value = P * error;
    I_value = I * error + I_value_previous;
%%------------------------------------------------------------------------
----
%% Saturate integral value
    if (I_value >= I_value_saturate)
        I_value = I_value_saturate;
    elseif (I_value <= -I_value_saturate)
        I_value = -I_value_saturate;
    end
    if (fsw == f_start)
        I_value = I_value_previous;
```

```
    end
%%-------------------------------------------------------------------------
----
%% Find PI output
    P_value_previous = P_value;
    I_value_previous = I_value;
    PI_OUT = P_value + I_value;

%%-------------------------------------------------------------------------
----
%% Limit maximum change to PI output
    if ( (PI_OUT - PI_OUT_LAST) > maxChange)
        PI_OUT = PI_OUT_LAST + maxChange;
    elseif ( (PI_OUT_LAST - PI_OUT) > maxChange)
        PI_OUT = PI_OUT_LAST - maxChange;
    end
    PI_OUT_LAST = PI_OUT;
%%-------------------------------------------------------------------------
----
%% Find switching frequency
    fsw = PI_OUT + OFFSET;
    count = 0; % clear count
else
    count = count + 1; % otherwise increment count value
end
%-------------------------------------------------------------
%% Changing direction
if (Vdirection > direction_upper) %approaches middle ZVS branch from
below
    direction = 1;
elseif(Vdirection < direction_lower) %approaches middle ZVS branch from
above
    direction = 0;
end
%-------------------------------------------------------------
%% Limit output frequency
if (fsw > f_upper)
    fsw = f_upper;
elseif (fsw < f_start)
    fsw = f_start;
end
%-------------------------------------------------------------
%% Outputs
fsw_OUT = fsw; % assign fsw_OUT to fsw for output
direction_OUT = direction;
P_OUT = P_value_previous;
I_OUT = I_value_previous;
PI_control_OUT = PI_OUT;
toggle_OUT = toggle;
```

Figure E-4 shows the first order RC filter used to transform square pulses into a dc value for frequency controller

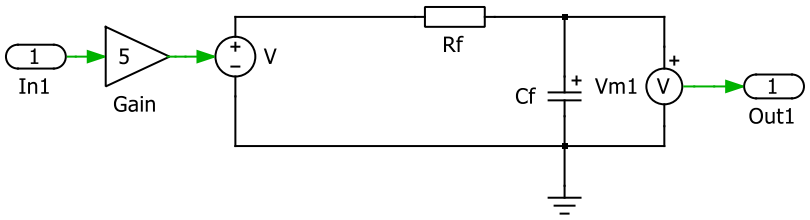


Figure E-4 Conversion from square pulse to a dc average equivalent

The following MATLAB code initialises the system before simulation.

```
clear all;
format long;
Tgap=2e-3;
tsim=Tgap*7;
%% Variable circuit parameters
k1=0.5;
k2=0.45;
k3=0.4;
k4=0.35;
k5=0.3;
k6=0.2;
k7=0.1;

T1=Tgap;
T2=Tgap*2;
T3=Tgap*3;
T4=Tgap*4;
T5=Tgap*5;
T6=Tgap*6;

R=10*pi^2/2;
Vin=10;
Vswitch_on = 1;
Vswitch_off = 0;
Rf = 15e3;
Cf = 10e-9;
%% Circuit components

L1=1e-3;
L2=1e-3;
Lp=11.3e-6;
Ls=3.31e-6;
Cp=47e-9;
Cs=168e-9;

RL1=0.46;
RL2=0.46;
RLp=73.1e-3;
RLs=26.7e-3;

M1=k1*sqrt(Lp*Ls);
M2=k2*sqrt(Lp*Ls);
M3=k3*sqrt(Lp*Ls);
M4=k4*sqrt(Lp*Ls);
M5=k5*sqrt(Lp*Ls);
M6=k6*sqrt(Lp*Ls);
M7=k7*sqrt(Lp*Ls);
```

```
%% Switching devices
Vf_diode=0.01;
Ron_diode=0.01;
Ron_MOSFET=20e-3;
I0=0;
Vth=1e-6;

%% PLECS parameters
Ts=1e-8;
Tol_rel=1e-9;
Ref_fact=1;
Tol_abs=1e-9;
Tzc=1e-9;
```

Appendix F CompactRIO implementation of the middle ZVS follower with blocking diode

The following is the Power_Track (FPGA).vi front panel. It has an input controlling the PWM frequency and three ADC readings from the physical circuit, namely V_{diode}, $V_{direction}$ and V_{load}. The frequency number required by CompactRIO can be found by using the actual frequency divided by the clock frequency.

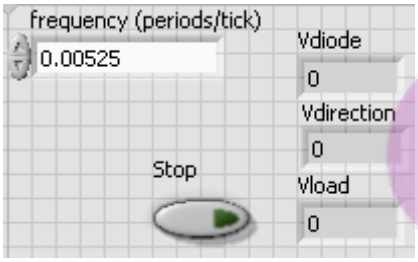


Figure F-1 CompactRIO front panel for FPGA mode with frequency control and three voltage readings

The following are the Power_Track (FPGA).vi block diagrams. They have a three part flat sequence structure, so that in the first part, the analogue input module is initialised and the digital module has its ports set to output. In the middle part of the sequence, a 'while' loop is used to continuously read three analogue inputs; a timed loop is used to output two complementary square waveforms of identical frequency and 50% duty cycle, the initial PWM frequency is set at 210kHz within the PWM symbol to avoid erroneous start-up frequency. On the last part of the sequence, the digital module has all its ports set to input to disable any possible waveforms present at the port. A stop latch is used as a manual switch to turn off the controller.

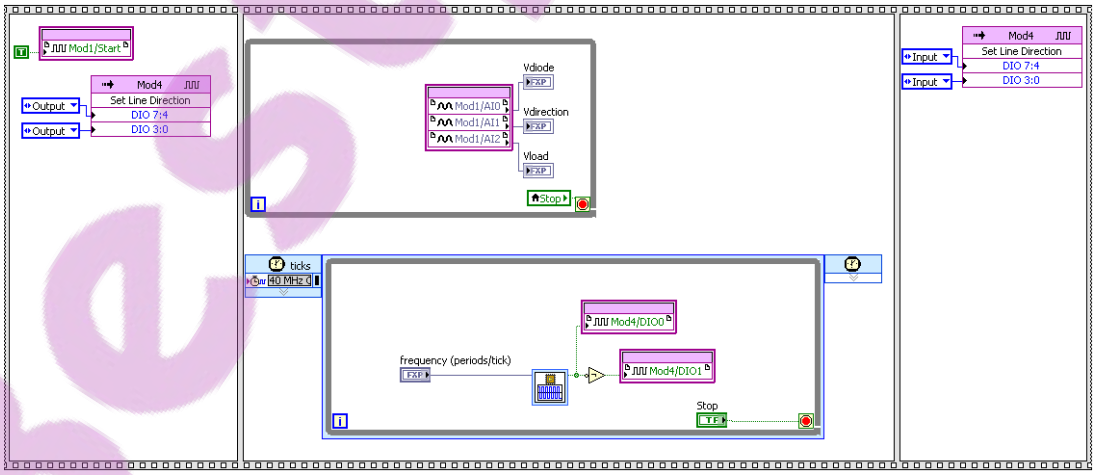


Figure F-2 FPGA mode block diagrams to output 50% duty cycle pulses and read three analogue inputs

The following is the Power_Track (Host).vi front panel, setting the upper (PWM_higher) and lower (PWM_lower) boundary frequency for PWM, proportional (Pgain) and integral (Igain) gains, integral term saturation limit (I_value_saturate), maximum change per iteration (maxChange), offset (OFFSET), frequency to reset toggle variable (PWM_toggle_freq), counts for toggle to be set (tog_cnt_max) and a wait timer (Wait) to control iteration speed. Two different V_{diode} references are used depending on the value of toggle variable. These indicate proximity to ZVS operation and ensure a smoother transition between non-bifurcated and bifurcated regions. If $V_{direction}$ falls between direction_upper_high and direction_upper_low, direction will be set to one; if it is above direction_lower_correction or below direction_lower, direction will be set to zero.

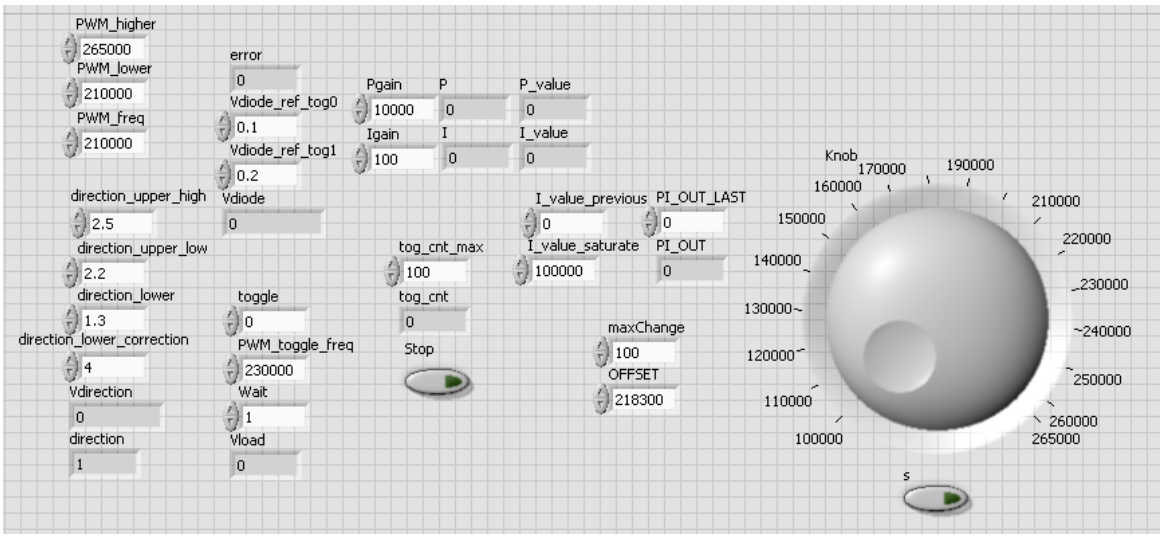


Figure F-3 Host mode front panel to control the ZVS follower with blocking diode

The Power_Track (Host).vi controls what is done on the CompactRIO host computer while Power_Track (FPGA).vi controls FPGA within the CompactRIO. Most of the controller calculations are completed on the host computer and the FPGA deals with high speed waveform generation and analogue voltage detection. Power_Track (Host).vi is written to call the Power_Track (FPGA).vi in order to modify the frequency of the PWM and attain the analogue voltage readings from the FPGA.

The following shows the Power_Track (Host).vi block diagrams. It shows a three part flat sequence structure. On the first part of the flat sequence, system variables are initialised, and the FPGA code is referenced and opened. On the third part of the structure the FPGA code is closed. The controller program resides in the middle part. The controller code is

placed within a ‘while’ loop to run continuously, and a stacked sequence structure is used to let different parts of the code run sequentially.

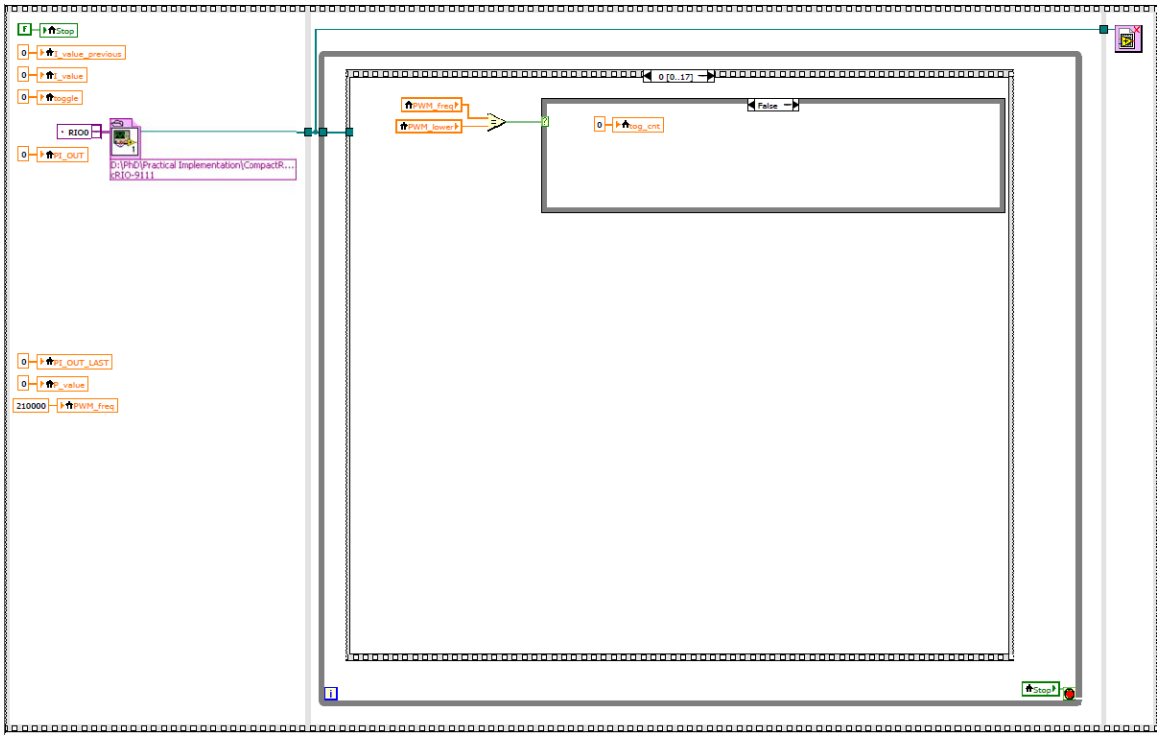


Figure F-4 Host mode general logic structure layout

Firstly if the PWM_freq is at the lower boundary and the toggle count is less than its maximum limit, toggle count increments. Once PWM_freq is no longer at lower bound toggle count resets to zero. (Frame 0)

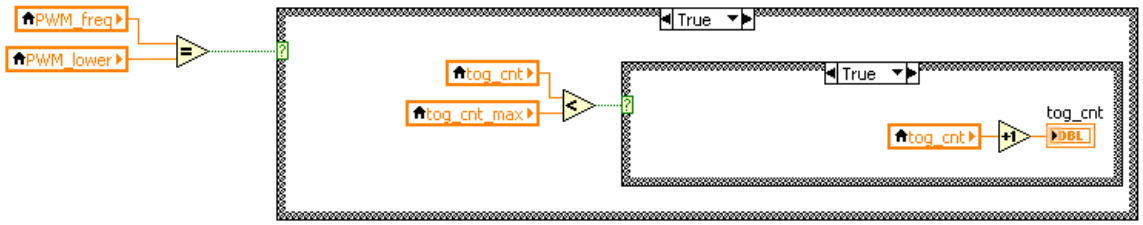


Figure F-5 Increment toggle counter until it reaches a pre-set maximum

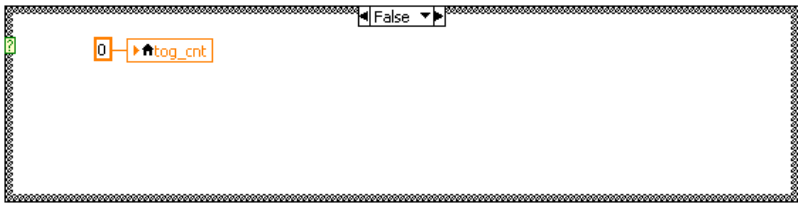


Figure F-6 Set toggle counter to zero when frequency depart from lower boundary

Once tog_cnt reaches the specified value, the value of the toggle variable is toggled between one and zero by using the following logic. The toggle counter is also reset. (Frame 1)

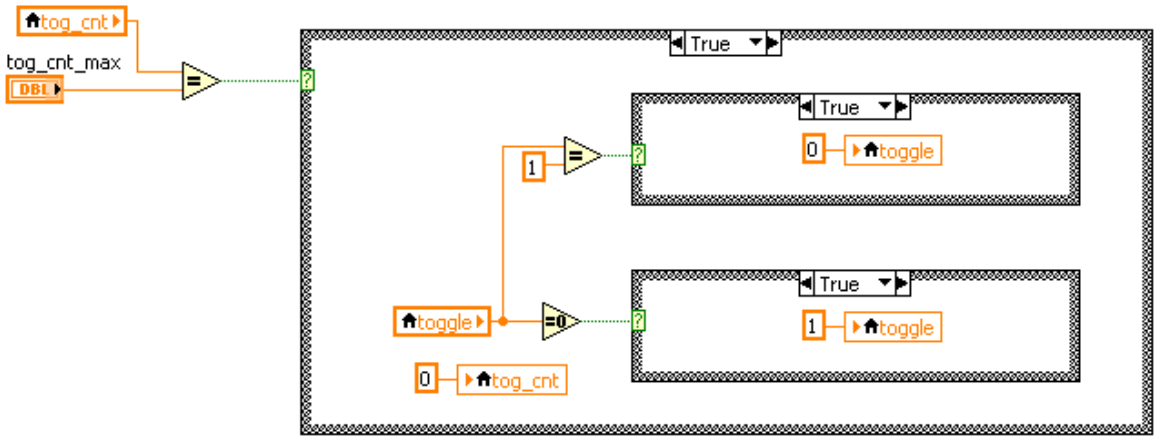


Figure F-7 When toggle counter reaches maximum, the toggle variable is swapped between 1 and 0

Toggle will be reset after the PWM frequency exceeds a set value (PWM_toggle_freq). (Frame 2)

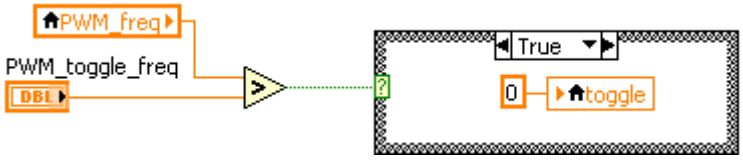


Figure F-8 When toggle frequency is reached, reset toggle

The graphical code shown in Figure F-9 will set proportional and integral gains according to the value of toggle and direction. (Frame 3)

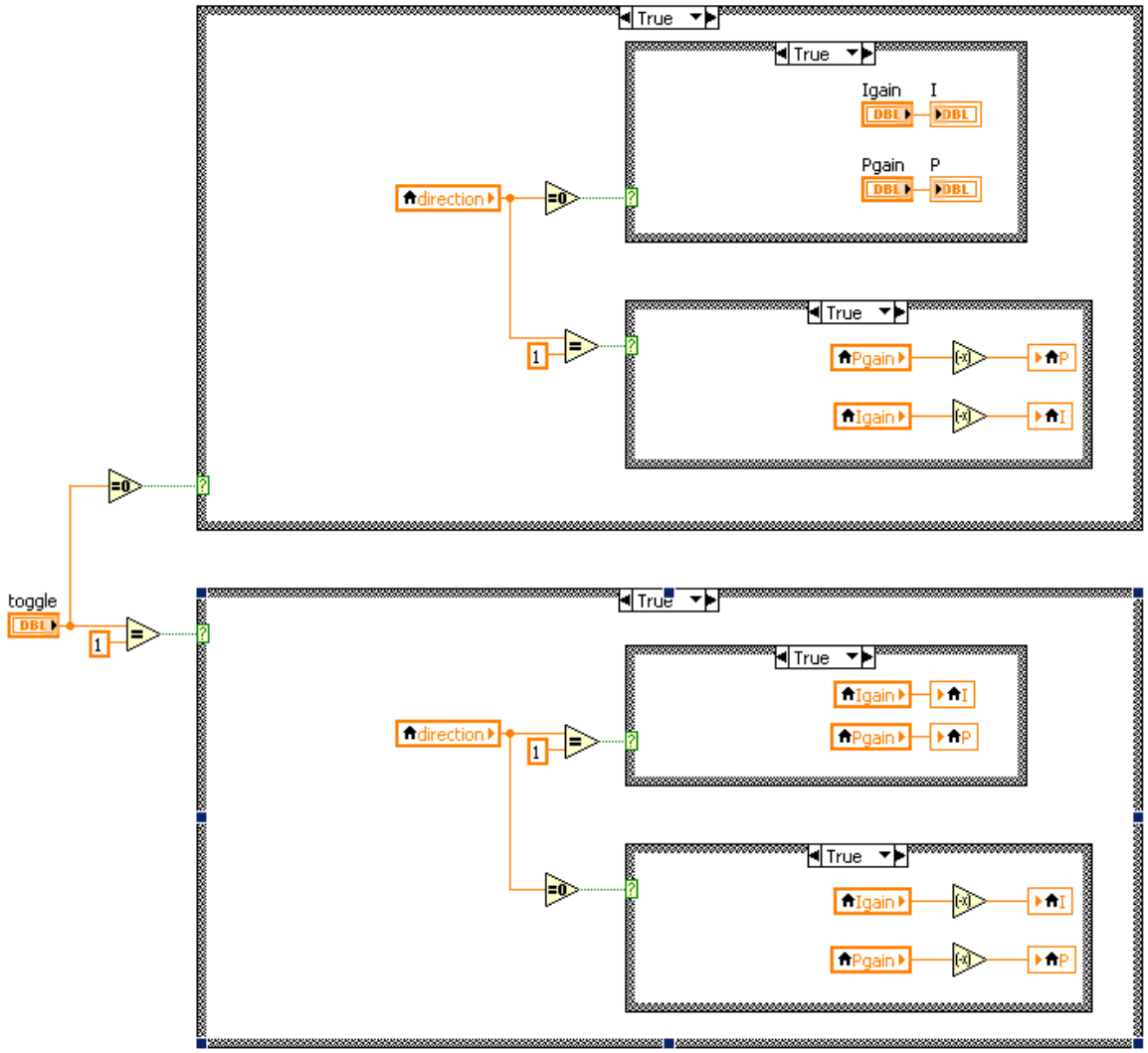


Figure F-9 Setting the proportional and integral gains according to the value of toggle and direction

The following code uses a different reference to calculate the error depending on the state of toggle variable. (Frame 4)

Figure F-10 Calculation of PI error

The following code finds the proportional term. (Frame 5)

Figure F-11 Find proportional term

The following code finds the continuously summing integral term. (Frame 6)

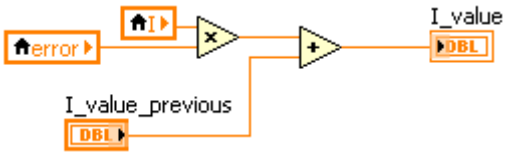


Figure F-12 Find integral term

The following code places a limit to the integral term. (Frame 7)

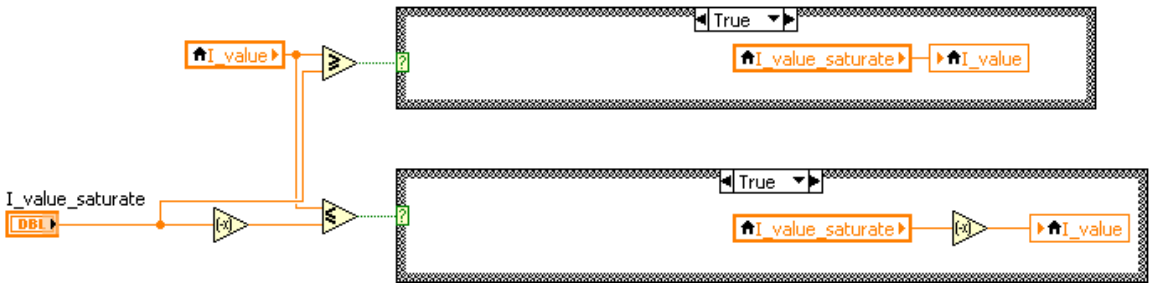


Figure F-13 Limit the integral term from unlimited ramping

The following code keeps the integral term constant while the PWM frequency is at the lower boundary. (Frame 8)

Figure F-14 While frequency at lower boundary, keep integral term constant

The following code keeps integral term constant when $V_{direction}$ is absent, which stops the frequency changing when the system is at ZVS. (Frame 9)

Figure F-15 Keep integral term constant in absence of $V_{direction}$

The following code remembers the current integral term for future summations; it also finds the sum of the proportional and integral terms. (Frame 10)

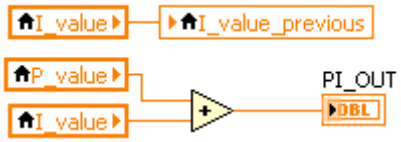


Figure F-16 Combine P and I and remember current I for future reference

The following code places a limit to the maximum change allowed in PI_OUT to prevent sharp variations in the output frequency. (Frame 11)

Figure F-17 Limit maximum change in PI output

The following remembers the current PI_OUT for future reference. (Frame 12)

Figure F-18 Remember current PI output for future reference

The following finds the actual PWM_freq from PI control. (Frame 13)

Figure F-19 Add offset to PI output

The following updates the direction according to several set boundaries for $V_{direction}$. (Frame 14)

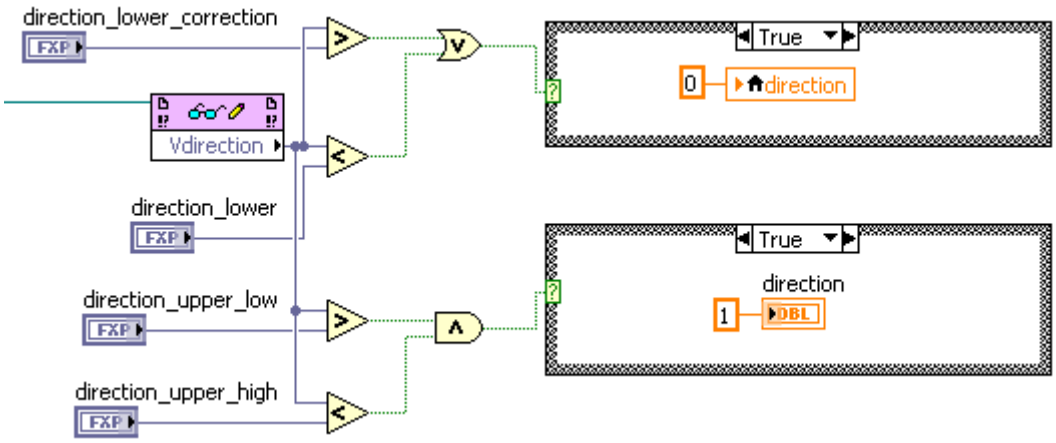


Figure F-20 Find direction indicator value

The following places an upper and lower boundary to the output switching frequency. (Frame 15)

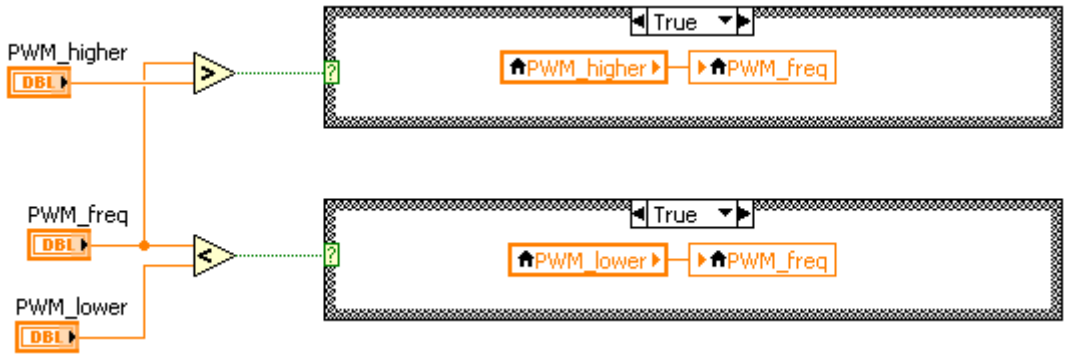


Figure F-21 Place an upper and lower boundary to frequency

A manual selection is used to switch between the calculated frequency and a manual override frequency via a control knob. The following communicates with the FPGA code, updating the output frequency of PWM and reading the V_{diode}, $V_{direction}$ and V_{load}. (Frame 16)

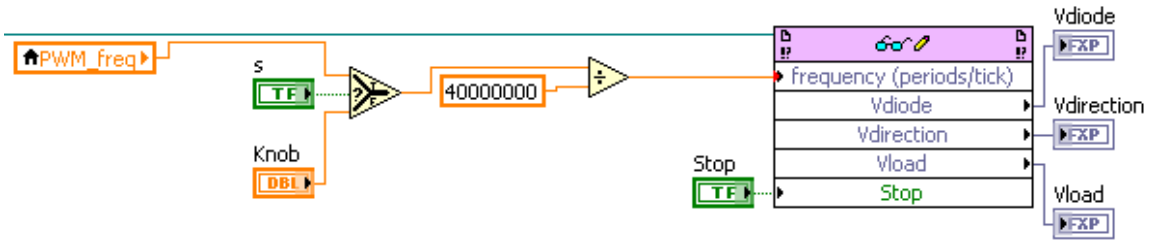


Figure F-22 Update the FPGA with calculated frequency and read new feedback values for control

The following places a wait timer to control the speed of code execution and the controller loop. (Frame 17)

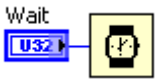


Figure F-23 Set a wait function to vary controller execution speed

Appendix G PLECS simulation of middle ZVS follower without blocking diode

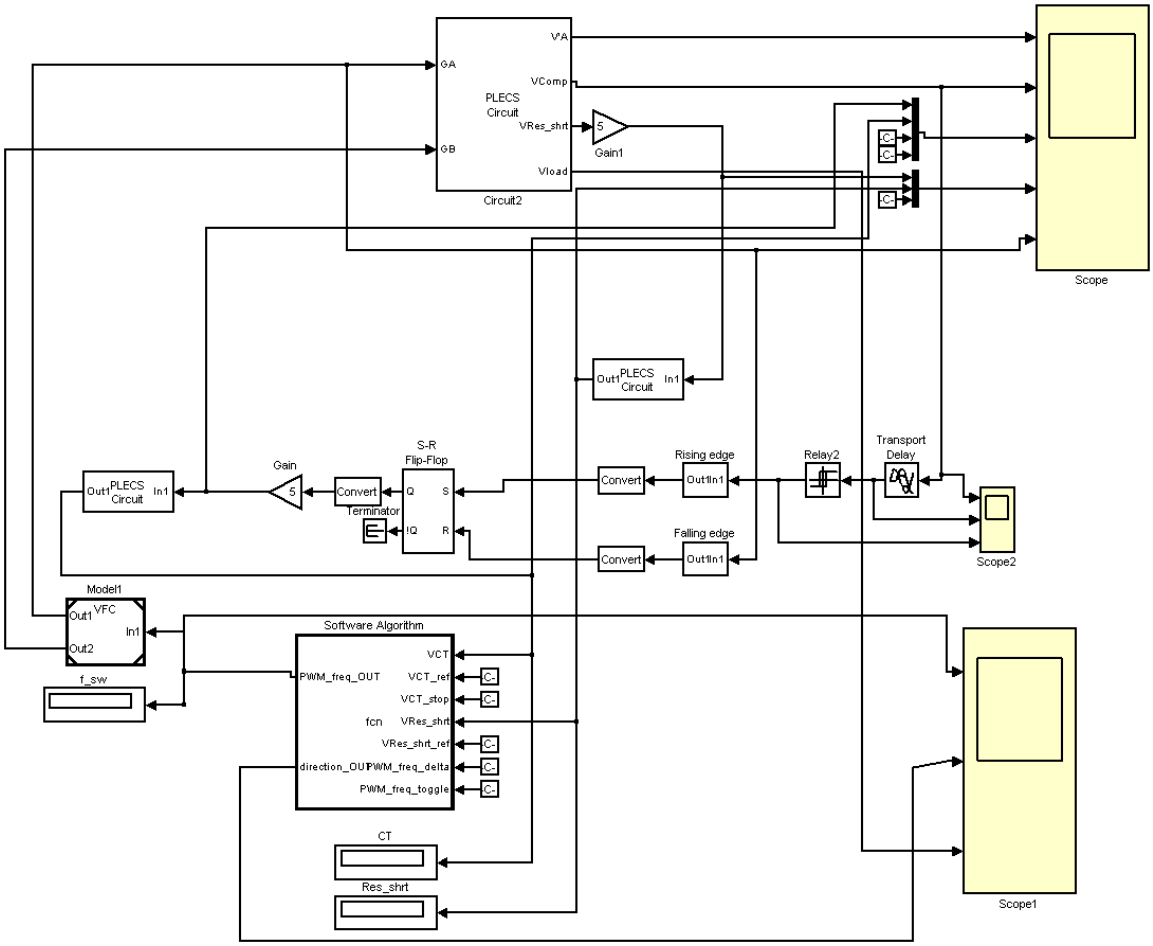


Figure G-1 PLECS schematic for middle ZVS follower without blocking diode

The PLECS simulation block diagrams are shown above. Voltage information is fed back to a digital software algorithm to alter the switching frequency in order to maintain middle ZVS operation upon bifurcation.

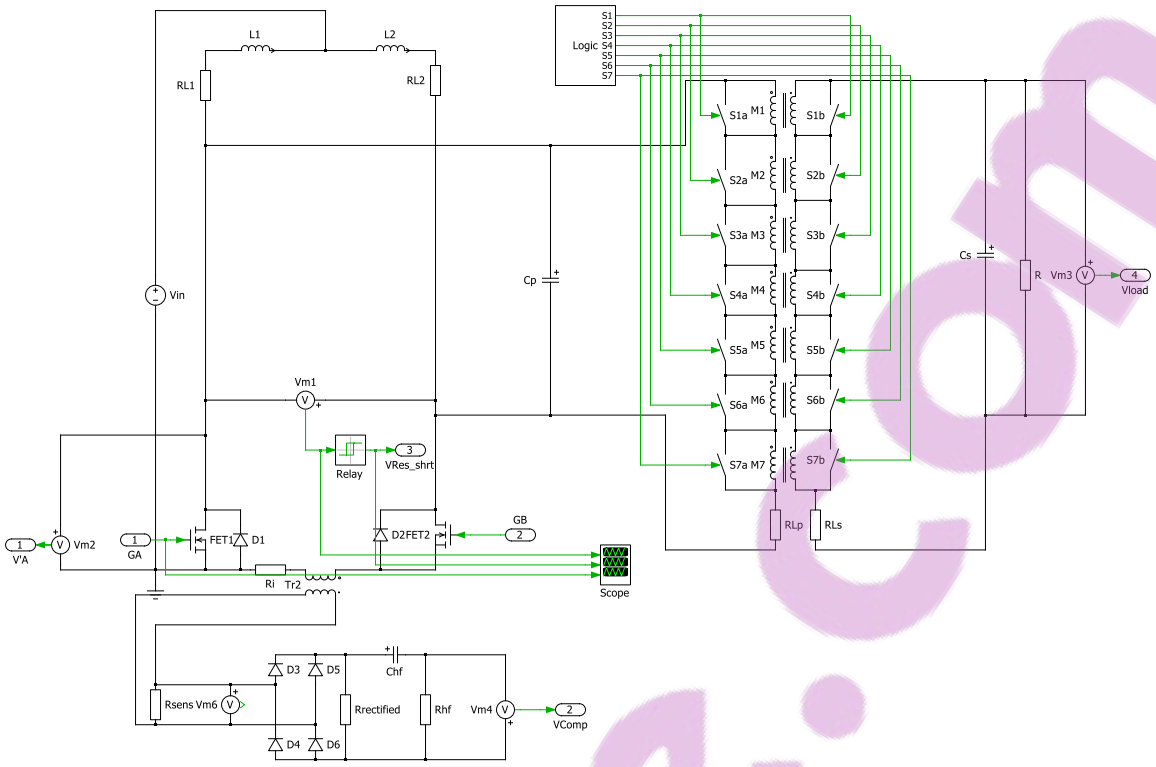


Figure G-2 PLECS circuit for primary and secondary with variable magnetic coupling and feedback signal acquisition

The above shows the system main switching circuit. Note that here, multiple switches are employed to select a pair of coils automatically at different times to simulate the system response to varying coupling levels. The logic circuit used to select the coils is identical to the one used for maintaining middle ZVS operation with blocking diode.

The following is a low pass filter used to convert voltage information to a simple dc level. This slow feedback loop means connection to a microcontroller can be done using low speed input ports.

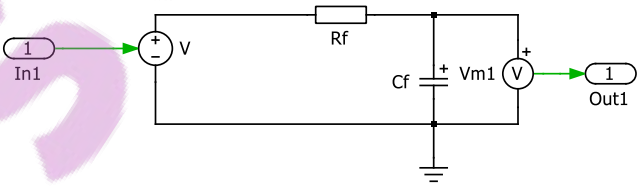


Figure G-3 PLECS circuit to convert feedback square pulses to their dc average equivalent

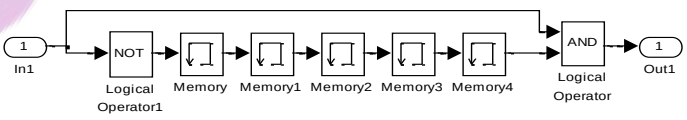


Figure G-4 Simulink implementation of a rising edge trigger

Figure G-4 outputs a trigger pulse when the input has a rising edge.

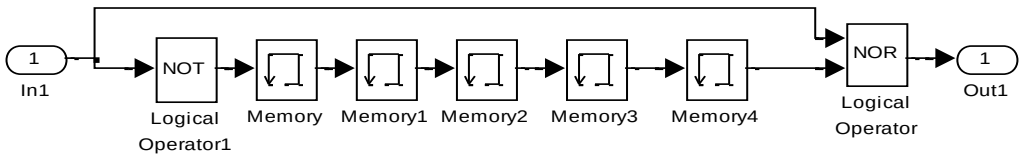


Figure G-5 Simulink implementation of a falling edge trigger

The above outputs a trigger pulse when the input has a falling edge.

The following code is embedded into the simulation to realise digital frequency control.

```
function [PWM_freq_OUT, direction_OUT] = fcn(VCT, VCT_ref, VCT_stop,
VRes_shrt, VRes_shrt_ref, PWM_freq_delta, PWM_freq_toggle)
%%-------------------------------------------------------------------------
----
%% Define variables
persistent PWM_freq
persistent count
persistent tog_cnt
persistent toggle

persistent start_up
persistent direction
persistent PWM_freq_prev

%%-------------------------------------------------------------------------
----
%% Initialise variables
PWM_lower = 210e3;
PWM_upper = 265e3;

count_max = 2e3;
tog_cnt_max = 100;

%%-------------------------------------------------------------------------
----
%% Initialise persistent variables
if isempty(start_up)
    start_up = 1;
    PWM_freq = PWM_freq_toggle;
    count = 0;
    tog_cnt = 0;
    toggle = 0;

    direction = 1;
    PWM_freq_prev = PWM_lower;
end
if (count == count_max) %delay
%%-------------------------------------------------------------------------
----
%% Toggle counter
    if(PWM_freq == PWM_lower || PWM_freq == PWM_upper)
```

```
        if(tog_cnt < tog_cnt_max)
            tog_cnt = tog_cnt + 1;
        else
            tog_cnt = 0;
        end
    end

%%-------------------------------------------------------------------------
----
%% Setting toggle
    if(tog_cnt == tog_cnt_max)
        if(toggle == 0)
            toggle = 1;
        end
        if(toggle == 1)
            toggle = 0;
        end
        tog_cnt = 0;
    end
%%-------------------------------------------------------------------------
----
%% Resetting toggle
    if(VRes_shrt < VRes_shrt_ref && PWM_freq > PWM_freq_toggle)
        toggle = 0;
    end
%%-------------------------------------------------------------------------
----
%% Change frequency
    if(toggle == 0)
        if(direction == 1)
            PWM_freq = PWM_freq + PWM_freq_delta;
        end
        if(direction == 0) %approaches middle ZVS branch from above
            PWM_freq = PWM_freq - PWM_freq_delta;
        end
    end
    if(toggle == 1)
        if(direction == 1)
            PWM_freq = PWM_freq - PWM_freq_delta;
        end
        if(direction == 0)
            PWM_freq = PWM_freq + PWM_freq_delta;
        end
    end
%%-------------------------------------------------------------------------
----
%% Changing direction
    if (VRes_shrt < VRes_shrt_ref && VCT < VCT_ref)
        direction = 0;
    end
    if(VRes_shrt > VRes_shrt_ref && VCT > VCT_ref)
        direction = 1;
    end
%%-------------------------------------------------------------------------
----
%% Stop frequency variations
    if (VCT < VCT_stop && VRes_shrt > VRes_shrt_ref)
        PWM_freq = PWM_freq_prev;
        direction = 2;
    end
```

```
%%-------------------------------------------------------------------------
----
%% Limit output frequency
    if (PWM_freq > PWM_upper)
        PWM_freq = PWM_upper;
    end
    if (PWM_freq < PWM_lower)
        PWM_freq = PWM_lower;
    end
%%-------------------------------------------------------------------------
----
    count = 0; % clear count
else
    count = count + 1; % otherwise increment count value
end
%%-------------------------------------------------------------------------
----
%% Outputs
% PWM_freq = 240e3;
PWM_freq_prev = PWM_freq;
PWM_freq_OUT = PWM_freq; % assign fsw_OUT to fsw for output
direction_OUT = direction;
```

The following MATLAB code initialises the system before simulation.

```
clear all;
format long;
%% Frequency controller parameters
VRes_shrt_ref = 2.2;

VCT_ref = 4.8;
VCT_stop = 4.8;

PWM_freq_delta = 80;
PWM_freq_toggle = 230e3;
%% Coupling change timing
Tstart=3e-3;
Tgap=3e-3;
tsim=Tstart+Tgap*6;
%% CT parameters
Ri=0.1;

Chf=1e-9;
Rhf=10;
Rsens=50;
Rrectified=10;

Np=20;
Ns=1000;

%% Low pass filters
Rf = 15e3;
Cf = 5e-9;

%% System coupling variations
k1=0.1;
k2=0.2;
```

```
k3=0.3;
k4=0.4;
k5=0.45;
k6=0.5;
k7=0.55;

T1=Tstart;
T2=Tstart+Tgap;
T3=Tstart+Tgap*2;
T4=Tstart+Tgap*3;
T5=Tstart+Tgap*4;
T6=Tstart+Tgap*5;

%% System parameters
R=10*pi^2/2;
Vin=8;

%% Circuit components
L1=1e-3;
L2=1e-3;
Lp=11.3e-6;
Ls=3.31e-6;
Cp=47e-9;
Cs=168e-9;

RL1=0.46;
RL2=0.46;
RLp=73.1e-3;
RLs=26.7e-3;

M1=k1*sqrt(Lp*Ls);
M2=k2*sqrt(Lp*Ls);
M3=k3*sqrt(Lp*Ls);
M4=k4*sqrt(Lp*Ls);
M5=k5*sqrt(Lp*Ls);
M6=k6*sqrt(Lp*Ls);
M7=k7*sqrt(Lp*Ls);

%% Switching devices
Vf_diode=0.01;
Ron_diode=0.01;
Ron_MOSFET=20e-3;
I0=0;
Vth=1e-6;

%% PLECS parameters
Ts=1e-8;
Tol_rel=1e-9;
Ref_fact=1;
Tol_abs=1e-9;
Tzc=1e-9;
```

Appendix H CompactRIO controller of middle ZVS follower without blocking diode

The following is the Power_Track (FPGA).vi front panel. It shows the desired frequency, the feedback information from the current transformer, resonant shorting detection and the load voltage.

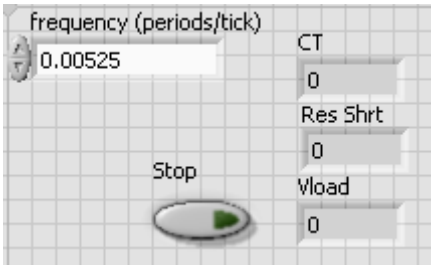


Figure H-1 FPGA mode front panel for frequency input, and three feedback voltages

The following is the Power_Track (FPGA).vi block diagrams view. This is a flat sequence coding structure from left to right. On the first sequence, the voltage sensing module is activated, and the digital modules set to output. On the middle sequence, the data is collected continuously using a 'while' loop; the square wave is generated continuously at the required frequency within a timed while loop. On the right hand side sequence, the digital blocks are set to input, which effectively shuts them off.

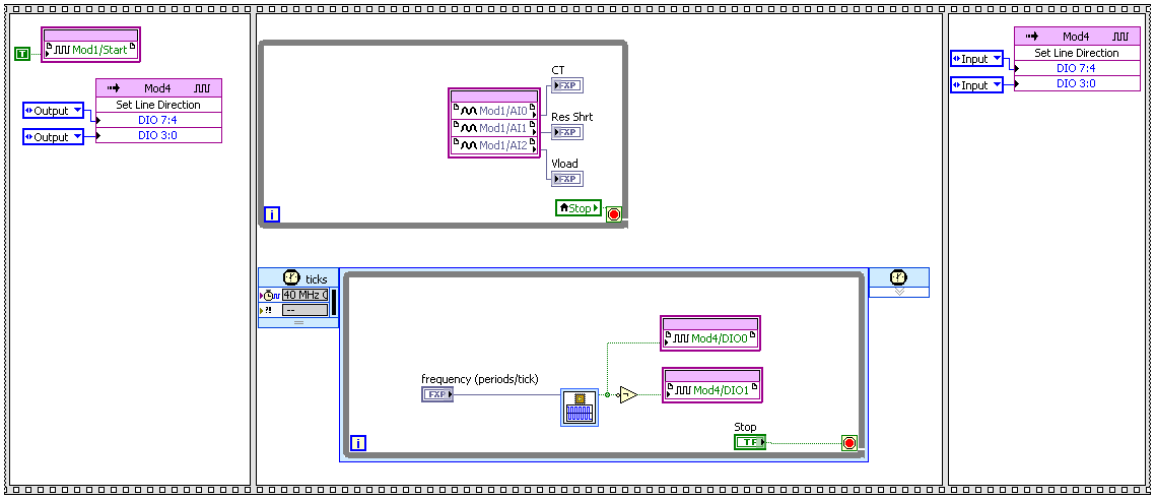


Figure H-2 FPGA mode block diagram with flat sequence logic structure, feedback sensing and PWM output

The following is the front panel of Power_Track (Host).vi. The upper and lower frequency boundaries are set by PWM_higher and PWM_lower respectively, and PWM_toggle sets the frequency when toggle would be reset. The current transformer and

resonate shorting references are CT_ref and Res_Shrt_ref respectively, CT_stop is defined to help identify ZVS condition where direction would be set as two.

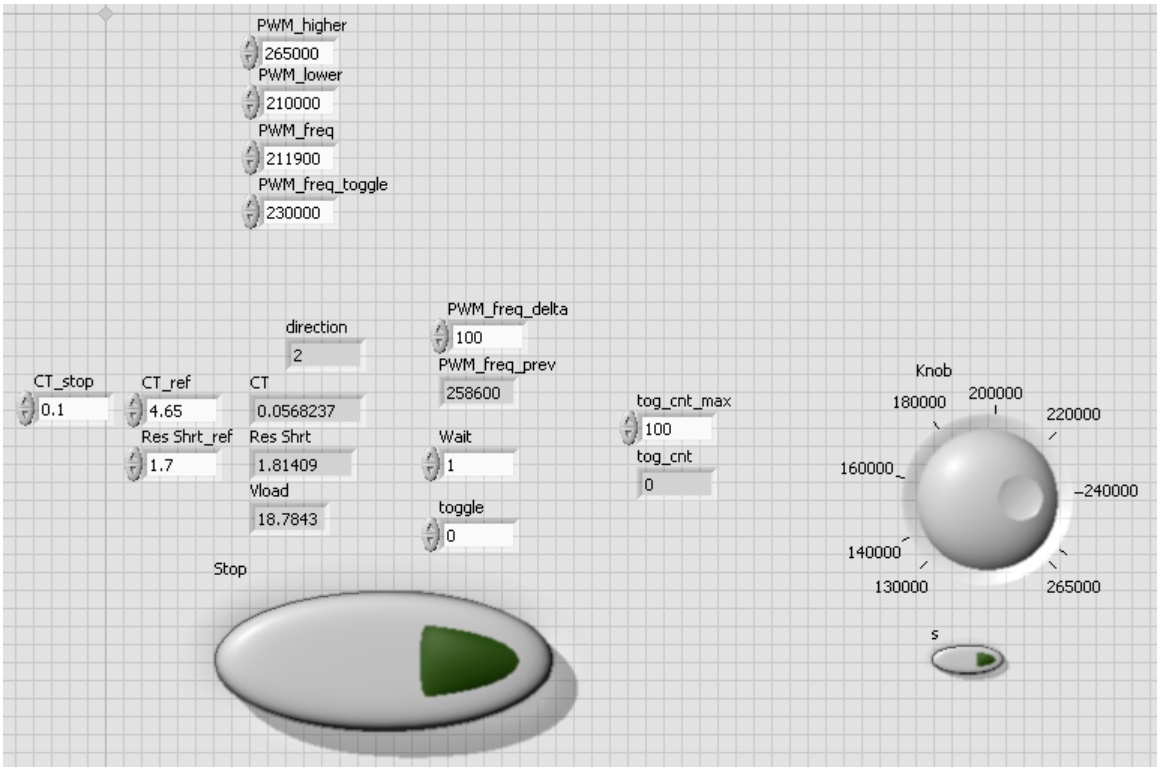


Figure H-3 Host front panel with reference setting and dynamic view of changes in system variables

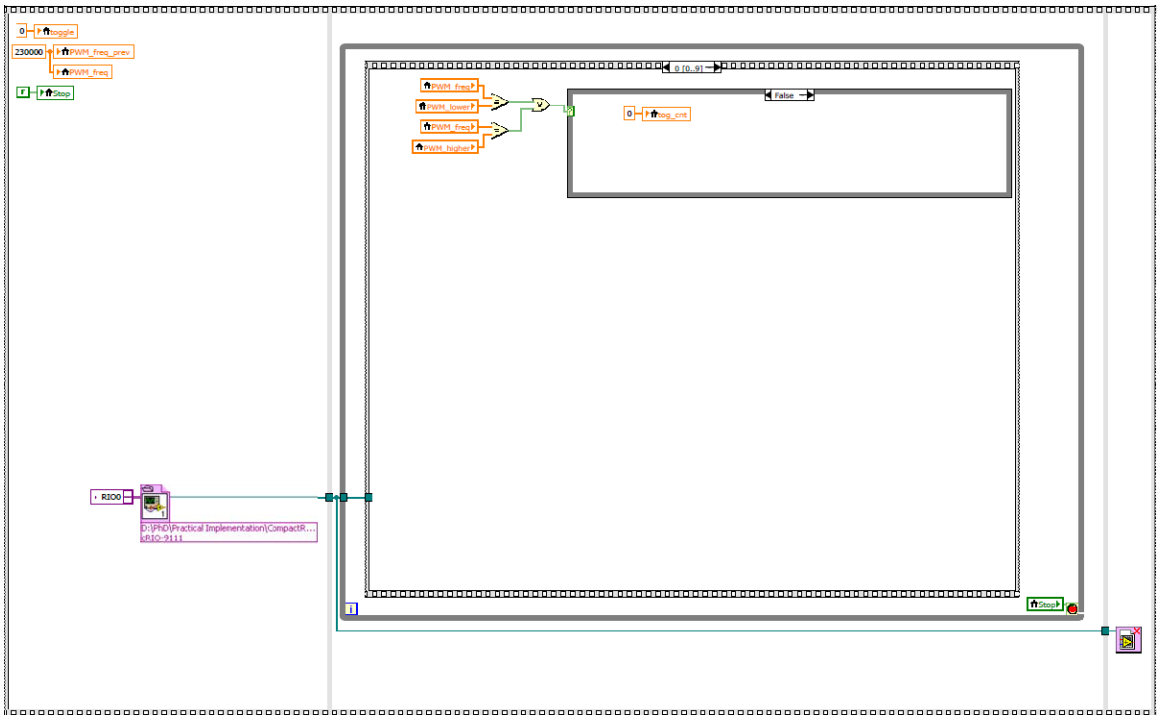


Figure H-4 Host block diagram view with stacked sequence structure within a flat sequence structure

Figure H-4 shows the block diagram view of Power_Track (Host).vi. This is a stacked sequence code placed in a flat sequence main structure. On the left hand side, several variables are initialised to a desired value; the FPGA is initialised, then the code enters the stacked sequence structure.

The following diagram shows that when the switching frequency equals the lower or the upper boundaries, the toggle count will be compared with the tog_cnt_max, if less toggle count is incremented. Otherwise the toggle count will be kept at zero (Frame 0).

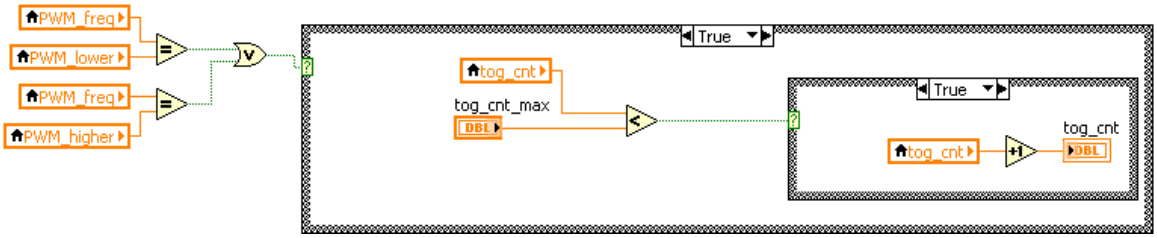


Figure H-5 Increment toggle counter when frequency is at upper or lower boundary

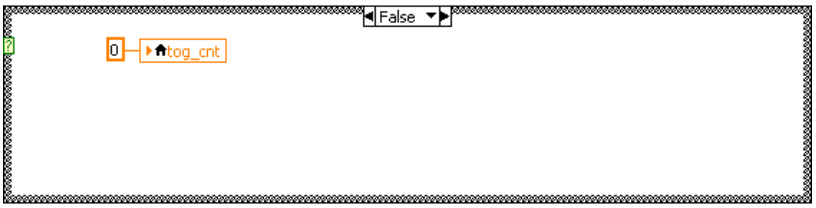


Figure H-6 Reset toggle counter when frequency is not at boundaries

The following diagram means that when toggle counter reaches maximum, toggle counter must be reset, and the toggle variable will be swapped between one and zero (Frame 1).

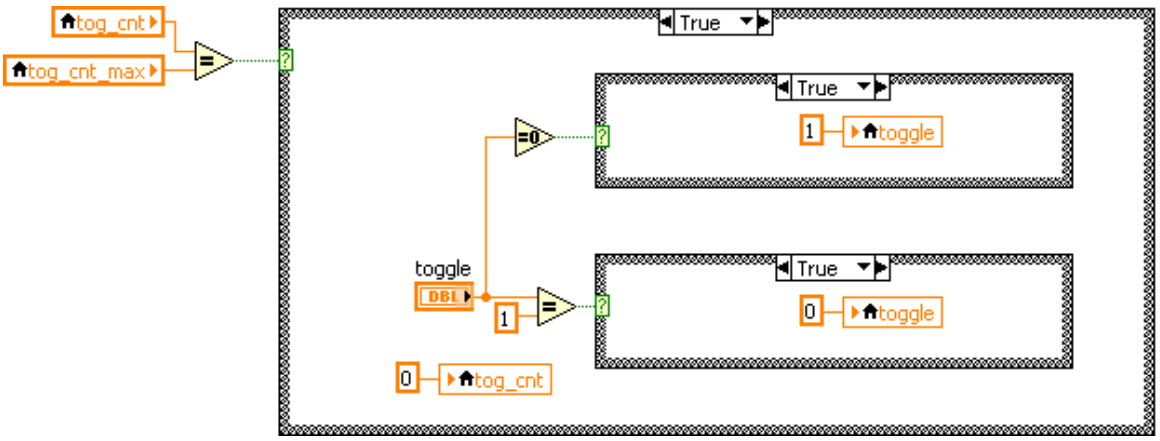


Figure H-7 Swap toggle between 1 and 0 when toggle counter reaches maximum

Figure H-8 shows that toggle must be reset when switching frequency is greater than toggle frequency and that system currently has resonant shorting period (Frame 2).

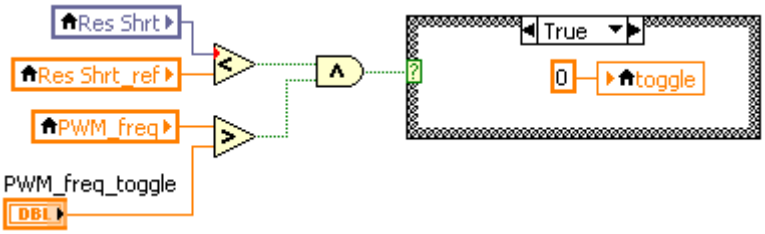


Figure H-8 Reset toggle when toggle frequency is reached in the presence of resonant shorting

The following shows that when toggle is zero, the frequency must increment when direction is one and decrement when direction is zero. However when toggle is set, increment and decrement is swapped around (Frame 3).

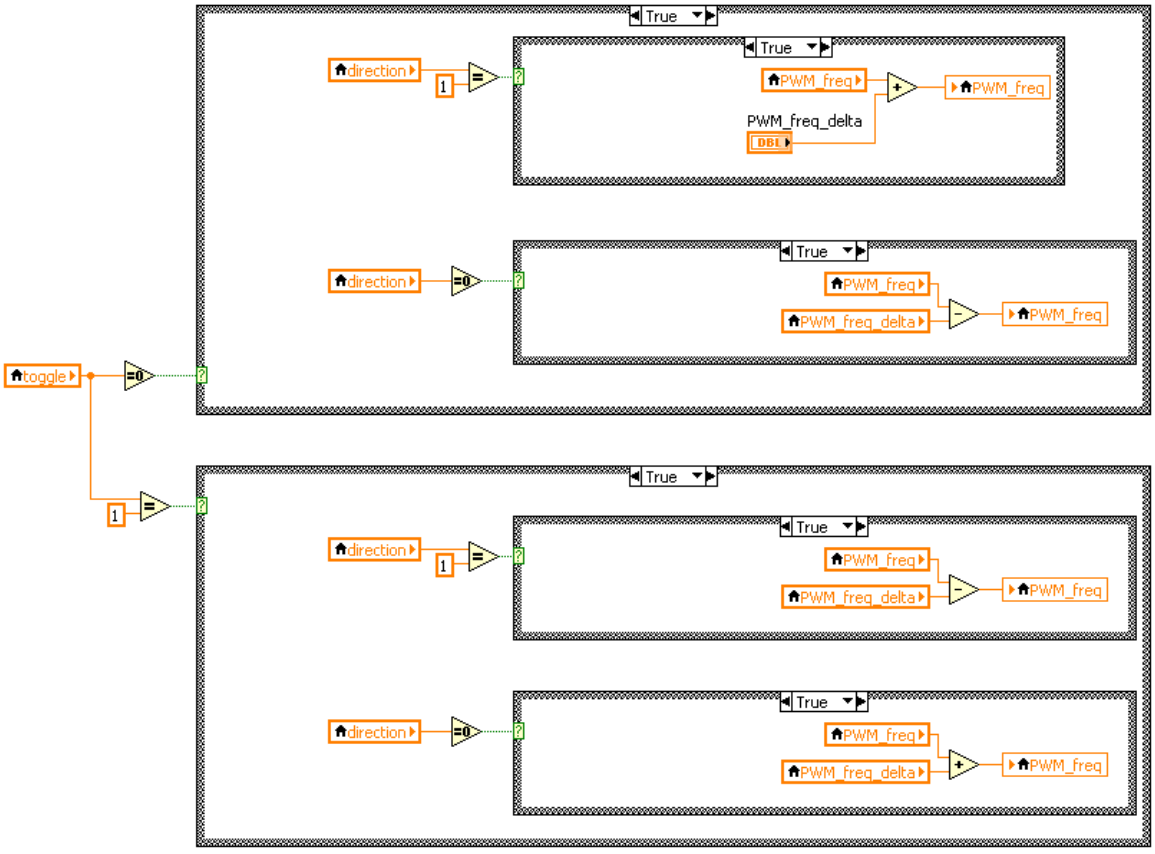


Figure H-9 Step the switching frequency according to toggle and direction

Figure H-10 shows that to attain a direction of zero, the resonant shorting and current transformer feedback must be less than their references. To attain a direction of one, the resonant shorting and the current transformer feedbacks should be greater than their references (Frame 4).

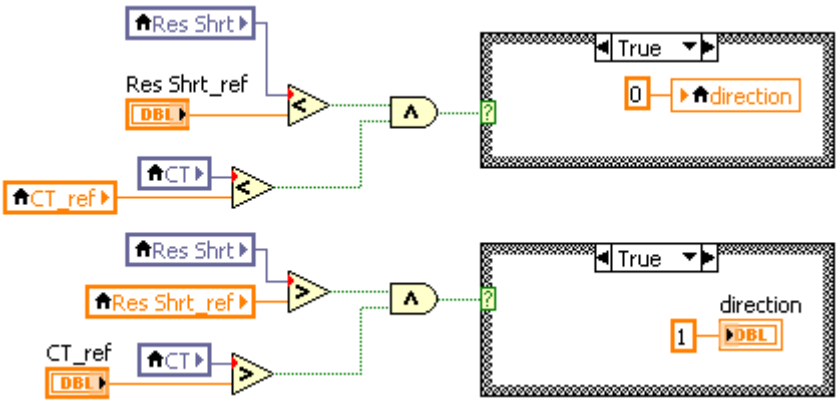


Figure H-10 Conditions required to change the value of direction to either 1 or 0

The following shows that to attain a direction of two, the CT must be less than CT_stop while Res_Shrt must be greater than Res_Shrt_ref. While direction is two, the switching frequency should remain unchanged, so the previous frequency overwrites the current (Frame 5).

Figure H-11 Conditions required to change direction to 2

The following shows that the switching frequency is bounded by an upper and lower boundary (Frame 6).

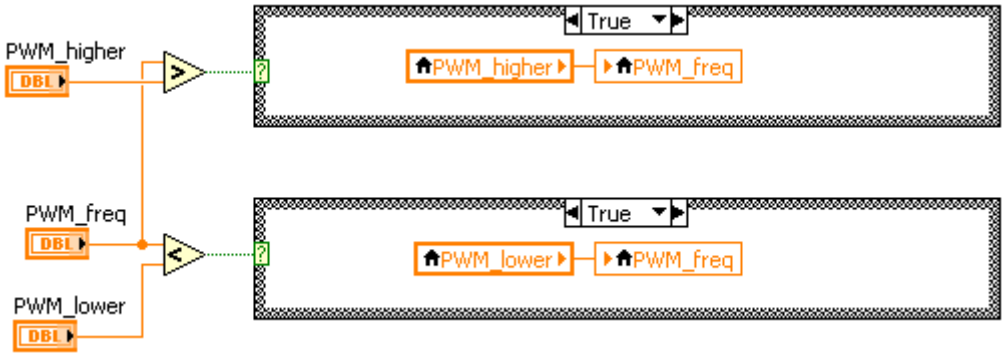


Figure H-12 Enforcing the upper and lower frequency boundaries

Figure H-13 shows that the previous frequency variable is updated with the current frequency for future reference in the next step cycle (Frame 7).

Figure H-13 Remember current frequency for future reference

The following shows a manual selection to choose between the frequency input from a manual knob or from the calculated frequency via the feedback loop. The system can be stopped by a stop button and the current transformer, and resonant shorting and load feedback information are read from the FPGA (Frame 8).

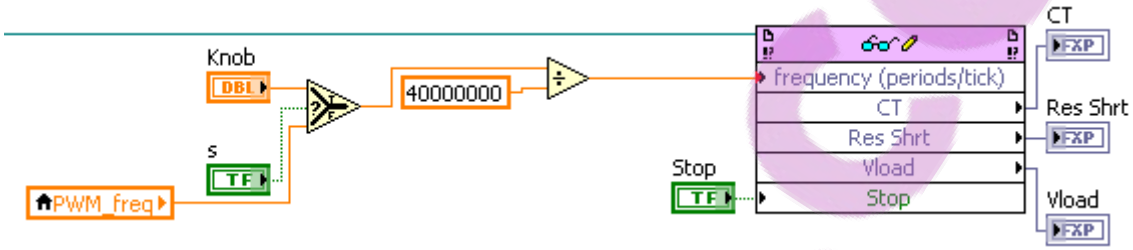


Figure H-14 Setting the frequency from calculated or a manual knob, reading feedback voltages

The following is a wait function to control how fast the code executes by introducing a variable delay (Frame 9)

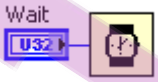


Figure H-15 Create a wait function to vary controller execution speed

Appendix I PLECS simulation for secondary power flow controller

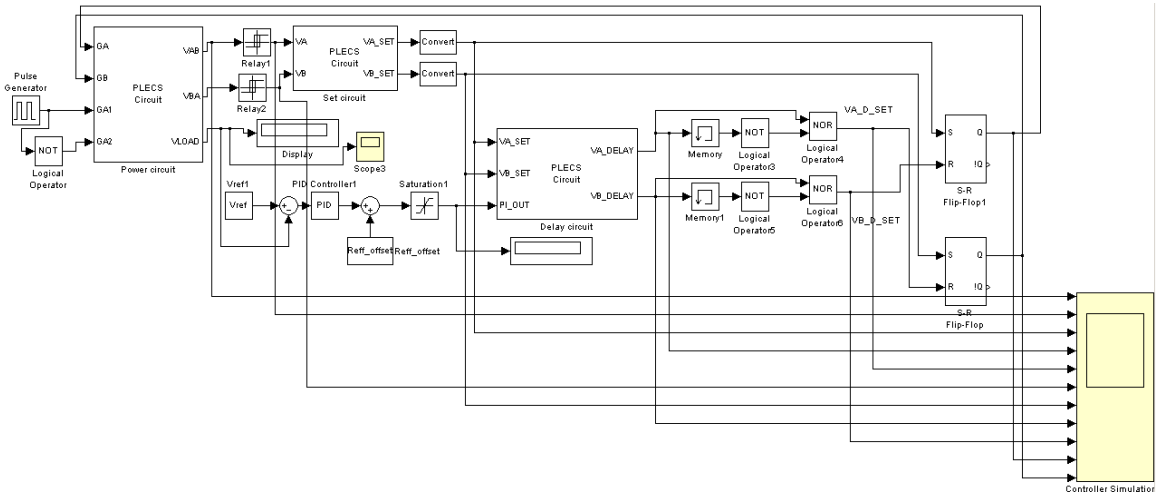


Figure I-1 PLECS schematic for secondary power flow controller

The resonant tank waveform of the above power circuit is compared to ground with a positive hysteresis. Two set signals are generated in the set circuit to set the SR flip flops, and a PI controller is used to determine the required resistance for the variable delay circuit, which outputs two pulses proportional in duration to the value of resistance. Further circuits are used to detect negative edge in the delay circuit outputs; the detected negative edge resets the SR flip flops.

The following power circuit consists of a parallel tuned current-fed push-pull primary and a parallel tuned current doubler synchronous rectifier.

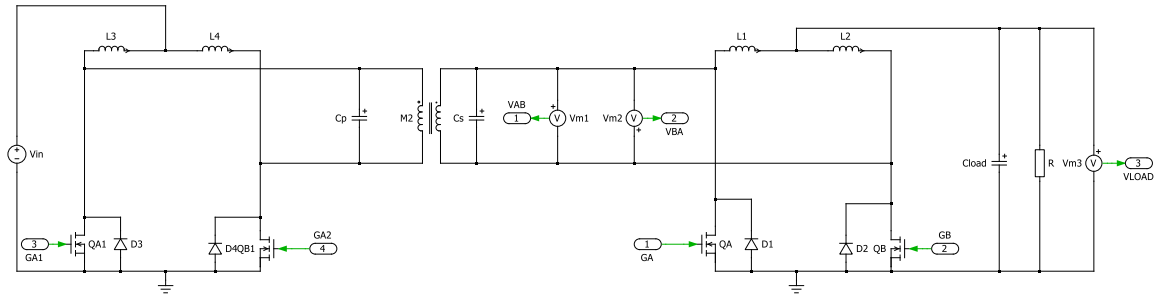


Figure I-2 PLECS primary and secondary side for power flow control

Figure I-3 shows the circuits to generate two set pulses for the two SR flip flops.

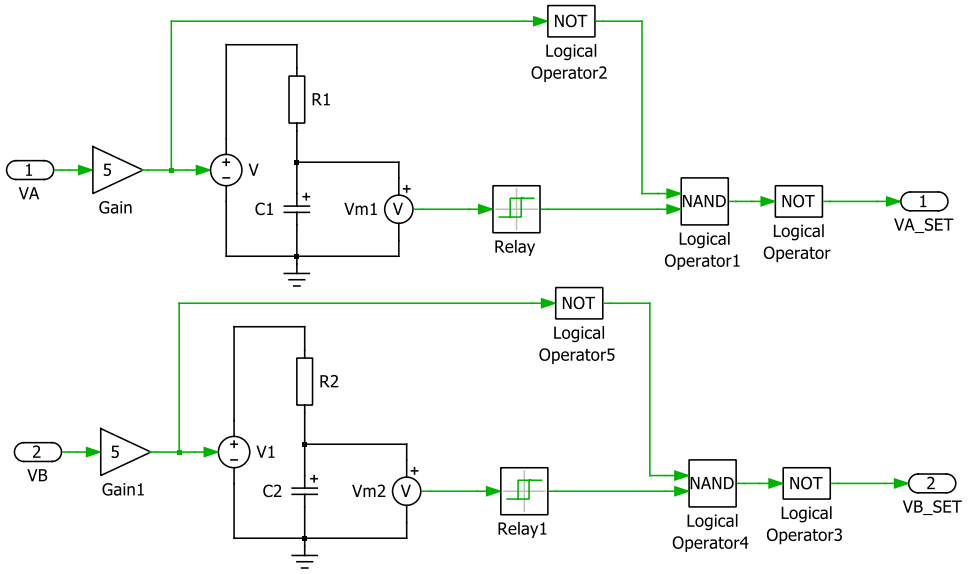


Figure I-3 Generation of two set pulses for SR flip flops

The following delay circuits generate two delay pulses with the delay duration proportional to the value of variable resistance controlled by a PI controller.

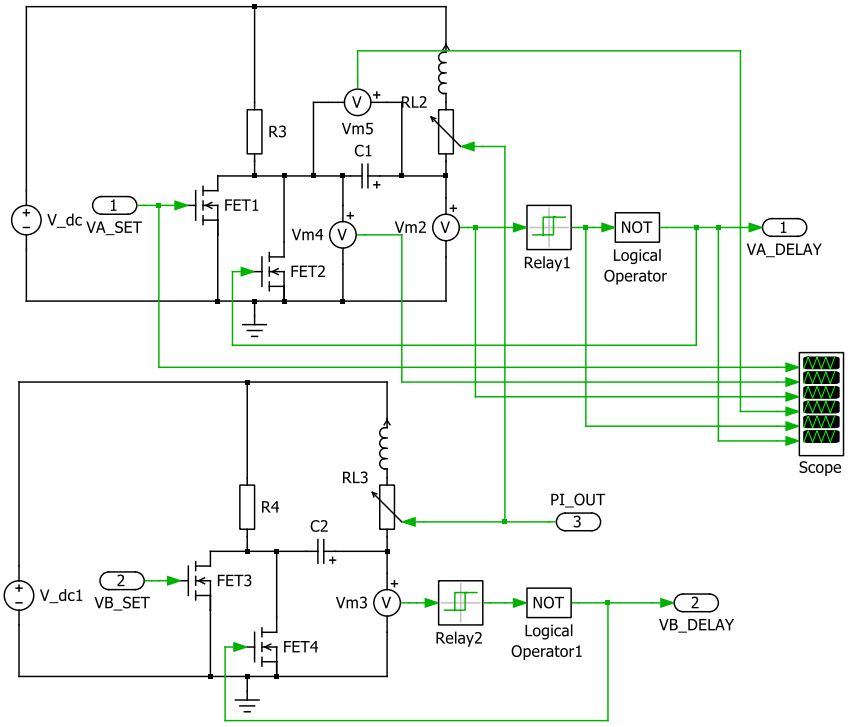


Figure I-4 PLECS circuit to generate two variable delay pulses controlled by the variable resistance

Appendix J ModelSim simulation of the secondary power flow controller logic

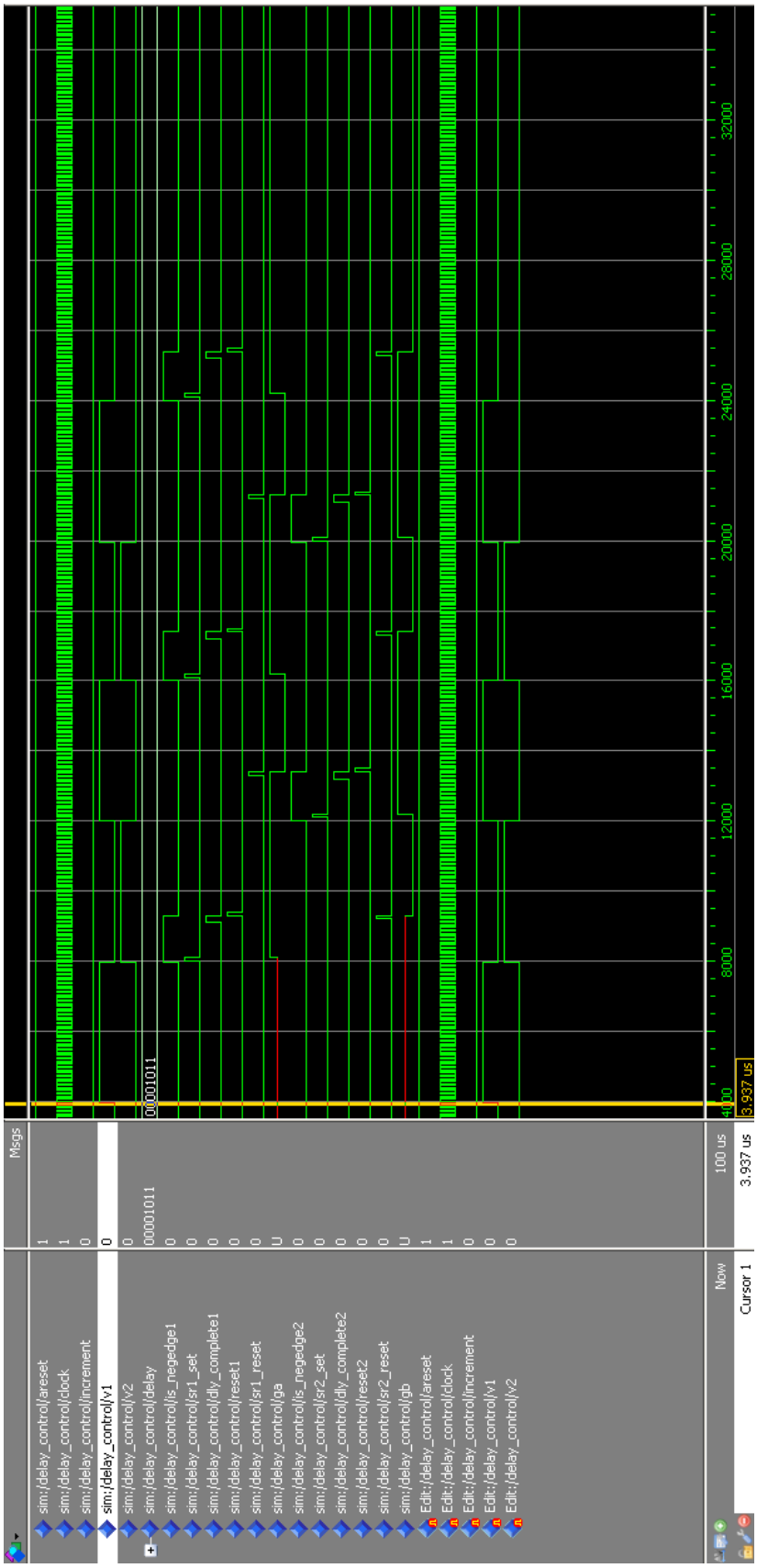


Figure J-1 Modelsim simulation of secondary power flow controller

Appendix K: VHDL programming for secondary power flow controller

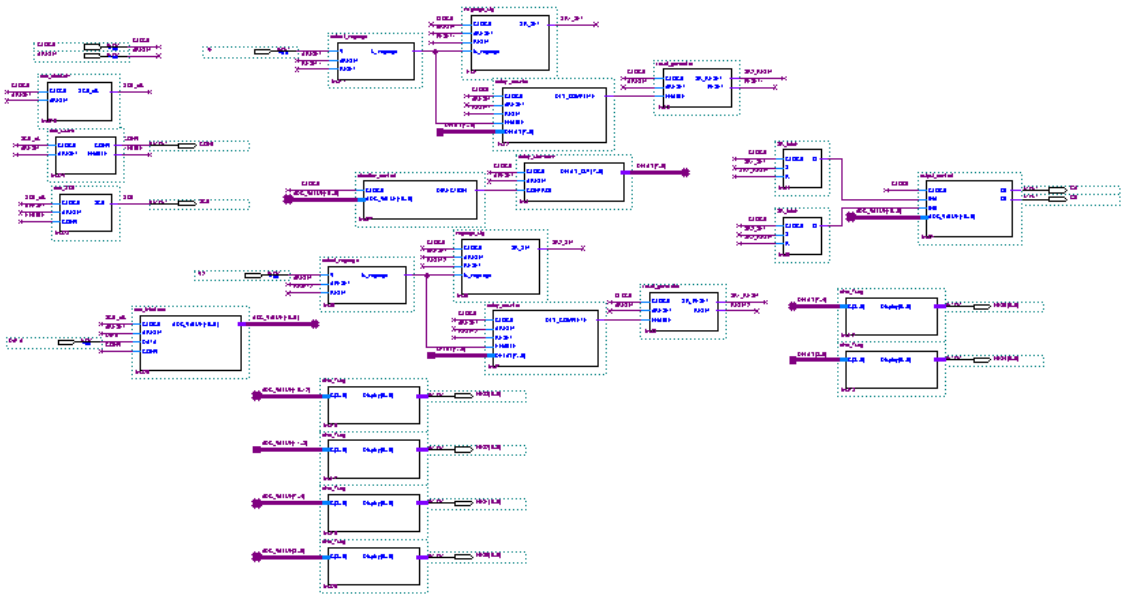


Figure K-1 Quartus II system schematic of secondary power flow controller

The adc_clockdiv symbol divides the system clock down to a slower version required for ADC conversion.

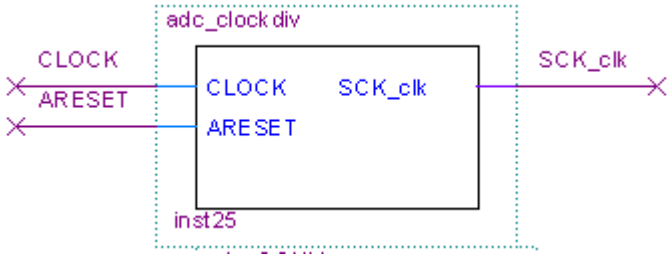


Figure K-2 Generate clock required by ADC

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;

ENTITY adc_clockdiv IS
 PORT (
        CLOCK, ARESET           : IN STD_LOGIC;
        SCK_clk                                 : OUT STD_LOGIC
 );
END adc_clockdiv;

ARCHITECTURE rtl OF adc_clockdiv IS
SIGNAL SCK_sig          :       STD_LOGIC;
BEGIN
```

```
 PROCESS(CLOCK, ARESET)
        VARIABLE i                                                    : INTEGER
RANGE 0 TO 50000 := 0;

 BEGIN
        IF (ARESET = '0') THEN
                SCK_sig <= '0';
  ELSIF (CLOCK'event AND CLOCK = '0') THEN  --Run code every falling clock edge
                IF(i = 100) THEN  -- clock dividing the FPGA clock
                        i := 0;
                        SCK_sig <= NOT(SCK_sig); -- 50% duty cycle square wave produced, bit
transmitted on falling edge, received on rising edge
                ELSE
                        i := i + 1; -- waiting time
                END IF;
        END IF;
 END PROCESS;
 SCK_clk <= SCK_sig; -- direct copy
END rtl;
```

The adc_CONV symbol generates control signals to the ADC chip to initiate ADC conversion.

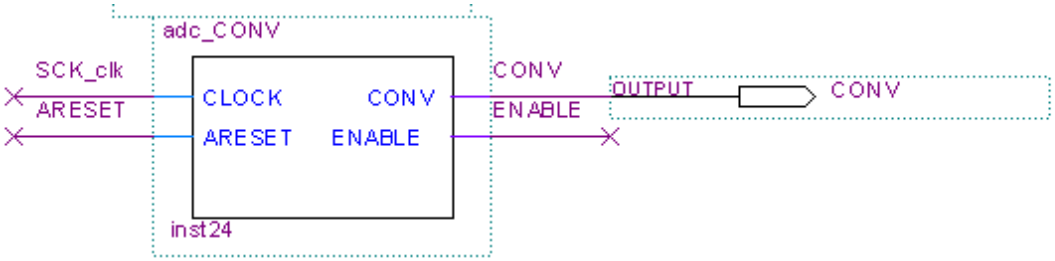


Figure K-3 Obtain signals required for communicating with the ADC chip

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;

ENTITY adc_CONV IS
 PORT (
        CLOCK, ARESET           : IN STD_LOGIC;
        CONV, ENABLE            : OUT STD_LOGIC
 );
END adc_CONV;

ARCHITECTURE rtl OF adc_CONV IS
SIGNAL CONV_sig : STD_LOGIC;
SIGNAL ENABLE_sig : STD_LOGIC;
```

```
BEGIN

 PROCESS(CLOCK, ARESET)
        VARIABLE i                                                    : INTEGER := 0;

 BEGIN
        IF (ARESET = '0') THEN
                CONV_sig <= '0';
                ENABLE_sig <= '0';
  ELSIF (CLOCK'event AND CLOCK = '0') THEN  --Run code every rising clock edge
                IF(i = 14) THEN  -- setting enable high
                        ENABLE_sig <= '1';
                        i := i + 1;
                ELSIF(i = 15) THEN --setting CONV_sig high
                        CONV_sig <= '1';
                        i := i + 1;
                ELSIF(i = 49) THEN  --setting enable to 0 one clock earlier
                        ENABLE_sig <= '0';
                        i := i + 1;
                ELSIF(i = 50) THEN -- attempting to make ON time more than OFF time
                        CONV_sig <= '0';
                        i := 0;
                ELSE
                        i := i + 1; -- keep incrementing
                END IF;
        END IF;
 END PROCESS;
 CONV <= CONV_sig; -- copy directly
 ENABLE <= ENABLE_sig; --copy direct
END rtl;
```

The adc_SCK symbol passes correct clock signals to the ADC chip with right timing specified on the component datasheet.

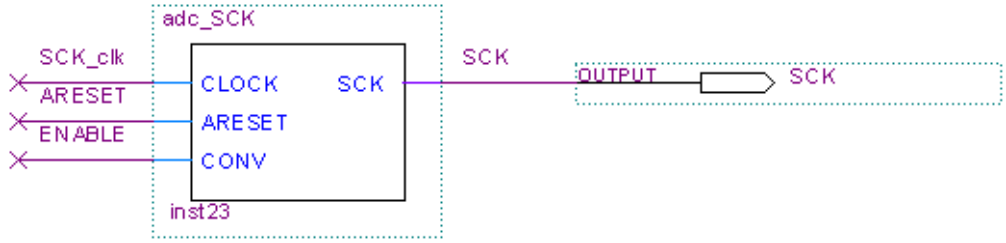


Figure K-4 Communicates the necessary clock signal during ADC conversion

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;

ENTITY adc_SCK IS
 PORT (
```

```
        CLOCK, ARESET, CONV          : IN STD_LOGIC;
        SCK                                  : OUT STD_LOGIC
 );
END adc_SCK;

ARCHITECTURE rtl OF adc_SCK IS
SIGNAL SCK_sig          :       STD_LOGIC;
BEGIN

 PROCESS(CLOCK, ARESET, CONV)

 BEGIN
        IF (ARESET = '0') THEN
                SCK_sig <= '0';
        ELSIF(CONV = '0') THEN
                SCK_sig <= CLOCK;
        ELSE
                SCK_sig <= '1';
        END IF;
 END PROCESS;
 SCK <= SCK_sig; -- direct copy
END rtl;
```

The adc_interface symbol communicates with the ADC chip and reads the 16 bits representation of the dc voltage.

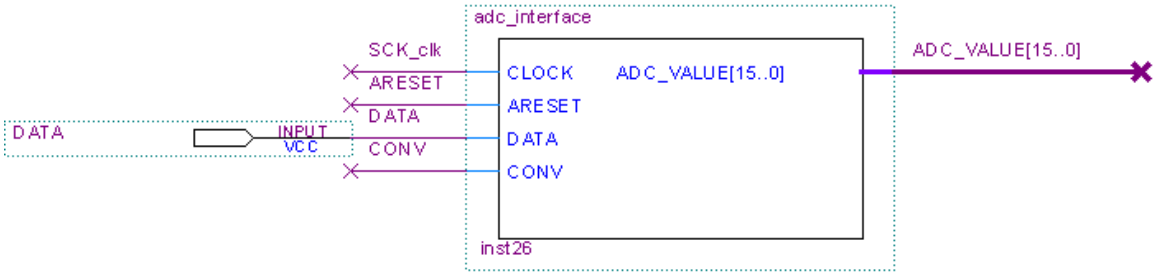


Figure K-5 Read the 16 bits of the ADC conversion

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;

ENTITY adc_interface IS
 PORT (
        CLOCK, ARESET          : IN STD_LOGIC;
        DATA                                 : IN STD_LOGIC;
        CONV                                 : IN STD_LOGIC;
```

```
        ADC_VALUE                       : OUT STD_LOGIC_VECTOR(15 DOWNTO 0)
 );
END adc_interface;

ARCHITECTURE rtl OF adc_interface IS
SIGNAL ADC_VALUE_sig            :       STD_LOGIC_VECTOR(15 DOWNTO 0);
BEGIN

 PROCESS(CLOCK, ARESET)
        VARIABLE i                                                              : INTEGER := 0;

 BEGIN
        IF (ARESET = '0') THEN
                ADC_VALUE_sig <= (OTHERS => '0');
  ELSIF (CLOCK'event AND CLOCK = '1') THEN  --Run code every rising clock edge
                IF(CONV = '0') THEN -- controlling enable
                        IF(i = 16) THEN -- bit receive complete
                                i := 0;
                        ELSE
                                ADC_VALUE_sig(15-i) <= DATA; --allocate serial bit into 16 bit
array for output
                                i := i + 1;
                        END IF;
                ELSE
                        i := 0;
                        ADC_VALUE <= ADC_VALUE_sig; --transfer adc result when reading
complete
                END IF;
        END IF;
 END PROCESS;
END rtl;
```

The direction_control symbol compares the detected load voltage with a set reference and determines the required direction to converge load voltage towards the reference.

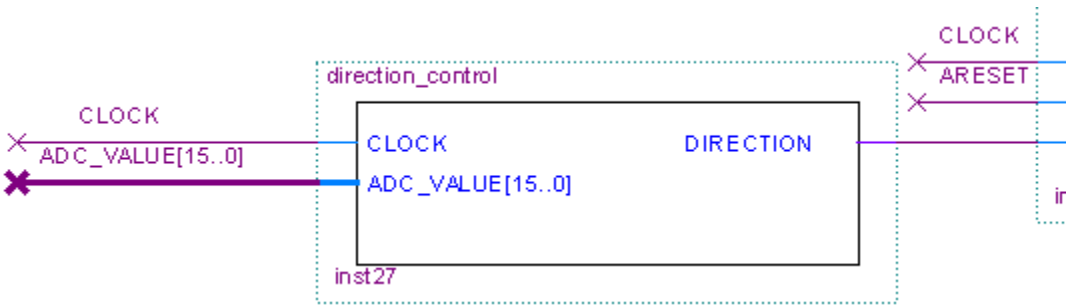


Figure K-6 Determine the value of direction to control the amount of resonant shorting for load regulation

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY direction_control IS  --SR latch to produce the gate driving signals
```

```
        PORT(   CLOCK           : IN      STD_LOGIC;
                        ADC_VALUE     : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
                        DIRECTION                       : OUT    STD_LOGIC
                );
END direction_control;

ARCHITECTURE Behavior OF direction_control IS
BEGIN
        PROCESS(CLOCK)
        BEGIN
                IF (CLOCK'event AND CLOCK = '1') THEN  --Run code every rising clock edge
                        IF(ADC_VALUE > "1011100000000000") THEN
                                DIRECTION <= '0';
                        ELSE
                                DIRECTION <= '1';
                        END IF;
                END IF;
        END PROCESS;
END Behavior;
```

The delay_slowdown symbol allows a smoother transition between adjacent delay values, which improves the resolution of change in the output voltage level.

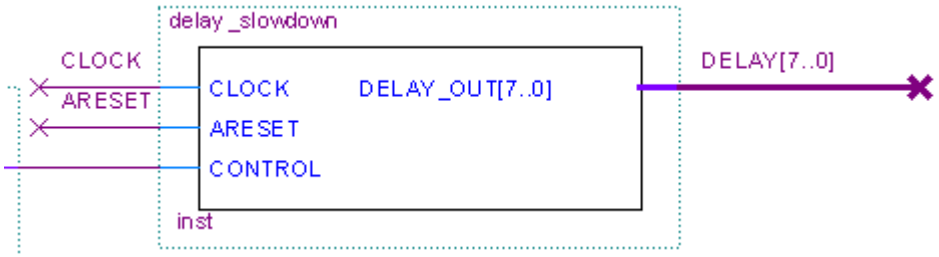


Figure K-7 Calculate the required delay value

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY delay_slowdown IS
PORT (
        CLOCK, ARESET           : IN STD_LOGIC;
        DELAY_OUT               : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
        CONTROL                 : IN STD_LOGIC
        );
END delay_slowdown;

ARCHITECTURE rtl OF delay_slowdown IS

BEGIN
PROCESS (CLOCK, ARESET, CONTROL)
        VARIABLE VALUE                  : INTEGER RANGE 0 TO 200000 := 0;
```

```
        VARIABLE VALUE_CMP          : INTEGER RANGE 0 TO 200000 := 100000;
        VARIABLE DELAY              : INTEGER RANGE 0 TO 30 := 2;
        VARIABLE DELAY_PRE          : INTEGER RANGE 0 TO 30 := 3;
        VARIABLE DELAY_TEMP         : INTEGER RANGE 0 TO 30 := 3;
BEGIN
        IF (ARESET = '0') THEN
                VALUE := 0; --Reset incrementing value
        ELSIF (CLOCK'event AND CLOCK = '1') THEN  --Run code every rising clock edge
                IF (VALUE = 200000) THEN  -- reaching max value
                        VALUE := 0;
                        IF (CONTROL = '1') THEN  -- if increasing
                                IF(VALUE_CMP < 200000) THEN -- if less than max
                                        VALUE_CMP := VALUE_CMP + 10000; -- increment
value_cmp,
                                END IF;
                                IF (DELAY < 25 AND VALUE_CMP = 200000) THEN -- if delay less
than max, value_cmp = max
                                        DELAY_PRE := DELAY;  -- delay_pre = delay
                                        DELAY := DELAY + 1;       -- increment delay
                                        VALUE_CMP := 10000;   -- preset value_cmp
                                END IF;
                        ELSIF (CONTROL = '0') THEN       -- elsif decreasing
                                IF (VALUE_CMP > 0) THEN          -- if value_cmp > 0
                                        VALUE_CMP := VALUE_CMP - 10000;      -- decrement
value_cmp
                                END IF;
                                IF (DELAY > 0 AND VALUE_CMP = 0) THEN          -- delay > 0
value_cmp = 0
                                        DELAY_PRE := DELAY;     -- delay_pre = delay
                                        DELAY := DELAY - 1;       -- decrement delay
                                        VALUE_CMP := 190000; -- preset value_cmp
                                END IF;
                        END IF;
                ELSIF (VALUE > VALUE_CMP) THEN  --When value is above its compare reference
                        IF(CONTROL = '1') THEN
                                DELAY_OUT <= STD_LOGIC_VECTOR(TO_UNSIGNED(DELAY_PRE,
8)); --Use the close loop delay value
                        ELSE
                                DELAY_OUT <= STD_LOGIC_VECTOR(TO_UNSIGNED(DELAY, 8));
                        END IF;
                                VALUE := VALUE + 1; --Increment VALUE every rising clock cycle
                ELSE
                        IF (CONTROL = '1') THEN
                                DELAY_OUT <= STD_LOGIC_VECTOR(TO_UNSIGNED(DELAY, 8));
                        ELSE
                                DELAY_OUT <= STD_LOGIC_VECTOR(TO_UNSIGNED(DELAY_PRE,
8));
                        END IF;
                                VALUE := VALUE + 1; --Increment VALUE every rising clock cycle
                END IF;
```

```
                IF (CONTROL = '1' AND DELAY_PRE > DELAY) THEN -- Swap delay_pre and delay
when direction changes
                        DELAY_TEMP := DELAY_PRE;
                        DELAY_PRE := DELAY;
                        DELAY := DELAY_TEMP;
                ELSIF (CONTROL = '0' AND DELAY_PRE < DELAY) THEN
                        DELAY_TEMP := DELAY_PRE;
                        DELAY_PRE := DELAY;
                        DELAY := DELAY_TEMP;
                END IF;
        END IF;
END PROCESS;
END rtl;
```

The detect_negedge symbol outputs a high after detecting a negative edge at its input. Two instances of this symbol are used to detect the negative edge in V_A and V_B respectively.

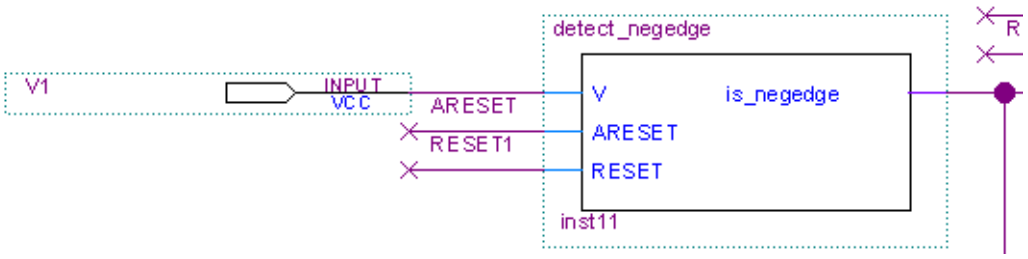


Figure K-8 Detect for negative edges in the input

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY detect_negedge IS
 PORT (
                V, ARESET, RESET : IN STD_LOGIC;
                is_negedge : OUT STD_LOGIC
 );
END detect_negedge;

ARCHITECTURE rtl OF detect_negedge IS
BEGIN
 PROCESS(V, ARESET, RESET)
        BEGIN
                IF(ARESET = '0' OR RESET = '1') THEN
                        is_negedge <= '0';
                ELSIF (V'event AND V = '0') THEN
                        is_negedge <= '1';
                END IF;
        END PROCESS;
END rtl;
```

The negedge_sig symbol is used to generate a pulse to trigger an SR flip flop. Two instances of this symbol are used to generate V_{A_SET} and V_{B_SET} pulses to set two different SR flip flops to generate gate drive signals G_A and G_B respectively.

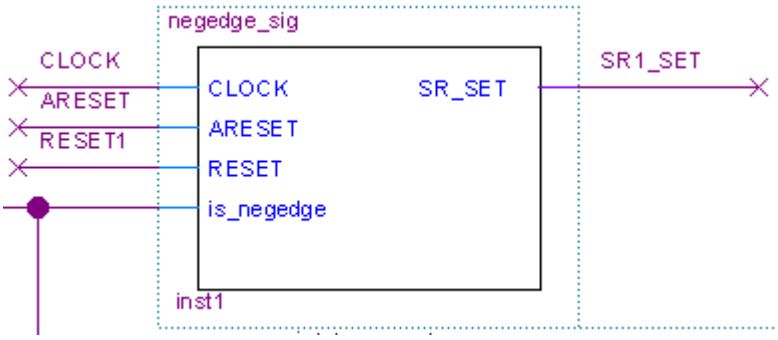


Figure K-9 Produce negative edge trigger for setting an SR flip flop

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY negedge_sig IS
 PORT (
                CLOCK, ARESET, RESET : IN STD_LOGIC;
                is_negedge : IN STD_LOGIC;
                SR_SET : OUT STD_LOGIC
 );
END negedge_sig;

ARCHITECTURE rtl OF negedge_sig IS
SIGNAL done_sig : STD_LOGIC;  --feedback signals
BEGIN
 PROCESS(CLOCK, ARESET, RESET)
        BEGIN
                IF(ARESET = '0' OR RESET = '1') THEN
                        SR_SET <= '0';
                        done_sig <= '0';
                ELSIF (CLOCK'event AND CLOCK = '1') THEN
                        IF (is_negedge = '1' AND done_sig = '0') THEN
                                SR_SET <= '1';
                                done_sig <= '1';
                        ELSE
                                SR_SET <= '0';
                        END IF;
                END IF;
        END PROCESS;
END rtl;
```

The delay_counter symbol counts up to the delay value specified at its input and then generate a high on count completion. Two separate instances of this symbol are used to count V_{A_DELAY} and V_{B_DELAY}.

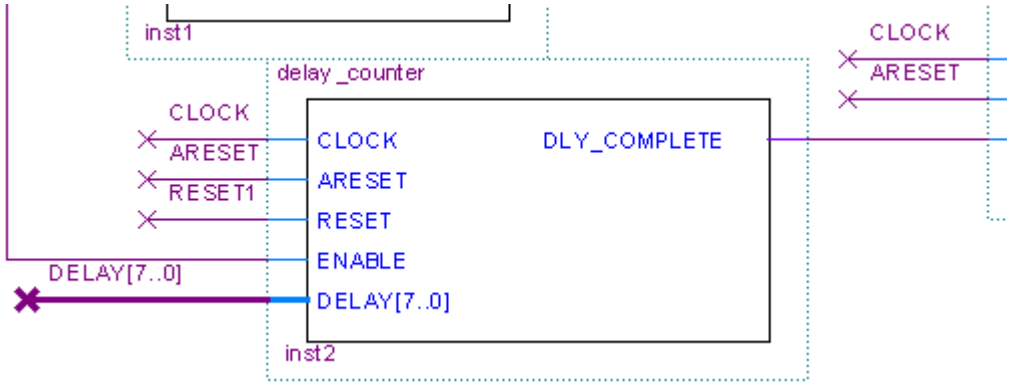


Figure K-10 Count for the duration set by the delay input

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;

ENTITY delay_counter IS
 PORT (
        CLOCK, ARESET, RESET                    : IN STD_LOGIC;
        ENABLE                          : IN STD_LOGIC;
        DELAY                                   : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
        DLY_COMPLETE: OUT STD_LOGIC
 );
END delay_counter;

ARCHITECTURE rtl OF delay_counter IS
        SIGNAL VALUE                                                    :
STD_LOGIC_VECTOR(7 DOWNTO 0) := (OTHERS => '0');
        SIGNAL DLY_COMPLETE_sig                                         : STD_LOGIC;
BEGIN
 PROCESS(CLOCK, ARESET, RESET)
 BEGIN
        IF (ARESET = '0' OR RESET = '1') THEN
                VALUE <= (OTHERS => '0'); --Reset incrementing value
                DLY_COMPLETE_sig <= '0'; --Signal complete to FSM
        ELSIF (CLOCK'event AND CLOCK = '1') THEN  --Run code every rising clock edge
                IF (ENABLE = '1') THEN --When instruction to start delay counter
                        IF (VALUE = DELAY) THEN  --When incrementing value equals to desired
delay duration
                                VALUE <= (OTHERS => '0'); --Reset incrementing value
                                DLY_COMPLETE_sig <= '1';
                        ELSIF (DLY_COMPLETE_sig = '0') THEN --Else if delay duration has not
been reached
                                VALUE <= VALUE + 1; --Increment VALUE every rising clock cycle
                        END IF;
                END IF;
   END IF;
 END PROCESS;
 DLY_COMPLETE <= DLY_COMPLETE_sig;
```

```
END rtl;
```

The reset_generator generates a pulse to reset a SR flip flop and then another pulse to reset all preceding symbols to restart negative edge triggering and delay value counting. Two instances of this symbol are used to generate $V_{A\_D\_SET}$ and $V_{B\_D\_SET}$ pulses to reset two SR flip flops to generate gate drive signals G_B and G_A respectively.

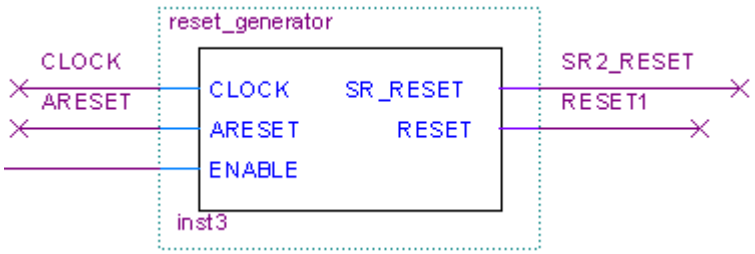


Figure K-11 Generate reset signal for SR flip flop

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY reset_generator IS
 PORT (
                CLOCK, ARESET : IN STD_LOGIC;
                ENABLE : IN STD_LOGIC;
                SR_RESET : OUT STD_LOGIC;
                RESET : OUT STD_LOGIC
 );
END reset_generator;

ARCHITECTURE rtl OF reset_generator IS
SIGNAL done_sig : STD_LOGIC;  --feedback signals
BEGIN
 PROCESS(CLOCK, ARESET)
        BEGIN
                IF(ARESET = '0') THEN
                        SR_RESET <= '0';
                        done_sig <= '0';
                ELSIF (CLOCK'event AND CLOCK = '1') THEN
                        IF (ENABLE = '1' AND done_sig = '0') THEN
                                SR_RESET <= '1';
                                done_sig <= '1';
                        ELSIF (ENABLE = '1' AND done_sig = '1') THEN
                                SR_RESET <= '0';
                                RESET <= '1';
                        ELSE
                                SR_RESET <= '0';
                                RESET <= '0';
                                done_sig <= '0';
                        END IF;
                END IF;
```

```
        END PROCESS;
END rtl;
```

The SR_latch symbol is an SR flip flop to store the correct states after setting and resetting trigger pulses. Two instances of this symbol are used to generate gate drive signals GA and GB.

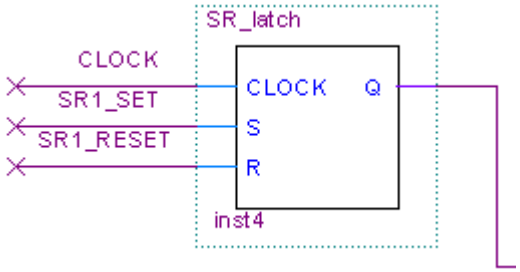


Figure K-12 SR flip flop

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY SR_latch IS  --SR latch to produce the gate driving signals
        PORT(   CLOCK, S, R             : IN    STD_LOGIC;
                        Q                       : OUT   STD_LOGIC
                );
END SR_latch;

ARCHITECTURE Behavior OF SR_latch IS
BEGIN
        PROCESS(CLOCK)
        BEGIN
                IF (CLOCK'event AND CLOCK = '1') THEN  --Run code every rising clock edge
                        IF(R = '1') THEN
                                Q <= '0';
                        ELSIF (S = '1') THEN
                                Q <= '1';
                        END IF;
                END IF;
        END PROCESS;
END Behavior;
```

The output_control symbol starts power flow control after a set load voltage reference has been reached. At start-up before reaching the reference level, passive diodes operate to build up the load voltage to power up the control circuitry.

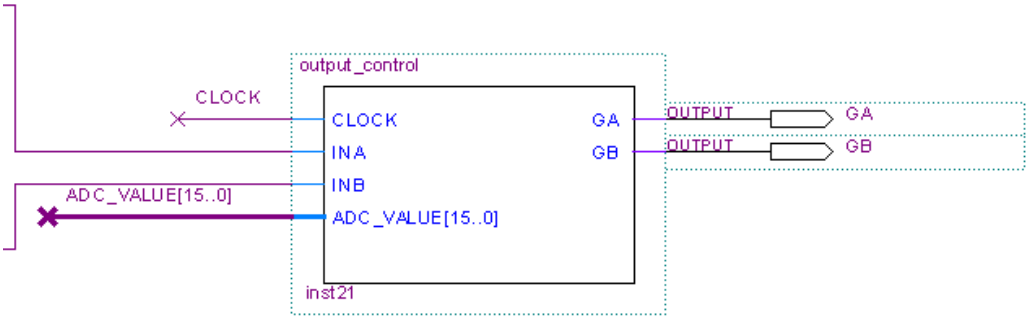


Figure K-13 Turn on gate signals after load voltage exceeds a threshold

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY output_control IS  --SR latch to produce the gate driving signals
        PORT(   CLOCK, INA, INB         : IN      STD_LOGIC;
                        ADC_VALUE       : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
                        GA, GB                  : OUT    STD_LOGIC
                );
END output_control;

ARCHITECTURE Behavior OF output_control IS
BEGIN
        PROCESS(CLOCK)
        BEGIN
                IF (CLOCK'event AND CLOCK = '1') THEN  --Run code every rising clock edge
                        IF(ADC_VALUE > "1001000000000000") THEN
                                GA <= INA;
                                GB <= INB;
                        ELSE
                                GA <= '0';
                                GB <= '0';
                        END IF;
                END IF;
        END PROCESS;
END Behavior;
```

The char_7seg symbol is used to display bits visually through 7-segment displays on the Altera DE2 board. Each instance of the symbol can display the hexadecimals 0_{hex} to F_{hex} on one 7-segment display.

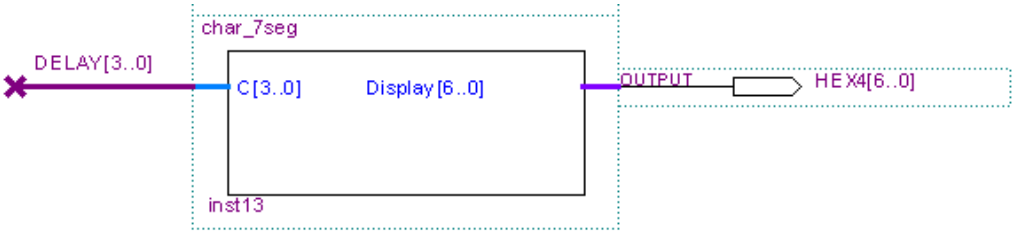


Figure K-14 Controls one 7-segment display

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY char_7seg IS
   PORT (  C : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
         Display : OUT STD_LOGIC_VECTOR(6 DOWNTO 0) );
END char_7seg;
ARCHITECTURE Behavior OF char_7seg IS
BEGIN
          PROCESS (C)
          BEGIN
    CASE C IS          --
                    WHEN "0000"    =>  Display <= "1000000";
                    WHEN "0001"    =>  Display <= "1111001";
                    WHEN "0010"    =>  Display <= "0100100";
                    WHEN "0011"    =>  Display <= "0110000";
                    WHEN "0100"    =>  Display <= "0011001";
                    WHEN "0101"    =>  Display <= "0010010";
                    WHEN "0110"    =>  Display <= "0000010";
                    WHEN "0111"    =>  Display <= "1111000";
                    WHEN "1000"    =>  Display <= "0000000";
                    WHEN "1001"    =>  Display <= "0010000";
                    WHEN "1010"    =>  Display <= "0001000";
                    WHEN "1011"    =>  Display <= "0000011";
                    WHEN "1100"    =>  Display <= "1000110";
                    WHEN "1101"    =>  Display <= "0100001";
                    WHEN "1110"    =>  Display <= "0000110";
                    WHEN "1111"    =>  Display <= "0001110";
                    WHEN OTHERS    =>  Display <= "0000000";
    END CASE;
  END PROCESS;
END Behavior
```

References

[1] E. A. Rose, A. C. Gelijns, A. J. Moskowitz, D. F. Heitjan, L. W. Stevenson, W. Dembitsky, *et al.*, "Long-Term Use of a Left Ventricular Assist Device for End-Stage Heart Failure," *New England Journal of Medicine*, vol. 345, pp. 1435-1443, 2001.

[2] Organ Donation Facts. (2013, 11 Feb). *For 2012, 12 Facts About Donation* [Article]. Available: http://www.donatelifeny.org/about-donation/quick-facts-about-donation/

[3] K. M. Zareba, "The artificial heart-past, present, and future," *Medical Science Monitor*, vol. 8, 2002.

[4] ISHLT. (2013, 5 Feb). *Overall Heart and Adult Heart Transplantation Statistics* [PowerPoint]. Available: http://www.ishlt.org/downloadables/slides/2011/heart_adult.ppt

[5] W. L. Holman, S. J. Park, J. W. Long, A. Weinberg, L. Gupta, A. R. Tierney, *et al.*, "Infection in permanent circulatory support: Experience from the REMATCH trial," *The Journal of Heart and Lung Transplantation*, vol. 23, pp. 1359-1365, 2004.

[6] Wikipedia. (2013, 5 Feb). *Ventricular assist device* [Article]. Available: http://en.wikipedia.org/wiki/Ventricular_assist_device

[7] R. J. Gordon, B. Quagliarello, and F. D. Lowy, "Ventricular assist device-related infections," *The Lancet Infectious Diseases*, vol. 6, pp. 426-437, 2006.

[8] H. Hoshi, T. Shinshi, and S. Takatani, "Third-generation Blood Pumps With Mechanical Noncontact Magnetic Bearings," *Artificial Organs*, vol. 30, pp. 324-338, 2006.

[9] R. Hetzer, Y. Weng, E. V. Potapov, M. Pasic, T. Drews, M. Jurmann, *et al.*, "First experiences with a novel magnetically suspended axial flow left ventricular assist device," *European Journal of Cardio-Thoracic Surgery*, vol. 25, pp. 964-970, June 1, 2004.

[10] E. Hennig and R. Hetzer, "Mechanical heart support at the Deutsches Herzzentrum Berlin: Recent developments (2011)," *Xenotransplantation*, vol. 19, pp. 11-11, 2012.

[11] J. L. Selekof and M. Lindsay. (2009). *Left Ventricular Assist Devices: An Innovative Approach to Decrease Infections Using a Silver Contact Dressing*. Available: http://silverlon.com/wp-content/uploads/2012/05/U_of_MD_VLAD_Poster_3_27_09_1.pdf

[12] Thoratec. *HeartMate II Left Ventricular Assist System*. Available: http://www.thoratec.com/medical-professionals/vad-product-information/heartmate-ll-lvad.aspx

[13] O. H. Frazier, T. J. Myers, R. K. Jarvik, S. Westaby, D. W. Pigott, I. D. Gregoric, *et al.*, "Research and development of an implantable, axial-flow left ventricular assist device: the Jarvik 2000 Heart," *Ann Thorac Surg*, vol. 71, pp. S125-132, March 1, 2001.

[14] Worldheart Corporation. (2013, 5 Feb). MiFlow™ VAD. [pdf]. Available: http://www.worldheart.com/documents/MIFLOW%20Product%20Profile_100511.pdf

[15] MicroMed Cardiovascular. (2013, 11 Feb). *HeartAssist 5* [Article]. Available: http://www.micromedcv.com/eu/index.php/Advanced-Design/meet-heartassist-5-the-next-generation-lvad.html

[16] B. Heart. *INCOR - The Left Ventricular Assist Device*. Available: http://www.berlinheart.de/index.php/patienten/content/patients_products/patients_products_incor

[17] HeartWare International Inc. (2013, 5 Feb). *HeartWare® Ventricular Assist System*. Available: http://www.heartware.com.au/IRM/content/international/products_HVAD.html

[18] W. Holman, J. Kirklin, D. Naftel, R. Kormos, P. Desvign-Nickens, and A. D Camacho M. (2013, 11 Feb). *Early Infection After MCSD Implant: Incidence, Location, and Outcome* [PowerPoint]. Available: https://www.google.co.nz/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&ved=0CDIQFjAA&url=http%3A%2F%2Fwww.uab.edu%2Fctsresearch%2Fintermacs%2FDocument%2520Library%2FHolman%2C%2520Early%2520Infection%2520After%2520MCSD%2520Implant%2C%2520Final.ppt&ei=0pgYUZ_YFYH9igLm3IHYDg&usg=AFQjCNGxcrnpsVMD0catcd2yXhRy_gtzPg&sig2=QlpfXeMIxmp6pHUeNsk0iA&bvm=bv.42080656,d.cGE

[19] R. A. Vilchez, M. C. McEllistrem, L. H. Harrison, K. R. McCurry, R. L. Kormos, and S. Kusne, "Relapsing bacteremia in patients with ventricular assist device: an emergent complication of extended circulatory support," *Ann Thorac Surg*, vol. 72, pp. 96-101, July 1, 2001.

[20] A. Zierer, S. J. Melby, R. K. Voeller, T. J. Guthrie, G. A. Ewald, K. Shelton, *et al.*, "Late-Onset Driveline Infections: The Achilles' Heel of Prolonged Left Ventricular Assist Device Support," *The Annals of Thoracic Surgery*, vol. 84, pp. 515-520, 2007.

[21] W. Holman, J. Kirklin, D. Naftel, R. Kormos, P. Desvign-Nickens, M. Camacho, *et al.*, "Infection after implantation of pulsatile mechanical circulatory support devices," *Thorac Cardiovasc Surg.*, vol. 139, pp. 1632-1636, 2010.

[22] L. Chao, A. P. Hu, and M. Budhia, "A generalized coupling model for Capacitive Power Transfer systems," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 274-279.

[23] L. Chao, A. P. Hu, B. Wang, and N. C. Nair, "A Capacitively Coupled Contactless Matrix Charging Platform With Soft Switched Transformer Control," *Industrial Electronics, IEEE Transactions on*, vol. 60, pp. 249-260, 2013.

[24] M. Budhia, G. Covic, and J. Boys, "A new IPT magnetic coupler for electric vehicle charging systems," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 2487-2492.

[25] Z. Wei, W. Siu-Chung, C. K. Tse, and C. Qianhong, "A study of sectional tracks in roadway inductive power transfer system," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 822-826.

[26] S. Mohagheghi, B. Parkhideh, and S. Bhattacharya, "Inductive power transfer for electric vehicles: Potential benefits for the distribution grid," in *Electric Vehicle Conference (IEVC), 2012 IEEE International*, 2012, pp. 1-8.

[27] A. P. Hu, *Wireless/Contactless Power Supply –Inductively coupled resonant converter solutions*. Germany: VDM Verlag Dr Mueller, 2009.

[28] A. W. Green and J. T. Boys, "10 kHz inductively coupled power transfer-concept and control," in *Power Electronics and Variable-Speed Drives, 1994. Fifth International Conference on*, 1994, pp. 694-699.

[29] R. Bansal, "The Future of Wireless Charging [AP-S Turnstile]," *Antennas and Propagation Magazine, IEEE*, vol. 51, pp. 153-153, 2009.

[30] A. E. Umenei, J. Schwannecke, S. Velpula, and D. Baarman, "Novel Method for Selective Nonlinear Flux Guide Switching for Contactless Inductive Power Transfer," *Magnetics, IEEE Transactions on*, vol. 48, pp. 2192-2195, 2012.

[31] L. D. Paulson, "New Technique Provides Energy Wirelessly," *IEEE Computer Society*, vol. 43, 2010.

[32] D. McCormick, A. P. Hu, P. D. Nielsen, S. Malpas, and D. Budgett, "Powering Implantable Telemetry Devices from Localized Magnetic Fields," in *Engineering in Medicine and Biology Society, 2007. EMBS 2007. 29th Annual International Conference of the IEEE*, 2007, pp. 2331-2335.

[33] D. Russell, D. McCormick, A. Taberner, P. Nielsen, P. Hu, D. Budgett, *et al.*, "Wireless power delivery system for mouse telemeter," in *Biomedical Circuits and Systems Conference, 2009. BioCAS 2009. IEEE*, 2009, pp. 273-276.

[34] T. D. Dissanayake, A. P. Hu, S. Malpas, L. Bennet, A. Taberner, L. Booth, *et al.*, "Experimental Study of a TET System for Implantable Biomedical Devices," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 3, pp. 370-378, 2009.

[35] P. Si, A. P. Hu, S. Malpas, and D. Budgett, "A Frequency Control Method for Regulating Wireless Power to Implantable Devices," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 2, pp. 22-29, 2008.

[36] X. Wei and J. Liu, "Power sources and electrical recharging strategies for implantable medical devices," *Frontiers of Energy and Power Engineering in China*, vol. 2, pp. 1-13, March 1, 2008.

[37] A. Danilov, G. Itkin, and S. Selishchev, "Progress in Methods for Transcutaneous Wireless Energy Supply to Implanted Ventricular Assist Devices," *Biomedical Engineering*, vol. 44, pp. 125-129, 2010.

[38] A. Berson, "Magnetic control and powering of surgically implanted instrumentation," *Magnetics, IEEE Transactions on*, vol. 19, pp. 2157-2161, 1983.

[39] PR Newswire Association LLC. (2013, Feb 12). *Thoratec Announces Development Agreement With WiTricity for Proprietary Energy Transfer Technology* [Article]. Available: http://www.prnewswire.com/news-releases/thoratec-announces-development-agreement-with-witricity-for-proprietary-energy-transfer-technology-121590778.html

[40] HeartWare International Inc. (2013, 5 Feb). *HeartWare and Dualis MedTech Announce Agreement to Develop Fully Implantable Ventricular Assist System* [Article]. Available: http://ir.heartware.com/phoenix.zhtml?c=187755&p=irol-newsArticle&id=1646139

[41] The Arrow LionHeart™ Left Ventricular Assist System (LVAS). (2013, 5 Feb). *LION HEART™* [Article]. Available: http://www.pennstatehershey.org/web/lionheart/home/technicalinfo#

[42] S. M. Mehta, W. E. Pae Jr, G. Rosenberg, A. J. Snyder, W. J. Weiss, J. P. Lewis, *et al.*, "The LionHeart LVD-2000: a completely implanted left ventricular assist device for chronic circulatory support," *The Annals of Thoracic Surgery*, vol. 71, pp. S156-S161, 2001.

[43] ABIOMED INC. (2013, 5 Feb). *AbioCor* [Article]. Available: http://www.abiomed.com/products/heart-replacement/

[44] R. D. Dowling, L. A. Gray Jr, S. W. Etoch, H. Laks, D. Marelli, L. Samuels, *et al.*, "Initial experience with the AbioCor implantable replacement heart system," *The Journal of Thoracic and Cardiovascular Surgery*, vol. 127, pp. 131-141, 2004.

[45] D. J. Burke, E. Burke, F. Parsaie, V. Poirier, K. Butler, D. Thomas, *et al.*, "The HeartMate II: Design and Development of a Fully Sealed Axial Flow Left Ventricular Assist System," *Artificial Organs*, vol. 25, pp. 380-385, 2001.

[46] A. El-Banayosy, L. Arusoglu, L. Kizner, M. Morshuis, G. Tenderich, W. E. Pae Jr, *et al.*, "Preliminary experience with the lionheart left ventricular assist device in patients with end-stage heart failure," *The Annals of Thoracic Surgery*, vol. 75, pp. 1469-1475, 2003.

[47] R. D. Dowling, S. W. Etoch, K. A. Stevens, A. C. Johnson, and L. A. Gray Jr, "Current status of the AbioCor implantable replacement heart," *The Annals of Thoracic Surgery*, vol. 71, pp. S147-S149, 2001.

[48] ABIOMED INC., "Transcutaneous Energy Transfer System with Vibration Inducing Warning Circuitry," US Patent PCT/US2011/065471, 28 June, 2012.

[49] ABIOMED INC., "Transcutaneous Energy Transfer System with Multiple Secondary Coils," US Patent PCT/US2011/065446, 28 June, 2012.

[50] ABIOMED INC., "A Compact Battery and Controller Module for a Transcutaneous Energy Transfer System," US Patent PCT/US2011/065454, 28 June, 2012.

[51] ABIOMED INC., "Method and Apparatus for Accurately Tracking Available Charge in a Transcutaneous Energy Transfer System," US Patent PCT/US2011/065463, 28 June, 2012.

[52] ABIOMED INC., "Transcutaneous Energy Transfer Coil with Integrated Radio Frequency Antenna," US Patent PCT/US2011/065477, 18 Oct, 2012.

[53] T. Yamane, "The present and future state of nonpulsatile artificial heart technology," *Journal of Artificial Organs*, vol. 5, pp. 0149-0155, September 1, 2002.

[54] O. H. Frazier, T. J. Myers, I. D. Gregoric, T. Khan, R. Delgado, M. Croitoru, *et al.*, "Initial Clinical Experience With the Jarvik 2000 Implantable Axial-Flow Left Ventricular Assist System," *Circulation*, vol. 105, pp. 2855-2860, June 18, 2002.

[55] M. Egemen Tuzun, Katy Roberts, BS, William E. Cohn, MD, Murat Sargin, MD, Courtney J. Gemmato, BS, Branislav Radovancevic, MD, and O. H. Frazier, MD, "In Vivo Evaluation of the HeartWare Centrifugal Ventricular Assist Device," *Texas Heart Institute Journal*, vol. 34, pp. 406-411.

[56] T. D. Dissanayake, "An effective transcutaneous energy transfer (TET) system for artificial hearts," PhD, Bioengineering, University of Auckland, 2010.

[57] Y. Mitamura, E. Okamoto, A. Hirano, and T. Mikami, "Development of an implantable motor-driven assist pump system," *Biomedical Engineering, IEEE Transactions on*, vol. 37, pp. 146-156, 1990.

[58] G. B. Bearnson, S. R. Krivoy, R. D. Jarmin, J. R. Fratto, P. Khanwilkar, K. R. Crump, *et al.*, "Electronics development for the Utah electrohydraulic total artificial heart," in *Computer-Based Medical Systems, 1993. Proceedings of Sixth Annual IEEE Symposium on*, 1993, pp. 247-252.

[59] A. Homma, Y. Taenaka, E. Tatsumi, Y. Takewa, T. Kamimura, H. Naitoh, *et al.*, "Current status of the National Cardiovascular Center totally implantable artificial heart system," in *SICE 2004 Annual Conference*, 2004, pp. 436-441 vol. 1.

[60] T. D. Dissanayake, D. M. Budgett, P. Hu, L. Bennet, S. Pyner, L. Booth, *et al.*, "A Novel Low Temperature Transcutaneous Energy Transfer System Suitable for

High Power Implantable Medical Devices: Performance and Validation in Sheep," *Artificial Organs*, vol. 34, pp. E160-E167, 2010.

[61] A. Ghahary and B. H. Cho, "Design of transcutaneous energy transmission system using a series resonant converter," *Power Electronics, IEEE Transactions on*, vol. 7, pp. 261-269, 1992.

[62] C. C. Tsai, B. S. Chen, and C. M. Tsai, "Design of wireless transcutaneous energy transmission system for totally artificial hearts," in *Circuits and Systems, 2000. IEEE APCCAS 2000. The 2000 IEEE Asia-Pacific Conference on*, 2000, pp. 646-649.

[63] A. Mizannojehdehi, M. Shams, and T. Mussivand, "Design and Analysis of A Class-E Frequency-Controlled Transcutaneous Energy Transfer System," in *Electronics, Circuits and Systems, 2006. ICECS '06. 13th IEEE International Conference on*, 2006, pp. 21-24.

[64] T. Mussivand, K. S. Holmes, A. Hum, and W. J. Keon, "Transcutaneous Energy Transfer with Voltage Regulation for Rotary Blood Pumps," *Artificial Organs*, vol. 20, pp. 621-624, 1996.

[65] C. Qianhong, W. Siu Chung, C. K. Tse, and R. Xinbo, "Analysis, Design, and Control of a Transcutaneous Power Regulator for Artificial Hearts," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 3, pp. 23-31, 2009.

[66] E. Okamoto, Y. Yamamoto, Y. Akasaka, T. Motomura, Y. Mitamura, and Y. Nosé, "A New Transcutaneous Energy Transmission System With Hybrid Energy Coils for Driving an Implantable Biventricular Assist Device," *Artificial Organs*, vol. 33, pp. 622-626, 2009.

[67] B. H. Waters, A. P. Sample, P. Bonde, and J. R. Smith, "Powering a Ventricular Assist Device (VAD) With the Free-Range Resonant Electrical Energy Delivery (FREE-D) System," *Proceedings of the IEEE*, vol. 100, pp. 138-149, 2012.

[68] G. Wang, L. Wentai, M. Sivaprakasam, and G. A. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, pp. 2109-2117, 2005.

[69] G. Wang, L. Wentai, R. Bashirullah, M. Sivaprakasam, G. A. Kendir, J. Ying, *et al.*, "A closed loop transcutaneous power transfer system for implantable devices with enhanced stability," in *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, 2004, pp. IV-17-20 Vol.4.

[70] P. Si, A. P. Hu, J. W. Hsu, M. Chiang, Y. Wang, S. Malpas, *et al.*, "Wireless Power Supply for Implantable Biomedical Device Based on Primary Input Voltage Regulation," in *Industrial Electronics and Applications, 2007. ICIEA 2007. 2nd IEEE Conference on*, 2007, pp. 235-239.

[71] C. S. Tang, S. Yue, S. Yu Gang, N. Sing Kiong, and A. P. Hu, "Determining Multiple Steady-State ZCS Operating Points of a Switch-Mode Contactless Power Transfer System," *Power Electronics, IEEE Transactions on*, vol. 24, pp. 416-425, 2009.

[72] Y. Wu, A. P. Hu, D. Budgett, S. C. Malpas, and T. Dissanayake, "Efficient Power-Transfer Capability Analysis of the TET System Using the Equivalent Small Parameter Method," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 5, pp. 272-282, 2011.

[73] T. Mussivand, J. A. Miller, P. J. Santerre, G. Belanger, K. C. Rajagopalan, P. J. Hendry, *et al.*, "Transcutaneous Energy Transfer System Performance Evaluation," *Artificial Organs*, vol. 17, pp. 940-947, 1993.

[74] P. Si, "Wireless power supply for implantable biomedical devices," PhD, Electrical and Electronic Engineering, University of Auckland, 2008.

[75] P. Si, A. P. Hu, S. Malpas, and D. Budgett, "Switching Frequency Analysis of Dynamically Detuned ICPT Power Pick-ups," in *Power System Technology, 2006. PowerCon 2006. International Conference on*, 2006, pp. 1-8.

[76] H. Matsuki, Y. Yamakata, N. Chubachi, S. I. Nitta, and H. Hashimoto, "Transcutaneous DC-DC converter for totally implantable artificial heart using synchronous rectifier," *Magnetics, IEEE Transactions on*, vol. 32, pp. 5118-5120, 1996.

[77] T. Gowrishankar, D. Stewart, G. Martin, and J. Weaver, "Transport lattice models of heat transport in skin with spatially heterogeneous, temperature-dependent perfusion," *BioMedical Engineering OnLine*, vol. 3, p. 42, 2004.

[78] H. Miura, S. Arai, F. Sato, H. Matsuki, and T. Sato, "A synchronous rectification using a digital PLL technique for contactless power supplies," *Magnetics, IEEE Transactions on*, vol. 41, pp. 3997-3999, 2005.

[79] H. Miura, S. Arai, Y. Kakubari, F. Sato, H. Matsuki, and T. Sato, "Improvement of the Transcutaneous Energy Transmission System Utilizing Ferrite Cored Coils for Artificial Hearts," *Magnetics, IEEE Transactions on*, vol. 42, pp. 3578-3580, 2006.

[80] H. Chen, A. P. Hu, and D. Budgett, "Power Loss Analysis of a TET System for High Power Implantable Devices," in *Industrial Electronics and Applications, 2007. ICIEA 2007. 2nd IEEE Conference on*, 2007, pp. 240-245.

[81] T. D. Dissanayake, D. Budgett, H. Patrick, and S. Malpas, "Experimental thermal study of a TET system for implantable biomedical devices," in *Biomedical Circuits and Systems Conference, 2008. BioCAS 2008. IEEE*, 2008, pp. 113-116.

[82] H. Y. Leung, D. M. Budgett, and A. P. Hu, "Minimizing Power Loss in Air-Cored Coils for TET Heart Pump Systems," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol. 1, pp. 412-419, 2011.

[83] H. Y. Leung, D. M. Budgett, and P. Hu, "Reactive component selection for TET powered medical devices," in *Engineering in Medicine and Biology Society,EMBC, 2011 Annual International Conference of the IEEE*, 2011, pp. 2913-2916.

[84] H. H. Wu, A. P. Hu, P. Si, D. Budgett, C. Tung, and S. Malpas, "A push-pull resonant converter with dual coils for Transcutaneous Energy Transfer systems," in *Industrial Electronics and Applications, 2009. ICIEA 2009. 4th IEEE Conference on*, 2009, pp. 1051-1056.

[85] H. Matsuki, M. Shiiki, K. Murakami, T. Yamamoto, S. Nitta, and H. Hashimoto, "High Efficient Energy Transmission for Implantable Artificial Heart," *Magnetics in Japan, IEEE Translation Journal on*, vol. 8, pp. 187-191, 1993.

[86] T. H. Nishimura, T. Eguchi, K. Hirachi, Y. Maejima, K. Kuwana, and M. Saito, "A large air gap flat transformer for a transcutaneous energy transmission system," in *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, 1994, pp. 1323-1329 vol.2.

[87] L. Zhao, C. F. Foo, K. J. Tseng, and W. K. Chan, "Transcutaneous transformers in power supply system for an artificial heart," in *Power Electronic Drives and Energy Systems for Industrial Growth Proceedings. International Conference on*, 1998, pp. 348-352 Vol.1.

[88] N. S. Artan, X. Li, R. Patel, C. Ning, N. Ludvig, and H. J. Chao, "Multi-layer coils for efficient Transcutaneous Power Transfer," in *Engineering in Medicine*

and Biology Society,EMBC, 2011 Annual International Conference of the IEEE, 2011, pp. 3031-3034.

[89] J. R. Smith. (2013, 5 Feb). *FREED (Free-range Resonant Electrical Energy Delivery)* [Article]. Available: http://sensor.cs.washington.edu/FREED.html

[90] J. T. Boys, G. A. Covic, and A. W. Green, "Stability and control of inductively coupled power transfer systems," *Electric Power Applications, IEE Proceedings -*, vol. 147, pp. 37-43, 2000.

[91] C.-S. Wang, G. A. Covic, and O. H. Stielau, "Power transfer capability and bifurcation phenomena of loosely coupled inductive power transfer systems," *Industrial Electronics, IEEE Transactions on*, vol. 51, pp. 148-157, 2004.

[92] A. Feng, H. Qin, Z. Mao, and P. Peng, "Analysis of Bifurcation Phenomena Based on Optimized Transformer in Loosely Coupled Inductive Power Transfer System," in *Electrical and Control Engineering (ICECE), 2010 International Conference on*, 2010, pp. 3324-3327.

[93] C. Tang, D. Xin, W. Zhihui, S. Yue, and A. P. Hu, "Frequency bifurcation phenomenon study of a soft switched push-pull contactless power transfer system," in *Industrial Electronics and Applications (ICIEA), 2011 6th IEEE Conference on*, 2011, pp. 1981-1986.

[94] Y. Wu, A. P. Hu, D. Budgett, S. Malpas, and T. Dissanayake, "Harmonic analysis of voltage-fed full-bridge converter for TET application," in *Industrial Electronics and Applications (ICIEA), 2010 the 5th IEEE Conference on*, 2010, pp. 1040-1045.

[95] A. Hu, "Selected resonant converter for IPT power supplies," PhD, Electrical and Electronic Engineering, The University of Auckland, 2001.

[96] D. M. Budgett, A. P. Hu, P. Si, W. T. Pallas, M. G. Donnelly, J. W. T. Broad, *et al.*, "Novel technology for the provision of power to implantable physiological devices," *Journal of Applied Physiology*, vol. 102, pp. 1658-1663, April 1, 2007.

[97] A. Karalis, J. D. Joannopoulos, and M. Soljačić, "Efficient wireless non-radiative mid-range energy transfer," *Annals of Physics*, vol. 323, pp. 34-48, 2008.

[98] A. Kurs, A. Karalis, R. Moffatt, J. D. Joannopoulos, P. Fisher, and M. Soljačić, "Wireless Power Transfer via Strongly Coupled Magnetic Resonances," *Science*, vol. 317, pp. 83-86, July 6, 2007.

[99] U. K. Madawala and D. J. Thrimawithana, "Operation of a Split-Capacitor Push-Pull Parallel Resonant Converter in Buck Mode," in *Industrial Electronics Society, 2007. IECON 2007. 33rd Annual Conference of the IEEE*, 2007, pp. 1586-1591.

[100] U. K. Madawala and D. J. Thrimawithana, "Mathematical model for split-capacitor push-pull parallel resonant converter in Buck mode," *Power Electronics, IET*, vol. 1, pp. 356-367, 2008.

[101] D. J. Thrimawithana and U. K. Madawala, "Analysis of Split-Capacitor Push-Pull Parallel Resonant Converter in normal mode," in *Power Electronics, Electrical Drives, Automation and Motion, 2008. SPEEDAM 2008. International Symposium on*, 2008, pp. 778-783.

[102] D. J. Thrimawithana and U. K. Madawala, "Analysis of Split-Capacitor Push-Pull Parallel-Resonant Converter in Boost Mode," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 359-368, 2008.

[103] D. J. Thrimawithana, U. K. Madawala, and P. Lunenburg, "A Novel Buck-Boost Control Technique for Push-Pull Parallel-Resonant Converters," in *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, 2006, pp. 2805-2811.

[104] C. Liu and A. P. Hu, "Steady state analysis of a capacitively coupled contactless power transfer system," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 3233-3238.

[105] B. Wang, A. P. Hu, and D. Budgett, "Power Flow Control Based Solely on Slow Feedback Loop for Heart Pump Applications," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. PP, pp. 1-1, 2011.

[106] C. Qianhong, W. Siu Chung, C. K. Tse, and R. Xinbo, "Analysis, design and control of a transcutaneous power regulator for artificial heart," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 1833-1838.

[107] J. Teng, X. Hong-xia, Q. Kun-xi, W. Hao, and W. Fang-qun, "Study on transcutaneous energy transmission system for heart pump," in *Mechanic Automation and Control Engineering (MACE), 2011 Second International Conference on*, 2011, pp. 6939-6942.

[108] B. H. Waters, A. P. Sample, and J. R. Smith, "Adaptive Impedance Matching for Magnetically Coupled Resonators," in *PIERS Proceedings*, Moscow, 2012.

[109] W. L. Holman, J. K. Kirklin, D. C. Naftel, R. L. Kormos, P. Desvign-Nickens, M. T. Camacho, *et al.*, "Infection after implantation of pulsatile mechanical circulatory support devices," *The Journal of Thoracic and Cardiovascular Surgery*, vol. 139, pp. 1632-1636.e2, 2010.

[110] B. Wang, A. P. Hu, and D. M. Budgett, "Development of a push-pull current doubler synchronous rectifier for powering heart pumps," in *Industrial Electronics and Applications (ICIEA), 2010 the 5th IEEE Conference on*, 2010, pp. 1368-1372.

[111] IFAC. (2012). *Calculation of the Dielectric Properties of Body Tissues in the frequency range 10 Hz - 100 GHz*. Available: http://niremf.ifac.cnr.it/tissprop/htmlclie/htmlclie.htm