CONTENTS

CHAPTER 1

Introduction

The first transistor invented in 1947 by J. Bardeen and W.H. Brattain used germanium (Ge) as the semi-conducting material [1]. This opened the door to countless applications of solid state electronics. From early 1970s, microelectronics has been primarily a silicon-based technology, not only because of its high abundance in the Earth's crust but also because of the stability and high quality SiO_2 and its interface with Si substrate. The solid phase reaction at sub-eutectic temperatures between a thin metal film and a single-crystal semiconductor has attracted much interest because of its importance in Schottky barrier and contact formation, epitaxial growth and device reliability [2]. In the manufacturing of semiconductor devices and metal contacts have always played a pivotal role, especially in metal-oxide semiconductor field effect transistors (MOSFET) and complementary metal-oxide semiconductor (CMOS) devices. Contacts to ultra large scale integration (ULSI) circuits and interconnections require metal-semiconductor (MS) contacts which are thermally stable, have low resistivity and are compatible with the process technology. A good MS contact is essential for the successful operation of the electronic circuits and devices [3]. Due to the shrinking of the advanced Si-based complementary metal-oxide-semiconductor (CMOS) device feature size, it is becoming increasingly difficult to further improve Si-based CMOS performance with traditional device scaling. Thus new material and device structures to relax the physical limitation in device scaling are now required. Ge has been regarded as the replacement for Si as the channel material in future high-speed CMOS technology, due to its lower effective mass of holes [4], higher carrier mobilities [5] compared to those of Si, and its relative compatibility with silicon processing [6]. The lack of a stable native Ge oxide has been the obstacle for the use of Ge in CMOS devices [5]. However, recent developments of next generation deposited high-k dielectrics, germanium oxynitride, ZrO_2,

Al_2O_3 and HfO_2 allow for the fabrication of high performance Ge-based metal-oxide semiconductor field effect transistors (MOSFETs) [5,7]. Low reactivity with oxygen in the high-k dielectric is expected in the germanide/high-k gate stack structure [8].

Much work has been done on transition metal-Si systems but data concerning the behaviour of metal thin films on germanium upon heat treatment is relatively scarce, as little attention has been paid to transition metal-Ge systems. Therefore optimal implementation of germanium technology will require an understanding of metal-germanium interactions, from both metallurgical and electronic standpoints, and dynamic properties of process-induced defects in Ge. Most of the studies on metal-Ge reaction up to date have been carried out using in-situ annealing by slowly-ramping annealing temperature or rapid thermal annealing processing (RTP), rather than using furnace annealing, and also with less emphasis on morphological evolution.

Metal-semiconductor (MS) interfaces are an essential part of virtually all semiconductor electronic devices [9]. The MS structures are important research tools in the characterization of new semiconductor materials [10]. Their interface properties have a dominant influence on the performance, reliability and stability of device [9,11,12]. These applications include microwave field effect transistors, radio-frequency detectors, phototransistors, heterojunction bipolar transistors, quantum confinement devices and space solar cells [13,14,15,16].

The objective of this study was to add to the knowledge about: metal-germanium electrical properties and surface morphological evolution at different furnace annealing temperatures; defects induced in n-Ge during contact fabrication and annealing processes; and the temperature dependence of n-Ge Schottky diodes' electrical parameters.

An overview of the semiconductor theory with emphasis on Schottky contacts and defects is presented in Chapter 2. Chapter 3 contains the experimental details of the research. The results obtained from the study are presented in chapters 4, 5, 6, 7 and 8, while chapter 9 gives a summary and discussion of the results.

References

[1] J. Bardeen, B.W. Brattain, Phys. Rev. **74** (1948) 230.

[2] M.G. Grimaldi, L. Weiluński, M.-A. Nicolet, Thin Solid Films **81** (1981) 207.

[3] A.R. Saha, S. Chattopadhyay, C.K. Maiti, Mater. Sci. Eng. B **114-115** (2004) 218.

[4] R. Hull, J.C. Bean (Eds.), Germanium Silicon: Physics and Materials, Semiconductor and Semimetals, Vol. 56, Academics Press, San Diego, 1999.

[5] D.Z. Chi, H.B. Yao, S.L. Liew, C.C. Tan, C.T. Chua, K.C. Chua, R. Li and S.J. Lee, 7th International Workshop on Junction Technology (2007) 81.

[6] S. Gaudet, C. Detavernier, A.J. Kellock, P. Desjardins, C. Lavoive, J. Vac. Sci. Techno. A **24** (2006) 474.

[7] C.O. Chui, S. Ramanathan, B.B. Triplett, P.C. McIntyre, K.C. Saraawat, IEEE Electron Dev. Lett. **23** (2002) 473.

[8] D. Ikeno, Y. Kaneko, H. Kondo, M. Sakashita, A. Sakai,. M. Ogawa, S. Zaima, Jpn. J. Appl. Phys. **46** (2007) 1865.

[9] R.T. Tung, Mater. Sci. Eng. R **35** (2001) 1.

[10] Ö.F. Yüksel, Physica B **404** (2009) 1993.

[11] W. Mönch, Semiconductor Surf. And Interfaces, 2nd ed. Springer, Berlin 1995.

[12] S.M. Sze, Physics of Semiconductor Devices, 2nd ed. Wiley, New York, 1981.

[13] J.H. Werner, H.H. Güttler, J. Appl. Phys. **69** (1991) 1522.

[14] S. Chand, J. Kumar, J. Appl. Phys. **80** (1996) 288.

[15] K.M. Hudait, K.P. Venkateswarlu, S.B. Krupanidhi, Solid-State Electron. **45** (2001) 133.

[16] M. Soylu, B. Abay, Microelectron. Eng. **86** (2009) 88.

CHAPTER 2

THEORETICAL ASPECTS

2.1 Introduction

In this chapter, semiconductor theoretical aspects are discussed. Section 2.2 and 2.3 present the crystal and the energy band structures respectively, for germanium. Metal-semiconductor contacts are discussed in section 2.4. Section 2.5 discusses the annealing studies and germanide formation. In section 2.6 and 2.7, the fundamentals of defects in semiconductors and the theoretical aspects of deep level transient spectroscopy are presented respectively.

2.2 Crystal structure of Ge

A crystalline structure is formed when a basis of atoms is attached to every lattice point, with every basis identical in composition, arrangement, and orientation [1]. Many semiconductors have a simple crystal structure with high degrees of symmetry. Elemental and compound semiconductors have either the diamond, zinc blende, or wurzite structures. Germanium, element number 32 [2], crystallizes into the diamond structure shown in Fig. 2.1, which is actually formed by two interpenetrating face-centered cubic (fcc) lattices. The primitive basis has two identical atoms at $000;\frac{1}{4}\frac{1}{4}\frac{1}{4}$ associated with each point of the fcc lattice [1].

2.3 Band structure of Ge

The essence of energy band theories for a crystalline solid is due to the fact that many physical and optical properties of a solid can be explained using its band structure. The band structure of a crystalline solid, that is, the energy-momentum (*E-k*) relationship, is usually obtained by solving the Schrodinger equation of an approximate one-electron problem [3]. In this method the total wave functions of electrons are chosen as a linear combination of the individual wave functions in which each wave function involves only the coordinates of one

electron [4]. The Bloch theorem states that the most generalized solution for a one-electron time-dependent Schödinger equation in a periodic crystal lattice is given by [3,4]

$$\phi_k(r) = u_k(r)e^{jk.r} \tag{2.1}$$

where $u_k(r)$ is the Bloch function, which has the same spatial periodicity of the crystal potential, and $k(=2\pi/\lambda)$ is the wave vector of an electron.

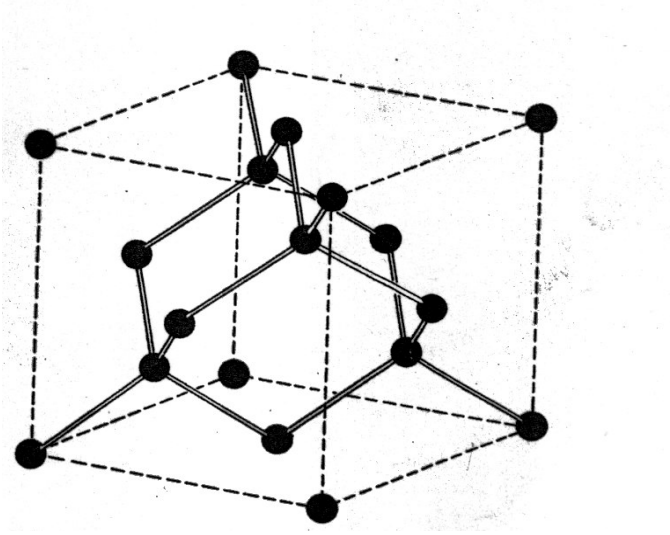


Fig. 2.1 *Crystal structure of diamond [1]*

The one-electron time-independent Schrödinger equation for which $\phi_k(r)$ is a solution can be written as [3,5]:

$$-\left(\frac{\hbar^2}{2m}\right)\nabla^2\phi_k(r) + V(r)\phi_k(r) = E_k\phi_k(r) \tag{2.2}$$

where $V(r)$ is the periodic crystal potential, which arises from the presence of ions at their regular lattice sites. From the Bloch theorem it can be shown that the energy E_k is periodic in the reciprocal lattice, and for a given band index, to label the energy uniquely, it is sufficient to use only k's in a primitive cell of the reciprocal lattice.

The energy band structures for the elemental (Si, Ge) and III-V compound semiconductors have been studied theoretically using a variety of numerical methods. The three methods most frequently used are the orthogonalized plane-wave method [6,7], the pseudopotential

method [8], and the k.p method [9]. In most cases theoretical calculations of the energy band structures for these semiconductor materials are guided by the experimental data from the optical absorption, photoluminescence and photoemission experiments [4]. For any semiconductor there is a forbidden energy region in which allowed states cannot exist. Energy bands are permitted above and below this forbidden energy region. The upper energy bands are called conduction bands and below the forbidden energy region, the valence bands. The separation between the energy of the lowest conduction band and that of the highest valence band is called the band gap E_g, which is the most important parameter in semiconductor physics. The conduction and valence bands of germanium are shown in Fig. 2.2. The Ge conduction band minimum and valence band maximum are not located at the same *k*-value, and so Ge is referred to as an indirect band gap semiconductor. The conduction band minimum of germanium crystal is located at the zone boundaries along the {111} axes. It is noted that the constant energy surfaces for electrons in germanium are ellipsoidal [4]. The value of the band gap for Ge at room temperature and under normal pressure is 0.66 eV [3].

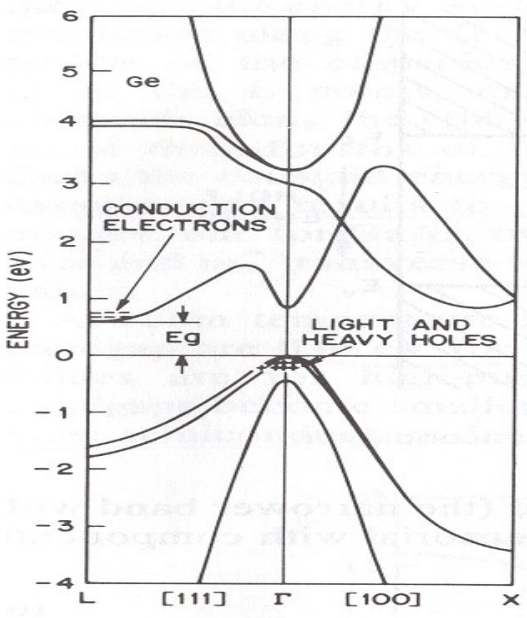


Fig. 2.2 *Energy band structure of Ge, where E_g is the energy band gap. Plus signs indicate the holes in the valence band and minus signs indicate electrons in the conduction band [1]*

The experimental results show that the band gap of Ge decreases with increasing temperature. The variation of the band gap with temperature can be expressed approximately by universal function [3]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(T+\beta)} \tag{2.3}$$

where $E_g(0) = 1.170$ eV, $\alpha = 4.774 \times 10^{-4}$eV/K and $\beta = 235$.

Also to note is that at near room temperature, the Ge band gap increases with pressure, and its dependence on pressure is given by [3]:

$$\frac{dE_g}{dP} = 5\times 10^{-6}\ \text{eV/(kg/cm}^2) \tag{2.4}$$

2.4 Metal-semiconductor contacts

2.4.1 Introduction

Metal-semiconductor (MS) interfaces are an essential part of virtually all semiconductor electronic and optoelectronic devices [10]. The physical properties of MS interfaces are widely studied, both for their basic physical properties and for their technological applications to electronic devices [11]. The MS structures are important research tools in the characterization of new semiconductor materials [12]. Their interface properties have a dominant influence on the performance, reliability and stability of devices [3,10,13]. Electronic properties of the MS contacts are characterised by their barrier height (BH). Boyarby et al. [14] suggested that the recent motivation for studying Schottky barrier formation is due to the recognition that both electronic and chemical equilibrium have to be considered together across a reactive interface between metal and semiconductor, as surface states and metal-induced gap states failed to take into consideration the chemical equilibrium at the interface. The chemical equilibrium results in interfacial atomic rearrangement, interdiffusion, and inter-metallic compound formation, which have a profound effect on the electronic equilibrium producing the Schottky barrier [15]. Therefore, the BH is likely to be a function of the interface atomic structure, and the atomic inhomogeneities at MS interface

which are caused by grain boundaries, multiple phases, facets, defects, a mixture of different phases, etc [16,17,18,19].

2.4.2 Schottky barrier formation

When a metal is evaporated onto the surface of a semiconductor, a potential barrier is formed at the MS interface. The Fermi levels in the two materials must be coincident at thermal equilibrium. According to the Schottky-Mott model, the barrier height of an ideal metal/n-type semiconductor Schottky contact is equal to the difference between the metal work function ϕ_m (the energy required to remove an electron from the material to the vacuum level) and the electron affinity χ_s of a semiconductor (energy released when an electron is added to the material), which can be written as [20,21]

$$\phi_{Bn} = \phi_m - \chi_s \tag{2.5}$$

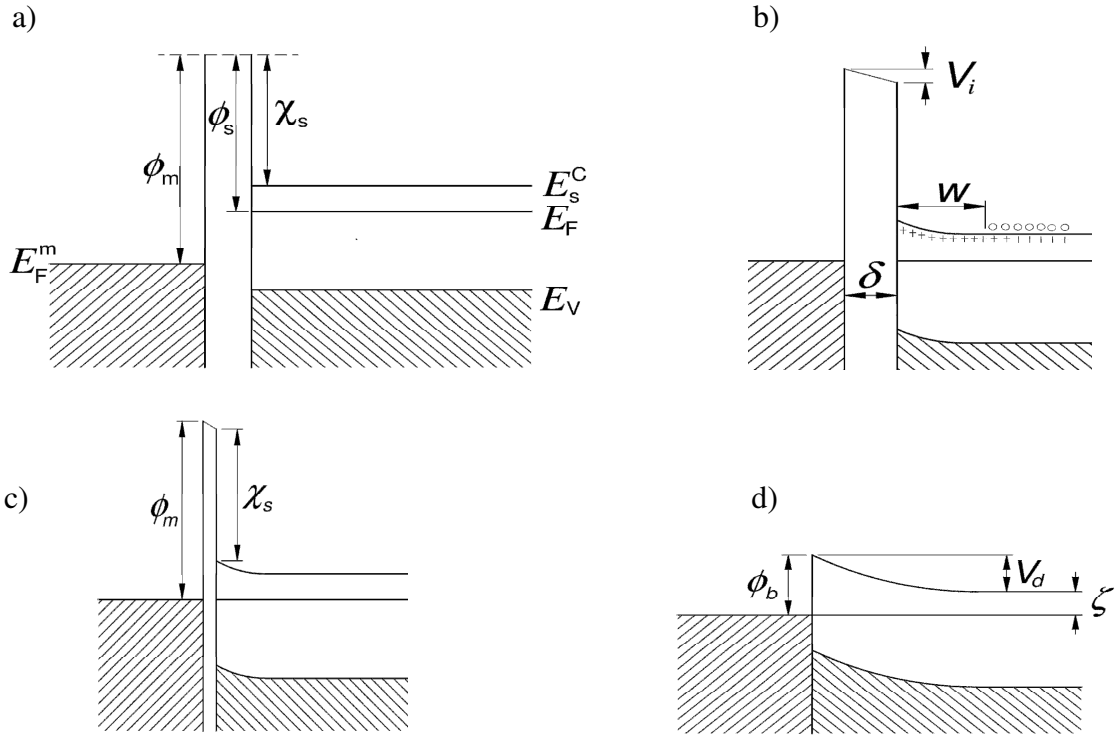


Fig. 2.3 *The formation of a Schottky barrier between a metal and a semiconductor (a) neutral and isolated states, (b) electrically connected, (c) separated by a narrow gap, and (d) in perfect contact, redrawn from ref.* 22

Fig. 2.3 shows the formation of a Schottky barrier. Part (a) shows the metal and the semiconductor in their isolated, electrically neutral states for an n-type semiconductor with work function ϕ_s less than that of the metal, which, in practice, is the most important case. If the semiconductor and metal are connected by means of a wire, electrons pass from the semiconductor to the metal. Due to the flow of the electrons, there must be a negative charge on the surface of the metal and a positive charge builds up on the surface of the semiconductor, resulting an electric field in the gap between the metal and the semiconductor. The equilibrium condition is established when the Fermi levels of the two materials coincide as illustrated in Fig. 2.3 (b).

The negative charge on the surface of the metal consists of extra conduction electrons contained within the Thomas-Fermi screening distance of about 0.5 Å. Because the semiconductor is n-type, the positive charge will be provided by conduction electrons moving from the surface leaving uncompensated positive donor ions in a region depleted of electrons. Due to the fact that the donor concentration is much lower than the concentration of electrons in the metal, the uncompensated donors occupy a layer of appreciable thickness w. The potential changes slowly over the depletion region, and results in bands bending downwards as shown in Fig. 2.3 (b). The difference between the electrostatic potentials outside the surface of the metal and semiconductor is given by $V_i = \delta E_i$, where δ is their separation and E_i is the electric field in the gap. As the metal and semiconductor approach each other, the electric field stays finite (Fig. 2.3 (c)), and results in V_i tending to zero as the gap diminishes. When the metal and semiconductor finally touch (Fig. 2.3 (d)), the barrier due to the vacuum disappears completely, and the only barrier seen by electrons, is that resulting from the bending of the bands in the semiconductor.

As shown in Fig. 2.3 (d), the height of the barrier relative to the position of the conduction band in the neutral region of the semiconductor is called the diffusion potential (also called the built-in-potential), V_d can be expressed by

$$V_d = \phi_{Bn} - \xi \tag{2.6}$$

where ξ is the Fermi (or chemical) potential of an n-type semiconductor (the energy difference between the Fermi level and conduction band) and is given by [3]

$$\xi = kT \ln\left(\frac{N_C}{N_D}\right) \tag{2.7}$$

where N_C is the density of states in the conduction band of the semiconductor, N_D is the doping density, k is the Boltzmann constant and T is the Kelvin temperature.

2.4.3 Schottky barrier behaviour under forward and reverse bias

A Schottky barrier diode is a majority-carrier device, as the current flow in such a device is due to the majority carriers (e.g electrons in an n-type semiconductor). Under zero bias conditions, electrons from both the semiconductor and the metal see the same barrier height relative to their Fermi levels. Therefore, there is no net flow of electrons over the barrier in either direction.

Applying a bias voltage to the contact so that the metal is positive, the bands in the semiconductor are raised in energy compared to those in the metal, causing the electric field in the barrier to decrease. The decrease in electric field takes place within the semiconductor barrier region and shape of the barrier changes as illustrated in Fig. 2.4 (a). The diffusion potential V_d is decreased compared to the zero-bias condition. The electrons can now cross from the semiconductor to the metal more easily as they now see a reduced barrier. However, if a positive potential is applied to the semiconductor, the Fermi level of the semiconductor is lowered relative to that of the metal, and the diffusion potential V_d is increased (Fig. 2.4 (b)), resulting in the number of electrons able to surmount the barrier into the metal decreasing. This also increases the width of the depletion region. Therefore, in the reverse biased mode, very little current flows through the device.

2.4.4 Depletion layer

For the determination of the spatial distributions of potential and electric fields, the depletion layer width, and the junction capacitance of a Schottky diode, a Poisson's equation in the space-charge region has to be solved using proper boundary conditions.

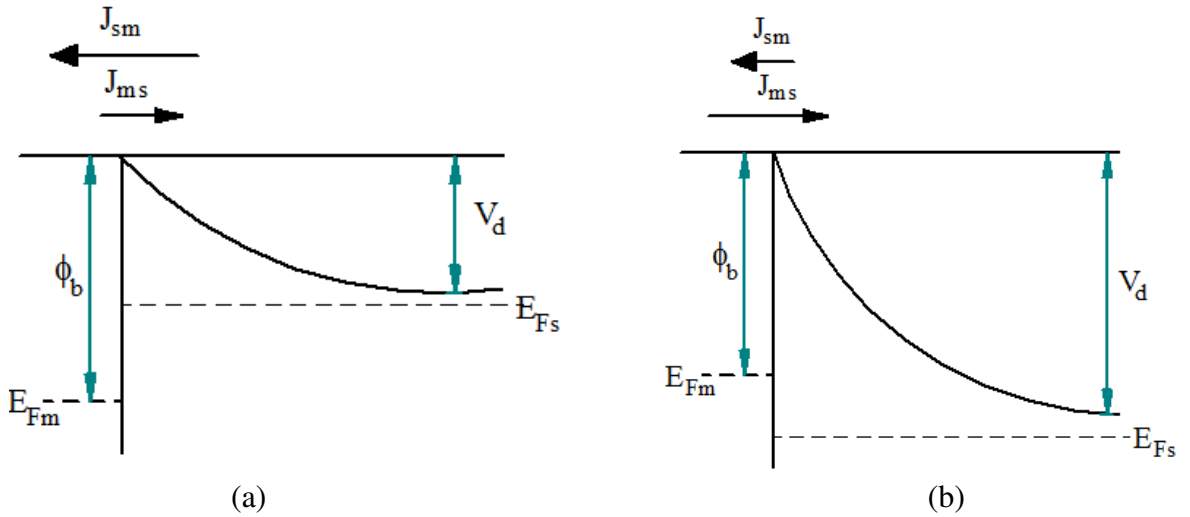


Fig. 2.4 *Schottky barrier (a) under forward bias, (b) under reverse bias, redrawn from ref. 22.*

The boundary conditions are obtained from the barrier height, and that there is no electric field in the bulk of the semiconductor. Considering that $x = 0$ at the interface, the boundary conditions can be written as $V(0) = V_d$ and $E(\infty) = 0$, where V is the contact potential and E is the electric field. The Poisson's equation in the depletion region of a Schottky diode can be written as

$$\frac{d^2V}{dx^2} = \frac{1}{\varepsilon_s}\rho(x) \tag{2.8}$$

where $\rho(x)$ is the total charge density in the semiconductor at depth x and ε_s is the permittivity of the semiconductor. In general, $\rho(x)$ should include contributions from valence band, conduction band, ionized donors and acceptors, and deep levels in the band gap. This will result to a complicated equation that can only be solved by numerical methods. The equation can be simplified by applying the depletion approximation. By using the depletion or abrupt approximation, it is assumed that the semiconductor can be divided into two regions: the depletion region, directly below the metal, which contains no free carriers, and the bulk of the semiconductor, which is electrically neutral and in which the electric field is zero. In the depletion region, as there are no electrons in the conduction band, the charge density $\rho(x)$ is qN_D. If the width of the depletion region is w, the charge density in the semiconductor can be written as

$$\rho(x) = \begin{cases} qN_D & if\ x \le w \\ 0 & if\ x > w \end{cases} \tag{2.9}$$

where N_D is the density of dopants and q is the electronic charge.

By integrating Eq. (2.8) twice and applying the boundary condition, the depletion width can be written as

$$w = \sqrt{\frac{2\varepsilon_s V_d}{qN_D}} \tag{2.10}$$

When the contact is biased by an externally applied voltage V_a, the depletion width can be expressed as

$$w = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_d - V_a - \frac{kT}{q}\right)} \tag{2.11}$$

where the term $\frac{kT}{q}$ arises from the contribution of the majority-carrier distribution tail (electrons in the n side). It is seen from Eq. (2.11) that the depletion layer width is directly proportional to square root of applied voltage and is inversely proportional to the square root of the dopant density of the semiconductor. The electric field and the potential in the depletion region are given respectively by

$$E(x) = \frac{qN_D}{\varepsilon_s}(x - w) \tag{2.12}$$

and

$$V(x) = -\left(\frac{qN_D}{\varepsilon_s}\right)\left(\frac{x^2}{2} - wx\right) - \phi_{Bn} \tag{2.13}$$

Fig. 2.5 shows a graph of $\rho(x)$, $E(x)$, and $V(x)$ for a Schottky barrier.

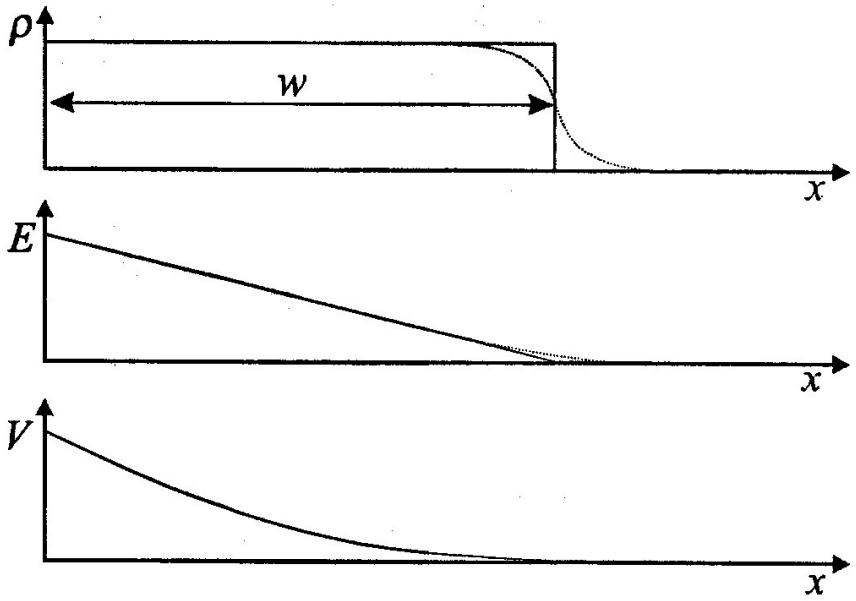


Fig. 2.5 *Graphs of the charge density $\rho(x)$, electric field E and electrostatic potential V.*

The space charge density Q_{sc} per unit area of the semiconductor and depletion layer capacitance C per unit area are given by

$$Q_{sc} = qN_D w = \sqrt{2q\varepsilon_s N_D (V_d - V_a - \frac{kT}{q})} \tag{2.14}$$

$$C = \frac{\partial Q_{sc}}{\partial V} = \sqrt{\frac{q\varepsilon_s N_D}{2(V_d - V_a - kT/q)}} = \frac{\varepsilon_s}{w} \tag{2.15}$$

Eq. (2.15) can also be expressed in the form,

$$\frac{1}{C^2} = \frac{2(V_d - V_a - kT/q)}{q\varepsilon_s N_D} \tag{2.16}$$

or

$$N_D = \frac{2}{q\varepsilon_s}\left[-\frac{1}{d(1/C^2)/dV}\right] \tag{2.17}$$

If N_D is constant throughout the depletion region, a straight line should be obtained by plotting $1/C^2$ versus V. If N_D is not constant, the differential capacitance method can be used to determine the doping profile from Eq. (2.17). From the intercept on the voltage axis, the barrier height can be determined:

$$\phi_{Bn} = V_i + \xi + \frac{kT}{q} - \Delta\phi \tag{2.18}$$

where V_i is the voltage intercept, and ξ is the depth of the Fermi level below the conduction band, which can be computed if the doping concentration is known and $\Delta\phi$ is the image force barrier lowering and is given by

$$\Delta\phi = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right]^{1/2} \tag{2.19}$$

with E_m being the maximum electric field and being given by

$$E_m = \left[\frac{2qN_DV_i}{\varepsilon_s\varepsilon_0}\right]^{1/2} \tag{2.20}$$

2.4.5 Image-force lowering of the barrier

When an electron is at a distance x from the metal, a positive charge will be induced on the metal surface. The force of attraction between the electron and the induced positive charge is equivalent to the force that would exist between the electron and the image charge located at $-x$. The image force is given by

$$F = \frac{-q^2}{16\pi\varepsilon_s x^2} \tag{2.21}$$

where ε_s is the permittivity of the semiconductor. The work done by an electron due to its transfer from infinity to the point x is given by

$$V(x) = \int_{\infty}^{x} F dx = \frac{q^2}{16\pi\varepsilon_s x}. \tag{2.22}$$

The energy above corresponds to the potential energy of an electron at distance x from metal surface, shown in Fig. 2.6, and is measured downwards from the x axis. When an external field E is applied, the total potential energy PE is given by

$$PE(x) = \frac{q^2}{16\pi\varepsilon_s x} + qEx \tag{2.23}$$

The maximum potential energy occurs at a position x_m where the resultant electric field is zero; i.e. the field due the image force is equal and opposite to the field in the depletion region, or

$$\frac{q}{16\pi\varepsilon_s x_m^2} = E_m \tag{2.24}$$

where E_m is the maximum electric field. As a result of the image force, the maximum potential in the barrier is lowered by an amount

$$\Delta\phi = x_m E_m + \frac{q}{16\pi\varepsilon_s x_m} = 2x_m E_m = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}} \tag{2.25}$$

The value ε_s may be different from the semiconductor static permittivity, as during the emission process, the electron transit time from metal-semiconductor interface to the barrier maximum x_m is shorter than the dielectric relaxation time, the semiconductor medium does not have enough time to be polarized, and smaller permittivity than the static value is expected [3].

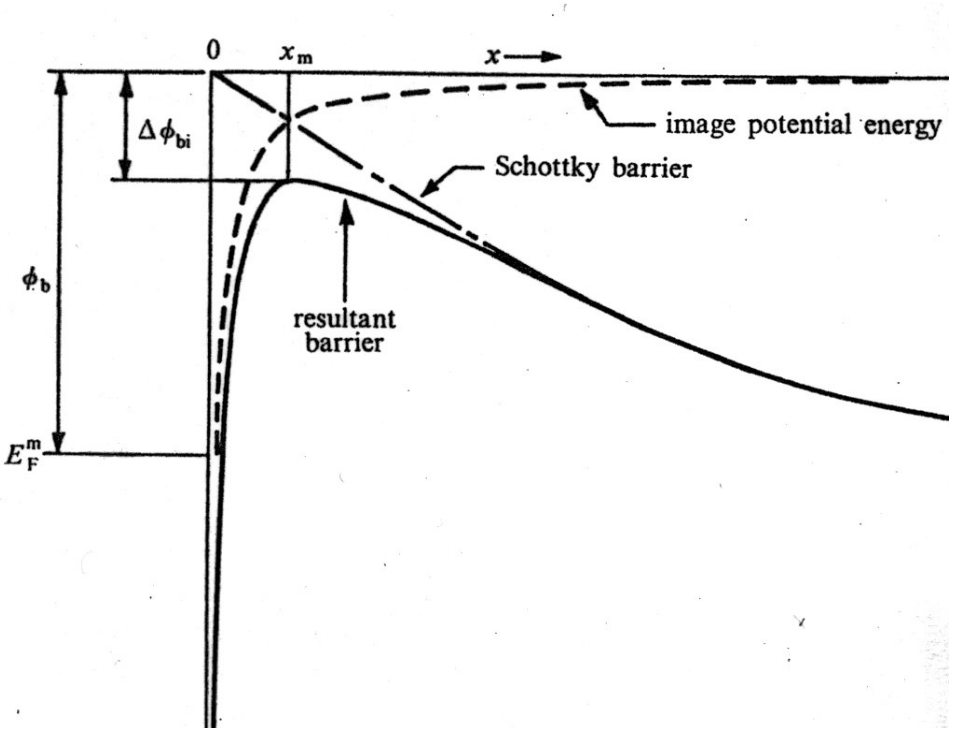


Fig. 2.6 *Image-force lowering of barrier, redrawn from ref. 22.*

2.4.6 Ohmic contact

An ohmic contact is a metal-semiconductor contact that has a negligible contact resistance R_c, relative to the bulk of the semiconductor. The contact resistance is defined as the reciprocal of the derivative of current density with respect to voltage. When evaluated at zero bias the contact resistance is given by

$$R_c = \left(\frac{\partial J}{\partial V} \right)_{V=0}^{-1}. \tag{2.26}$$

A satisfactory ohmic contact should not significantly perturb device performance, and it can supply the required current with a voltage drop that is sufficiently small compared with the drop across the active region of the device [3]. To achieve ohmic contacts to semiconductors, for an *n*-type semiconductor, the metal work function, ϕ_m must be less than that of the semiconductor ϕ_s as depicted in Fig. 2.7 (a) and (b), and ϕ_m must be greater than ϕ_s in case of a *p*-type semiconductor. For an n-type semiconductor at equilibrium, electrons are transferred from the metal to the semiconductor, resulting in the aligning of the Fermi Levels.

This raises the semiconductor energy bands, reducing the barrier to electron flow between the metal and semiconductor.

A more practical ohmic contact is a tunnel contact, shown in Fig. 2.7 (c). Such contacts have a high doping in the semiconductor such that there is only a thin barrier separating the metal from the semiconductor, and carriers can easily tunnel across the barrier. The doping density to achieve a tunnel contact should be 10^{19} cm^{-3} or higher.

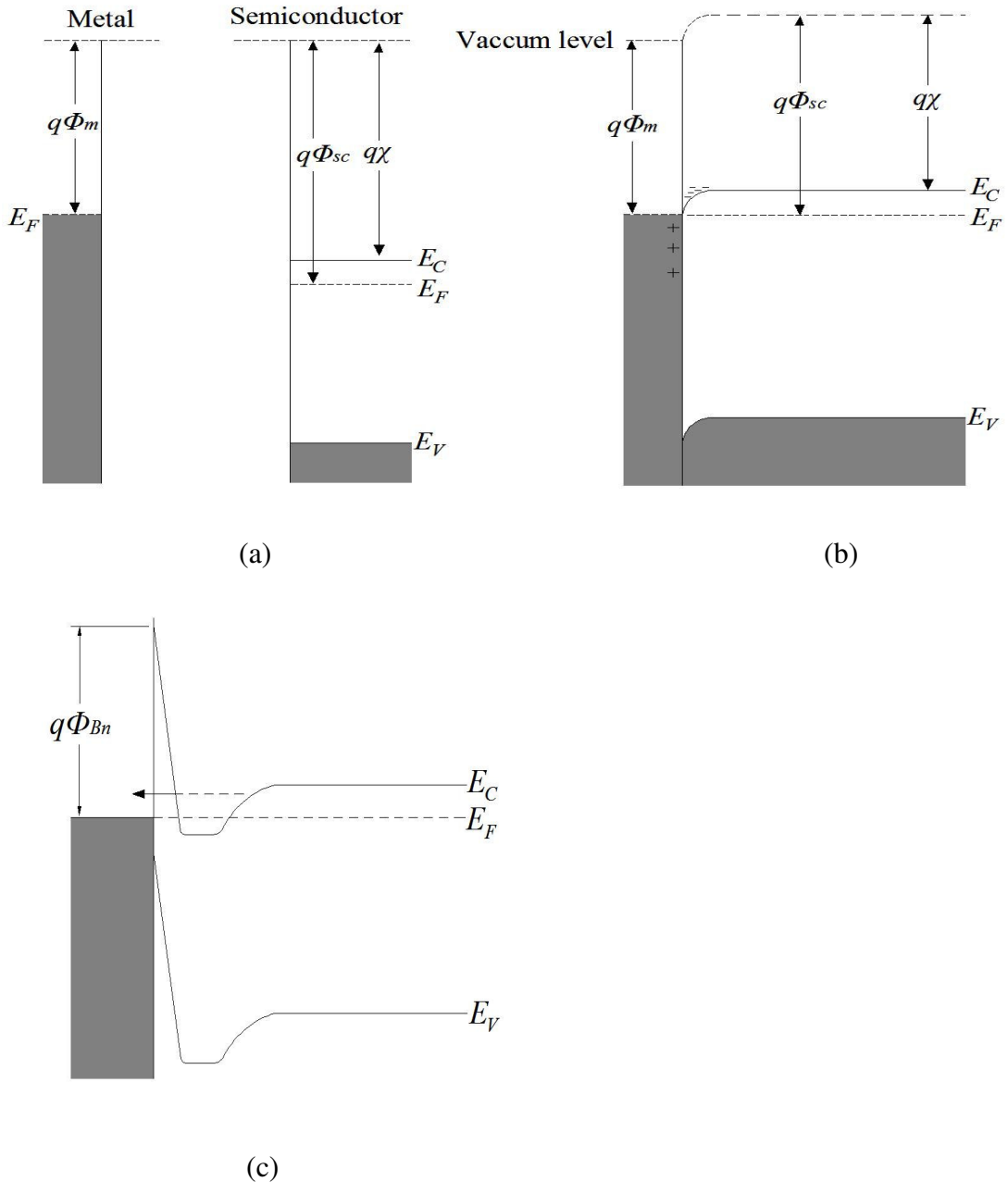


Fig. 2.7 *Energy band diagrams of a metal/n-type semiconductor with* $\Phi_m < \Phi_{sc}$.

2.4.7 Current transport mechanisms

The current transport in metal-semiconductor contacts is mainly due to majority carriers, unlike in p-n junction, where the minority carriers are responsible. There are four main mechanisms by which carrier transport can occur in Schottky barriers in forward biased direction [3]. The transport mechanisms are shown in Fig. 2.8. The mechanisms are:

A: thermionic emission over the potential barrier into the metal,

B: quantum-mechanical tunnelling through the barrier (important for heavily doped semiconductors and responsible for most ohmic contacts),

C: recombination and/or generation in the space charge region, and

D: hole injection from the metal to the semiconductor (equivalent to recombination in the neutral region).

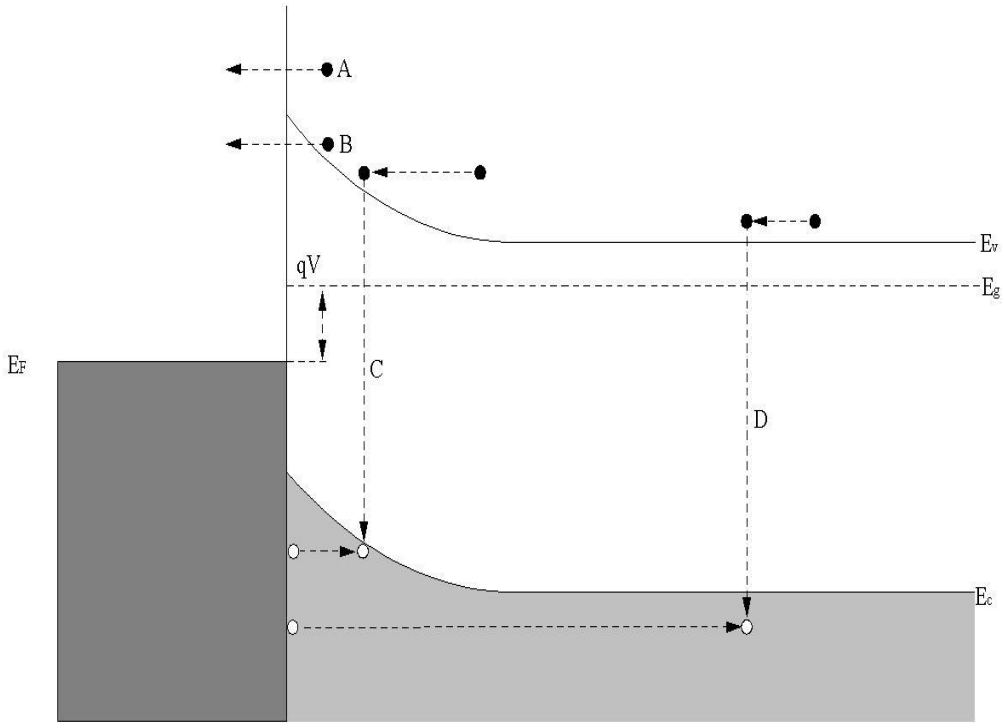


Fig. 2.8 *Current transport mechanisms redrawn from ref. 22.*

2.4.7.1 *Thermionic emission current.*

This mechanism is dominant for Schottky diodes with moderately doped semiconductors operated at moderate temperatures (e.g. 300 K) [3]. Emission of electrons over the barrier into the metal are governed by two basic processes, (i) electrons are transported from the interior of the semiconductor to the interface by the mechanism of drift and diffusion in the electric field of the barrier, and (ii) at interface, their emission into the metal is determined by the rate of transfer of electrons across the boundary between the metal and the semiconductor. These two processes are effectively in series, and the current is determined predominantly by whichever causes the larger impediment to the flow of electrons [22]. For high-mobility semiconductors (e.g. Si and Ge) the current transport can be described by the thermionic emission theory by Bethe [23] using the assumptions that the barrier height ϕ_{Bn} is much larger than kT, thermal equilibrium established at the plane that determines emission, and the existence of a net current flow does not affect thermal equilibrium so that one can superimpose two current fluxes. Because of these assumptions, the shape of the barrier profile is immaterial and current flow depends solely on the barrier height [3]. The current density $J_{s\to m}$ from the semiconductor to the metal can be expressed as:

$$J_{s\to m} = \int_{E_F+q\phi_B}^{\infty} qv_x dn \tag{2.27}$$

where $E_F + q\phi_B$ is the minimum energy required for thermionic emission into metal, and v_x is the carrier velocity in the direction of transport. The electron density can be expressed in an incremental range as:

$$dn = N(E)F(E)dE$$

$$= \frac{4\pi(2m^*)^{\frac{3}{2}}}{h^3}\sqrt{E-E_c}\exp[-(E-E_c+qV_n)/kT]dE \tag{2.28}$$

where $N(E)$ and $F(E)$ are the density of states and the distribution function, respectively; m^* is the effective mass of the semiconductor; and qV_n is $(E_C - E_F)$.

Postulating that all the energy of electrons in the conduction band is kinetic energy, then

$$E - E_C = \frac{1}{2} m^* v^2$$

$$dE = m^* v dv$$

$$\sqrt{E - E_C} = v\sqrt{m^*/2}. \tag{2.29}$$

Substituting Eq. (2.29) into Eq. (2.28) results

$$dn = 2\left(\frac{m^*}{h}\right)^3 \exp\left(-\frac{qV_n}{kT}\right)\exp\left(\frac{-m^* v^2}{2kT}\right)(4\pi v^2 dv) \tag{2.30}$$

Eq. (2.30) gives the number of electrons per unit volume with speeds between v and $v + dv$ distributed over all directions [3]. Resolving the speed into components along the axes with the x axis parallel to the transport direction, we have

$$v^2 = v_x^2 + v_y^2 + v_z^2 \tag{2.31}$$

With the transformation $4\pi v^2 dv = dv_x dv_y dv_z$ we obtain from Eqs. (2.27), (2.30) and (2.31)

$$J_{s\to m} = \left(\frac{4\pi q m^* k^2}{h^3}\right) T^2 \exp(-\frac{qV_n}{kT})\exp\left(-\frac{m^* v_{ox}^2}{2kT}\right) \tag{2.32}$$

where v_{ox} is the minimum velocity required in the x direction to surmount the barrier and is given by

$$\frac{1}{2} m^* v_{ox}^2 = q(V_d - V) \tag{2.33}$$

where V_d is the built-in potential at zero bias. Substituting Eq. (2.33) into (2.32) we get

$$J_{s\to m} = \left(\frac{4\pi q m^* k^2}{h^3}\right) T^2 \exp\left(-\frac{q(V_n + V_d}{kT}\right)\exp\left(\frac{qV}{kT}\right)$$

$$= A^{*}T^{2}\exp\left(-\frac{q\phi_B}{kT}\right)\exp\left(\frac{qV}{kT}\right) \tag{2.34}$$

where ϕ_B is the barrier height and equals the sum of V_n and V_d , and

$$A^{*} = \frac{4\pi q m^{*} k^{2}}{h^{3}} \tag{2.35}$$

is the effective Richardson constant for thermionic emission.

Since the barrier height for electrons moving from the metal into the semiconductor remains the same, the current flowing into the semiconductor is thus unaffected by the applied voltage [3]. It must therefore be equal to the current flowing from the semiconductor into the metal when equilibrium prevails (i.e., when $V = 0$). The corresponding current density at equilibrium is

$$J_{m\to s} = -A^{*}T^{2}\exp\left(-\frac{q\phi_B}{kT}\right) \tag{2.36}$$

The total current density is given by the sum of Eqs.(2.34) and (2.36).

$$J_n = \left[A^{*}T^{2}\exp\left(-\frac{q\phi_B}{kT}\right)\right]\left[\exp\left(\frac{qV}{kT}\right)-1\right]$$

$$= J_{ST}\left[\exp\left(\frac{qV}{kT}\right)-1\right] \tag{2.37}$$

where J_{ST} is the saturation current density given by

$$J_{ST} = A^{*}T^{2}\exp\left(-\frac{q\phi_B}{kT}\right) \tag{2.38}$$

Eq. 2.37 is the current density of an ideal diode. For a non-ideal diode, the series resistance R_s, and the ideality factor, n need to be factored into Eq. (2.37). The resulting expression becomes,

$$J_n = J_{ST} \exp\left[\frac{q(V - IR_s)}{nkT}\right]\left(1 - \exp\left[-\frac{q(V - IR_s)}{kT}\right]\right) \tag{2.39}$$

The ideality factor is obtained as the gradient of the slope of the linear region of the semi logarithmic *I-V* plot and is given by [3]

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \tag{2.40}$$

2.4.7.2 *Quantum-mechanical tunnelling.*

This is usually the dominant transport mechanism in a heavily doped semiconductor at low temperatures. The current in the forward direction arises from the tunnelling of electrons with energies close to the Fermi energy in the semiconductor. This is known as 'field' emission [22]. If the temperature is raised, electrons are excited to higher energies and tunnelling probability increases very rapidly because the electrons 'see' a thinner and lower barrier. Although the number of excited electrons decrease very rapidly with increasing energy, there is a maximum contribution to the current from electrons which have energy well above the bottom of the conduction band. This mechanism is known as thermionic-field emission. When the tunnelling current dominates the current flow, the transmission coefficient is given by [3]

$$T(\eta) \approx \exp\left(-\frac{q\phi_B}{E_{00}}\right) \tag{2.41}$$

where E_{00} is the characteristic energy level given by

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon_s m^*}} \tag{2.42}$$

The tunnelling current density is given by

$$J_t = \exp\left(-\frac{q\phi_B}{E_{00}}\right) \tag{2.43}$$

2.4.7.3 *Generation recombination current.*

This mechanism is as a result of the generation and recombination of carriers within the space charge region. The recombination normally takes place via localized centres, and the most effective centres are those with the energies lying near to the centre of the gap. The theory of the current due to such a recombination centre is the same for a Schottky diode as for p-n junction [22], and the current density is given by

$$J_r = J_{r0}\exp\left(\frac{qV}{2kT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{2.44}$$

where $J_{r0} = qn_i w/2\tau_r$, n_i is the intrinsic electron concentration, proportional to $\exp(-qE_g/2kT)$, w is the depletion width and τ_r is the lifetime within the depletion region. The two main processes for recombination are direct and indirect recombination [24]. In the direct recombination process, an electron falls from the conduction band and recombines directly with a hole in the valence band. This is also called band to band recombination. This process is common as radiative transitions in direct bandgap semiconductors. For this process energy is conserved as the electrons and holes recombining are located close to the band edges of the semiconductor. In indirect recombination, an electron falls into a trap where it can later recombine with a hole.

2.4.8 Barrier height determination

The Schottky barrier height of a metal-semiconductor contact can be determined by current – voltage (*I-V*) and the capacitance-voltage (*C-V*) measurement techniques. First, considering the *I-V* measurement technique, the barrier heights are deduced from the *I-V* characteristics, which are analysed by the thermionic emission model given by the Eq. (2.37). The extrapolated value of current at zero voltage in the semi-log forward bias *ln I-V* characteristics is the saturation current I_o, and the barrier height can be obtained from the equation

$$\phi_{Bn} = \frac{kT}{q}\ln\left(\frac{A^* AT^2}{I_0}\right) \tag{2.45}$$

where A is the diode effective are.

The barrier height can also be determined using the capacitance-voltage measurement technique. In this technique, the concept of the induced or image charge in the metal and semiconductor is used. To use this type of method for barrier height determination, it must be assumed that the diode should be nearly ideal such that the doping concentration remains uniform in the semiconductor. From the plot of $1/C^2$ *vs* V, the barrier height can be calculated as given in Eq. (2.18).

2.4.9 Barrier height inhomogeneities

The most interesting form of Schottky barrier height (SBH) inhomogeneity is the presence of small regions of the metal-semiconductor interface with a low SBH, embedded in an interface with an otherwise uniform high SBH [25]. This will result in the lateral variations of the electrostatic potential at the interface, causing the current to flow preferentially through the lower barriers in the potential distribution [26]. Assuming a Gaussian distribution of the inhomogeneous barrier heights with a mean value $\bar{\phi}_B$ and a standard deviation σ_s in the form [27]:

$$P(\phi_B) = \frac{1}{\sigma_s \sqrt{2\pi}} \exp\left(\frac{(\phi_B - \bar{\phi}_B)^2}{2\sigma_s^2} \right) \tag{2.46}$$

where $1/\sigma_s \sqrt{2\pi}$ is the normalization constant. The total current $I(V)$ is given by [27]

$$I(V) = \int_{-\infty}^{+\infty} I(\phi_B, V) P(\phi_B) d\phi \tag{2.47}$$

On integration

$$I(V) = A^* A T^2 \exp\left(-\frac{q\phi_{ap}}{kT} \right) \exp\left(\frac{qV}{n_{ap} kT} \right) \left[1 - \exp\left(-\frac{qV}{kT} \right) \right] \tag{2.48}$$

with

$$I_0 = A^* A T^2 \exp\left(-\frac{q\phi_B}{kT} \right) \tag{2.49}$$

where I_0 is the saturation current, ϕ_{ap} and n_{ap} are the apparent barrier height and apparent ideality factor at zero bias respectively:

$$\phi_{ap} = \bar{\phi}_{B0(T=0)} - \frac{q\sigma_{s0}^2}{2kT} \tag{2.50}$$

and

$$\left(\frac{1}{n_{ap}} - 1\right) = \rho_2 - \frac{q\rho_3}{2kT} \tag{2.51}$$

It is also assumed that the standard deviation σ_s and the mean value of the Schottky barrier height $\bar{\phi}_B$ are linearly bias-dependent on Gaussian parameters that are given by $\bar{\phi}_B = \bar{\phi}_{B0} + \rho_2 V$ and $\sigma_s = \sigma_{s0} + \rho_3 V$, where ρ_2 and ρ_3 are the voltage coefficient that may depend on temperature (T) and they quantify the voltage deformation of the barrier height distribution [27,28]. The decrease of zero-bias barrier height is caused by the existence of the Gaussian distribution and the extent of influence is determined by the standard deviation itself [26,27]. The effect is particularly significant at low temperatures, as at low temperatures, charge carriers have very low energies to surpass the barrier, tunnelling of electrons is the dominant process. Because the barrier is non-homogeneous, further tunnelling through the low barrier regions cause the deviation of the barrier height from the value that could be obtained for a uniformly distributed barrier at the metal-semiconductor interface [29]. From Eq. (2.50), the plot of ϕ_{ap} versus 1000/T should be a straight line giving $\bar{\phi}_{B0}$ and σ_{s0} from the intercept and slope respectively. The standard deviation is a measure of the barrier homogeneity. The lower the value of σ_{s0} corresponds to a more homogeneous barrier height and better diode rectifying properties.

Following the barrier height inhomogeneities correction, the Richardson plot is modified by combining Eqs. (2.49) and (2.50):

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_{s0}^2}{2k^2T^2}\right) = \ln(A^{**}A) - \frac{q\bar{\phi}_{B0}}{kT} \tag{2.52}$$

where A^{**} is the modified Richardson constant. A plot of the modified $\ln\left(\frac{I_0}{T^2}\right)-\left(\frac{q^2\sigma_{s0}^2}{2k^2T^2}\right)$ versus 1000/T yields a straight line with the slope giving the mean barrier height and the intercept giving the modified Richardson constant.

2.5 Annealing studies and germanides formation

Annealing is a heat treatment wherein a material is altered, causing changes in its properties [30]. Isothermal annealing is when the heat treatment is carried out at a constant temperature, and isochronal annealing, is when the heat treatment is carried out at constant time duration. Annealing occurs by the diffusion of atoms within a solid material, so that the material progresses towards its equilibrium state. To avoid oxidation, annealing is carried out in Ar gas. The solid state reaction at subeutectic temperatures between a thin metal film and a single-crystal semiconductor has attracted much interest because of its importance in Schottky barrier and contact formation, epitaxial growth and device reliability [31]. Inter-diffusion, contaminations, chemical reaction, compound formation, interface roughening, defect generation, dopant migration, etc. can all be derived by thermodynamics due to the thermal annealing [32]. It is well known that the chemical reactions between metals and semiconductors at an interface can play an important role in the electrical properties of devices. During the annealing process, metals may react with germanium and new compounds (germanides) would form, resulting in the change of barrier heights. Hence, the change of barrier heights may be attributed to the combined effects of interfacial reaction and phase transformation [33]. Thermal degradation at high annealing temperatures includes two mechanisms: agglomeration and phase transformation [34]. Agglomeration starts with grain boundary grooving and results in islands formation. Agglomeration is driven by the minimization of the total surface/interface energy of the germanide and germanium substrate [35]. In this work, the effects of thermal treatment on the electrical and morphological evolution characteristics of metal germanides at different annealing temperatures were investigated.

2.6 Fundamentals of defects in semiconductors

2.6.1 Introduction

It is generally known that a perfect crystal lattice does not exist in real crystals. Defects or imperfections are always found in all crystalline solids. The existence of defects has a profound effect on the physical properties of a crystal. These imperfections may introduce electronic energy states into the semiconductor bandgap, either as shallow levels or deep levels. Shallow level defects are located near the valence band for acceptors and conduction band for donors. These shallow levels, which are ionized at room temperature, are normally created by impurity elements used as dopants in semiconductors and provide free carriers to form *p*-type or *n*-type semiconductor. Deep level defects are those found deeper in the band gap than dopant levels. The deep levels do not contribute much to the free charge carriers, as they have higher ionization energies. The deep level defects act either as traps or as recombination centres in the semiconductors, depending on the capture cross section of the electrons and holes [36]. The semiconductor free carrier density is reduced by traps, whereas recombination centres introduce generation-recombination currents in rectifying devices. In the electronic industry the trap-induced carrier reduction is utilised to form areas of high resistivity for device isolation [36]. Depending on the application, these defects may either be beneficial or detrimental for optimum device functioning [37]. The discussion in this section is more focused on the vacancy defects, interstitial defects, the *E*-centre and the *A*-centre.

2.6.2 Vacancy Defect

A vacancy defect (V) is created when an atom moves out of its regular site, and is shown in Fig. 2.9. A vacancy lattice site is considered as the simplest of all defects [38]. In some semiconductors (e.g. Ge), the vacancy can have up to five charge states, V^{++}, V^{+}, V^{0}, V^{-} and $V^{=}$.

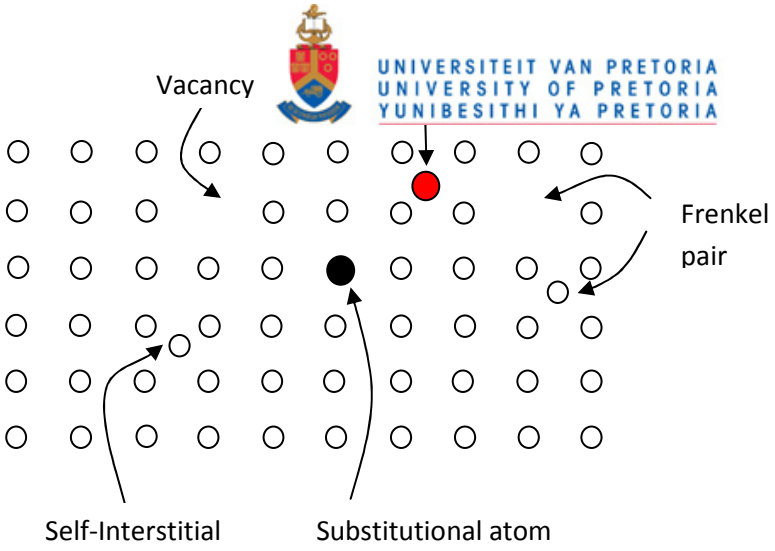
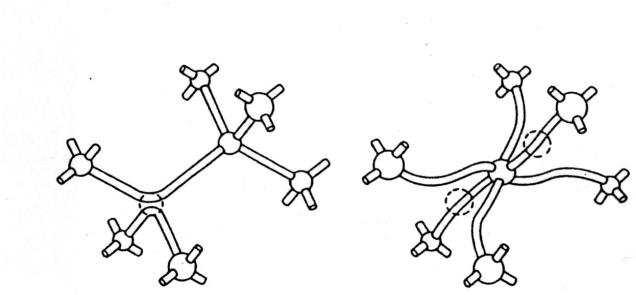


Fig. 2.9 *Schematic representation of the vacancy, Interstitial and Substitutional defects*

Fig. 2.10 (a) depicts a vacancy defect in a diamond lattice. In order to form a vacancy, four bonds are broken. The broken bonds (dangling) bonds can form new bonds leading to atomic displacements [39]. The number of electrons which occupy these dangling bonds depend on the charge state of the vacancy. These small atomic displacements of the neighbours of the vacancy can be inward or outward displacements, which may either, preserve the local symmetry (relaxation) or alter it (distortion). The amplitude of these displacements as well as the new symmetry depends on the type of the bonding [39]. The split-vacancy is shown in Fig. 2.10 (b), where a one neighbour of the vacancy is displaced half way between its original position and the centre of the vacancy. This configuration is also known as the saddle-point configuration for vacancy migration in the diamond lattice. The split-vacancy is often important primarily to help describe the transition state in vacancy migration [40]. The divacancy results from the removal of two neighbouring atoms. In general the divacancies can be created in semiconductors by particle irradiation either as a primary defect (when collision casacade is dense enough) or as a secondary defect by pairing of single vacancies diffusing randomly.



(a) (b)

Fig. 2.10 *Configuration of (a) the vacancy in a diamond lattice and (b) the saddle-point.*

2.6.3 Interstitial Defect

An interstitial defect is due to an atom occupying a site in the crystal structure, which is not its regular lattice site as depicted in Fig. 2.9. It can be of the same species as the atoms of the lattice or of different species (interstitial impurity). The energy of formation of an interstitial defect is higher than the corresponding energy for a vacancy. The introduction of interstitial results in large lattice strain, and the motion of such defect reduce this strain; hence interstitial occurs more readily than a vacancy. In radiation damage, interstitials and vacancies occur in equal numbers, and more often the interstitial is associated with a nearby vacancy, the vacancy having resulted from the same collision event. This Frenkel or interstitial-vacancy pair can be taken as a single defect.

2.6.4 The E-centre and A-centre

The *E*-centre or vacancy-donor pair is the dominant defect produced in electron- or gamma-irradiated float zone silicon, oxygen lean silicon-germanium and germanium [41]. The *E*-centre results from a vacancy trapped next to a substitutional donor atom. It can form either as a primary defect or when the impurity atom captures a mobile vacancy. It has been found that the *E*-centre has at least three charge states in Ge: the double negative, the single negative, and the neutral [42]. For the V-Sb pair, the ionization enthalpy of the double-acceptor is $\Delta H_{na} = 0.377$ eV as determined by reverse biasing DLTS [43,44], and that of the single acceptor is $\Delta H_{pa} = 0.307$ eV as determined by forward-pulsing DLTS [43,44]. The *A*-centre or vacancy-oxygen complex is produced when a vacancy is trapped next to an oxygen atom in an interstitial position. Also an *A*-centre defect can be formed as a primary defect or when an oxygen impurity traps a mobile vacancy. The *A*-centre defect concentration is dependent on the O impurity concentration in the sample. The *A*-centre is a dominant defect induced by irradiation with high energy particles (electrons, protons, etc) in Si crystals grown by the Czochralski method [45] and oxygen-rich Ge crystals [46]. In Si the *A*-centre is known to exist in two charge states: singly negatively charged and neutral with the corresponding acceptor level at about E_c-0.17 eV [46,47]. It was argued in Refs. [48,49] that the *A*-centre in Ge has three charge states, double negative (VO^{--}), singly negative (VO^{-}) and neutral (VO^{0}) and confirmed by Markevich et al. [46] that the E_cń 0.21 eV and E_v+0.27 eV traps in Ge are related to (--/-) and (-/0) levels of the *A*-centre.

2.7 Aspects of Deep Level Transient Spectroscopy

2.7.1 Introduction

Deep levels are quantum states which are within the forbidden bandgap of the semiconductor; deep levels influence the electrical and the optical properties of semiconductor materials. Since deep level defects can be detrimental to or enhance the operation of devices fabricated on semiconductors, it is important to know the electrical properties of these deep levels. Many processes that occur in deep levels are nonradiative, and therefore cannot be observed by optical techniques. Deep level transient spectroscopy (DLTS) is one of the techniques used to determine the electrical properties of deep defects.

2.7.2 Deep level transient spectroscopy

In this study, deep level transient spectroscopy (DLTS) was used to evaluate and characterise the electrically-active defects induced in Ge Schottky contacts during contact fabrication and annealing processes. This is a powerful and sensitive high-frequency capacitance transient thermal scanning technique, which is useful for observing traps in semiconductors. This technique was developed by Lang [50] in 1974, and it monitors the change in capacitance of the depletion layer of a p-n junction or Schottky diode as a result of charge transfer between the deep levels and conduction or valence bands. It displays the spectrum of traps in a crystal as positive and negative peaks on a flat baseline as a function of temperature. The sign of the peak shows whether the deep level is near the valence band or conduction band, the height of the peak is proportional to the trap concentration, and the position, in temperature, of the peak is determined by the thermal emission properties of the trap [50]. Furthermore, one can measure the activation energy, and electron- and hole-capture cross sections for each trap.

2.7.3 Emission and capture of carriers by trapping centres

Whenever the thermal equilibrium condition of a system is perturbed, there are processes that take place to restore the system to equilibrium. This may involve the emission and capture of the electrons and holes. A defect level is defined as an electron trap as one which tends to have deficiency of electrons, and thus capable of capturing them from the conduction band. Likewise, a hole trap is one which is full of electrons, and thus capable of having a trapped electron recombining with a hole [50]. An electron trap occurs when the electron capture rate

c_n from the conduction band is much larger than the hole capture rate c_p from the valence band, i.e. $c_n >> c_p$, and a hole trap has to have $c_p >> c_n$. A recombination centre is one for which c_n and c_p are almost similar, i.e. $c_n \approx c_p$. Fig. 2.11 depicts the four common processes that a deep level (E_T) can interact with the conduction band and the valence band. If the trap is neutral it may capture an electron from the conduction band (Fig. 2.11 (a)), characterized by c_n. After an electron capture, one of the two events can take place, the centre can either emit the electron back to the conduction band, i.e. electron emission e_n (Fig. 2.11 (b)), or it can capture a hole from the valence band, depicted in Fig 2.11 (c) as c_p. Similarly for a hole trap, occupied by a hole, either it emits the hole back to the valence band e_p in Fig 2.11 (d) or captures an electron (Fig. 2.11 (a)).

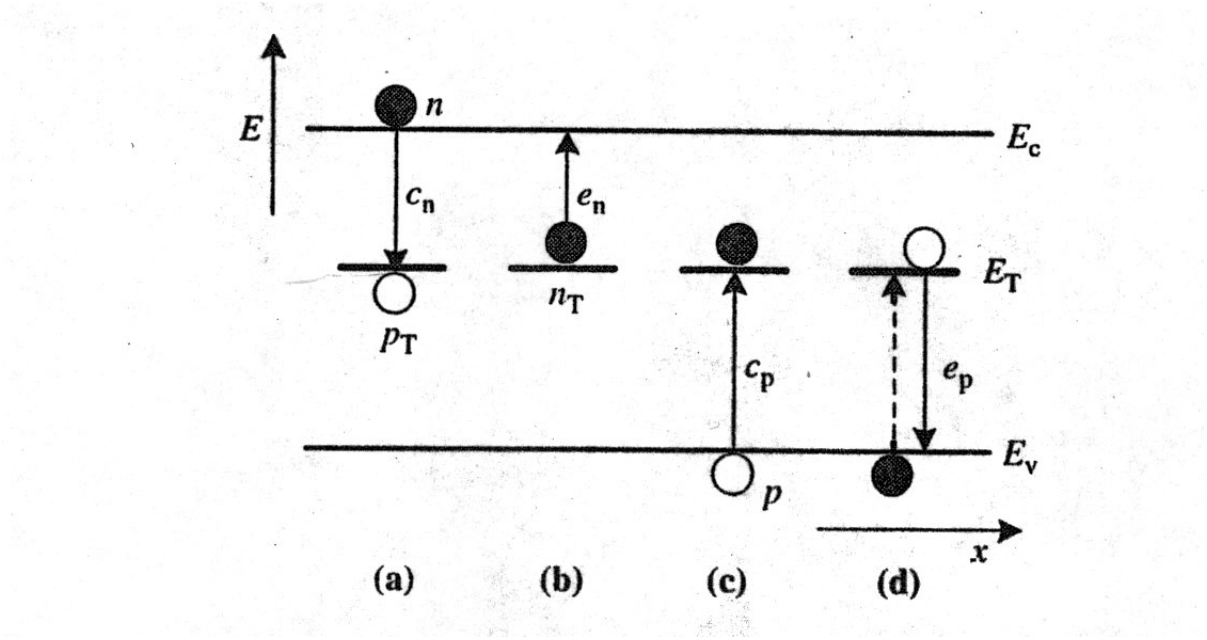


Fig. 2.11 *Emission and capture processes involved by trapping at a deep level E_T.*

Shockley et al. [51], Hall [52] and Bourgoin et al. [53], have extensively discussed the kinetics of emission and capture of carriers from defect levels. The electron and hole capture rates are given by:

$$c_n = \sigma_n < v_n > n, \tag{2.53}$$

$$c_p = \sigma_p < v_p > p, \tag{2.54}$$

where σ_n and σ_p are defect's capture cross-sections for capturing electrons and holes respectively, and n is the electron concentration, p is the hole concentration and $<v_n>$ is the average electron thermal velocity:

$$< v_n >= \sqrt{\left(\frac{3kT}{m^*}\right)} \tag{2.55}$$

where m^* is the effective mass of the electron, k is the Boltzmann constant, and T is the temperature in Kelvin. A similar equation can be written for v_p. The thermal emission rate e_n, of electrons deep level to the conduction band is proportional to the Boltzmann factor $\exp(-E_T/kT)$, and can be written as [54,55]

$$e_n(T) = \frac{\sigma_n < v_n > N_C}{g} \exp\left[-\frac{\Delta E_T}{kT}\right] \tag{2.56}$$

where $\Delta E_T = E_C - E_T$, is the activation energy of the defect level, g is the degeneracy of the defect level, T is the temperature in Kelvin, N_C is the effective density of states in the conduction band given by

$$N_C = 2M_C\left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}} \tag{2.57}$$

where M_C is the number of conduction-band minima, h is Planck's constant. The emission rate for holes is also expressed in an analogous way.

If the capture cross-section of the defect is assumed to be independent of temperature, the product $< v_n > N_C$ in Eq. (2.56) has T^2 dependence. It follows that an Arrhenius plot of $\ln\left(\frac{e_n}{T^2}\right)$ as a function of $\frac{1}{T}$ should be a linear relationship from which the defect's energy E_T and capture cross-section σ_n may be determined. These two parameters are referred to as the defect's signature. The defect signature is one of the essential parameters used to identify a defect during electrical characterization. If the capture cross-section is assumed to be temperature-dependent, it takes the form [56]:

$$\sigma_n(T) = \sigma_\infty \exp\left(\frac{\Delta E_\sigma}{kT}\right) \tag{2.58}$$

where σ_∞ is the capture cross-section extrapolated to $T = \infty$ and ΔE_σ is the thermal activation energy of the capture cross-section (i.e. thermal barrier for carrier capture). The temperature dependence of a capture cross-section may be determined from the plot of $\ln(\sigma_n)$ versus $\frac{1}{T}$, where ΔE_σ is extracted from the slope and σ_∞ after extrapolation to $T = \infty$. The corrected activation energy for a deep level which exhibits a temperature-dependent capture cross-section is given by

$$\Delta E_a = \Delta E_T + \Delta E_\sigma \tag{2.59}$$

A more general expression of the thermal emission rate can now be written as,

$$e_n(T) = \frac{\sigma_n < v_n > N_C}{g} \exp\left[-\frac{\Delta E_T + \Delta E_\sigma}{kT}\right] \tag{2.60}$$

The parameter ΔE_T, is the Gibbs free energy change for the ionization of the state given by [57]

$$\Delta E_T = \Delta H - T\Delta S \tag{2.61}$$

where ΔH and ΔS are the changes in enthalpy and entropy due to the change in charge state of the level. Substituting Eq. (2.61) into 2.56 yields

$$e_n(T) = \frac{\sigma_n < v_n > N_C}{g} \exp\left[-\frac{\Delta S}{k}\right] \exp\left[-\frac{\Delta H}{kT}\right] \tag{2.62}$$

Therefore, the Arrhenius plot yields the activation enthalpy of the deep level, and not the free energy, which can only be determined from the optical measurements [54,55].

2.7.4 Capacitance transient

The DLTS technique uses a fast, sensitive capacitance meter to measure the capacitance of a reverse-biased Schottky, MOS or p-n junction [50]. This discussion is limited to Schottky barrier diodes. The capacitance of a reverse-biased diode is related to the width of the depletion region (Eq. (2.15)), which also depends on the charge in the depletion region

(Eq. (2.11)), due to dopants as well as deep defects. When a reverse bias is applied to the metal-semiconductor system, a space-charge region is created i.e. region depleted of mobile free carriers. In this space-charge region there are ionised impurities. If the trapped charges in deep levels, in this space-charge region can be altered then the occupancy can be detected by monitoring the junction capacitance.

Consider a Schottky diode on an *n*-type semiconductor, as shown in Fig. 2.12 (1), with an electron trap which introduces a deep level trap E_T . The deep levels under the Fermi level are assumed to be filled and those above are empty as governed by the Fermi distribution function. In Fig. (2.12), shaded and open circles indicate filled and empty traps respectively.

At the start of the DLTS cycle, a majority carrier filling pulse is applied across the diode (Fig. 2.12 (2)). This pulse will collapse the space-charge region, increasing the capacitance of the Schottky diode drastically, and trapping electrons in those levels that are now below the Fermi level. After the filling pulse is removed, the reverse bias is returned to its quiescent level (Fig. 2.12 (3)). The increase in the reverse bias increases the width of the depletion region again. Since some of the deep level traps in the space-charge region are filled, the charge density in the space-charge region is less than it was in Fig. 2.12 (1). Therefore the depletion width is slightly wider and the capacitance slightly lower than it was in (1). This excess charge in the space-charge region may be transferred to the conduction band through the emission process as depicted in Fig. 2,12 (4), causing the charge density in the depletion region to increase, reducing its width and increasing the capacitance of the junction. The density of occupied defect levels at time t after removing the filling pulse is given by [55].

$$N(t) = N_T \exp(-e_n t) \tag{2.63}$$

where e_n is the electron thermal emission rate and N_T is the defect concentration. If it is assumed that $N_T << N_D$, there will not be much change in the depletion width during the emission of carriers. Therefore it is assumed that the emission of carriers from the space-charge region may be described by an exponential decay (Eq. (2.63)). The capacitance of the Schottky diode is assumed to have the form:

$$C(t) = C_\infty - \Delta C \exp(-e_n t) \tag{2.64}$$

where $C(t)$ is the capacitance transient at time t, C_∞ is the quiescent reverse bias capacitance at time $(t) = \infty$ and ΔC is the difference between C_∞ and the capacitance measured at $(t) = 0$. The concentration of a specific trap can be determined from the change in capacitance as a function of the region being sampled. If the carrier charge density N_D and trap level concentration N_T are spatially uniform, and N_T is much lower than N_D, then the defect concentration is given by the following approximation

$$N_T \approx 2N_D \frac{\Delta C}{C} \tag{2.65}$$

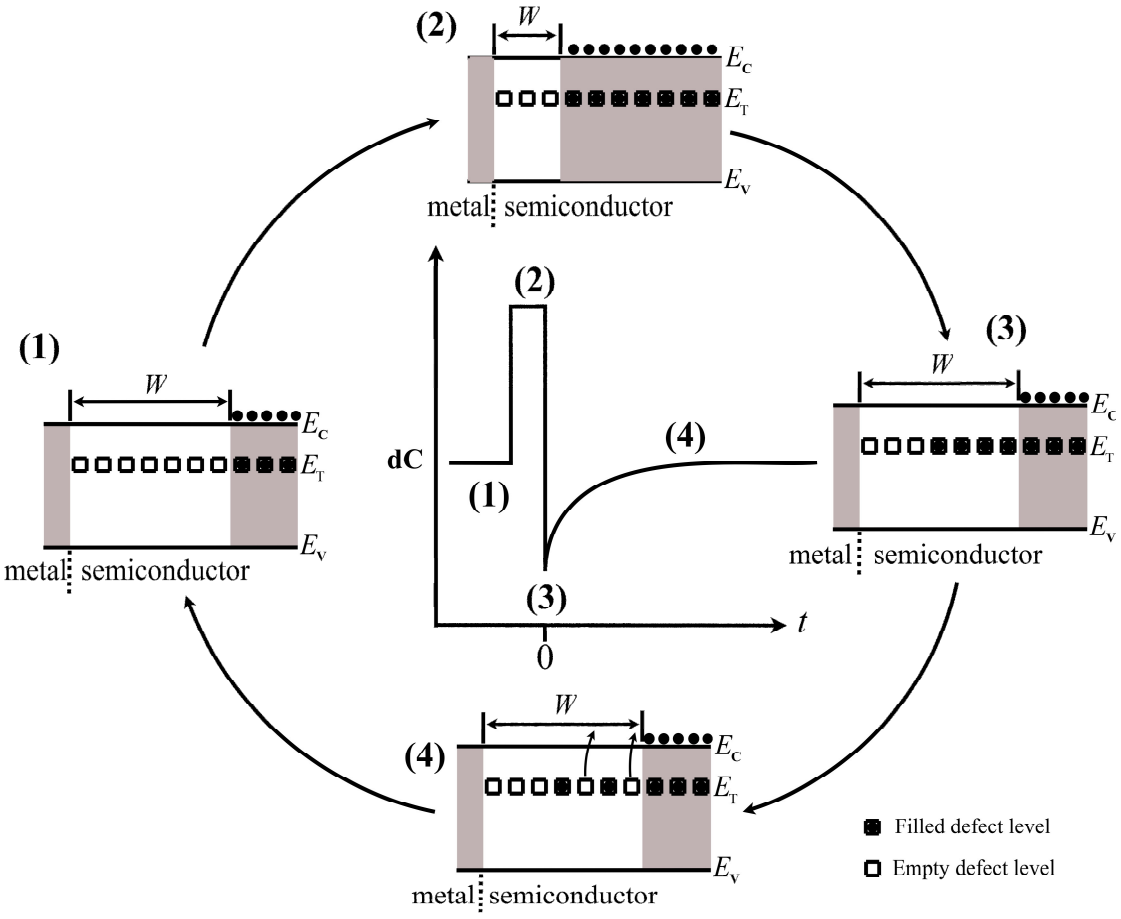


Fig. 2.12 *The capacitance transient due to an electron trap in n-type material. (1): Quiescent state, (2): Filling pulse, (3) Reverse bias; (4) Exponential decay as carriers are emitted.*

2.7.5 *Principles of DLTS*

Lang [50] introduced the 'rate window' concept to deep level characterization. The measurement system produces a maximum output only when a transient with a rate within this narrow window occurs. As the emission rate is strongly temperature dependent, a thermal scan only reveals the presence of different traps at characteristic temperature when their emission rates coincide with the rate window. Also the maximum signal output is proportional to the defect concentration. Early DLTS systems employed the dual-gated (double boxcar) signal filter for determining the rate window and averaging transients to enhance the signal-to-noise ratio (SNR) of the output, enabling detection of low concentration defects [50,54]. The DLTS signal is obtained from the difference between the capacitance measured at time t_2 and the capacitance at time t_1 and produces an output proportional to their average difference. As depicted in Fig. 2.13 (a), at low temperature there is a slow transient, such that the DLTS signal $S = C(t_1) - C(t_2)$ is very low. As the temperature is increased, the transient decay rate increases causing a greater change in the capacitance between times t_1 and t_2, and resulting in the DLTS signal increase. This increase in DLTS signal continues until the transient decays so fast that most of the decay occurs before t_1. A further increase in time will now decrease the DLTS signal. Fig. 2.13 (b) shows a peak that is observed when the DLTS signal is plotted as a function of temperature. The time constant at which the maximum DLTS signal is observed is given by:

$$\tau_{\max} = \frac{t_1 - t_2}{\ln\left(\frac{t_1}{t_2}\right)} \tag{2.66}$$

In most of the modern analogue DLTS systems, a lock-in amplifier is used to analyse the DLTS transient. In a lock-in amplifier set-up, response to the transient is the integral product of the capacitance signal and the weighting function $w(t)$ given by

$$S(\tau) = \frac{1}{\tau}\int_0^{\tau} C(t)w(t)dt \tag{2.67}$$

where $w(t) = \sin\left(\frac{2\pi t}{\tau}\right)$ is a sine wave of fixed frequency.

The result obtained is the same as that obtained from the double boxcar method. Since the lock-in amplifier method uses more of the signal, therefore it is less sensitive to noise than the double boxcar method. For an exponential transient with a sine wave weighting function, the DLTS signal reaches a maximum when $\lambda = \left(\frac{1}{0.423\tau}\right)$.

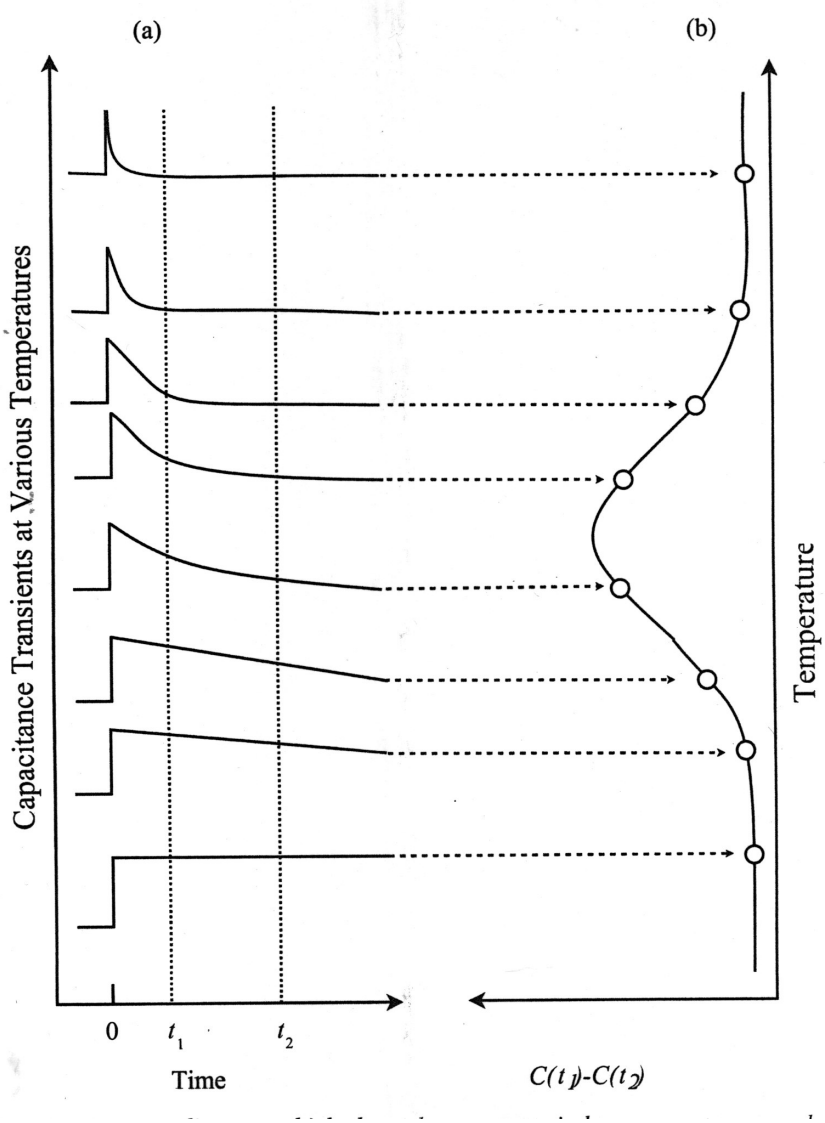


Fig. 2.13 *(a) The change in capacitance transient with increasing temperature and (b) the DLTS signal obtained from the transients plotted as a function of temperature, after ref. 50.*

2.7.6 *Defect depth profiling*

The concentration of deep levels is given in Eq. (2.65). This equation is only applicable if the minority carrier pulse or majority carrier pulse is large and long enough to completely fill the trap and $\Delta C << C$. The appropriate pulse for deep level concentration determination can be checked by making several scans with increasing larger and longer pulses, until the deep level peak no longer increase in size. Lang [50] has reported that, using Eq. 2.65, N_T is underestimated, especially for thin films and at low reverse bias voltage. In order to find the corrected expression for N_T one has to consider the region λ, where the deep level crosses the Fermi level a distance λ shallower than the depletion region edge as depicted in Fig. 2.14. The traps in this region are occupied and do not contribute to capacitance change when filling pulse is applied. The width of this region is given [58].

$$\lambda = \left(\frac{2\varepsilon (E_F - E_T}{q^2 N_D} \right)^{\frac{1}{2}} \tag{2.68}$$

where ε is the semiconductor dielectric constant E_F is the Fermi level and q is the electronic charge. The depth profiling technique uses a fixed bias voltage and a variable filling pulse [59]. In this method, the incremental change in capacitance $\delta(\Delta C)$ is monitored as the majority carrier pulse V_P is varied by a small amount δV_P. The relative incremental change in capacitance due to the pulse increment is given by [58].

$$\delta\left(\frac{\Delta C}{C}\right) = \left(\frac{\varepsilon}{qw^2 N_D}\right)\frac{N_T(x)}{N_D(x)}\delta V_P \tag{2.69}$$

where x is the depth below the junction, N_D is the ionized shallow impurity concentration and w is the depletion width, corresponding to a steady-state reverse biased condition.

The carrier charge density $N_D(x)$ is obtained from $C-V$ measurements, and the corrected deep level concentration can be expressed as [58];

$$N_T = \frac{2\Delta C(0) N_D(x)}{C}\left[\left(\frac{x-\lambda}{x}\right)^2 - \left(\frac{x_p - \lambda_p}{x}\right)^2\right]^{-1} \tag{2.70}$$

where $x-\lambda$ and $x_p-\lambda_p$ are the depletion region width before and after applying a filling pulse respectively and λ_p is the value of λ during the pulse. Values of 10^{-5}-10^{-6} for $\frac{\Delta C}{C}$ can be achieved in the low noise measurements and a low defect concentration of the order 10^{10} cm^{-3} is detectable if the shallow dopants concentration is $N_D \approx 10^{16}$ cm^{-3}.

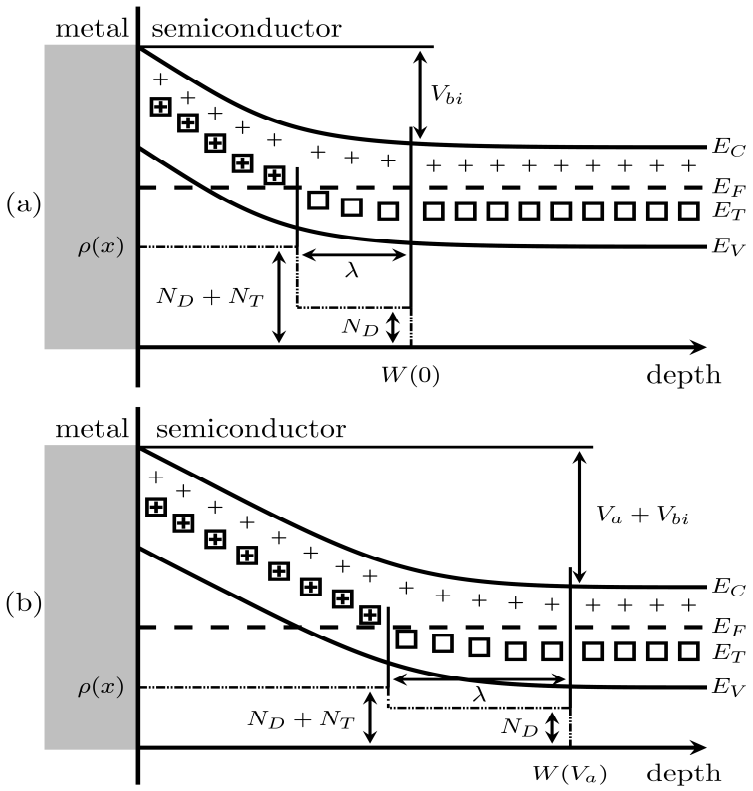


Fig. 2.14 *Energy band diagram, the λ and space charge for an n-type metal-semiconductor junction with deep levels for unbiased and after applying a quiescent reverse bias of V_a (after ref. 58)*

2.7.7 Principles of Laplace-DLTS

DLTS technique has limitations in separating closely spaced transients due to its poor emission rate and time constant resolution. In 1990, Dobaczewski et al [56,60] developed an improved high-resolution version of DLTS, called Laplace-DLTS (LDLTS).

Generally, there are two DLTS classes of transient processing methods, which are analog and digital signal processing. Analog signal processing is carried out in real-time process which involves extracting the capacitance transients as temperature is ramped. The output produced

by an analog filter will be proportional to the signal input within a particular time constant range. The digital signal processing digitizes the analog transient output of the capacitance meter and averages many of these digitized transients to reduce noise. The concept of digitizing capacitance at constant temperature and extracting the time constant is the basis of high resolution of LDLTS. A numerical algorithm is employed to extract all accessible time constants from the transients.

For the quantitative description of non-exponential behaviour in the capacitance transients, we need to assume that the recorded transients *f(t)* are characterized by a spectrum of emission rates [61]

$$f(t) = \int_0^\infty F(s)e^{-st}ds \tag{2.71}$$

where *f(t)* is the Laplace transform of the true spectral density *F(s)*. To determine a real spectrum of emission rates in the transient, an inverse Laplace transform for the function *f(t)* should be performed, producing a spectrum of delta-like peaks for multi-, mono-exponential transients.

LDLTS gives an intensity output as a function of emission rate. The area under each peak is related to the initial trap concentration. The measurement is carried out at a fixed temperature, and capacitance transients are recorded and averaged. LDLTS provides an order of magnitude higher energy resolution than the conventional DLTS technique [61]. Consequently, LDLTS can separate states with very similar emission rates.

2.7.8 Field dependence of the emission rate

Although it is often assumed that the electric field affecting deep levels in the space-charge region is negligible, there is strong evidence that in some cases the emission rate does depend upon the applied bias and doping. The electric field will distort the shape of the potential well. This distortion of the potential well may enhance the emission probability of a carrier trapped in the well, adversely affecting the accurate determination of defect concentration [62], as saturation of the defect peak amplitudes may occur depending on the effect of the electric field on the emission of electrons from the defect. Pons et.al [63], have reported that the DLTS signal of a defect that saturates quickly with an increase in filling pulse amplitude has an emission rate that depends strongly on electric field strength in the space-charge

region. The influence of the electric field can affect the emission process in different ways, as depicted in Fig. 2.15. The most well known emission enhancement mechanism is the Poole-Frenkel mechanism [64]. This mechanism enhances the emission rate of a defect by lowering the deep level potential. The Poole-Frenkel effect leads to a decrease (ΔE_{PF}) of the ionisation energy (ΔE_T) of a coulombic well placed in an electric field F , and

$$\Delta E_{PF} = \sqrt{\frac{qF}{\pi\varepsilon}} \tag{2.72}$$

where ε is the dielectric constant of the material and q the electron charge.

When substituted in Eq. 2.56, the emission rate of the defect is now given by

$$e_n^{'} = e(0)\exp\left(\frac{1}{kT}\sqrt{\frac{qF}{\pi\varepsilon}}\right) \tag{2.73}$$

where $e(0)$ is the emission rate at zero electric field, k is the Boltzmann's constant and T is the absolute temperature.

The dependence of the emission rate ($e_n^{'}$) on electric field F for a coulombic well, i.e. $\ln(e_n^{'})$ proportional to $F^{\frac{1}{2}}$, has been used as experimental evidence to distinguish between donor and acceptor defects. The linearity of this dependence shows a charge leaving a centre of opposite sign. This implies a donor type trap in *n*-type material and acceptor type defect in *p*-type material.

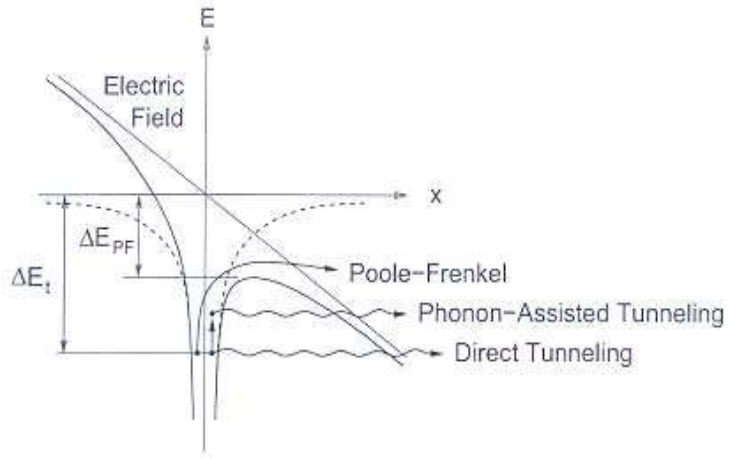


Fig. 2.15 *Field-enhanced emission mechanisms*

The other mechanisms shown in Fig. 2.15 are phonon-assisted tunnelling and direct tunnelling. These mechanisms favour the deeper-lying defects, with direct tunnelling mechanism being dominant in the high field regions (> 10^8 Vm^{-1}).

The phonon-assisted tunnelling mechanism occurs in defects with a significant electron-lattice coupling. Because of this coupling, the trapped defect can occupy a set of stationary quasi-levels separated by $\hbar\omega$, where $\hbar\omega$ is the phonon energy. From these quasi levels, elastic tunnelling can then occur to the conduction band. The coupling constant is given by [65],

$$S = \frac{\Delta E}{\hbar\omega} \tag{2.74}$$

where ΔE is the vibrational energy loss.

The field emission rate due to phonon-assisted tunnelling is represented by [63],

$$e_f = \sum_p \Pi_p(\Delta_p)(1 - f_{1,p}) \tag{2.75}$$

where $(1 - f_{1,p})$ is the Fermi-Dirac probability of finding an empty conduction band state, $\Gamma(\Delta_p)$ is the tunnelling emission probability for an electron at a quasi level p with energy Δ_p above the ground state and Π_p is the probability of finding the electron at quasi level p.

The probability (Π_p) of finding the trapped electron at a given quasi-level $E_c - \Delta_p$, where $p = 0, \pm 1, \pm 2, ...$ may be calculated from [63];

$$\Pi_p = \left(1 - \exp^{-\hbar\omega/kT}\right) \sum_{n=0}^{+\infty} \exp^{-n\hbar\omega/kT} J_p^2\left(2\sqrt{S\left(n + \frac{1}{2}\right)}\right) \tag{2.76}$$

where J_p is a Bessel function of the first kind and n the integer number of phonons. This model is based on the assumption that the phonons have a single well-defined angular frequency ω.

References

[1] C. Kittel, Introduction to Solid State Physics, Wiley & Sons, New York, 1976.

[2] E.E Haller, Mat. Sci. Semcond. Proc. **9** (2006) 408

[3] S.M. Sze, Physics of Semiconductor devices, Wiley & Sons, Canada, 1981.

[4] S. Li, Semiconductor Physical Electronics, Springer, 2006.

[5] C. Kettel, Quantum Theory of Solids, Wiley & Sons, New York, 1963.

[6] L.C. Allen, Phys. Rev, **98** (1955) 93

[7] F. Herman, Proc. IRE, **43** (1955) 1703.

[8] J.C. Philips, Phys. Rev. **112** (1958) 685.

[9] R.A Smith, Semiconductors, 2nd ed., Cambridge University Press, London, 1979.

[10] R.T. Tung, Mater. Sci. Eng. R **35** (2001) 1.

[11] M. Sağlam, F.E. Cimilli, A. Türüt, Physica B **348** (2004) 397.

[12] Ö. F. Yüksel, Physica B **404** (2009) 1993.

[13] W. Mönch, Semiconductor Surf. And Interfaces, 2nd ed., Springer, Berlin 1995.

[14] B. Boyarby, H. Çetin, M. Kaya, E. Ayyildiz, Microelectron. Eng. **85** (2008) 721.

[15] R.D. Thomson, K.N. Tu, J. Appl. Phys. **53** (1982) 4285.

[16] J.H. Werner, H. Guttler, J. Appl. Phys. **69** (1991) 1522.

[17] S. Chand, J. Kumar, J. Appl. Phys. **82** (1997) 5005.

[18] H. Çetin, E. Ayyildiz, Semicond. Sci. Technol. **20** (2005) 625.

[19] R.T. Tung, Phys. Rev. B. **45** (1992) 13509.

[20] W. Schottky, Naturwissenschaften **26** (1938) 843.

[21] N.F. Mott, Proc. Camb. Phil. Soc. **34** (1938) 568.

[22] E. H. Rhoderick, Metal-Semiconductor Contacts, Clarendon, Oxford, 1978.

[23] H.A. Bethe, MIT Radiant. Lab. Rep. **43** (1942) 12.

[24] B.G. Streetman, Solid State Electronic Devices, 5th Ed. Prentice Hall, New Jersey (2000)

[25] R.T. Tung, Mater. Sci. Eng. R **35** (2001) 1.

[26] Ş. Karadeniz, M. Şahin, N. Touğluoğlu, H. Şafak, Semicond. Sci. Technol. **19** (2004) 91098.

[27] S. Acar, S. Karadeniz, N. Tuğluoğlu, A.B. Selçuk, M. Kasap, Appl. Surf. Sci. **233** (2004) 373.

[28] A. Gümüş, A. Türüt, N. Yalçin, J. Appl. Phys. **91** (2002) 245.

[29] W. Mtangi, F.D. Auret, C. Nyamhere, P.J. Janse van Rensburg, M. Diale, A. Chawanda, Physica B **404** (2009) 1092.

[30] http://en.wikipedia.org/wiki/annealing_(metallurgy), 19/04/2010.

[31] M.G. Grimaldi, L. Wieluński, and M.-A. Nicolet, Thin Solid Films, **81** (1981) 207.

[32] H. Doğan, N. Yildirim, A. Türüt, Microelectron. Eng. **85** (2008) 655.

[33] Y. Sun, X.M. Shen, J. Wang, D.G. Zhao, G. Feng, Y. Fu, S.M. Zhang, Z.H. Zhang, Z.H. Feng,Y.X. Bai, H.Yang, J. Phys. D: Appl. Phys. **35** (2002) 2648.

[34] Q. Zhang, N. Wu, T. Osipowicz, L.K. Bera, C. Zhu, Jan. J. Appl. Phys. **44** (2005) L1389.

[35] J.P. Gambino, E.G. Colgan, Mater. Chem. Phys. **52** (1998) 99.

[36] P. Jayavel, K. Asokan, D. Kanjilal, J. Kumar, Mater. Sci. Semicond. Proc. **3** (2000) 195.

[37] F.D. Auret, W.E. Meyer, S. Coelho, and M. Hayes, Appl. Phys. Lett. **88** (2006) 242110.

[38] M.W. Thompson, Defects and Radiation Damage in Metals, Cambridge University Printing House, (1969) 11.

[39] M. Lannoo and J. Bourngoin, Point Defects in Semiconductors I, Theoretical Aspects Springer series in Solid State science 22 (1981).

[40] S.A. Centoni, B. Sadigh, G.H. Gilmer, T.J. Lenosky, T.D. de la Rubia, C.B. Musgrave, Phys. Rev**. B 72** (2005) 195206.

[41] A.R. Peaker, V.P. Markevich, F.D. Auret, L. Dobaczewski and N. Abrosimov, J.Phys. Condens. Matter **17** (2005) S2293.

[42] C.E. Linbergy, J. L. Hansen, P. Bomholt, A. Mesli, K. B. Nielsen, A. N. Lasen, L. Dobaczewski, Appl. Phys Lett. **87** (2005) 172103.

[43] J. Fage-Pedersen, A. Nylandsted Lartsen, and A. Mesli, Phys. Rev. B **62** (2001) 10116.

[44] V.P. Markevich, A.R. Peaker, V.V. Litvinov, V.V. Emstsev, and L.I. Murin, J. Appl. Phys. **95** (2004) 4078.

[45] V.P. Markevich, A.R. Peaker, L.I. Murin and N.V. Abrosimov, J.Phys.:Condens. Matter **15** (2003) S2835.

[46] V.P. Markevich, V.V. Litvinov, L. Dobaczewski, J.L. Lindström, L.I. Murin, S.V. Vetrov, I.D. Hawakins, A.R. Peaker, Physica B **340-342** (2003) 844.

[47] G.D. Watkins, J.W. Corbett, Phys. Rev. **121** (1961) 1001.

[48] V.P. Markevich, et al., Phys. Stat. Sol. (c) **0** (2003) 702.

[49] V.P. Markevich, et al., Appl. Phys. Lett. **81** (2002) 1821.

[50] D.V. Lang, J. Appl. Phys. **45** (1974) 3023.

[51] W. Shockley, W.T. Read, Phys. Rev. **87** (1952) 835.

[52] R.N. HallPhys. Rev. **87** (1952) 387.

[53] J. Bourgoin, M. Lannoo, Point defects in semiconductors II, Berlin: Springer (1983).

[54] G.L. Miller, D.V. Land, L.C. Kimerling, Ann. Rev. Mater. Sci. **7** (1977) 377

[55] F.D. Auret and P.N.K. Deenapanray, Crit. Rev. Sol. Stat. Mater. Sci. **29** (2004) 4689.

[56] L. Dobaczewski, A.R. Peaker and K.B. Nielsen, J. Appl. Phys. **96** (2004) 4689.

[57] V.P. Markevich, I.D. Hawkins, A.R. Peaker, K.V. Emtse, V.V. Litvinov, L.I. Murin, and L. Dobaczewski, Phys. Rev. B **70** (2004) 235213.

[58] Y.Zohta and M.O. Watanabe, J. Appl. Phys. **53** (1982) 1809.

[59] D.V. Lang, In "Thermally Stimulated Relxation of Solids" (P. Braunlich, ed.), Springer-Verlag, Berlin 1979.

[60] L. Dobaczewski, P. Kaczor, I.D. Hawkins and A.R. Peaker, J. Appl. Phys. **76** (1994) 194.

[61] D.K. Schroder, Semiconductor Material and Device Characterization, Wiley & Sons,2006.

[62] H. Lefevre and M. Schulz, J. Appl. Phys. 12 (1977) 45.

[63] D. Pons and S. Makran-Ebeid, J. Phys. **40** (1979) 1161.

[64] J. Frenkel, Phys. Rev. **54** (1938) 657.

[65] S. Makram-Ebeid and M. Lannoo, Appl. Phys. Lett. **37** (1980) 464.

CHAPTER 3

EXPERIMENTAL TECHNIQUES

3.1 Introduction

In this chapter, the apparatus and techniques used will be described. Section 3.2 presents sample preparation, i.e. cleaning process, ohmic and Schottky contact fabrication. In section 3.3 Schottky diode characterization techniques (i.e. current-voltage (I-*V*), capacitance-voltage (*C*-*V*), and temperature dependent *I*-*V* and *C*-*V* are discussed. Deep level transient spectroscopy (DLTS), a defect characterization technique is outlined in section 3.4. Section 3.5 deals with the Rutherford backscattering spectrometry, utilised to study the in-diffusion of thin film metals on germanium. Scanning electron microscope system is presented in section 3. 6. This chapter ends with a discussion of annealing apparatus in section 3.7.

3.2 Sample preparations

Prior to metallization, the germanium samples were cut into (0.5 × 0.3) cm^2 followed by a chemical cleaning process. Cleanliness is essential to achieving high yields and reproducible process in the production of any microelectronic devices [1]. Before metallization the semiconductor should be atomically as clean as possible and stoichiometrically perfect [2], in order to obtain high quality Schottky barrier diodes with a low leakage current when reverse biased.

3.2.1 Germanium cleaning process

Before metallization the following cleaning procedure was followed:

i) Degreasing the samples in trichloroethylene (TCE), acetone and then methanol, each for five minutes in an ultrasonic bath at room temperature. The degreasing process is followed by rinsing the sample in de-ionized water of resistivity < 18 MΩcm.

ii) Etching in a solution of 30% H_2O_2:H_2O (1:5) for one minute for the removal of the remaining oxide layer and insoluble organic contaminants and then followed by rinsing in de-ionized water.

iii) The samples are blown-dry in a stream of filtered, dry, nitrogen gas, and ready for metallization.

3.2.2 Ohmic and Schottky contact fabrication

The ohmic contacts were fabricated by resistively evaporating a 100 nm thick layer of Au-Sb (0.6% Sb) on the back surface of the germanium samples. The deposition follows the evacuating of the deposition chamber to pressure below 10^{-6} Torr. The samples were then annealed for ten minutes at 350°C in Ar, to optimize the ohmic contact by lowering the barrier height, hence reducing its resistivity [3]. The annealing process results in the infusion of Sb into the backside of the germanium resulting in the increase of doping concentration. This leads to a very thin depletion region, known as a tunnel junction [4], through which field emission can take place. The use of Ar gas reduces oxidation of the metal during the annealing process, while it can also reduce interfacial oxide between the semiconductor and the metal.

A schematic of the vacuum resistive deposition system is shown in Fig. 3.1. A current flows through the crucible containing the metal to be evaporated. The molten metal evaporates and deposits onto the sample mounted above the crucible. Only metals with melting points less than 1 600°C are evaporated from this system.

Before Schottky contact deposition, the samples were again chemically cleaned as described in section 3.2.1. The Schottky contacts 0.6 mm in diameter, 30 nm thick were either fabricated by resistive deposition or electron beam deposition.

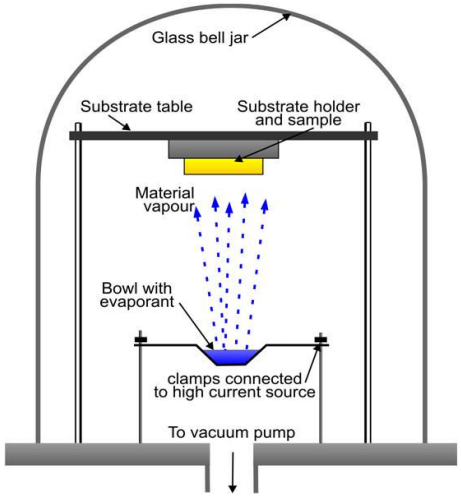


Fig. 3.1 *A Schematic representation of the vacuum resistive deposition system*

The electron beam deposition (EBD) system is depicted in Fig. 3.2. In the electron beam deposition system, a hot filament emits a beam of electrons, focused onto the crucible containing the metal by magnetic and electric fields, resulting in the melting and evaporation of the metal which deposits onto the sample. Fig. 3.3 shows the sample after the metallization process.

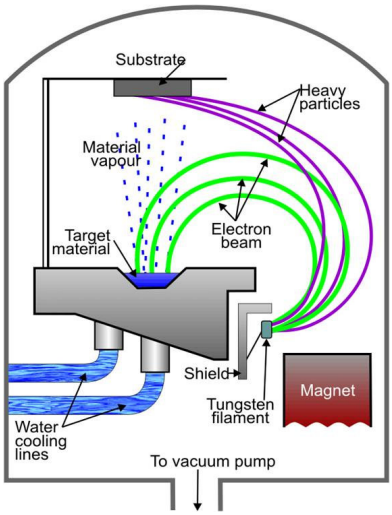


Fig. 3.2 *A schematic representation of the electron beam deposition system*

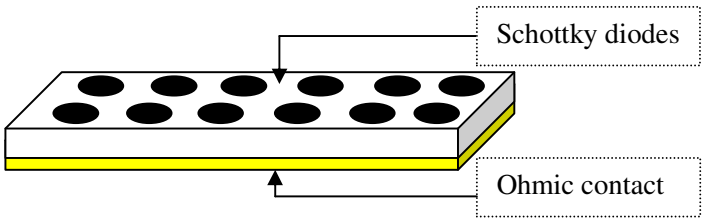


Fig. 3.3 *A sample showing Schottky contacts and ohmic layer.*

3.3 Current-Voltage and Capacitance-Voltage measurements

After contact fabrication, electrical characterization through current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements were carried out at room temperature. The (*I-V*) measurements were made by an HP 4140 B pA meter/ DC voltage source, capable of measuring current limit of 10^{-14} A. The (*C-V*) characteristics were measured by an HP 4192A LF Impedance Analyzer. The samples were measured in the dark and screened from electrical noise by enclosing them in a light-tight metal box. The most important diode parameters obtained from the (*I-V*) and (*C-V*) measurements are series resistance R_s, the barrier height $\phi_{B(I-V)}$, the ideality factor n, reverse current I_r measured at a reverse bias of 1 V and free carrier density N_D. Fig. 3.4 depicts a schematic diagram of the (*I-V*), (*C-V*) station used during the electrical characterization of the samples. Isochronal annealing of the samples was performed in the temperature range 25°C to 700°C in steps of 25°C for 30 minutes in Ar atmosphere. *I-V* and *C-V* measurements followed each annealing cycle.

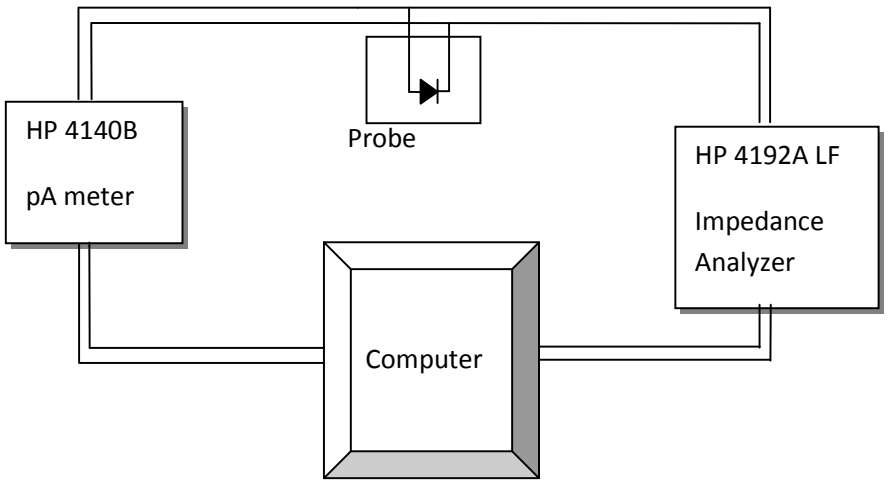


Fig. 3.4 *Block diagram of (I-V) and (C-V) station for determining the diode characteristics.*

Temperature dependent (*I-V*) measurements, in the 20-300 K temperature range were performed in a He cryostat using an automated Labview program. From the measurements, ideality factor (n), series resistance (R_s), reverse saturation current (I_r), and barrier height ($\Phi_{B(I-V)}$) as function of temperature, were extracted. Temperature dependent (*C-V*) measurements were recorded at a frequency of 1 MHz for voltage ranging from 0 V to –1 V and temperature range of 20-300 K via a Labview program. The barrier height ($\Phi_{B(I-V)}$) and the carrier concentration (N_D) were obtained from the plot of $1/C^2$ *vs* V.

3.4 Deep level transient spectroscopy (DLTS) and Laplace-DLTS system

The layout of the DLTS and LDLTS system used in this study is illustrated in Fig. 3.5. The system consists of:

i) A cryostat, in which the sample is mounted. The cryostat temperature is controlled by a Lakeshore 340 temperature controller in the range 16-380 K.

ii) Boonton 7200 capacitance meter, with 100 mV, 1 MHz AC ripple voltage, and it monitors thermal emission after excitation by a pulse generator.

iii) A Laplace card, which has an internal pulse generator for generating the appropriate quiescent bias and pulses. This card is also the data collection and processing system which analyses and averages the transients prior to displaying the spectra for either the conventional DLTS or L-DLTS.

iv) HP 33120 15 MHz Function waveform external generator, for providing the desired quiescent bias and filling pulse to the diode which are not provided by the Laplace card.

The Laplace card sets the sample excitation parameters, capacitance transient acquisition conditions, and then initiates the measurement, acquiring the transient and converts it into either a DLTS or LDLTS spectrum depending on the measurements. For conventional DLTS the capacitance transients after excitation are measured by the capacitance meter. These transients are then processed by the Laplace card. As the temperature is ramped a DLTS spectrum is displayed on a computer for a particular rate window. L-DLTS gives an intensity output as a function of emission rate. The measurement is carried out at a fixed temperature, and several capacitance transients are captured and averaged. In the isothermal DLTS method, the sample temperature is held constant while the sampling time is varied. This technique also uses the equation

$$C(t) = C_0\left[1-\left(\frac{n_T(0)}{2N_D}\right)\exp\left(-\frac{t}{\tau_e}\right)\right] \tag{3.1}$$

From Eq. (3.1) the function $tdC(t)/dt$ plotted against t has a maximum value $n_T(0)C_0/2N_D)(1/e)$ at $t=\tau_e$. From a series of $tdC(t)/dt$ against t plots at various constant temperatures permits an Arrhenius plot of $\ln(\tau_e T^2)$ against $1/T$, similar to a conventional DLTS plot. The main difference is the constancy of the temperature during measurement. In the conventional DLTS C (t) measurements have to be made over a wide time range, requiring high frequency capacitance meters.

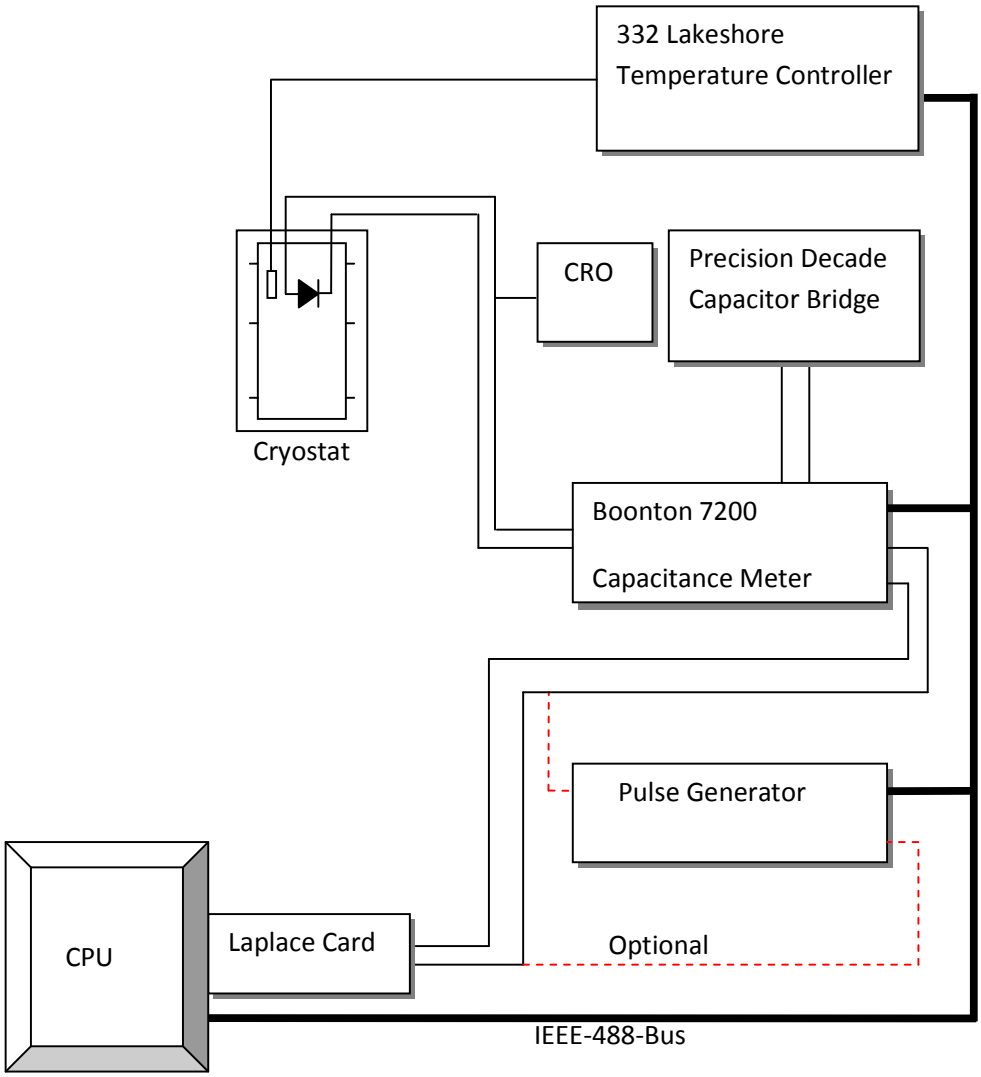


Fig. 3.5 *Block diagram of the DLTS and LDLTS*

3.5 Rutherford backscattering spectrometry

Rutherford backscattering spectrometry (RBS) is a technique based on the analysis of the energy of the backscattered charged particles such as He^+ used in this study. In this study, RBS technique was used to investigate the in-diffusion of metals deposited on Ge at different annealing temperatures. The schematic diagram of the RBS system attached to a Van de Graaff 2.5 MeV at the University of Pretoria is depicted in Fig. 3.6. The charged particles are generated from a gas introduced into the ion source, and accelerated to high energies up to 1.8 MeV by applying a large potential difference across the accelerator tube. The energy of 1.6 MeV was used in this study. The acceleration voltage is generated from a moving insulating belt that carries charge that is sprayed on at base plate, and this charge is removed as a column current flowing through a set of resistors [5].

The dipole magnet in front of the Van de Graaff accelerator acts as an energy and mass separator. It deflects the beam into either the left beam line or right beam line. The Left Beam line is designed to operate below room temperature while the right beam line operates at room temperature. For this study, the right beam line was used. The beam of positively-charged ions (He^+) passes through slits that stabilise the accelerating voltage, and they are collimated into a specific size before they reach the target. Secondary electrons are suppressed by a negative voltage of 200 V connected to a ring electrode in front of the target holder.

The backscattered alpha particles are detected by a Si surface barrier detector operating with a reverse bias of 40 V, and connected to a pre-amplifier where it is integrated into a voltage signal that is proportional to backscattered energy. This voltage signal is amplified before it is converted to a digital signal by an analogue to digital converter (ADC) inside the multi-channel analyzer (MCA). The MCA output is a spectrum of the yield (counts) *versus* channel number. The yield is the number of backscattered particles at 165°, while the channel number is proportional to the backscattered energy.

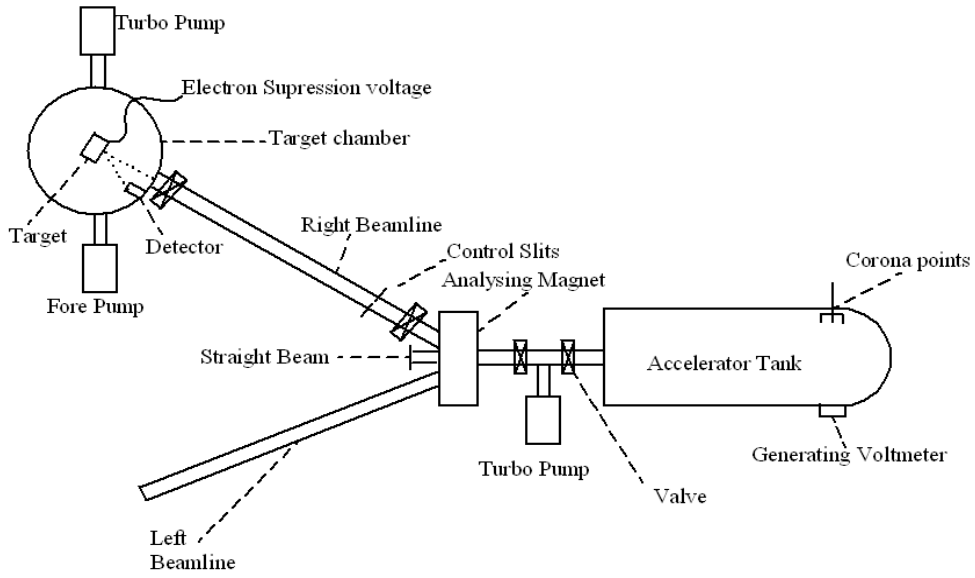


Fig. 3.6 *Block diagram of the Rutherford backscattering spectrometry attached to Van de Graaf accelerator at the University of Pretoria.*

3.6 Scanning electron microscopy

A scanning electron microscope (SEM), shown in Fig 3.7 is a high resolution microscope that uses electrons rather than light for imaging on conducting materials. A highly focused electron beam is created in the electron gun by the heated filament. The electron gun provides a stable electron beam of adjustable energy. The electron beam is guided into the aperture by lenses. When focused on the surface, the electron beam stimulates the emission of different electrons such as back scattered electrons and secondary electrons, and the signal produced is detected and amplified to increase the brightness of the Cathode Ray Tube (CRT) display. The energy of the electrons is directly related to the desired image. The ZEISS ULTRA PLUS and the JEOL JSM-5800LV SEM systems were operated at a pressure below 10^{-6} Torr and at voltages of 1 kV and 5 KV, respectively.

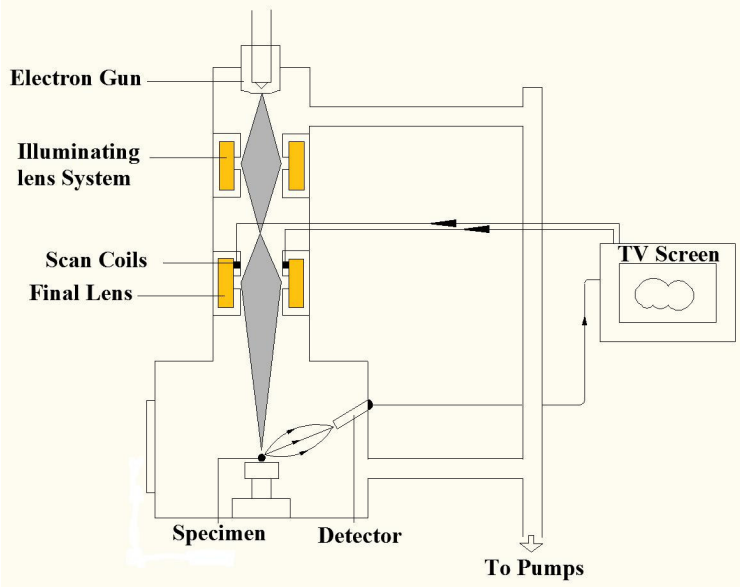


Fig. 3.7 *Scanning electron microscope system.*

3.7 Annealing apparatus

All the annealing experiments were carried out in a Lindberg "heavy duty" furnace (200-1200^{o}C), in argon atmosphere at an approximate flow rate of 2 litres/min. The annealing temperature was monitored by a thermocouple placed inside the sample holder just under the sample. The annealing furnace used in this study is shown schematically in Fig 3.8.

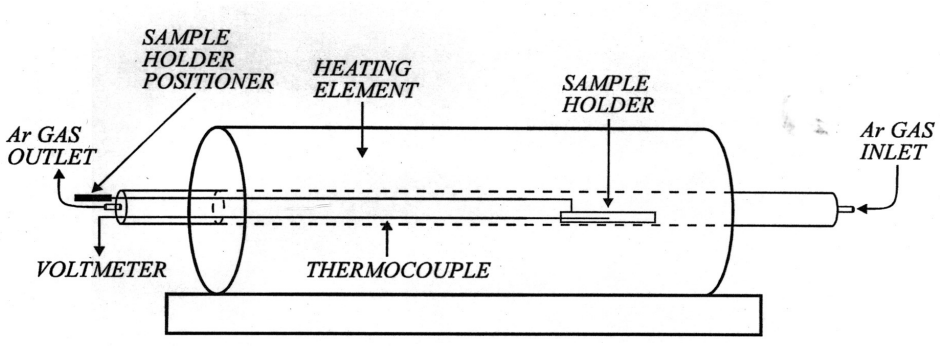


Fig. 3.8 *Lindberg "Heavy duty" annealing furnace*

References

[1] R.E. Williams: Gallium Arsenide Processing Techniques (Artech House) (1984) 85.

[2] F.D. Auret, W.O. Barnard, G. Myburg and L.J. Bredell: S. Afr. J. Sci. **87** (1991) 127.

[3] F.D. Auret, P.J. Janse van Rensburg, M. Hayes, J.M. Nel, S. Coelho, W.E. Meyer, S. Decoster, V. Matias, A. Vantomme, D. Smeets, Nucl. Instr. And Meth. B **257** (2007) 169.

[4] R.R. Lieten, S. Degroote, M. Kuijk, and G. Borghs, Appl. Phys. Lett. **92** (2006) 022106.

[5] R.J. van de Graaf, Phys Rev. **38** (1931) 1919.

CHAPTER 4: RESULTS

Thermal annealing behaviour of metal Schottky contacts on n-Ge (100)

4.1 Introduction

So far, several studies have been done concerning the reactions of Ge with platinum (Pt) [1,2,3,4,5,6], nickel (Ni) [2,3,7,8,9,10,11,12,13], titanium (Ti) [3,14], cobalt (Co) [3,15,16,17], palladium (Pd) [3,15,18,19,20], iridium (Ir) [21,22,23,24,25,26] and ruthenium (Ru) [3], using electrical and structural characterization techniques. Yao et al. [2] studied the current-voltage (*I-V*) characteristics of Pt/n-Ge (001) and Ni/ n-Ge (001) after subjecting the Schottky contacts to rapid thermal anneal (RTA) in N_2 ambient at 250-700°C for 20 s. Łsazcz et al. [5] studied the mechanisms of the Pt germanide formation by RTA process in Ge/Pt/Ge/SiO_2 structure at 200–600°C range. Their results depict that, during annealing of the Ge/Pt/Ge/SiO_2 structure at 200°C, the whole Pt layer had reacted with a part of the Ge layer and after 300°C anneal the whole Ge reacted with Pt. Thanailakis et. al [7] established a relationship between as-deposited Ni/n-Ge (111) and Pd/n-Ge (111) Schottky contacts barrier height values, the metal work functions and the density of surface states germanium substrate. Their results show a linear correlation of the as-deposited Schottky barrier height (SBH) values and work functions for the metals Pd and Ni, confirming the Effective Work Function model. Peng et al [9] reported the Ni/n-Ge (100) Schottky diodes *I-V* characteristics and the nickel germanide induced strain after subjecting the Schottky contacts to RTA in the temperature range 300-600°C. Their results show that the orthorhombic structure of NiGe induces epitaxial tensile strain on Ge substrate due to the difference in lattice constants. They also suggested that the increase of barrier height with annealing temperature may be due to the conduction band edge shift by the strain after germanidation process. An et al. [10] have investigated the impact of ion implantation on nickel germanides formation with pure-Ge substrate and electrical dependence of NiGe/Ge Schottky diodes on contact size. Their results reveal that ion implantation of BF_2 before germanidation is favourable for the formation of low-resistivity monogermanide phase (NiGe). They also showed that the Schottky barrier

height of Ni/Ge (100) Schottky diodes formed on pure-Ge substrate decreased with deceasing contact size, while the ideality factor increased remarkably, which may provide the guideline for the application to Schottky source/drain germanium transistors [10]. Peng et al. [11] have carried out micro-Raman studies on nickel germanides formed on (110) crystalline Ge. From XRD analysis they found that Ni_5Ge_3, NiGe and Ni_2Ge phases are formed sequentially with increasing annealing temperatures from 300°C to 600°C on n-Ge (110) substrate. Their results depicted a strong tensile stress in the underlying Ge (110) substrate, which was attributed to the lattice mismatch between nickel germanides and germanium substrate. An et al. [12] have also successfully demonstrated the modulation of Schottky barrier height of Ni/n-Ge (111) by a germanidation-induced dopant segregation technique. Their results showed that the change of the Schottky barrier height was not attributed to the phase change of nickel germanides but to dopant segregation at the interface of germanides/germanium which causes conduction energy band bending. Perrin et al. [13] have studied both systems (Ni-Si and Ni-Ge) in order to compare their phase formation and growth kinetics. Ni thin films and armorphous semiconductor layers (a-Si and a-Ge) had been deposited on undoped (100) Si wafers. They have showed that Ni-Si system has three major phases (Ni_2Si, NiSi and $NiSi_2$) that grow sequentially while Ni-Ge system showed only two phases (Ni_5Ge and NiGe) that grow simultaneously. Dedong et al. [14] studied changes in the electrical properties of Ti and Ni germanide Schottky contacts on n-Ge (100) substrate in the temperature range 300-500°C. Habanyama et al. [26] have used ion beam analysis employing micro-Rutherford backscattering spectrometry to investigate the interaction between iridium and germanium in lateral diffusion couple. Gaudet et al. [3] have investigated the phase formation sequence of Ru thin films on germanium using the x-ray diffraction technique.

Studies on germanides formation up to date have been carried out. The majority of them have reported the use of in-situ annealing by slowly-ramping annealing temperature or RTA in the temperature range 200-700℃. In this study we investigated the change in the electrical properties of Pt/-, Ni/-, Ti/-, Co/-, Pd/-, Ir/- and Ru/n-Ge (100) Schottky contacts at different furnace annealing temperatures in the temperature range 25-600°C. Results presented here are based on the effects of thermal annealing on the current-voltage characteristics of the metal Schottky contacts at different annealing temperatures, which may be attributed to combined effects of interfacial reaction and phase transformation [27], during the annealing process.

4.2 Experimental procedures

To study the thermal annealing behaviour of the Schottky contacts, we used bulk-grown (100) oriented, n-type Ge, doped with antimony (Sb) to a density of (1.5-3) $\times 10^{15}$ cm^{-3} supplied by Umicore. Before metallization, the samples were first degreased and subsequently etched in a mixture of H_2O_2 (30%):H_2O (1:5) for 1 min. Immediately after cleaning they were inserted into a vacuum chamber where 100 nm of AuSb (0.6%), was deposited by resistive evaporation on their back surfaces as ohmic contacts. The samples were then annealed at 350°C in Ar ambient for ten minutes to minimize the ohmic contact resistivity [28]. Before Schottky contact deposition, the samples were again chemically cleaned as described above. Pt, Ti, Ir or Ru Schottky contacts 0.6 mm in diameter, 300 nm thick were deposited by electron beam deposition under vacuum below 10^{-6} Torr through a metal contact mask, while Ni, Co-, or Pd Schottky contacts were resistively deposited. The metal layer thickness and deposition rates were monitored in situ using a quartz crystal thickness monitor. Eight of each Pt/-, Ni/-, Ti/- Co/- Pd/-, Ir/- and Ru/n-Ge (100) Schottky barrier diodes (SBDs) were fabricated. After contact fabrication, current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements were used to extract the free carrier concentration and to determine the quality of the diodes. Isochronal annealing of the samples was performed in the temperature range 25-600°C in steps of 25°C for 30 min. *I-V* measurements followed each annealing cycle.

4.3 Results

The barrier heights of the contacts were calculated from *I-V* characteristics, which were analyzed by the thermionic emission model given by the following equation [29,30]:

$$I(V) = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \tag{4.1}$$

where

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \tag{4.2}$$

is the saturation current obtained as the intercept from the straight line of $\ln I$ *versus* V, A^* is the effective Richardson constant, A is the diode area, T the measurement temperature in Kelvin, k is the Boltzmann constant, ϕ_B is the zero bias effective Schottky barrier height (SBH), q is the electronic charge and n is the ideality factor which can be determined accurately from the slope of the linear part of a $\ln I$ versus V plot. Assuming pure thermionic emission, n can be obtained from Eq. (4.1) as

$$n = \frac{q}{kT}\frac{dV}{d(\ln(I))} \tag{4.3}$$

which is equal to unity for an ideal diode and usually has a value greater than unity. The values of effective SBH were determined from the intercepts of the straight lines of the semilog-forward bias $I-V$ characteristics with the help of Eq. (4.2). The effective SBHs and ideality factors vary from diode to diode; therefore it is common practice to take averages.

4.3.1 Pt/n-Ge (100) Schottky diodes

Fig. 4.1 presents the forward and reverse bias $I-V$ characteristics of the Pt/n-Ge (100) SBDs annealed in the 25-600°C temperature range. Fig. 4.2 shows the variation of the Schottky barrier height and reverse current at –1 V with annealing temperature for Pt Schottky contacts. The SBH and reverse current at a bias voltage of –1 V for as-deposited Pt Schottky contacts were found to be (0.584 ± 0.005) eV and (5.46 ± 0.02) μA, respectively.

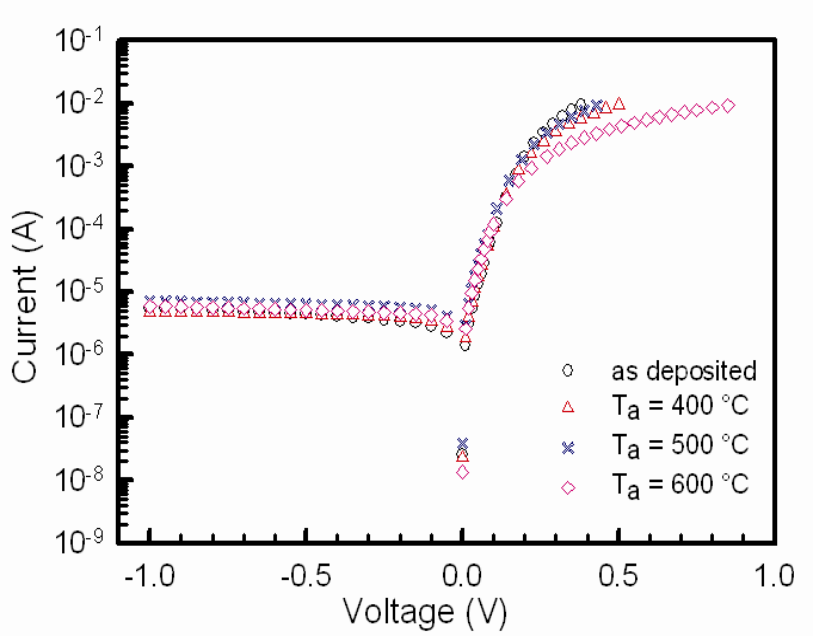


Fig.4.1 *Experimental forward and reverse I-V characteristics of one of the Pt/n-Ge (100) Schottky barrier diodes after isochronal thermal treatment for 30 min at different annealing temperatures: as-deposited, 400°C, 500°C and 600°C.*

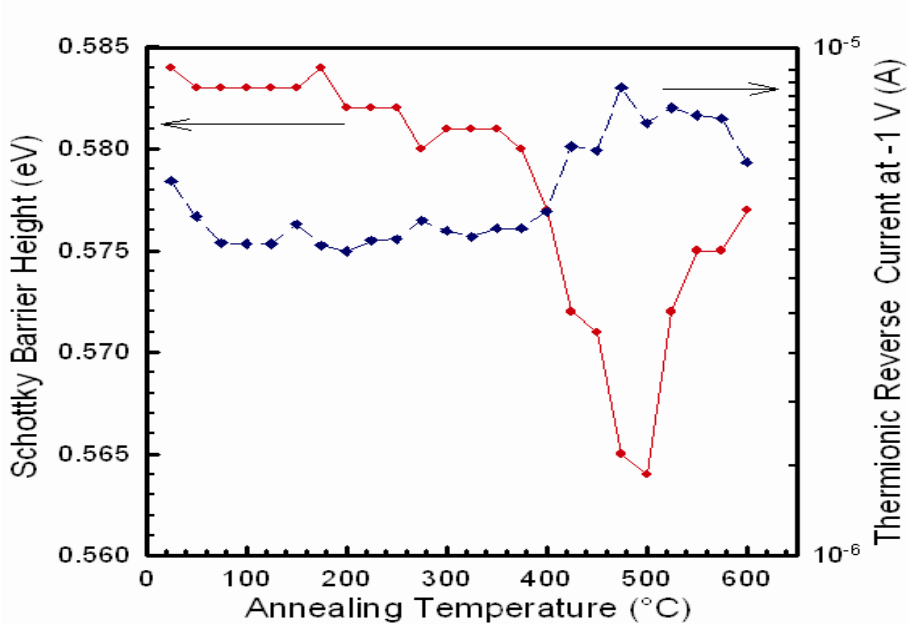


Fig. 4.2 *Plot of the Schottky barrier height and reverse current at –1 V as a function of annealing temperature for Pt Schottky contacts on n-Ge (100).*

The barrier height (BH) was approximately a constant within experimental error up to an annealing temperature of 350°C. The BH then drops to (0.564 ± 0.005) eV after annealing at 500°C. It is evident that the BH decreases significantly above 350°C annealing. We can say

that there is a significant reaction between Pt and the Ge substrate. The change coincides with the initial phase formation of a germanide Ge_3Pt_2, which has been reported to form at 400°C [1,2]. After annealing at 600°C, the barrier height (BH) increased to (0.577±0.005) eV. The change in BH after the 500°C anneal coincides with the temperature range of formation of platinum germanide Ge_2Pt as reported by [1,2]. Throughout the annealing process, the reverse current at –1 V remains in the same order of magnitude (10^{-5} to 10^{-6}) A.

Fig. 4.3 (a) shows the variation of ideality factor of Pt/n-Ge(100) Schottky contacts with annealing temperature. The ideality factor was found to be between 1.09 and 1.30. The ideality factor is almost a constant, 1.09 up to a temperature of 575°C. It then increases to 1.30 after annealing at 600°C.

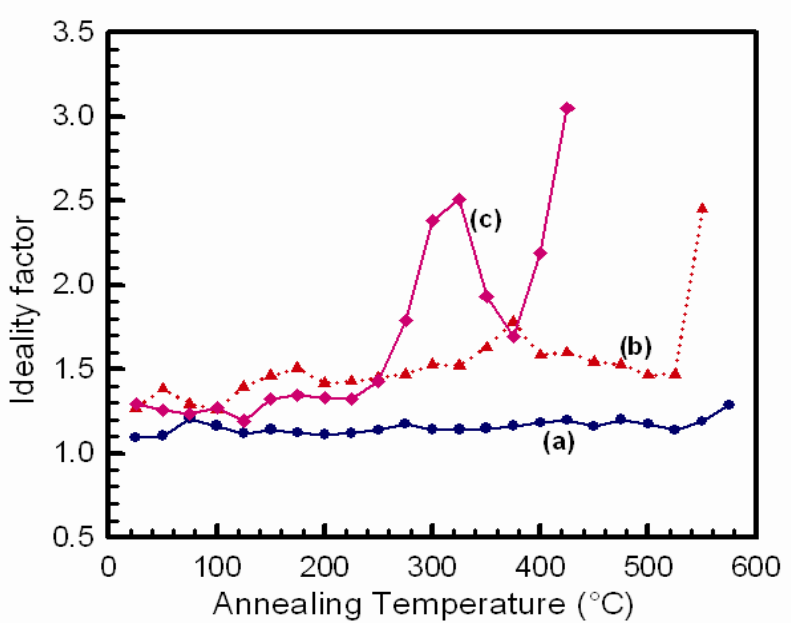


Fig. 4.3 *Plot of ideality factor as a function of annealing temperature for: (a) Pt Schottky contacts on n-Ge (100); (b) Ni Schottky contacts on n-Ge (100) and (c) Ti Schottky contacts on n-Ge (100).*

4.3.2 Ni/n-Ge (100) Schottky diodes

Fig. 4.4 depicts the semilog forward and reverse bias $I-V$ characteristics of Ni/n-Ge (100) Schottky diodes annealed in the 25-550°C temperature range, together with those of as-deposited diodes. Fig. 4.5 shows the variation of the Schottky barrier height and reverse current at –1 V with annealing temperature for Ni/n-Ge (100) Schottky contacts.

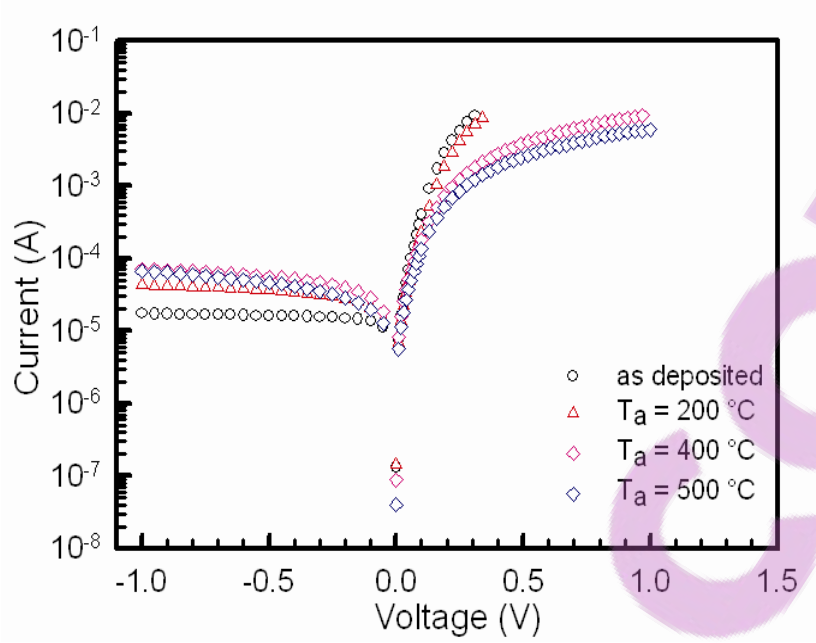


Fig. 4.4 *Experimental forward and reverse I-V characteristics of one of the Ni/n-Ge (100) Schottky barrier diodes after isochronal thermal treatment for 30 min at different annealing temperatures: as-deposited, 200°C, 400°C and 500°C.*

The as-deposited SBH and reverse current at –1 V for Ni/n-Ge (100) were found to be (0.532 ± 0.005) eV and (29.20 ± 0.02) μA, respectively. The barrier height remains almost constant within experimental error in the temperature range 100-550°C. The near constant barrier height with annealing temperature in Ni/n-Ge (100) Schottky contacts may be attributed to the strong Fermi level pining effect between Ni-germanide/n-Ge (100) substrates [14]. Studies by Gaudet et al. [3], Peng et al. [9] and An et al. [10] revealed the existence of only one germanide phase, NiGe for Ni in this temperature range. Fig. 4.3 (b) shows the variation of ideality factor with annealing temperature for the Ni/n-Ge (100) Schottky diodes. The ideality factors were on the average between 1.27 and 1.47 at annealing temperatures between 25°C and 550°C.

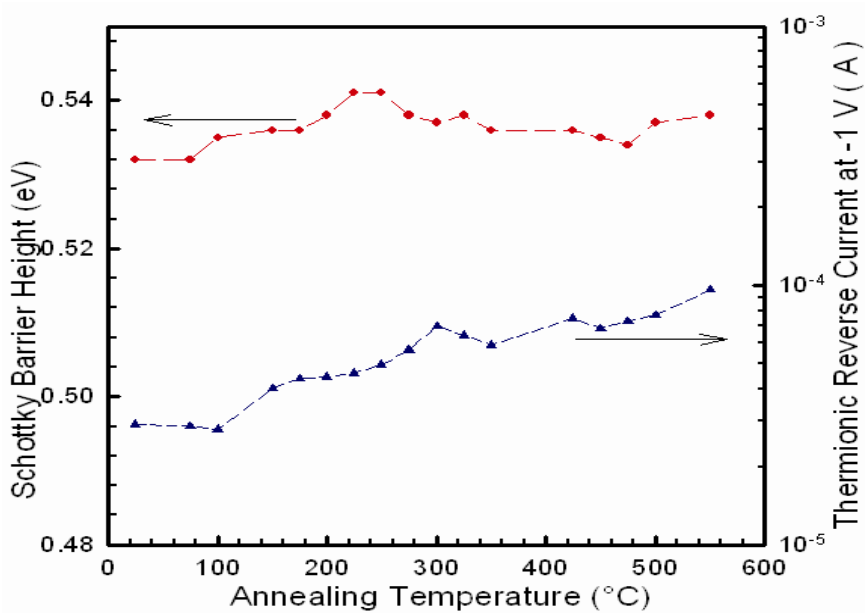


Fig. 4.5 *Plot of the Schottky barrier height and reverse current at –1 V as a function of annealing temperature for Ni/n-Ge (100) Schottky contacts.*

4.3.3 Ti/n-Ge (100) Schottky diodes

The semilog forward and reverse bias $I-V$ characteristics of Ti/n-Ge (100) Schottky barrier diodes annealed in 25-425°C temperature range, together with those of as-deposited diodes are presented in Fig. 4.6.

The as-deposited Schottky barrier height and reverse current at –1 V for Ti/n-Ge (100) Schottky contacts were found to be (0.566 ± 0.005) eV and (7.76 ± 0.02) μA, respectively. Variation of barrier height and reverse current at a bias voltage of –1 V with annealing temperature for Ti/n-Ge (100) contacts is shown in Fig 4.7. The barrier height was approximately constant within experimental error up to an annealing temperature of 225°C. After further annealing at higher temperatures the barrier height decreased, reaching a minimum value of (0.497 ± 0.005) eV at 300°C. This change in barrier height could be associated with the phase formation of a germanide Ti_6Ge_5, which has been reported to form at 300°C [14]. The subsequent increase in barrier height after annealing at temperatures higher than 300°C coincides with the temperature range for the formation of germanide Ti_5Ge_3 [14].

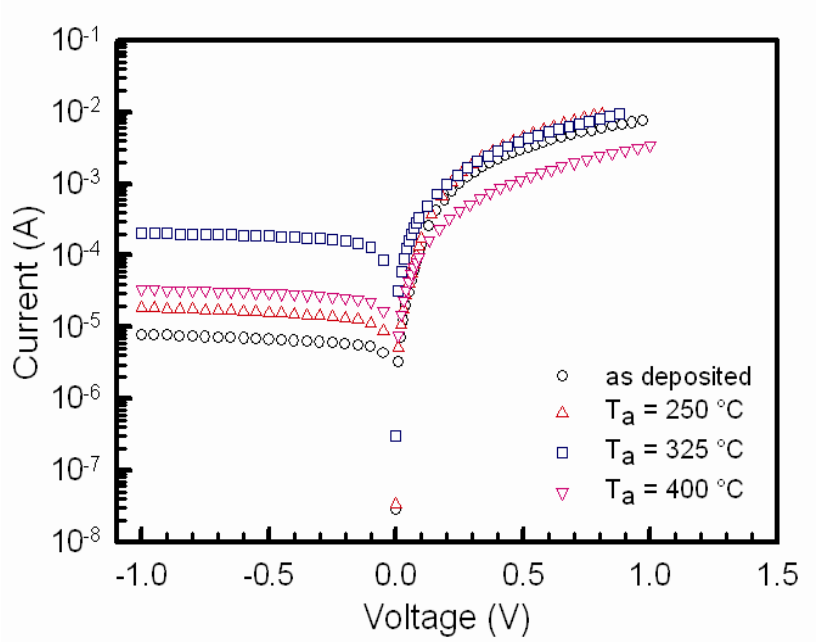


Fig. 4.6 *Experimental forward and reverse I-V characteristics of one of the Ti/n-Ge (100) Schottky barrier diodes after isochronal thermal treatment for 30 min at different annealing temperatures: as-deposited, 250°C, 325°C and 400°C.*

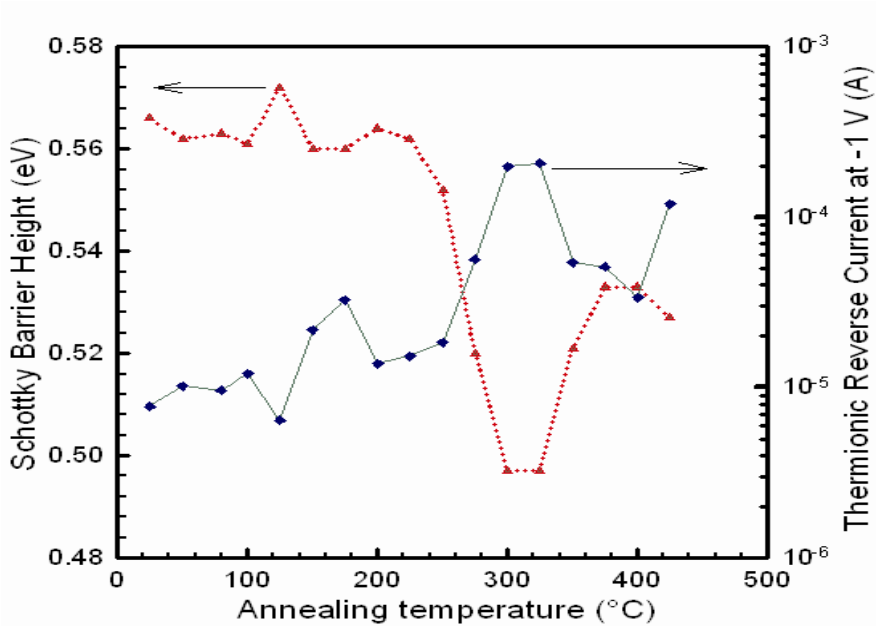


Fig 4.7 *Plot of the Schottky barrier height and reverse current at –1 V as a function of annealing temperature for Ti/n-Ge (100) Schottky contacts.*

After a 425°C anneal, $I-V$ characteristics of the Ti/n-Ge (100) severely deteriorated, and the contacts became near-ohmic. Even after subjecting these contacts to a temperature of 20 K, *I-V* measurements revealed no improvement in their rectifying behaviour.

The variation of ideality factor with annealing temperature for Ti/n-Ge (100) Schottky diodes is shown in Fig. 4.3 (c). The ideality factors were between 1.29 and 3.05 at annealing temperatures between 25°C and 425°C.

4.3.4 Co/n-Ge (100) Schottky diodes

The variation in the electrical parameters, SBH and reverse current at –1 V for Co/n-Ge (100) Schottky contacts (Fig. 4.8) coincides with the temperature ranges of Co germanide phases formed by annealing as reported by Hsieh et al. [16] and Sun et al. [31], with CoGe forming between 100-300°C, Co_5Ge_7 forming around 300°C and $CoGe_2$ forming at temperatures above 425°C. Fig 4.9 (a) depicts the variation of Co/n-Ge (100) ideality factors with annealing temperatures in the 25-550°C temperature range.

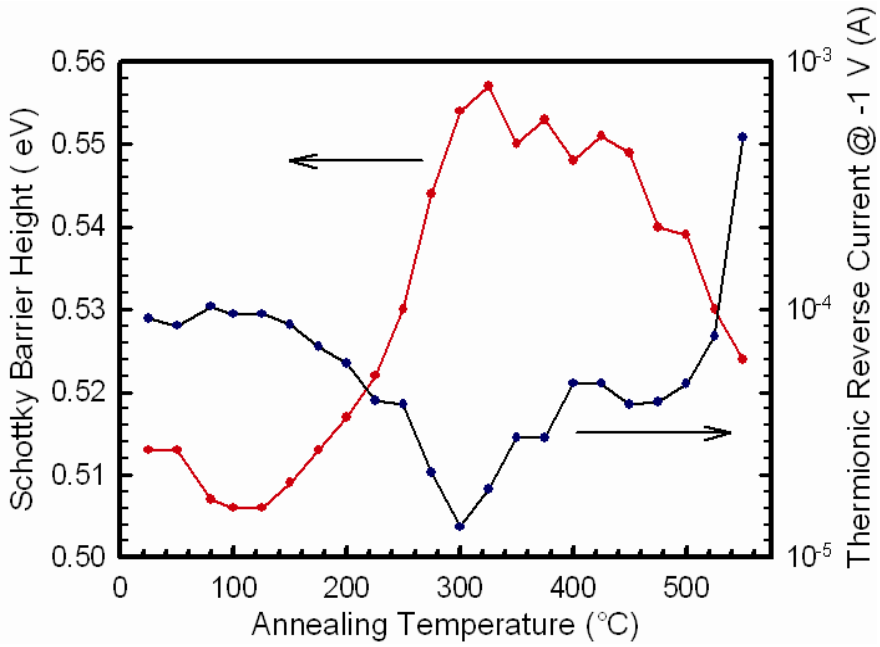


Fig. 4.8 *Plot of the Schottky barrier height and reverse current at –1 V as a function of annealing temperature for Co/n-Ge (100) Schottky diodes.*

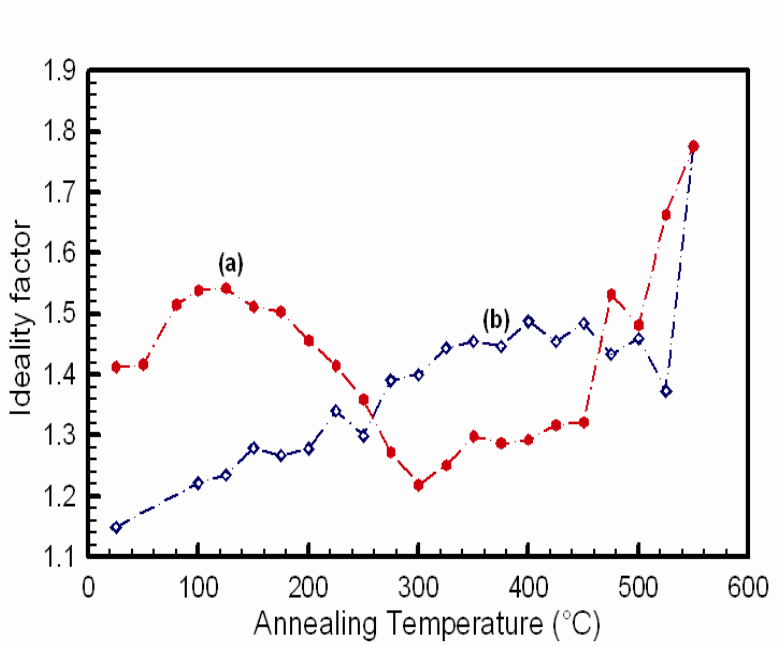


Fig. 4.9 *Plot of the ideality factor as a function of annealing temperature for (a) Co/n-Ge (100) and (b) Pd/n-Ge (100) Schottky diodes.*

4.3.5 Pd/n-Ge (100) Schottky diodes

Fig. 4.10 shows the variation of the SBH and reverse current at –1 V with annealing temperature for Pd Schottky contacts on n-Ge (100). The SBH and reverse current at a bias voltage of –1 V for as-deposited Pd/n-Ge (100) Schottky diodes were found to be (0.540 ± 0.005) eV and (17.00 ± 0.02) μA, respectively. The variation of Pd/n-Ge (100) Schottky contacts barrier height between 100-500°C is approximately constant within experimental error. According to Gaudet et al. [3], only one germanide phase, PdGe exists for Pd on n-Ge (100) in this temperature range. This germanide is stable over a wide range of temperature. The variation of Pd/n-Ge (100) Schottky contacts ideality factors with annealing temperature is shown in Fig. 4.9 (b).

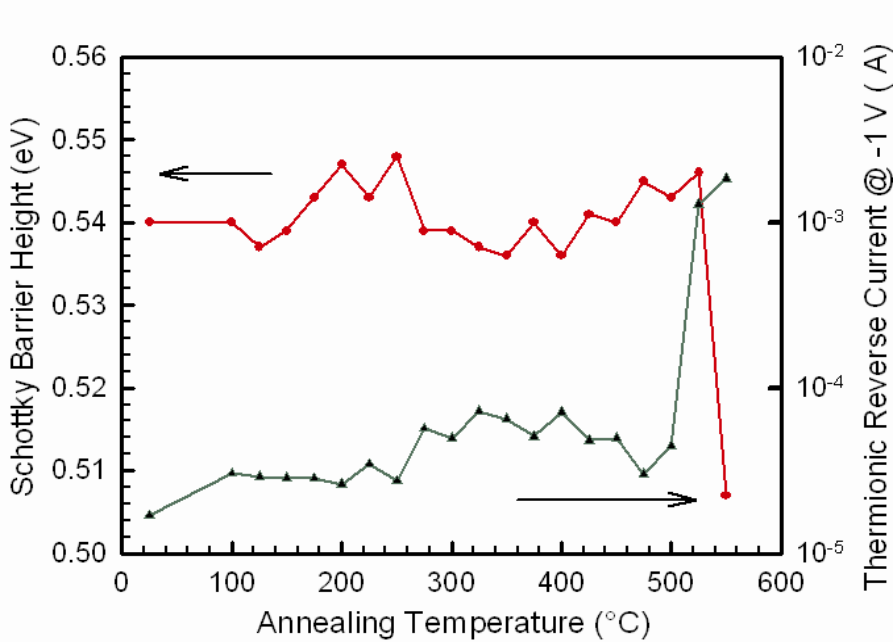


Fig. 4.10 *Plot of the Schottky barrier height and reverse current at –1 V as a function of annealing temperature for Pd/n-Ge (100) Schottky diodes.*

4.3.6 Ir/n-Ge (100) Schottky diodes

Fig. 4.11 shows the semilog forward and reverse bias $I-V$ characteristics of Ir/n-Ge (100) Schottky diodes annealed in the temperature range 25-500°C, together with those of as-deposited samples. Fig. 4.12 represents the variation of the Schottky barrier height and reverse current at –1 V with annealing temperature for the Ir Schottky diodes on n-Ge (100). The SBH and reverse current at a bias voltage of –1 V for as-deposited Ir/n-Ge (100) Schottky diodes were found to be (0.574 ± 0.005) eV and (2.57 ± 0.02) μA, respectively. After annealing at temperatures higher than 200°C, the barrier height drops significantly, reaching (0.542 ± 0.05) eV after a 400°C anneal, suggesting that a significant reaction occurred between Ir and Ge. The change coincides with the initial phase formation of the IrGe and Ir_4Ge_5 germanides, which have been reported by Habanyama et al. [26] to coexist and form at annealing temperatures around 350°C. Bhan and Scubert [32] also reported the phases IrGe and Ir_4Ge_5 to coexist in bulk diffusion couples. The change in the barrier height after the 400°C anneal also coincides with the temperature of formation of germanide Ir_3Ge_7 reported by Habanyama et al. [26]. Fig. 4.12 also depicts that, throughout the annealing process the reverse current at –1 V remains in the same order of magnitude, i.e. 10^{-6} A. After

a 525°C anneal, the electrical characteristics of the Ir Schottky contacts severely deteriorated, the contacts became near ohmic and further evaluation was impossible.

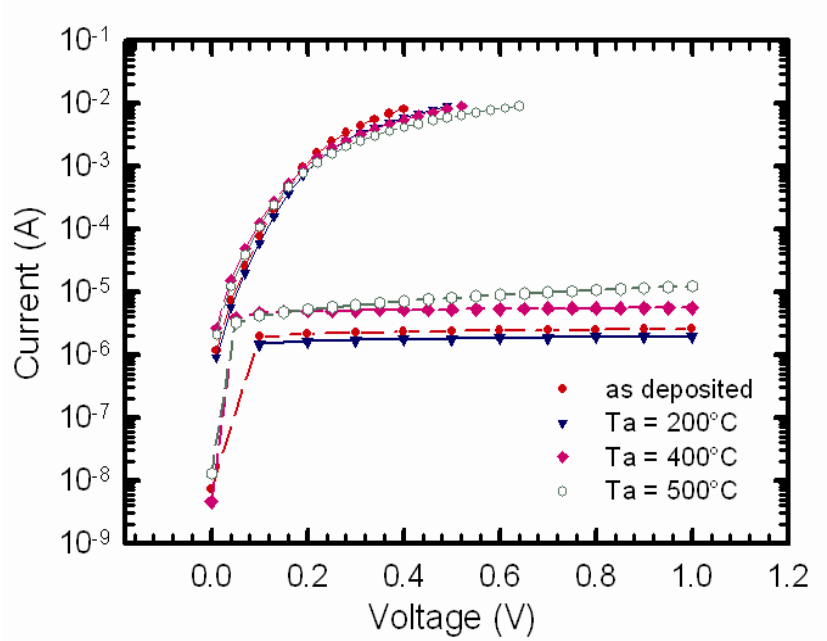


Fig 4.11 *Experimental forward and reverse I-V characteristics of one of the Ir/n-Ge (100) Schottky barrier diodes after isochronal thermal treatment at different annealing temperatures: as-deposited, 200°C, 400°C and 500°C.*

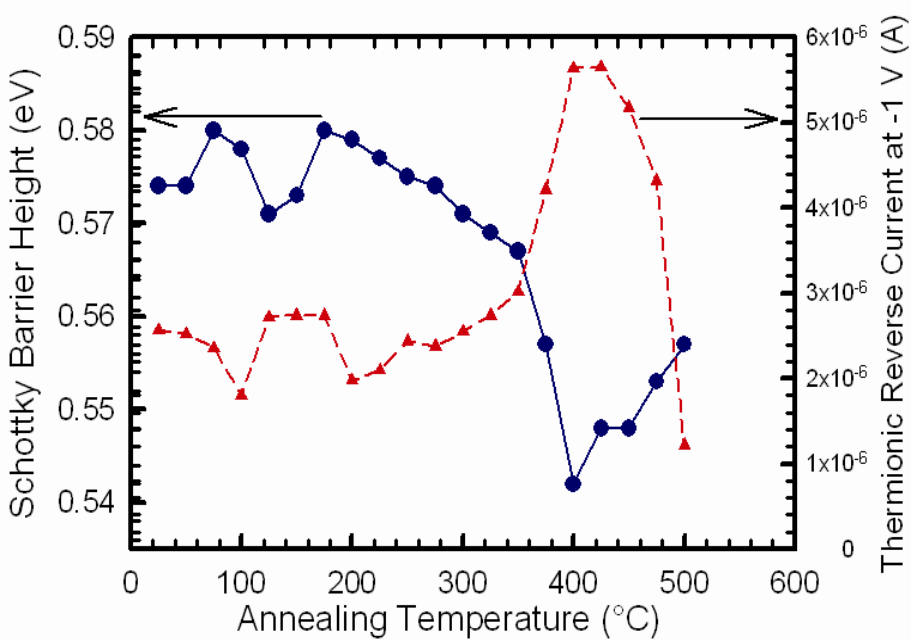


Fig. 4.12 *Plot of the Schottky barrier height and reverse current at –1 V as a function of annealing temperature for Ir Schottky contacts on n-Ge (100).*

Fig. 4.13 shows a plot of barrier heights as a function of their respective ideality factors, obtained during the annealing process in the temperature range 25-500°C. The straight line in Fig. 4.13 is the least squares fit to experimental data. Since the results show a linear correlation between barrier heights and ideality factors, we then extrapolated the plot to ideality factor, n = 1.0 and obtained a laterally homogeneous barrier height of (0.595 ± 0.005) eV for Ir/n-Ge (100) structures. The homogeneous barrier heights rather than effective BHs of contacts or their mean values should be used to discuss theories on the physical mechanisms that determine the BHs of metal-semiconductor contacts [33,34].

Fig 4.14 shows the plots of the reverse bias C^{-2} *versus* V characteristics at 1.0 MHz of Ir/n-Ge (100) Schottky diodes at different annealing temperatures. The plots of C^{-2} as a function of reverse bias voltage are linear, indicating the formation of Schottky diodes [35] and a constant donor concentration. In Schottky diodes, the depletion layer capacitance (C) , can be expressed as [29,36]

$$\frac{1}{C^2} = \frac{2(V_0 - V)}{q\varepsilon_s A^2 N_D} \tag{4.4}$$

where A is the area of the diode, ε_s is the permittivity of the semiconductor, N_D is the carrier doping density, V is the magnitude of the reverse bias and V_0 is the diffusion

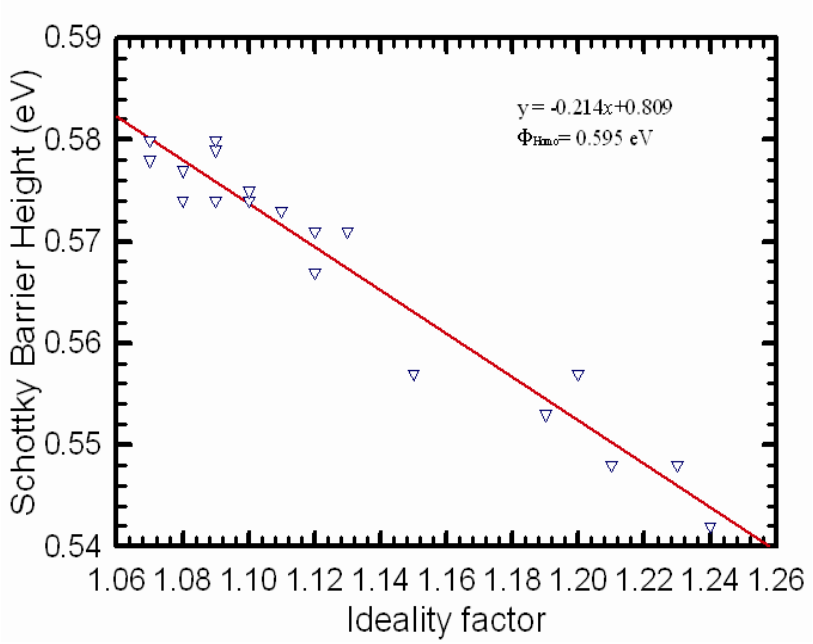


Fig 4.13 *The plot of barrier heights as a function of their respective ideality factors of the Ir/n-Ge (100) Schottky barrier diodes at various annealing temperatures.*

potential at zero bias. From Eq. (4.4), the values of V_0 and N_D can be determined from the intercept and slope of the C^{-2}-V plot respectively.

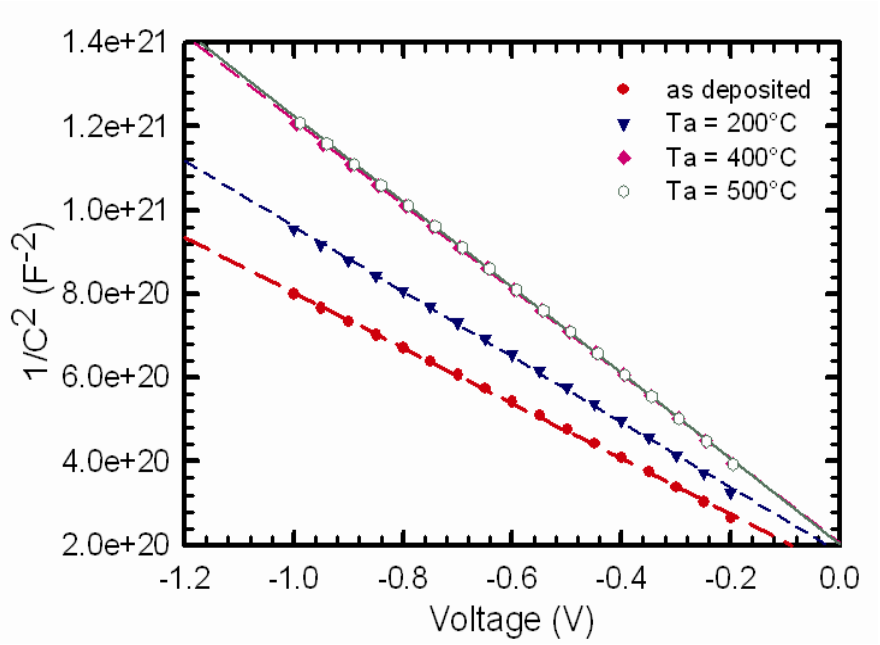


Fig. 4.14 *C^{-2}-V characteristics of one of the Ir/n-Ge (100) Schottky diodes at frequency of 1.0 MHz after isochronal treatment for 30 min at different annealing temperatures: as-deposited, 200°C, 400°C and 500°C measured at room temperature.*

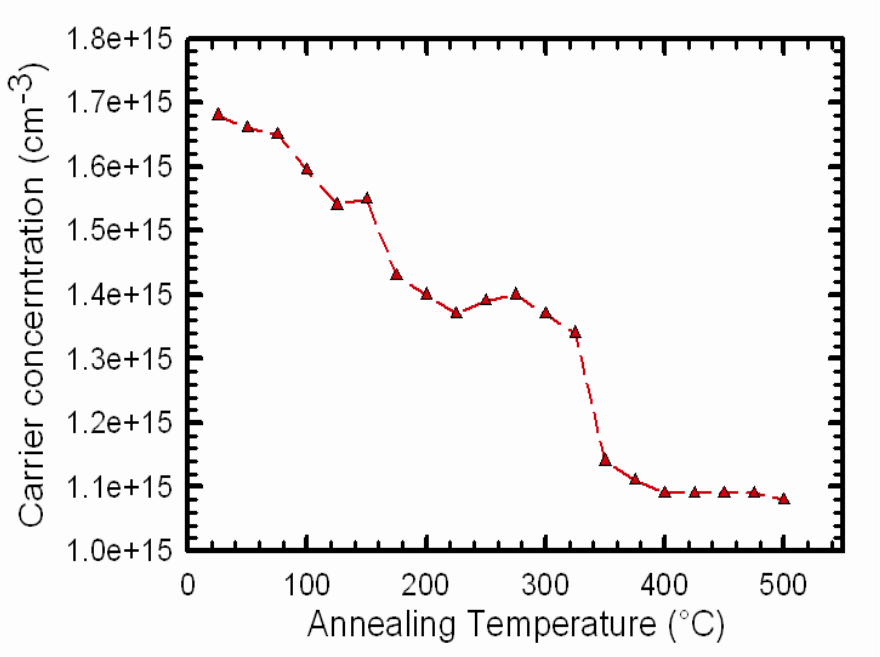


Fig. 4.15 *The variation of the carrier concentration with annealing temperature.*

Fig 4.15 depicts the variation of carrier doping concentration with annealing temperature. The carrier concentration decreases with increasing annealing temperature. Similar results have been reported by Serin [37], Nuhoglu et. al [38] and Opsomer et al. [39]. This may be due to either the presence of high density of compensating deep acceptor levels [37], possibly related to in-diffused Ir or the decrease in the dangling bonds due to annealing [38] and formation of Iridium germanide [26].

4.3.7 Ru/n-Ge (100) Schottky diodes

The variation of Schottky barrier height and reverse current at –1 V with annealing temperature for the Ru/n-Ge (100) Schottky diodes is depicted in Fig. 4.16. The values of SBH and reverse current at a bias of –1 V for as-deposited samples were determined to be (0.557 ± 0.005) eV and (5.79 ± 0.02) μA, respectively. The results (Fig. 4.16) indicate nearly a constant Schottky barrier height in the temperature range 50-150°C. After annealing at temperatures higher than 150°C the barrier height decreases with annealing temperature and a low Schottky barrier of (0.467 ± 0.005) eV is achieved after a 280°C anneal, suggesting a significant reaction between Ru and the Ge substrate forming a germanide.

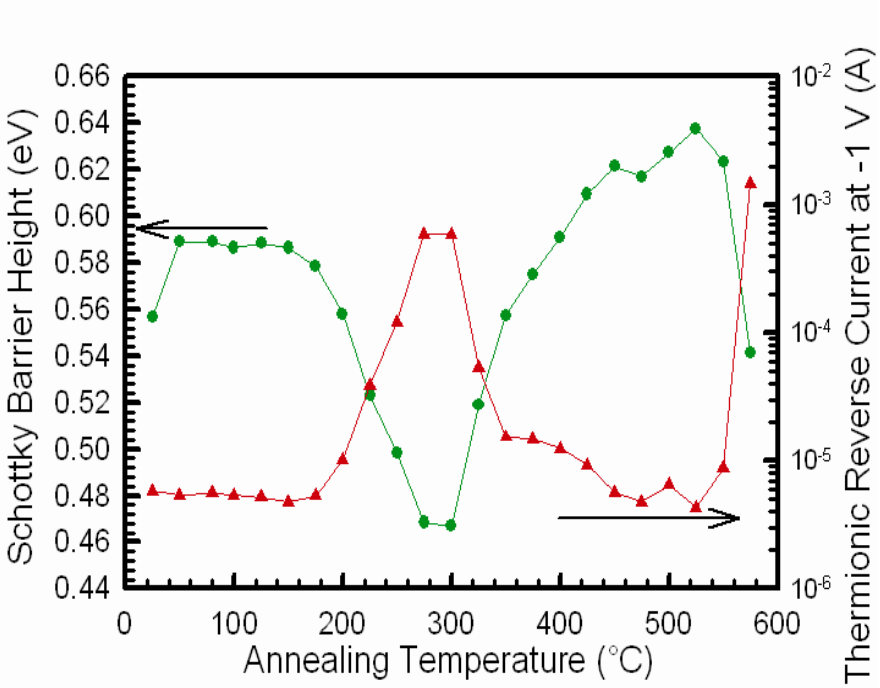


Fig. 4.16 *Plot of the Schottky barrier height and reverse current at –1 V as a function of annealing temperature for Ru/n-Ge (100) Schottky diodes.*

Although Gaudet et al. [3] have reported the first phase of Ru germanide, Ru+Ru_2Ge_3 forming at 450°C after ramp anneal, we propose that after subjecting the Schottky contacts to isochronal annealing, the first phase of Ru germanide is formed in the temperature range 150-300°C, as the SBH decreases significantly above 150°C annealing. The subsequent increase in barrier height after annealing at temperatures higher than 300°C depicts the formation of the Ru germanide Ru_2Ge_3, in the temperature range 325-525°C. After a 550°C anneal the contacts became near-ohmic and further evaluation was impossible.

Fig. 4.17 shows the variation of ideality factor (*n)* with annealing temperature for the Ru/n-Ge (100) Schottky contacts. The value of *n* for as-deposited samples was determined to be 1.08. This ideality factor is almost a constant within experimental error up to an annealing temperature of 175°C. After annealing at temperatures higher than 175°C the ideality factors were greater than 1.1.

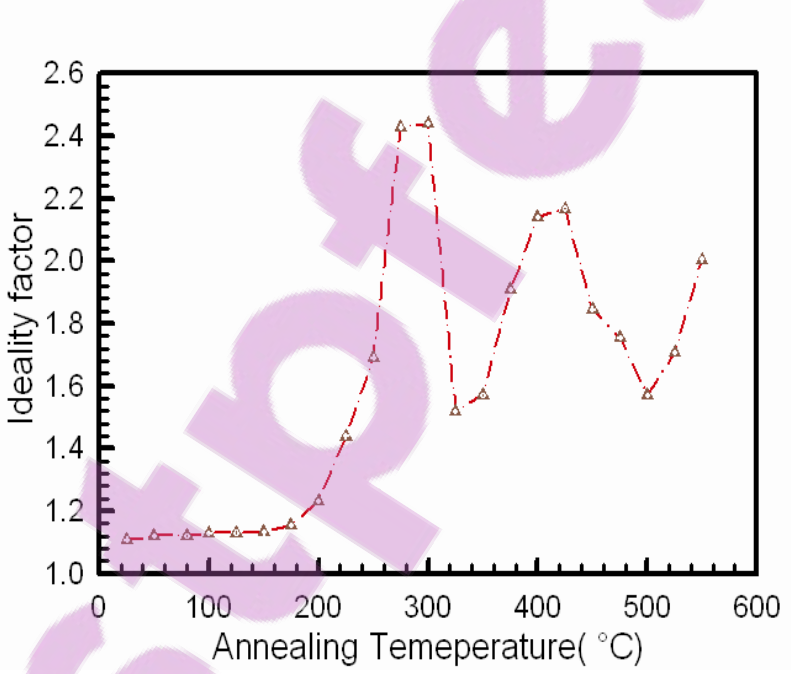


Fig. 4.17 *Plot of ideality factor as a function of annealing temperature for Ru/n-Ge (100) Schottky contacts.*

4.4 Discussion

The fundamental mechanisms that determine the barrier height are still not fully understood [36,40,41,42]. The barrier height is likely to be a function of the interface atomic structure and atomic inhomogeneities at the metal-semiconductor interface which are caused by grain

boundaries, multiple phases, facets, defects, a mixture of different phases, etc [43,44]. It is well known that the chemical reactions between metals and semiconductors at interfaces can play an important role in the electrical properties of devices. Boyarbay et al. [45] suggested that the recent motivation for studying Schottky barrier formation is due to the recognition that both electronic and chemical equilibrium have to be considered together across a reactive interface between metal and semiconductor as surface states and metal-induced gap states failed to take into consideration the chemical equilibrium at the interface. During the annealing process, metals may react with semiconductors. The chemical equilibrium after heat treatment results in interfacial atomic rearrangement, interdiffusion and compound formation, which should have a profound effect on the electronic equilibrium producing the Schottky barrier [46]. Hence, the change in the Schottky barrier heights may be attributed to combined effects of interfacial reactions and phase transformation [27]. The Schottky barrier height is also temperature dependent, due to the fact that the measured current across a Schottky junction is a combination of thermionic emission and recombination currents [47]. Furthermore, the barrier height change in Schottky contacts can be explained according to the effective work function (EWF) model [48], where the barrier height value is determined by the work function of microclusters of one or more phases resulting from either oxygen contamination or metal-semiconductor reactions which occur during metallization and annealing, and each phase having its own effective work function [49].

For ideal Schottky contacts the ideality factor is 1.0. The ideality factors for Schottky contacts found to be greater than 1.1, indicates that the transport properties are not well modelled by thermionic emission alone although these contacts remain rectifying [50]. The deviation from ideality has been attributed mostly to the states associated with the defects near surface of the semiconductor [47]. These interface states, inter-diffusion, chemical reaction, compound formation, defects generation, etc. can all be derived from thermodynamics due to thermal annealing [51,52,53]. These may lead to recombination centres [50] and SBH inhomogeneities [54], which cause a flow of excess current leading to a deviation from the ideal thermionic emission behaviour.

4.5 Summary and conclusion

Pt/-, Ti/-, Ir/- and Ru/n-Ge (100) Schottky contacts were fabricated by electron beam deposition. Ni/-, Co/- and Pd/n-Ge (100) Schottky diodes were fabricated by resistive deposition. The Schottky contacts behaviour was investigated under various annealing conditions. The variation of Schottky barrier heights and ideality factors with annealing temperature may be attributed to interfacial reactions of metals (Pt, Ni, Ti, Co, Pd, Ir, Ru) with germanium and the phase transformation of the metal-germanides during annealing. The electrical properties of the metal Schottky contacts reveal that Pt/n-Ge (100) and Ir/n-Ge (100) Schottky contacts are of high quality with low reverse currents at –1 V of the order (10^{-5} to 10^{-6}) A and as-deposited ideality factors as low as 1.09. The as-deposited barrier heights of nearly equal in magnitude to the bandgap of Ge in the Pt/-, Ni/-, Ti/- and Ir/n-Ge (100) Schottky contacts imply good Schottky source/drain contact materials in p-channel Ge-MOSFETS, for the hole injection from source into inverted p-channel [2]. The results also show that Pt/n-Ge (100) and Ru/n-Ge (100) Schottky contacts are highly thermally stable over a wide range of temperatures compared to Ni/-, Ti/-, Co/-,Pd/- and Ir/n-Ge (100) Schottky contacts.

References

[1] M. G. Grimaldi, L. Weilunski, M.-A. Nicolet, Thin Solid Films **81** (1981) 207.

[2] H.B. Yao, C.C. Tan, S.L. Liew, C.T. Chua, C.K. Chua, R. Li, R.T.P. Lee, S.J. Lee, D.Z. Chi, International Workshop on Junction Technology Processing, (2006) 164.

[3] S. Gaudet, C. Detavernier, A.J. Kellock, P. Desjardins, C. Lavoie, J. Vac. Sci. Technol. A **24** (3) (2006) 474.

[4] R. Gumeniuk, W. Schnelle, H. Rosner, M. Nicklas, A. Leithe-Jasper, Yu Grin, Phys. Rev. Lett. **100** (2008) 0170021.

[5] A. Łaszcz, J. Ratajczak, A. Czerwinski, J. Kątcki, V. Srot, F. Philipp, P.A. van Aken, N. Breil, G. Larrieu, E. Dubois, Mater. Sci. Eng. B **154-155** (2008) 175.

[6] F. Ohtsu, H. Fukuoka, S. Yamanaka, J. Alloys Compd. **487** (2009) 712.

[7] A. Thanaillakis, D.C. Northrop, Solid State Electron. **16** (1973) 249.

[8] F. Nemouchi, D. Mangelinck, J.L. Lábár, M. Putero, C. Bergman, P. Gas, Microelectron. Eng. **83** (2006) 2101.

[9] C.-Y. Peng, Y.-H. Yang, C.-M. Lin, Y.-J. Yang, C.-F. Huang, C.W. Liu, International Conference on Solid-State and Integrated Circuits Technology Proceeding (ICSICT), art. No. 4734645 (2008) 681

[10] X. An. C. Fan. R. Huang, X. Zhang, Proceedings- Electrochemical Society, PV 1 (2008) 408.

[11] C.-Y. Peng, C.-F. Huang, Y.-J. Yang, C.W. Liu, ECS Trans. **16** (2008) 249.

[12] X. An, C. Fan, R. Huang, X. Zhang, Chin. Phys. Lett. **26** (2009) 0873041.

[13] C. Perrin, D. Mangelinck, F. Nemouchi, J. Labar, C. Lavoie, C. Bergman, P. Gas, Mater. Sci. Eng. B **154-155** (2008) 163

[14] H. Dedong, W. Xin, W.Yi, Wang, T. Dayu, W. Wei,L. Xiaoyan, K. Jinfeng, H. Ruqi, Microelectron. Eng. **82** (2005) 93

[15] M. Wittmer, M.A. Nicolet, and J.W. Mayer, Thin Solid Films **42** (1977) 51.

[16] Y.F. Hsieh, L.J. Chen, L.J. Marshall, and S.S. Lau, Appl. Phys. Lett. **51** (1987)1588.

[17] S.P. Ashburn, M.C. Öztürk, G. Harris, and D.M. Maher, J. Appl. Phys. **74** (1993) 4455.

[18] E.D. Marshall, C.S. Wu, C.S. Pai, D.M. Scott, and S.S. Lau, Thin Solid Films: Material Research Society (MRS) Symposia Proceedings, Pittsburg, PA, (1985) 161.

[19] G. Ottaviani, C. Canali, G. Ferrari, G. Majni, M. Prudenziati, and S.S. Lau, Thin Solid Films **47** (1977) 187.

[20] Y.F. Hsieh and L.J. Chen, Thin Solid Films **162** (1988) 295)

[21] P.S. Salamakha, O.I. Bodak, V.K. Percharskii, V.K. Bel'skii, Russian Metallurgy, Metally **1** (1989) 210.

[22] B. Pene, M. Hofmann, J. Leciejewicz, M. Ślaski, A. Szytuła, J. Alloys Compd. **287** (1999) 18.

[23] U.C. Rodewald, R. Pöttgen, Solid State Sci. **5** (2005) 487.

[24] D.X. Li, S. Nimori, Y. Homma, Y. Shiokawa, J. Appl. Phys. **97** (2005) 073903-1.

[25] K. Katoh, T. Tsutsumi, K. Yamada, G. Terui, Y. Niide, A. Ochiai, Physica B **373** (2006).

[26] A. Habanyama, C.M. Comrie, Thin Solid Films **516** (2008) 5137.

[27] Y. Sun, X.M. Shen, J. Wang, D.G. Zhao, G. Feng, Y. Fu, S.M. Zhang, Z.H. Zhang, Z.H. Feng, Y.X. Bai, H. Yang, J. Phys. D.: Appl. Phys. **35** (2002) 2648.

[28] F.D. Auret, P.J. Janse van Rensburg, M. Hayes, J.M. Nel, S. Coelho, W.E. Meyer, S. Decoster, V. Matias, A. Vantomme, D. Smeets, Nucl. Instrum. Methds B **257** (2007) 169.

[29] S.M. Sze, Physics of Semiconductor Devices, New York, 1981, p. 245.

[30] B. Li, S. Chua, Y. Nikolai, L. Wang, E. Sia, Solid State Electron. **47** (2003) 602.

[31] H.P. Sun, Y.B Chen, X.Q. Pan, D.Z. Chi, R. Nath, and Y.L. Foo, Appl. Phys. Lett. **86** (2005) 071904.

[32] S. Bhan, K. Schubert, Z. Metallkunde. **51** (1960) 327.

[33] R.F. Schmitsdorf, T.U. Kampen, W. Mönch, J. Vac. Sci. Technol. B. **15** (1997) 1221.

[34] H. Çetin, B. Şahin, E. Ayyilidiz, A. Turut, Semicon. Sci. Technol. **19** (2004) 1113

[35] V. Saxen, R. Prakash, Polym. Bull. **45** (2000) 267.

[36] E.H. Rhoderick, R.H. Williams, Metal-Semiconductor Contacts, Clarendon Press Oxford, 1988.

[37] T. Serin, Tr. J. Phys. **22** (1998) 423.

[38] C. Nuhoglu, Y. Gulen, Vacuum **84** (2010) 812.

[39] K. Opsomer, E. Simoen, C. Clayes, K. Maex, C. Detavernier, R.L. Van Meirhaeghe, S. Forment, P. Clauws, Mater. Sci. Semicond. Processing **9** (2006) 554.

[40] E. Hökelek, G.Y. Robinson, Solid State Electron. **99** (1981) 24.

[41] K. Bourenane, A. Keffous, G. Nezzal, Vacuum **81** (2007) 663.

[42] S. Chand, S. Bala, Physica B **390** (2007) 179.

[43] J.P. Sullivan, R.T. Tung, M.R. Pinto, W.R. Graham, J. Appl. Phys. **70** (1991) 7403.

[44] R.T. Tung, Mater. Sci. Eng. R **35** (2001) 1.

[45] B. Boyarby, H. Çetin, M. Kaya, E. Ayyildiz, Microelectron. Eng. **85** (2008) 721

[46] R.D. Thomson, K.N. Tu, J. Appl. Phys. **53** (1982) 4285.

[47] A.R. Saha, S. Chattopadhyay, C.K. Maiti, Mater. Sci. Eng. B **114-115** (2004) 218.

[48] J.L. Freeouf, J.M. Woodall, Appl. Phys. Lett. **29** (1976) 263.

[49] E. Ayyildiz, A. Türüt, Solid State Electron. **43** (1999) 521.

[50] H. Dogan, N. Yildirim, A. Turut, Microelectron. Eng. **85** (2008) 655.

[51] T. Sands, Appl. Phys. Lett. **52** (1988) 197.

[52] S.K. Cheung, N.W. Cheung, Appl. Phys. Lett. **49** (1986) 85.

[53] J.L. Everaet, R.L. Van Meirhaeghe, W.H. Laflĕre, F. Cardon, Semicond. Sci. Technol. **5** (1990) 60.

[54] R.T. Tung, J.P. Sullivan, F. Schrey, Mater. Sci. Eng. B **14** (1992) 266.

List of publications

1. A. Chawanda, C. Nyamhere, F.D. Auret, W. Mtangi, T.T. Hlatshwayo, M. Diale, J.M. Nel, Physica B **404** (2009) 4482.

2. A. Chawanda, C. Nyamhere, F.D. Auret, W. Mtangi, M. Diale, J.M. Nel, J. Alloys Compd. **492** (2010) 649.

3. A. Chawanda, C. Nyamhere, F.D. Auret, W. Mtangi, M. Diale, and J.M. Nel, Phys. Status Solidi, **7** (2010) 248.

CHAPTER 5: RESULTS

Morphological evolution of metal Schottky contacts on n-Ge (100)

5.1 Introduction

As device dimensions are scaled to submicrometer dimensions in silicon-based microelectronics, new processes and materials are becoming necessary to overcome the limitations of the conventional methods [1]. Of interest are silicon compatible materials that provide better device performance. Germanium (Ge) is a promising material for high mobility devices due to its higher and more symmetric carrier mobility compared with silicon [2], and its excellent compatibility with high-k materials [3]. Metal germanides may be used as contact materials in future germanium technology. Compared with silicides that have been extensively investigated in the past [3,4], formation of germanides on single crystal germanium surface attracted less attention. However, most of the studies on germanide formation up to date have been carried out using in-situ annealing by slowly-ramping annealing temperature or rapid thermal annealing processing (RTP), rather than using furnace annealing, and also with less emphasis on morphological evolution [5]. In this study, we investigated the evolution and microstructure stability of metal (Pt, Ni, Ti, Ir, and Ru) films on n-Ge (100) after furnace annealing.

5.2 Experimental procedures

Ge (100) n-type substrates were used in this study. The substrates were first degreased and subsequently etched in a mixture of H_2O_2 (30%): H_2O (1:5) for 1 min. Metal films of 30 nm were deposited by electron beam or resistive evaporation with base pressure less than 10^{-6} Torr. The metal layer thickness and deposition rates were monitored with a quartz crystal thickness monitor. The metal films were isochronally annealed in an oven under flowing Ar ambient in the temperature range 25-800°C for 30 min.

The characterization of the films for as-deposited and after different annealing temperatures was accomplished using a JEOLJSM-5800LV and a ZEISS ULTRA PLUS scanning electron microscopy (SEM) systems operating at 5 kV and 1 kV, respectively.

5.3 Results and Discussion

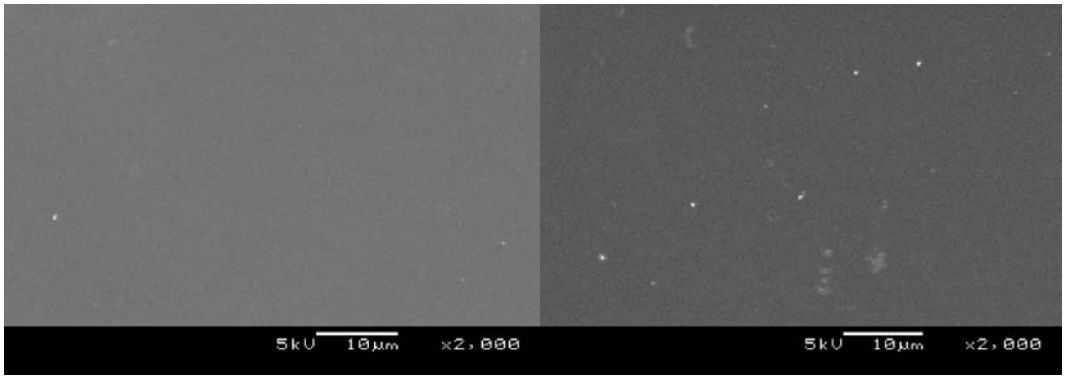
In this section results on the morphological evolution and microstructure stability of metal (Pt, Ni, Ti, Ir, Ru) films on n-Ge (100) using furnace annealing are presented.

5.3.1 Morphological evolution of Pt films on n-Ge (100)

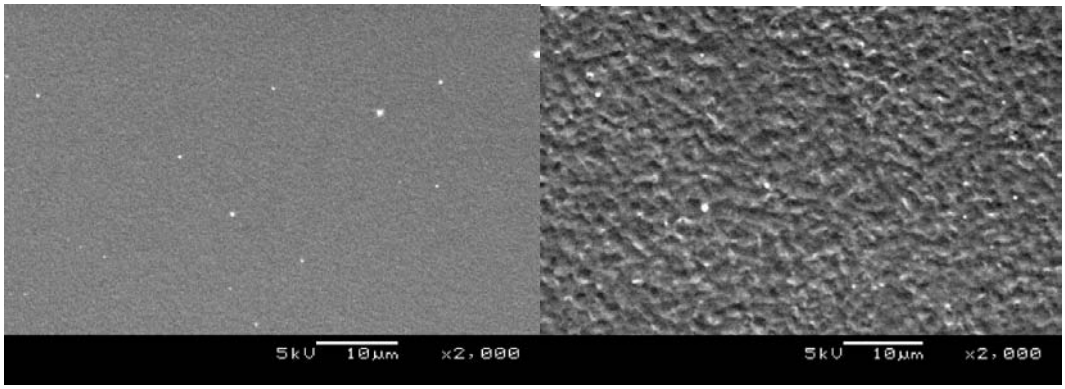
Scanning electron microscopy (SEM) observations were conducted for Pt/n-Ge (100) samples, as-deposited and after annealing at different temperatures. The morphological evolution of Pt/n-Ge (100) is shown in Fig. 5.1. As shown in Fig. 5.1 (a), (b) and (c), metal surfaces show little change when samples were annealed below 600°C. This is in agreement with what was reported by Yao et al. [6] that the Pt-germanide exhibited no sign of agglomeration even up to 500°C anneal, suggesting good morphological stability for Pt-germanide films. Onset of surface roughening occurs at 500 °C. At 600°C anneal and above (see Fig. 5.1 (d-e)), the surface becomes rough, indicating the agglomeration of Pt, finally destroying the contact, as evidenced by the loss of rectifying properties of the Pt Schottky contacts after 600°C anneal (reported in Chapter 4, section 4.3.1). From the results, it can be concluded that the onset temperature for agglomeration in the 30 nm Pt/Ge (100) system occurs at 600 – 700°C.

5.3.2 Morphological evolution of Ni films on n-Ge (100)

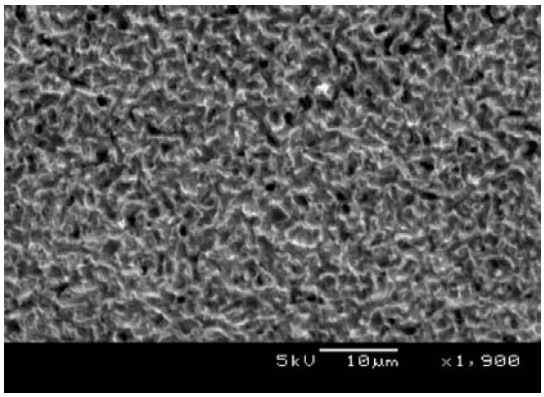
Fig. 5.2 shows the evolution of surface morphology for Ni/n-Ge (100) with annealing temperature. Although Lee et al. [5] and Zhang et al. [7] have reported grain growth and groove deepening at the surface after a 400°C anneal for Ni film thickness of 15 nm, with Yao et al. [6] reporting the development of severe grain boundary grooving after 500°C anneal (onset temperature for 15 nm Ni film agglomeration), prominent grain growth at the surface of 30 nm layer (see Fig. 5.2 (c)) were evident from 500°C, indicating inception of agglomeration.



(a) (b)



(c) (d)



(e)

Fig. 5.1 *SEM observation for Pt films deposited on germanium after isochronal thermal treatment for 30 min at different annealing temperatures: (a) as-deposited, (b) 400°C, (c) 500°C, (d) 600°C and (e) 700°C*

Agglomeration starts with grain boundary grooving and progresses to island formation [5]. After a 600°C anneal, we observed development of severe grain grooving. The temperature at which grain growth and agglomeration occurs decreases with reduced film thickness [4]. This is consistent with the grooving model for agglomeration [4], as in our study the metal film thickness was 30 nm. We also observed that after 700°C (see Fig. 5.2 (e)), film continuity was severely interrupted as indicated by dark spots caused by exposed Ge regions. The agglomeration is driven by the minimization of the total surface/interface energy of the metal-germanide and germanium substrate [8]. We have found that the onset of the agglomeration process for 30 nm Ni/n-Ge(100) system to be in 500 – 600°C.

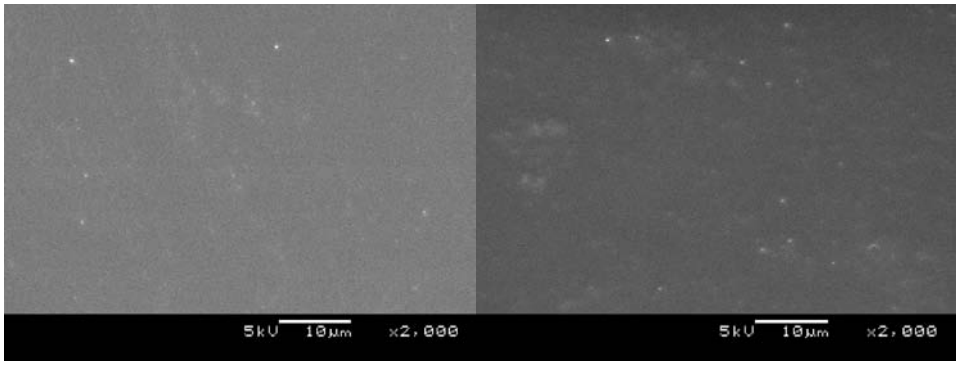
5.3.3 Morphological evolution of Ti films on n-Ge (100)

Fig 5.3 shows the SEM images of Ti/n-Ge (100) films at different annealing temperatures. Although Ti/Schottky contacts lost their rectifying behaviour after 425°C anneal, the metal surface shows no change when the sample was annealed below 600°C. Grain growth and grove deepening at the surface were evident from 700°C, suggesting better morphological stability than Pt and Ni films.

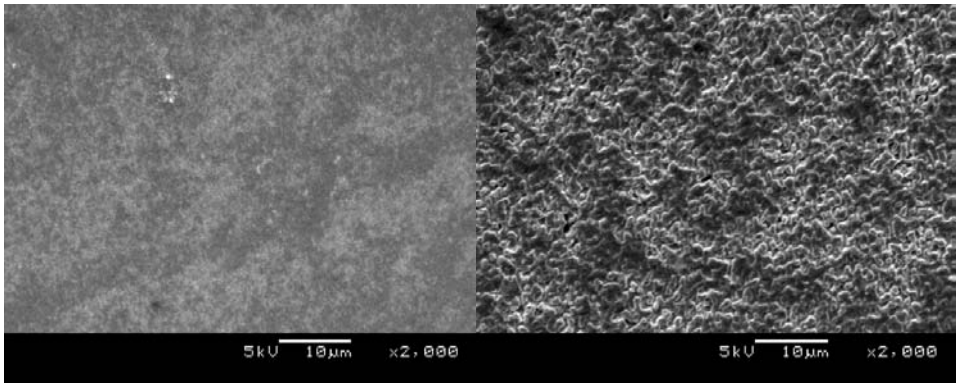
5.3.4 Morphological evolution of Ir films on n-Ge (100)

SEM observations of the Ir/n-Ge (100) for as-deposited sample and morphological evolution of the samples after annealing at different temperatures are shown in Fig. 5.4. In Fig. 5.4 (a) and (b) the metal surface shows little change when annealed below 400°C. Grain growth at the surface (see Fig. 5.4 (c)) was evident after a 500°C anneal. From this we suggest a relatively good morphological stability for Ir germanide films. A severe grain grooving was observed after 600°C anneal (see Fig. 5.4 (d)). We also observed that after 700°C anneal (see Fig. 5.4 (e)), film continuity was severely interrupted due to grain growth.

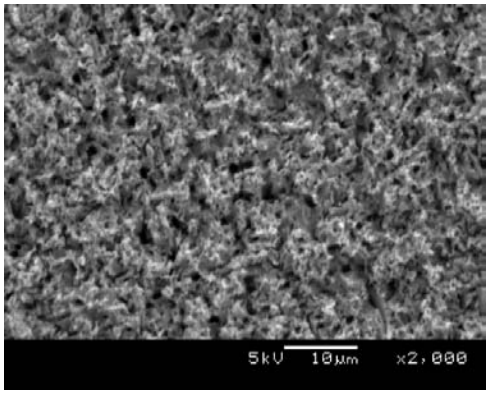
From these observations we conclude that the onset of the agglomeration process for 30 nm Ir/n-Ge (100) system occurs at 600 – 700°C.



(a) (b)

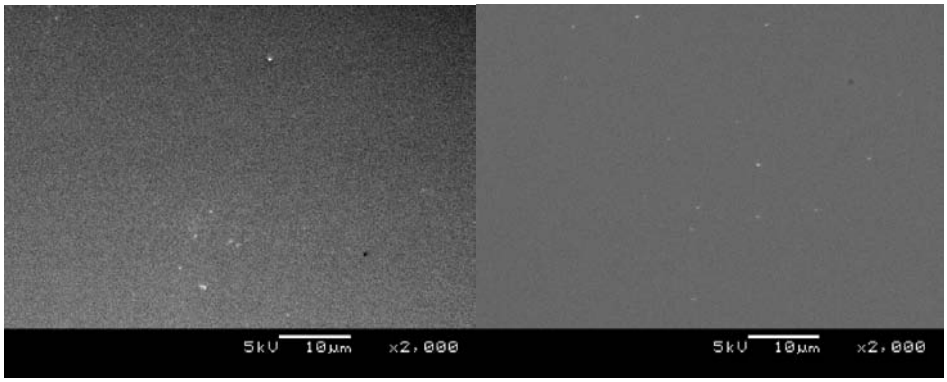


(c) (d)

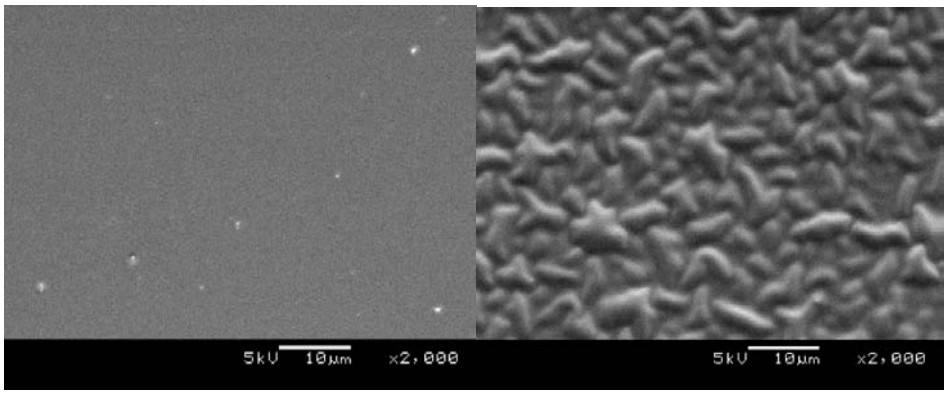


(e)

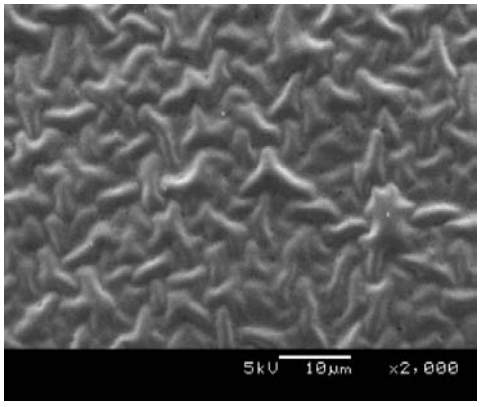
Fig. 5.2 *SEM observation for Ni films deposited on germanium after isochronal thermal treat for 30 min at different annealing temperatures: (a) as-deposited, (b) 400°C, (c) 500°C, (d) 600°C and (e) 700°C.*



(a) (b)

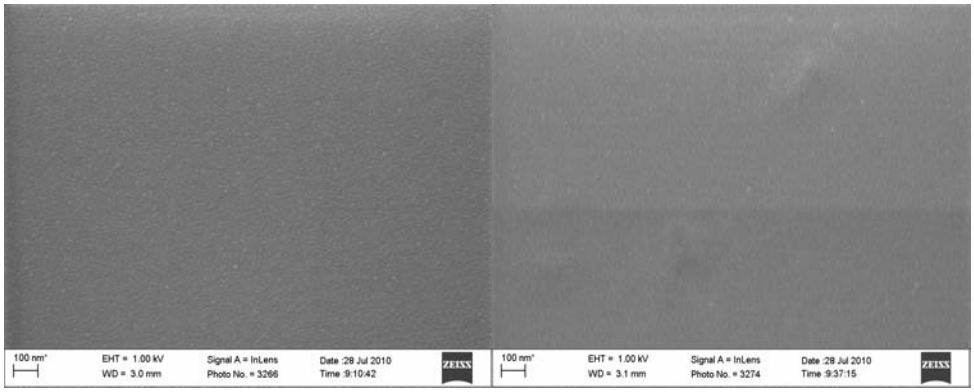


(c) (d)

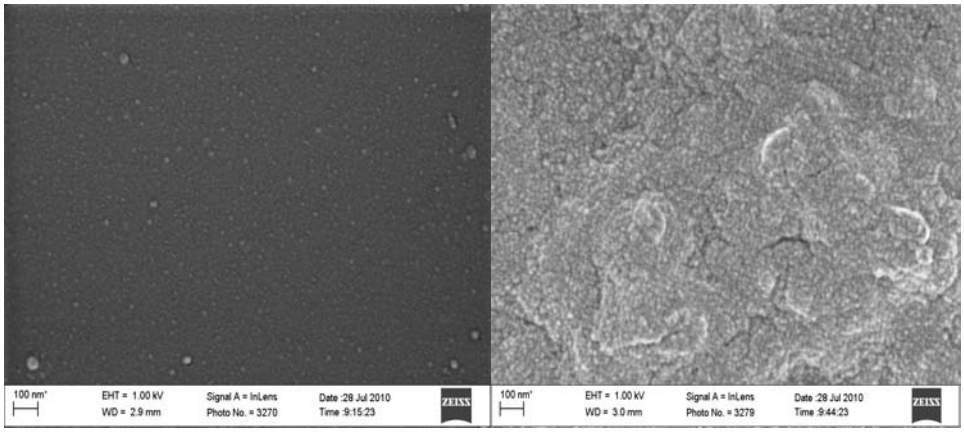


(e)

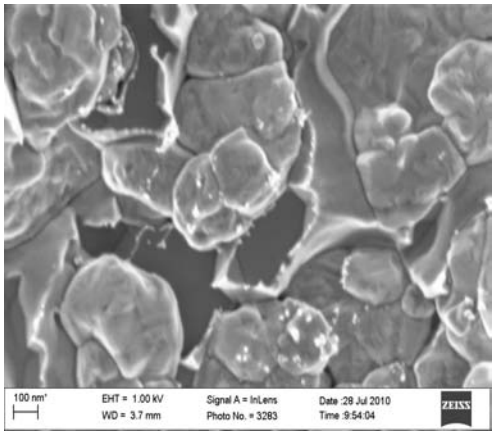
Fig. 5.3 *SEM observation for Ti films deposited on germanium after isochronal thermal treat for 30 min at different annealing temperatures: (a) as-deposited, (b) 500°C, (c) 600°C, (d) 700°C and (e) 800°C.*



(a) (b)

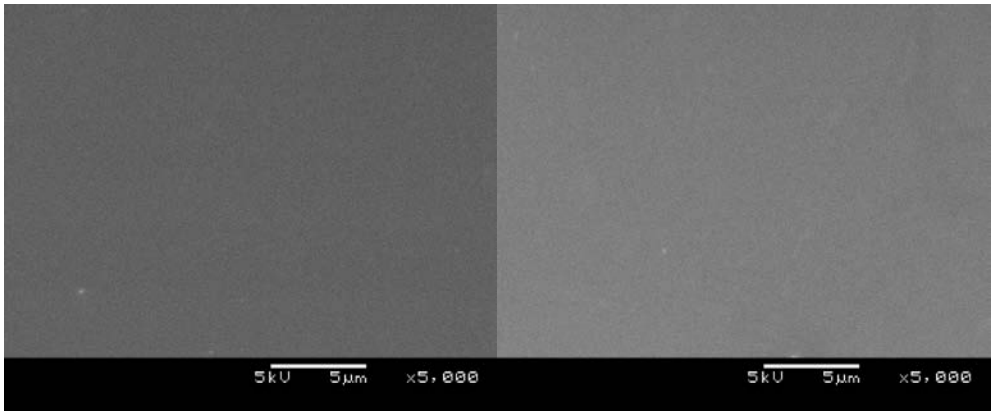


(c) (d)

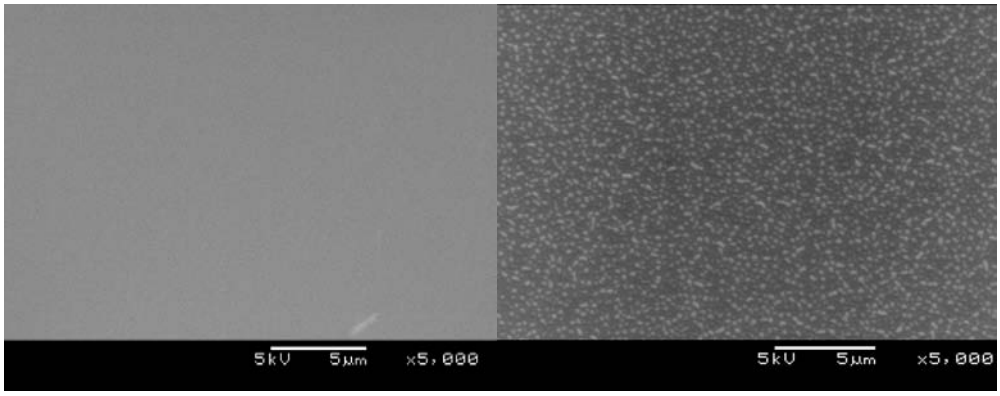


(e)

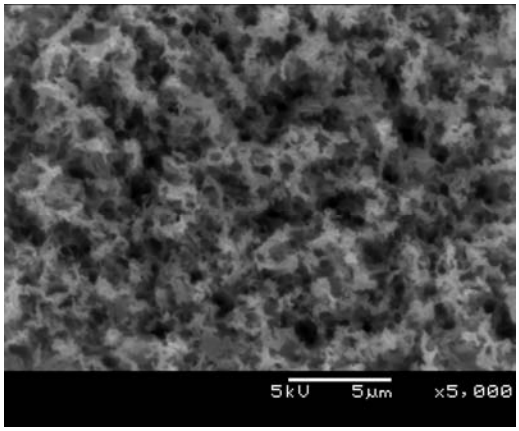
Fig. 5.4 *SEM observation for Ir films deposited on germanium after isochronal thermal treat for 30 min at different annealing temperatures: (a) as-deposited, (b) 400°C, (c) 500°C, (d) 600°C and (e) 700°C.*



(a) (b)



(c) (d)



(e)

Fig. 5.5 *SEM observation for Ru films deposited on germanium after isochronal thermal treat for 30 min at different annealing temperatures: (a) as-deposited, (b) 400°C, (c) 500°C, (d) 600°C and (e) 700°C.*

5.3.5 Morphological evolution of Ru films on n-Ge (100)

SEM observations of the Ru/n-Ge (100) for as-deposited and morphological evolution of the samples after annealing at different temperatures are shown in Fig. 5.5. In Fig. 5.5 (a), (b) and (c) the metal surface shows little change when annealed below 500°C. Grain growth at the surface was evident after a 600°C anneal (see Fig. 5.5 (d)). After annealing at 700°C (see Fig. 5.5 (e)), film continuity was interrupted as indicated by dark spots caused by exposed Ge regions. It can be concluded from the SEM micrographs that the onset of agglomeration in the Ru/n-Ge (100) system is at 600 – 700°C.

5.4 Summary and Conclusions

Pt, Ti, Ir, and Ru films were deposited by electron beam system, while Ni films were deposited by resistive evaporation on n-Ge. SEM observations were conducted for samples annealed at different temperatures. From SEM observations, it can be concluded that the onset temperature in 30 nm Ni/n-Ge (100), and Pt-, Ir- and Ru/n-Ge (100) systems occurs at 500 – 600 °C and 600 – 700°C, respectively. Grain growth at the surface of these metals was evident from 500°C, suggesting a better morphological stability.

References

[1] S.P. Ashburn, M. Öztürk,, G. Harris and D. M. Maher, J. Appl. Phys. **74** (1993) 4455.

[2] X. An, C. Fan, R. Huang, X. Zhang, Chin. Phys. Lett. **26** (2009) 087304.

[3] H.P. Sun, Y.B. Chen, X.Q. Pan, D.Z. Chi, R. Nath, and Y.L. Floo, Appl. Phys. Lett. **86** (2005) 071904.

[4] S.L. Zhang and M. Ostling, Crit. Rev. Solid State Mater. Sci. **28** (2003) 1.

[5] K.Y. Lee, S.L. Liew, S.J. Chua, D.Z. Chi, H.P. Sun and X.Q. Pan, Mat. Res. Symp. Proc. **810** (2004) C.2.4.1.

[6] H. B. Yao, C.C. Tan, S.L. Liew, C.T. Chua, R. Li, R. T.P. Lee. S.J. Lee, D.Z. Chi, International Workshop on Junction Technology Proceeding, 2006, p. 164.

[7] Q. Zhang, N.W. Wu, T. Osipowicz, L.K. Bera, C. Zhu, Jpn. J. Appl. Phys. **44** (2005) L1389.

[8] J.P. Gambino, E.G. Colgan, Mater. Chem. Phy. **52** (1998) 99.

List of publications

1. A. Chawanda, C. Nyamhere, F.D. Auret, W. Mtangi, m. Diale, J.M. Nel, J. Alloys Compd. **492** (2010) 649.

2. J.M. Nel, A. Chawanda, F.D. Auret, W. Jordaan, R.Q. Odendaal, M. Hayes, S. Coelho, Physica B **404** (2009) 4493.

CHAPTER 6: RESULTS

The barrier height distribution in identically prepared metal Schottky contacts on n-Ge (100)

6.1 Introduction

The Schottky barrier height (SBH) is one of the most interesting properties of a MS interface [1]. The electronic properties of the MS contacts are characterized by their SBH. The SBH is, therefore, of vital importance to the successful operation of any semiconductor device [1]. The mechanisms that determine the SBH are still not fully understood [2,3,4,5]. It is only in the past two decades that an inhomogeneous contact has been considered as an explanation for a voltage-dependent SBH [1,2,6]. The SBH is likely to be a function of the interface atomic structure and the atomic inhomogeneities at MS interface, which are caused by grain boundaries, multiple phases, facets, defects, a mixture of different phases, etc. [7,8,9,10]. It has also been suggested by Song et al. [11] that the barrier inhomogeneities can occur as a result of inhomogeneities in the interfacial oxide layer composition, nonuniformity of the interfacial charges and interfacial oxide layer thickness. The presence of barrier inhomogeneities may greatly influence the current across the MS contact [11]. Tung et al. [10,12] assumed lateral variations of SBH to model imperfect Schottky structures, and they depicted larger ideality factors and smaller effective SBHs when they increased the inhomogeneity of barriers. The experimental effective SBHs and ideality factors obtained from the current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics differ from diode to diode even if they are identically prepared [10, 12,13,14,15]. This finding has been attributed to interfacial patches, i.e. small regions with lower SBH than the junction's main SBH [1,12].

Although studies have been performed to investigate the relationship between the effective BHs and ideality factors of the metal/Si Schottky diodes [16,17,18,19,20], nothing has yet been reported on the relationship between effective SBHs and ideality factors from forward bias *I-V*

and reverse bias *C-V* characteristics of the metals/Ge Schottky diodes. In this study palladium (Pd), nickel (Ni) and gold (Au) Schottky diodes on n-type germanium were fabricated under experimentally identical conditions in order to investigate the relationship between the effective BHs and ideality factors obtained from the forward bias *I-V* and reverse bias *C-V* characteristics of these metals Schottky diodes. The homogeneous SBH values for Pd/n-Ge (111), Ni/n-Ge (100) and Au/n-Ge (100) Schottky diodes were obtained from the linear relationship between the experimental effective SBHs and ideality factors which is experimentally [15,21,22,23,24] and theoretically [10,12 ,25] confirmed. The homogeneity or uniformity of the SBH is an issue with important implications on the theory of SBH formation [26], and important ramifications for the operation of Schottky diodes [13,15,23 24]. The importance of this homogeneous BH is that, it depicts the real meaningful value characteristic for the MS system [18], which should be used to develop theories of physical mechanisms determining these BHs of Schottky contacts [27]. The rest of the Chapter is organised as follows: Section 6.2, briefly describes the experimental procedure. Results and discussions are presented in Section 6.3. A summary of the work is given in section 6.4.

6.2 Experimental procedures

We used bulk-grown, (100)-oriented, n-type Ge, doped with antimony (Sb) to a density of about 2.5×10^{15} cm^{-3} and supplied by Umicore. Before metallization, the samples were first degreased and subsequently etched in a mixture of H_2O_2(30%):H_2O (1:5) for 1 minute. Immediately after cleaning, the samples were inserted into a vacuum chamber where AuSb (0.6%Sb), 100 nm thick, was deposited by resistive evaporation on the back surfaces as Ohmic contacts. The samples were then annealed at 350°C in Ar atmosphere for 10 minutes to minimise the contact resistivity of the Ohmic contacts [28]. Before Schottky contacts deposition, the samples were again chemically cleaned as described above. Pd, Ni and Au Schottky contacts were deposited onto Ge wafers by using vacuum resistive evaporation at a pressure below 10^{-6} Torr. The contacts were 0.6 mm in diameter and 30 nm thick. The thickness of the metal layer and the deposition rates were monitored with the help of a quartz crystal thickness monitor. After the contact fabrication, the Schottky barrier diodes (SBDs) were characterized by using *I-V* and *C-V* measurements at room temperature.

6.3 Results and discussions

The BHs of the contacts were deduced from the *I-V* characteristics, which were analysed by using the thermionic emission model given by the following equation [2,29]:

$$I(V) = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{6.1}$$

with

$$I_0 = A^* A T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \tag{6.2}$$

where I_0 is the saturation current derived from straight line intercept of the $\ln(I)-V$ plot at $V=0$, V is the bias voltage, T is the absolute temperature, q is the electronic charge, k is the Boltzmann constant, A is the effective diode area, A^* is the effective Richard constant, Φ_B is the zero bias effective SBH. From Eq. (6.2) we have:

$$\Phi_B = \frac{kT}{q}\ln\left(\frac{A^* A T^2}{I_0}\right) \tag{6.3}$$

and n is the ideality factor, which is a measure of conformity of the diode to pure thermionic emission. The values of n are calculated from slope of the linear part of an $\ln(I)$ *versus* V plot, assuming pure thermionic emission

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \tag{6.4}$$

which is equal to 1 for an ideal diode and usually has a value greater than unit for practical diodes.

We fabricated 20 contacts (Schottky barrier diodes) for Pd-/, Ni-/ and Au/n-Ge (100) on the same n-type semiconductor substrate by evaporation of Pd, Ni or Au as the Schottky contact. Figs. 6.1 - 6.3 show the room temperature experimental forward and reverse bias *I-V*

characteristics of Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) Schottky barrier diodes (SBDs). The *I-V* effective BHs for the Pd, Ni and Au diodes varied from 0.513 to 0.558 eV, 0.487 to 0.508 eV and 0.507 to 0.598 eV, respectively, and ideality factors for Pd, Ni and Au diodes ranged from 1.11 to 1.57, 1.34 to 1.53 and 1.12 to 2.03, respectively.

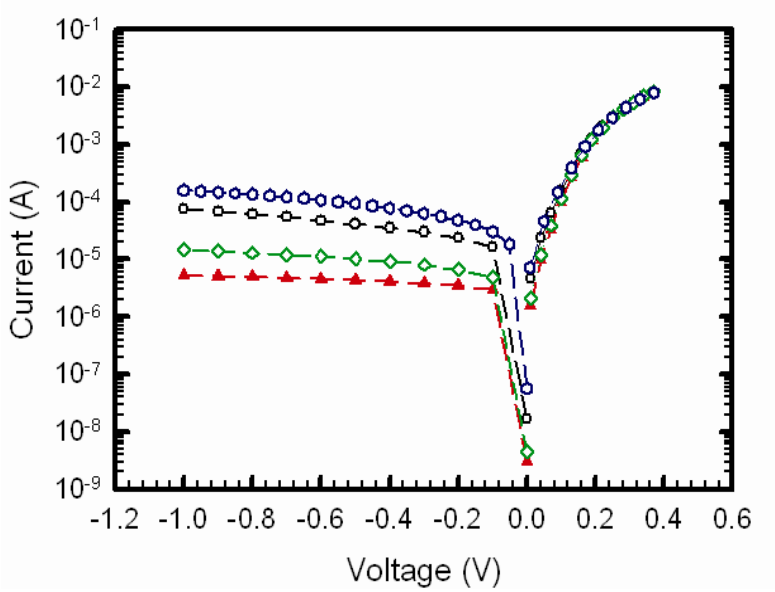


Fig. 6.1 *The plot of the forward and reverse bias current-voltage (I-V) characteristics for five Pd/n-Ge (100) Schottky diodes at room temperature.*

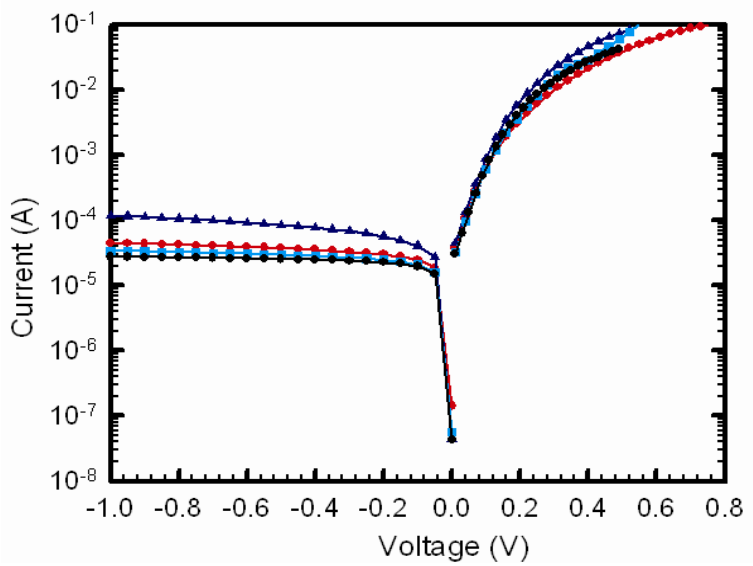


Fig. 6.2 *The plot of the forward and reverse bias current-voltage (I-V) characteristics for four Ni/n-Ge (100) Schottky diodes at room temperature.*

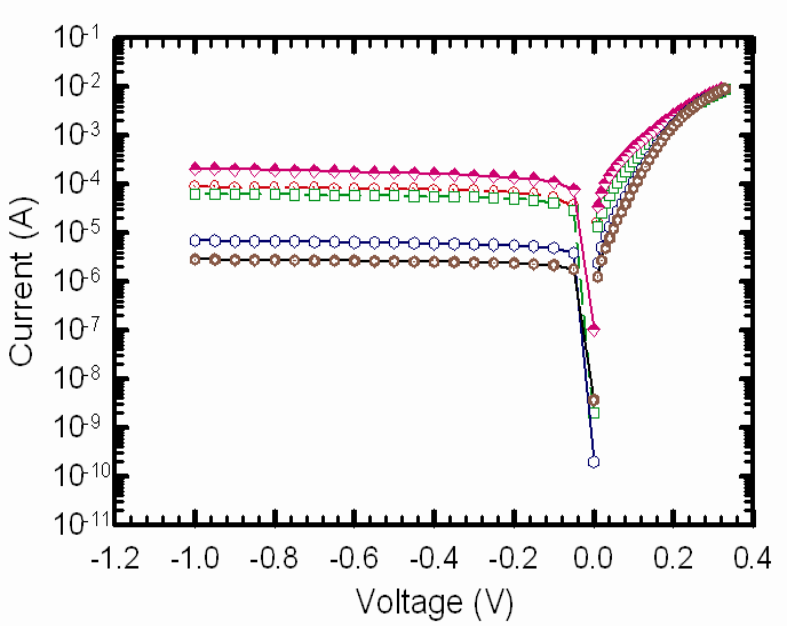


Fig. 6.3 *The plot of the forward and reverse bias current-voltage (I-V) characteristics for five Au/n-Ge (100) Schottky diodes at room temperature.*

Thus, the experimental effective SBHs and ideality factors from the *I-V* characteristics can differ from diode to diode even though they were identically prepared on the same sample.

In Schottky diodes, the depletion layer capacitance, *C* can be expressed as [2]:

$$\frac{1}{C^2} = \frac{2(V_i - V)}{q\varepsilon_s A^2 N_D} \tag{6.5}$$

where A is the area of the diode, ε_s is the dielectric constant of the semiconductor, V_i is obtained from the intercept of C^{-2} with the voltage axis and is given by:

$$V_i = V_d - kT / q \tag{6.6}$$

and N_D is the donor concentration of the n-type semiconductor substrate. From Eq. (6.5), the values of N_D can be determined from the slope of the $C^{-2} - V$ plot. Figs. 6.4 - 6.6 show room temperature reverse bias $C^{-2} - V$ characteristics for selected samples of the Pd/n-Ge (100), Ni/n-

Ge (100) and Au/n-Ge (100) Schottky diodes recorded at 1 MHz. The values of the BH $\Phi_B(C-V)$ can be obtained from Figs 6.4 - 6.6 as

$$\Phi_B(C-V) = V_d + \xi - \Delta\Phi_B \tag{6.7}$$

where ξ is the energy difference between the bulk Fermi level and the conduction band edge, V_d is the diffusion potential and $\Delta\Phi_B$ is the image force barrier lowering and is given by [2,29]

$$\Delta\Phi_B = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right]^{\frac{1}{2}}, \tag{6.8}$$

where ε_0 is the free space dielectric constant and E_m is the maximum electric field and is given by

$$E_m = \left[\frac{2qN_DV_0}{\varepsilon_s\varepsilon_0}\right]^{\frac{1}{2}} \tag{6.9}$$

The plots of C^{-2} as a function of reverse bias voltage (Figs 6.4-6.6) are linear, which indicate the formation of Schottky diodes [30] and a nearly constant donor concentration profile in the region close to the substrate surface.

The capacitance-voltage BH for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) diodes ranges from 0.320 to 0.381 eV, 0.358 to 0.418 eV and 0.286 to 0.429 eV, respectively. These results depict that the parameters of Schottky diodes vary from diode to diode even if they are identically prepared. Therefore, their averages should be used [12,13,14,21,25].

Figs. 6.7 - 6.9 show the histograms of BHs from the forward bias *I-V* plots of Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) MS structures, respectively. Figs. 6.10-6.12 show the statistical distribution of BHs from $C^{-2}-V$ plots of the same diodes. Gaussian distribution function was used to obtain fits to the histograms.

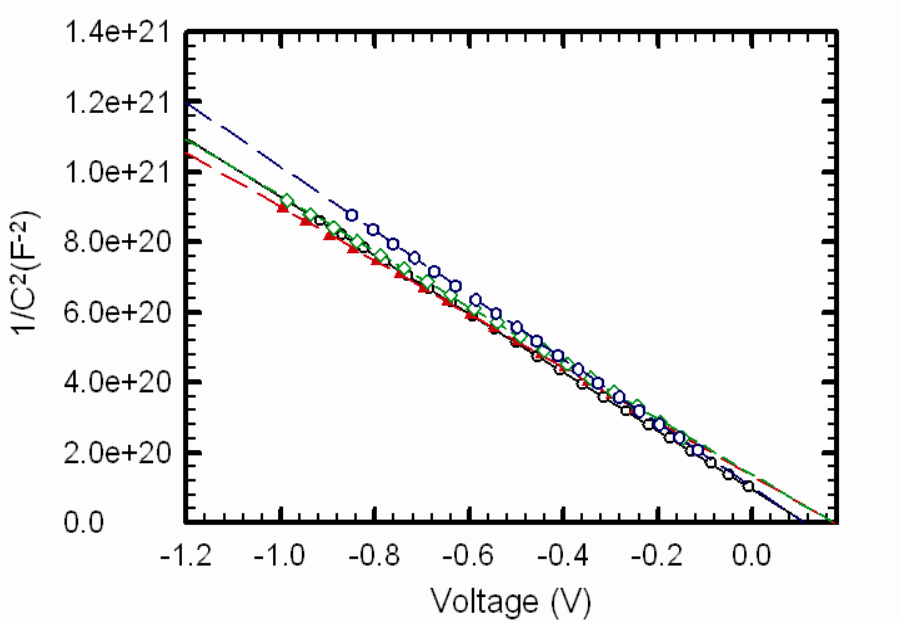


Fig. 6.4 *Reverse bias $C^{-2} - V$ characteristics for five Pd/n-Ge (100) Schottky diodes recorded at 1 MHz and room temperature.*

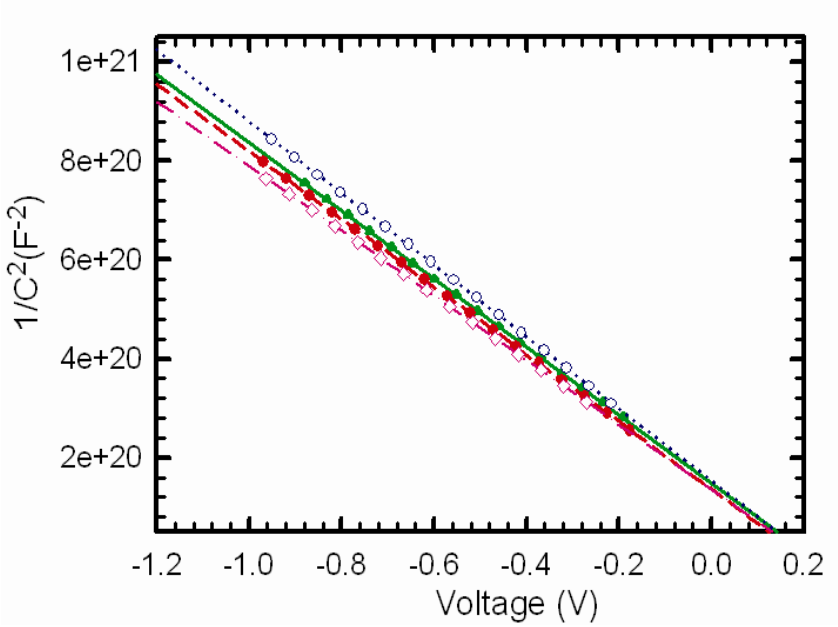


Fig. 6.5 *Reverse bias $C^{-2} - V$ characteristics for four Ni/n-Ge (100) Schottky diodes recorded at a frequency of 1 MHz and room temperature.*

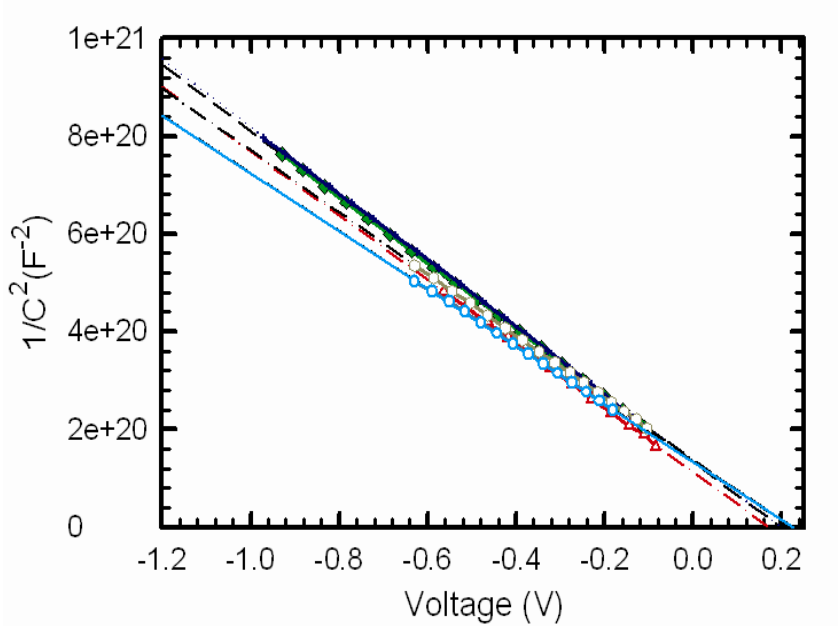


Fig. 6.6 *Reverse bias $C^{-2}-V$ characteristics for samples Au/n-Ge (100) Schottky diodes recorded at a frequency of 1 MHz and room temperature.*

The probability of SBH $P(\Phi_B)$ has the form [31,32]:

$$P(\Phi_B) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left\{-\frac{(\Phi_B - \overline{\Phi}_B)^2}{2\sigma^2}\right\}, \tag{6.10}$$

where $\overline{\Phi}_B$ is the mean value of SBH, σ is the standard deviation and $1/\sigma\sqrt{2\pi}$ is the normalization constant. The statistical analysis of the *I-V* BHs for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) reveals the mean SBH values of 0.541 ± 0.012 eV, 0.503 ± 0.006 eV and 0.549 ± 0.030 eV, respectively.

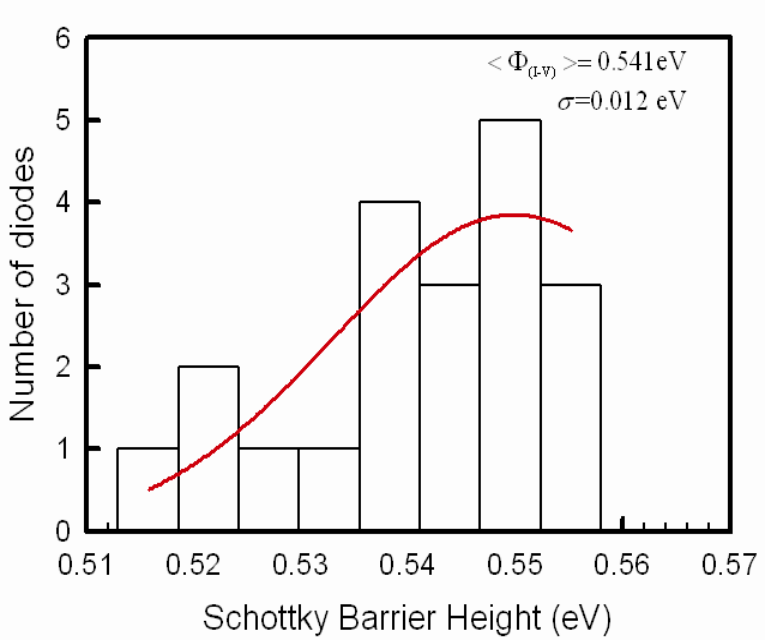


Fig. 6.7 *Distribution of barrier heights from the forward bias I-V characteristics of the Pd/n-Ge (100) Schottky barrier at room temperature.*

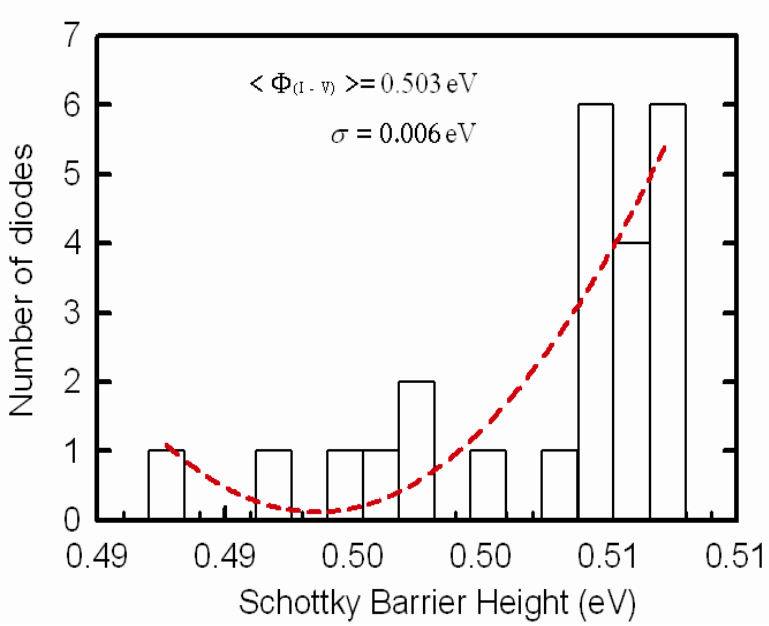


Fig. 6.8 *Distribution of barrier heights from the forward bias I-V characteristics of the Ni/n-Ge (100) Schottky barrier at room temperature.*

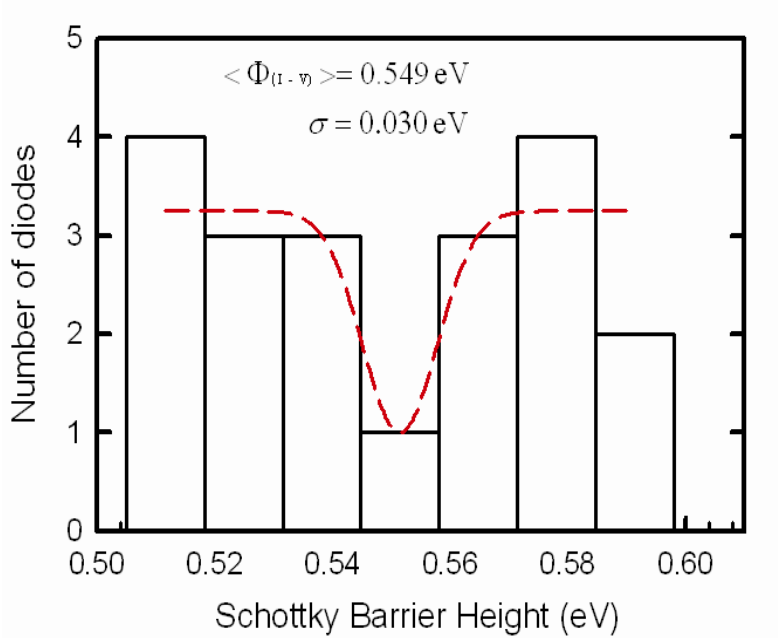


Fig. 6.9 *Distribution of barrier heights from the forward bias I-V characteristics of the Au/n-Ge (100) Schottky barrier at room temperature.*

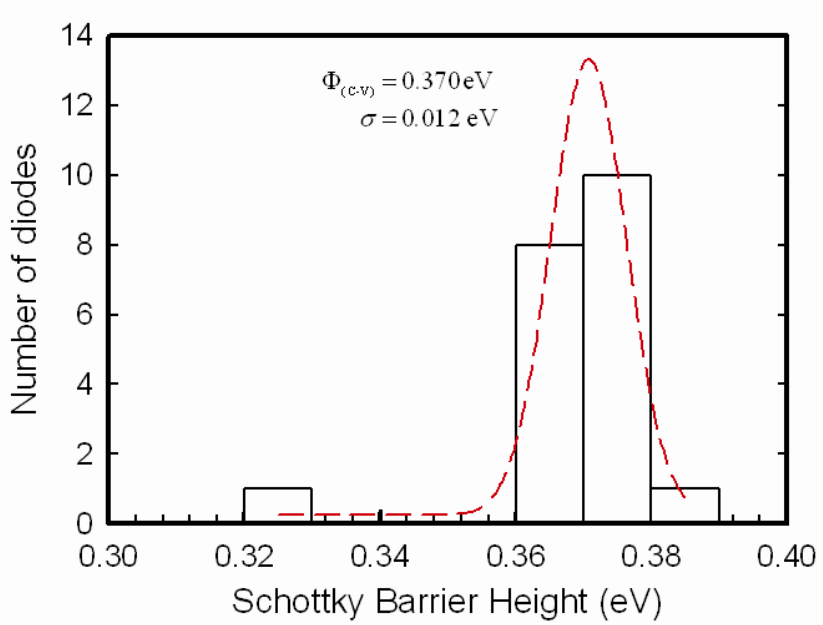


Fig. 6.10 *Distribution of barrier heights from the reverse bias* $C^{-2} - V$ *characteristics of the Pd/n-Ge (100) Schottky barrier recorded at 1 MHz and room temperature.*

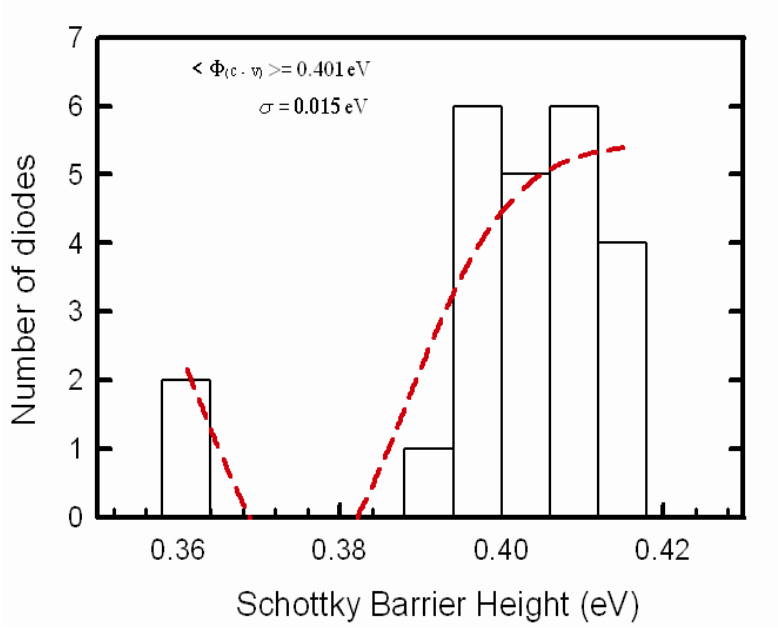


Fig. 6.11 *Distribution of barrier heights from the reverse bias $C^{-2} - V$ characteristics of the Ni/n-Ge (100) Schottky barrier recorded at 1 MHz and room temperature.*

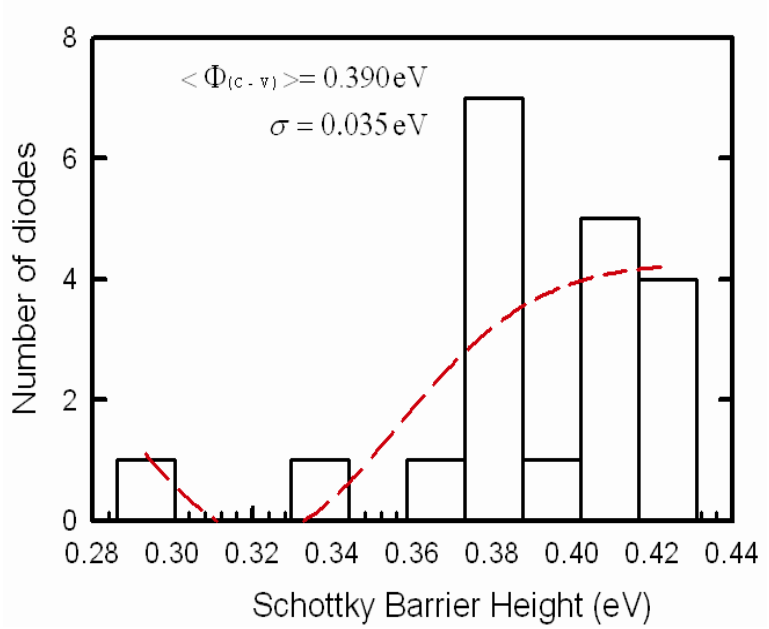


Fig. 6.12 *Distribution of barrier heights from the reverse bias $C^{-2} - V$ characteristics of the Au/n-Ge (100) Schottky barrier recorded at 1 MHz and room temperature.*

In the distribution of the BHs from the reverse bias $C^{-2} - V$ characteristics at 1 MHz (Figs. 6.10 - 6.12), the statistical analysis of BHs for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) yielded mean BH values of 0.370 ± 0.012 eV, 0.401 ± 0.015 eV and 0.390 ± 0.035 eV, respectively. Due to the different nature of the measurement techniques (*I-V* and *C-V*), BHs deduced from them are not always the same [18]. Although, in general BHs from *C-V* measurements are higher than BHs from *I-V* measurements, in this study we obtained *I-V* BHs which are higher than the BHs from *C-V* measurements. Therefore, further studies are needed to clarify these results.

Figs. 6.13 - 6.15 show the statistical distribution of ideality factors from the forward bias *I-V* characteristics for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100), respectively. Gaussian distribution was used to obtain a fit to the histograms. The statistical analysis of the ideality factors for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) yielded average values of 1.239 ± 0.146, 1.422 ± 0.064 and 1.535 ± 0.263, respectively.

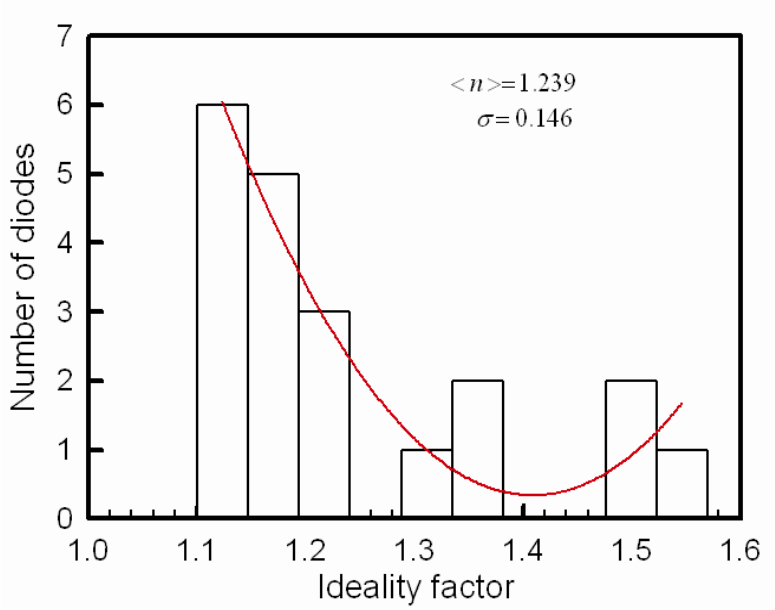


Fig. 6.13 *Distribution of ideality factors from the forward bias I-V characteristics of the Pd/n-Ge (100) Schottky barrier diodes at room temperature.*

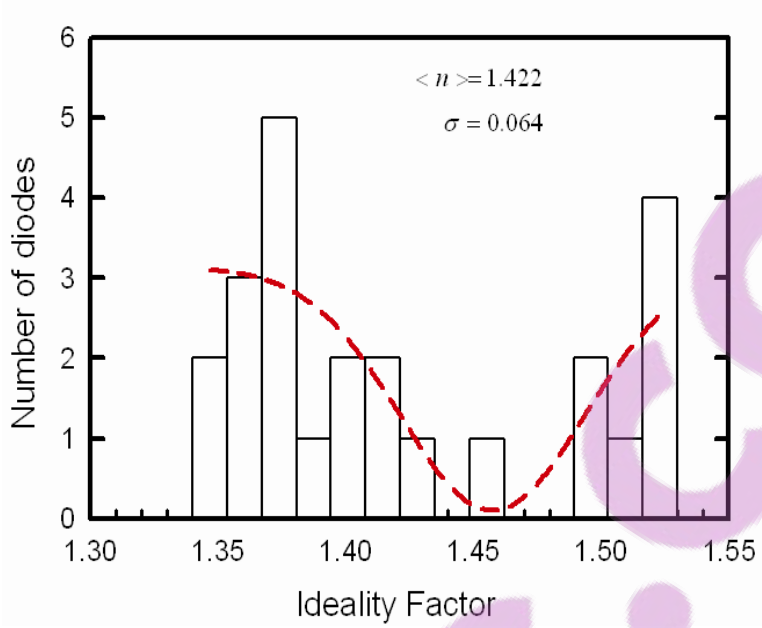


Fig. 6.14 *Distribution of ideality factors from the forward bias I-V characteristics of the Ni/n-Ge (100) Schottky barrier at room temperature.*

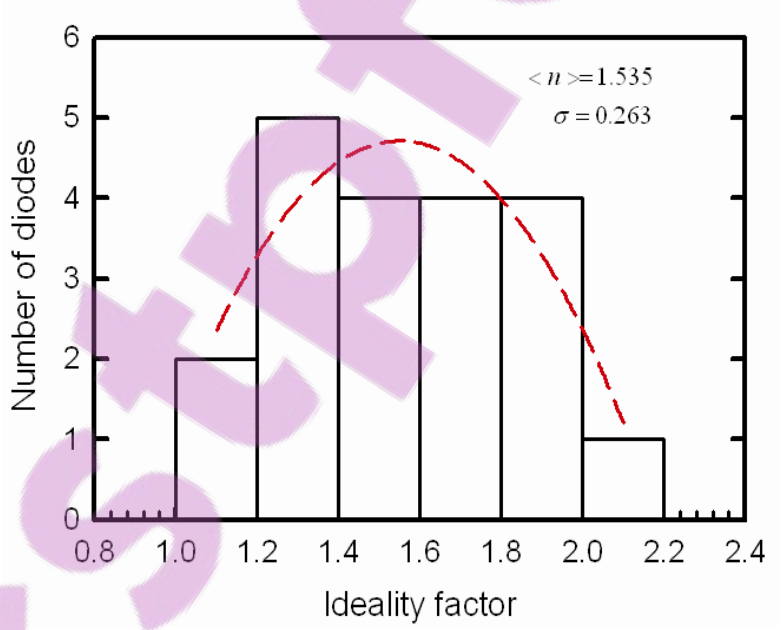


Fig. 6.15 *Distribution of ideality factors from the forward bias I-V characteristics of the Au/n-Ge (100) Schottky barrier at room temperature.*

The data clearly show that the diodes have ideality factors that are considerably larger than 1.01, the value determined by the image effect alone [1,2,11, 17,29,32]. The ideality factor determined by image-force effect should be close to 1.01 or 1.02 [21]. Therefore these diodes are patchy [21,14,15,25]. Schottky contacts, ideality factor greater than 1.0 indicate that the transport properties are not well modelled by thermionic emission alone although the contacts remain rectifying [33]. Explanations for the deviations of the ideality factor from unity ranged from assumptions of a generation-recombination current in the space-charge region [17,29,34], interface dielectric layers or field emission [17] or thermionic field emission [35] due to secondary mechanisms at the interface [5,15]. For example, interface defects may lead to a lateral inhomogeneous distribution of SBHs at the interface resulting in excess current leading to a deviation from ideal thermionic emission behaviour at low voltages and temperatures.

Figs. 6.16 - 6.18 show plots of the *I-V* effective barrier heights as a function of the respective ideality factors for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100), respectively. The straight lines are least-squares fit to the experimental data. The SBHs decreases as the ideality factors increase. That is, there is a linear relationship between experimental effective SBHs and ideality factors of Schottky contacts [26].

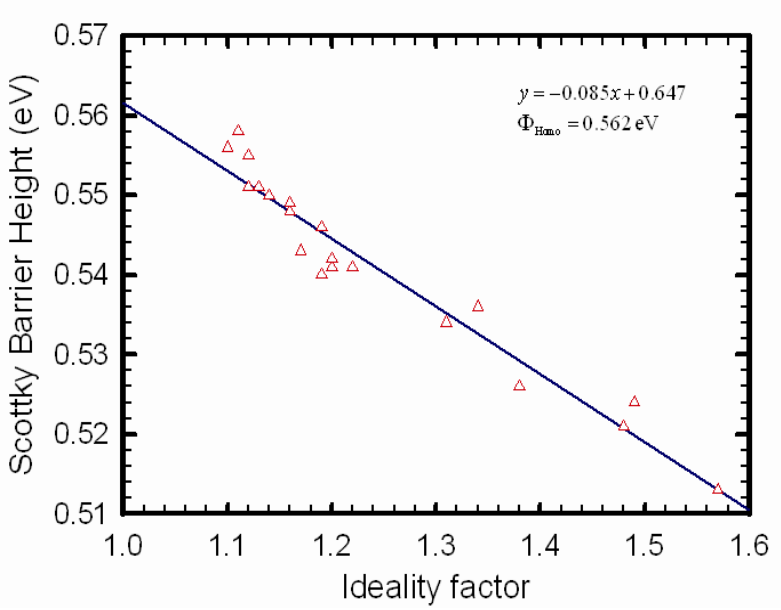


Fig. 6.16 *The experimental I-V Schottky barrier heights versus the ideality factors plot of the Pd/n-Ge (100) Schottky diodes for the barrier inhomogeneity model.*

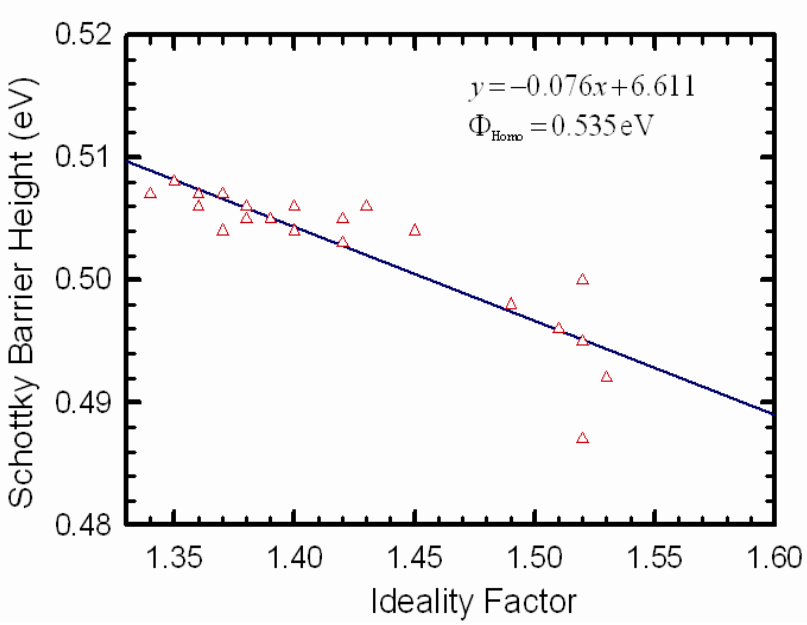


Fig. 6.17 *The experimental Schottky barrier heights versus the ideality factors plot of the Ni /n-Ge (100) Schottky diodes for the barrier inhomogeneity model*

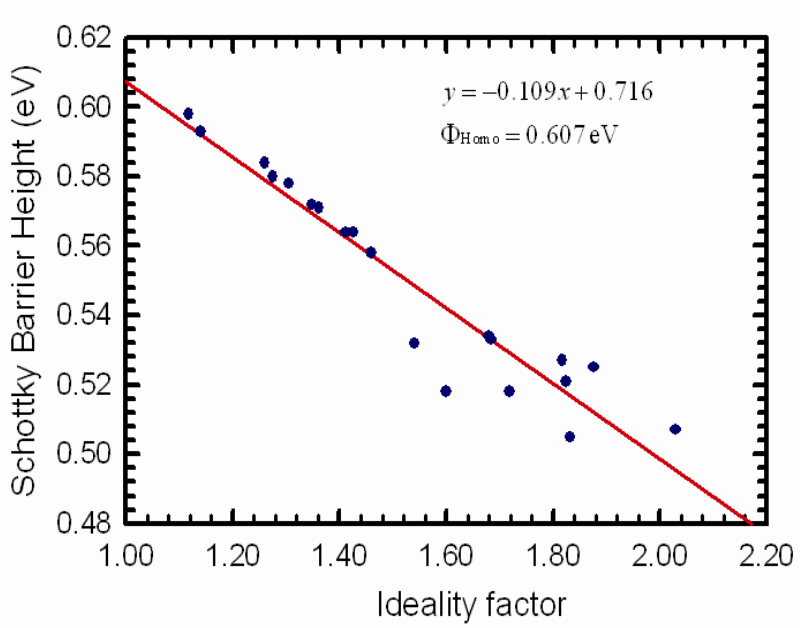


Fig. 6.18 *The experimental Schottky barrier heights versus the ideality factors plot of the Au /n-Ge (100) Schottky diodes for the barrier inhomogeneity model.*

Güler et al. [18] also mentioned that higher ideality factors among identically prepared diodes were often found to accompany lower observed SBHs. This may be attributed to lateral inhomogeneities of the effective SBHs in Schottky barrier diodes [1,12,13,15,36]. Such behaviours of SBH and ideality factors can be explained by means of bias dependence of saddle-point of an inhomogeneous SBH [1,12]. Mönch et al [21] have also proposed that interface defects induced during contacts fabrication could exist in addition to metal-induced gap states (MIGS) and alter the SBH. The defects give rise to additional discrete levels in the band gap and the Fermi level is pinned to one of these levels, possibly quite far away from the charge neutrality level [16]. Laterally homogeneous BH values of 0.562 eV, 0.535 eV and 0.607 eV for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) Schottky structures, respectively, were obtained from the extrapolation of the plots (Figs. 6.16 - 6.18) to n = 1.00. The homogeneous barrier heights, rather than effective SBHs, of individual contacts or mean values should be used to discuss theories on the physical mechanisms that determine the SBHs of MS contacts [25,27].

6.3 Summary and conclusions

Pd, Ni and Au Schottky diodes on n-Ge (100) were fabricated by resistive deposition under experimentally identical conditions. The BHs and ideality factors values were obtained from individual *I-V* characteristics of MS contacts. It has been shown that BHs and ideality factors varied from diode to diode even though they are were identically fabricated. Laterally homogeneous SBH values of 0.562 eV, 0.535 eV and 0.607 eV were obtained for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) Schottky structures, respectively, from the linear relationship between the *I-V* effective BHs and ideality factors, which can be explained by lateral inhomogeneities.

The statistical analysis of the *I-V* BHs for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) yielded mean SBH values of 0.541 ± 0.012 eV, 0.503 ± 0.006 eV and 0.549 ± 0.030 eV, respectively. Ideality factors for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) Schottky contacts yielded average values of 1.239 ± 0.146, 1.422 ± 0.064 and 1.535 ± 0.263, respectively. In the distribution of the BHs from the reverse bias $C^{-2} - V$ characteristics at 1 MHz, the statistical analysis of BHs for Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) yielded mean SBH values of 0.370 ± 0.012 eV, 0.401 ± 0.015 eV and 0.390 ± 0.035 eV, respectively.

Furthermore, it has been shown experimentally that the data on Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) contacts become an interesting experimental illustration of the theoretical predictions.

References

[1] R.T. Tung, Mater. Sci. Eng. R **35** (2001) 1.

[2] E.H. Rhoderick, R.H. Williams, Metal-Semiconductor Contacts, Claredon Press, Oxford, 1988.

[3] G.A. Baraff, M. Schlüter, Phys. Rev. B. **33** (1986) 7346.

[4] R.L. Van Meirhaeghe, W.H. laflere, F. Cardon, J. Appl. Phys. **76** (1994) 403

[5] S. Chand, S. Bala, Physica B **390** (2007) 179.

[6] J.M. Werner, H.H. Guttler, J. Appl. Phys. **69** (1991) 1522.

[7] J.M. Werner, H.H. Guttler, J. Appl. Phys. **69** (1991) 1522.

[8] S. Chand, J. Kumar, J. Appl. Phys. **82** (1997) 2005.

[9] H. Çetin, E. Ayyildiz, Semicond. Sci. Technol. **20** (2005) 625.

[10] R.T. Tung, Phys. Rev. B. **45** (1992) 13509.

[11] Y.P. Song, R.L. Van Meirhaeghe, W.H. Laflere, F. Cardon, Solid-State Electron **29** (1986) 633.

[12] J.P. Sullivan, R.T. Tung, M.R. Pinto, W.R. Graham, J. Appl. Phys. **70** (1991) 7403.

[13] T.U. Kampen, W. Mönch, Surf. Sci. **333** (1995) 490.

[14] W. Mönch, Phys. Rev. B **37** (1988) 7129.

[15] W. Mönch, J. Vac. Sci. Technol. B **17** (1999) 1867.

[16] M. Sa□lam, F.E. Cimili, A. Türüt, Physica B **348** (2004) 397.

[17] B. Boyarbay, H. Cetin, M. Kaya, E. Ayyildiz, Microelectron. Eng. **85** (2008) 721.

[18] G. Güler, Ş. Karataş, Ö. Güllül, Ö. F. Bakkaloğlu, J. All.Com. doi:10.1016/j.jallcom.2009.06163

[19] Ş. Altindal, H. Kanbur, A. Tataroğlu, M.M. Bülbül, Physica B **399** (2007) 146.

[20] A. Tataroğlu, Ş. Altindal, J. Alloys Compd. **479** (2009) 893.

[21] W. Mönch, Semiconductor Surf. And Interfaces, 2nd ed. Springer, Berlin 1995.

[22] T.U. Kampen, W. Mönch, Surf. Sci. **331-333** (1995) 490.

[23] K. Akkilic, M.E. Aydin, A. Turut, Physica Scripta. **70** (2004) 364.

[24] W.P. Leroy, K. Opsomer, S. Forment, R.L. Van Meirhaeghe, Solid-State Electron. **49** (2005) 878.

[25] R.F. Schmitsdorf, T.U. Kampen, W. Mönch, **15** (1997) 1221.

[26] S. Asubay, Ö. Güllü, A. Turut, Appl. Surf. Sci. **254** (2008) 3558.

[27] H. Çetin, B. Şahin, E. Ayyildiz, A. Türüt, Semicon. Sci. Technol. **19** (2004) 1113.

[28] Germanium Silicon: Physics and Materials, Semiconductors and Semi-metals Vol. 56, edited by R. Hull and J.C. Bean (Academic, San Diego, 1999)

[29] S.M. Sze, Physics of Semiconductor Devices, 2nd ed. Wiley, New York, 1981.

[30] V. Saxena, R. Prakash, Polym. Bull. **45** (2000) 267.

[31] H.H. Güttler, J.H. Werner, Appl. Lett. **56** (1990) 1113.

[32] J.H. Werner, H.H. Güttler, J. Appl. Phys. **69** (1991) 1522.

[33] H. Doğan, N. Yildirim, A. Türüt, Microelectron. Eng. **85** (2008) 655.

[34] E. Hökelek, G.Y. Robinson, Solid-State Electron. **99** (1981) 24

[35] E. Ayyildiz, H. Çetin, Zs. Horváth, J. Appl. Surf. Sci. **252** (2005) 1153.

[36] G. Güler, Ö. Güllü, Ö.F. Bakkaloglu, A. Türüt, Semicon. Sci. Technol. **19** (2008) 1113.

List of publications

1. **A. Chawanda**, J.M. Nel, F.D. Auret, W. Mtangi, C. Nyamhere, M. Diale and L. Leach, Journal of the Korean Physical Society 57 **61** (2010) 1970.

CHAPTER 7: RESULTS

Studies of defects induced in Sb doped Ge during contacts fabrication and annealing process.

7.1 Introduction

The high carrier mobility at low electric field [1], and the low effective mass of holes in Ge has opened up possibility of using Ge in ultrafast complimentary metal-oxide-semiconductor (CMOS) devices [2]. This has led to renewed interest in the complete understanding of dynamic properties of radiation and process-induced defects in Ge because defects ultimately determine the performance of devices. Depending on the application, these defects may either be beneficial or detrimental to optimum device functioning [3]. For example, for Si it has been shown that the defects introduced during high-energy electron and proton irradiation increases the switching speed of devices [4]. A lot of research work has been performed on the electrical properties of defects introduced during high-energy, electron and proton irradiation of Ge [5,6,7,8,9,10]. The defects introduced during electron beam deposition of Pt Schottky contacts on n-Ge and the electronic properties of defects introduced during the implantation of Ge with heavier ions, such as dopants have also been reported [3,11]. Metallization is a critical processing step in semiconductor industry. Electron beam deposition (EBD), Sputter deposition and Resistive evaporation are commonly used metallization methods. EBD and Sputter deposition methods introduce defects in semiconductors. Defects introduced in Ge during metallization processes have been investigated [12,13,14,15,16,17]. In this study we investigate on the defects introduced in Ge during contacts fabrication and annealing process, since a practical concern is whether the germanidation process introduces defects, because this may affect the leakage current of the source-drain junctions.

7.2 Experimental procedures

We have used bulk grown n-type Ge with (100) crystal orientation, doped with antimony, (Sb) to a density of 2.5 × 10^{15} cm^{-3} supplied by Umicore. Before metallization the samples were first degreased and then etched in a mixture of H_2O_2(30%):H_2O (1:5) for 1 minute. Immediately after cleaning they were inserted into a vacuum chamber where AuSb (0.6% Sb), 100 nm thick was deposited by resistive evaporation as back ohmic contacts. The samples were then annealed at 350°C in Ar ambient for ten minutes to minimize the ohmic contact resistivity [3]. Before Schottky contacts deposition, the samples were again chemically cleaned as described above. Cobalt (Co) and ruthenium (Ru) Schottky contacts were deposited onto the Ge in an electron beam deposition system, while palladium (Pd) and some Co Schottky contacts were deposited by vacuum resistive evaporation. These contacts were deposited under vacuum at a pressure below 10^{-6} Torr. The contacts were 0.6 mm in diameter and 30 nm thick. Following contact fabrication, current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements were performed to assess the quality of the diodes and to determine the free carrier density of the Ge, respectively. Thereafter, electrical characterization was repeated after every isochronal annealing cycle in Ar ambient for 30 minutes between room temperature and 600°C. Both conventional deep-level transient spectroscopy (DLTS) [18] and Laplace-DLTS (LDLTS) [19,20] were used to study the defects introduced in the Ge during the contact fabrication and annealing process. The '*signatures*' of metallization induced defects (i.e. energy position in band gap relative to the conduction band and valence band for the electron and hole traps, respectively, E_T, and their apparent capture cross section, σ_a) were determined from the Arrhenius plots of ln(T^2/e) *versus* 1000/T, where '*e*' is either the hole or electron emission rate, and T is the measurement temperature in K.

7.3 Results and discussions

In this section the electronic and annealing properties of defects introduced in n-type Ge during electron beam deposition and annealing process are presented. In the nomenclature used here "*E*" means electron trap and the number following it is the energy level of this trap below the conduction band. Similarly, "*H*" means hole trap and number following it is the energy level of this trap above the valence band.

7.3.1 Pd/n-Ge (100) Schottky diodes

Fig. 7.1 shows a conventional DLTS spectrum obtained from Pd Schottky contacts annealed from room temperature to 350°C. Fig. 7.1 (a) depicts that no defects are observable (within the detection limit of our DLTS system which is approximately $>10^{11}cm^{-3}$) for resistively evaporated Pd Schottky contacts, indicating that the Ge is of high quality [12]. A hole trap *H*(0.33) with capture cross-section of 1.0×10^{-14} cm^{-2} was observed after annealing at 300°C. Although Churms et al. [21] reported Pd-Ge inter-diffusion at 300°C anneal during a study of Pd/Ge interaction by microbeam Rutherford backscattering spectrometry, we propose to assign this hole trap to vacancy (V)- related defect complex, since it annealed out after a 350°C anneal. Also, it has been suggested by [1] that the germanide formation causes the injection of vacancies into the semiconductor bulk and, hence the occurrence of V-related defects. The annealing studies were carried out up to 525°C to determine if there are any other defects induced in Ge during the annealing process.

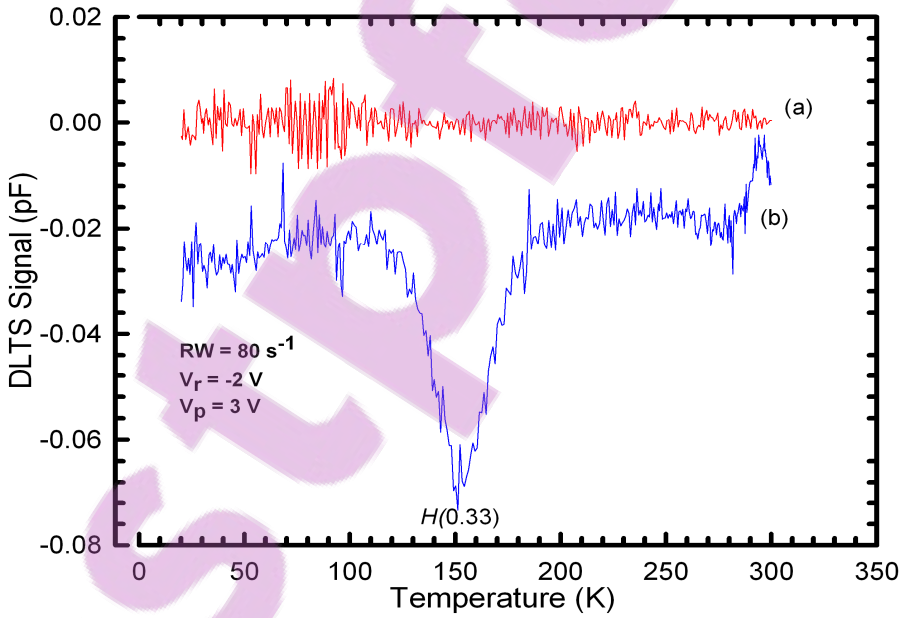


Fig. 7.1 *DLTS spectra of the Pd Schottky contacts on n-Ge (100) (a) as-deposited and (b) after annealing at 300°C. These spectra were recorded at a rate window of* $80s^{-1}$ *and quiescent reverse bias of –2 V with a filling pulse of 3 V.*

7.3.2 Co/n-Ge (100) Schottky diodes

An electron trap at *E*(0.37) and a hole trap at *H*(0.29) with capture cross sections of 4.0×10^{-14} cm^{-2} and 3.0×10^{-14} cm^{-2}, respectively were observed in as-deposited Co Schottky contacts fabricated with electron beam deposition (EBD), as shown in Fig. 7.2. The defects electronic properties were extracted from the Arrhenius plot shown in Fig. 7.3. The electron trap *E*(0.37) is the well known (=/–) charge state of the *E*-centre (V-Sb) in Sb-doped Ge [15], whilst the hole trap *H*(0.29) corresponds closely to that reported for the H(0.307), the (–/0), the single acceptor level of Sb-V centre in Ge [5,6], created during electron irradition. In the case of electron beam deposition, the *E*-centre forms when energetic particles (originating in the region of the filament) impinge on the Ge, creating vacancies and interstitials at and close to Ge surface [12,22]. These vacancies are mobile at room temperature and migrate into Ge where they combine with Sb-dopant atoms to form Sb-V pairs (*E*-centre) [12,23]. The hole trap *H*(0.29) is thermally stable up to an annealing temperature of 150°C and anneals out at 200°C [24].

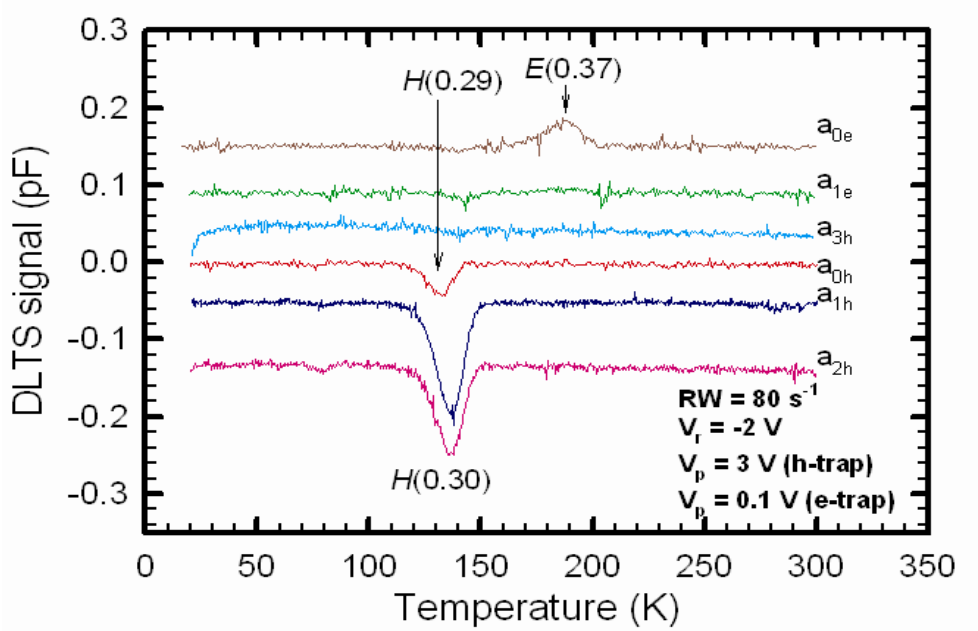


Fig. 7.2 *DLTS spectra of the EBD deposited Co Schottky contacts on n-Ge (100) (a_0) as-deposited and after annealing at (a_1) 200°C, (a_2) 300°C and (a_3) 350°C. The subscripts 'e' and 'h' on the graph labels stand for electron and hole traps, respectively. These spectra were recorded at a rate window of 80 s^{-1} and quiescent reverse bias of –2 V with filling of 0.1 V and 3 V for electron and hole traps, respectively*

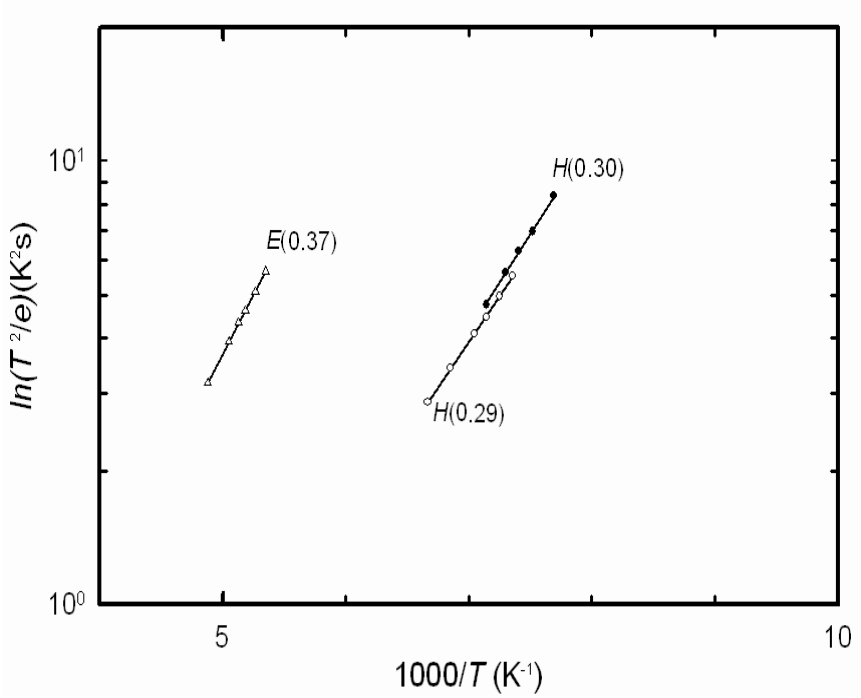


Fig. 7.3 *Arrhenius plot of an electron and hole traps introduced in n-Ge (100) after Co Schottky contact fabrication using EBD and during annealing process.*

Further annealing studies in the temperature range from 200 to 350°C, reveal a hole trap *H*(0.30), shown in Fig. 7.2 with capture cross section of 7.8×10^{-14} cm^{-2} which anneals-out between 300 and 350°C.

The signature of the *H*(0.30) defect corresponds to that reported during DLTS studies of cobalt Schottky contacts sputter deposited onto the n-type Ge, after subjecting the contacts to rapid thermal annealing for 30 s at 750°C. This defect is assigned to substitutional Co (Co_s) double acceptor level ($Co_s^{-/2-}$) with activation energy 0.3 eV [25]. Although Opsomer et al. [25] reported Co-Ge in-diffusion of Co sputter deposited on n-type Ge after rapid thermal annealing of the contacts at temperatures higher than 600°C for 30 s, in this study Co-Ge inter-diffusion is revealed after isochronal annealing at a temperature of 350°C for 30 minutes, as shown in RBS studies (see Fig 7.4). This is also in agreement with what was reported by Sun et al [26]. Co atoms will diffuse into bulk Ge at a relatively low temperature of ~ 150°C.

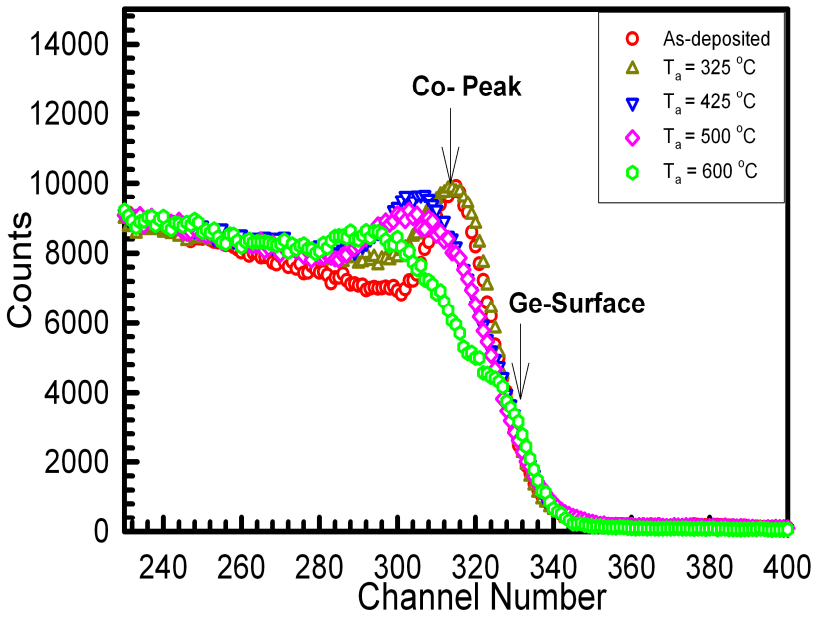


Fig. 7.4 *RBS spectra of 1.6 MeV He^+ ions for cobalt films deposited on germanium after isochronal thermal treatment for 30 min at different annealing temperatures: as-deposited, 325, 425, 500, and 600°C.*

Increasing the anneal temperature to 350°C, the hole trap *H*(0.30) completely vanished (Fig. 7.2). The annealing studies were carried out up to 525°C to determine if there are any other defects induced in Ge during the annealing process. After 525°C anneal, the Co Schottky contacts severely deteriorated, and contacts became near ohmic.

7.3.3 Ru/n-Ge (100) Schottky diodes

7.3.3.1 Electron traps

DLTS spectra for electron traps induced in Ge after electron beam deposition of Ru/n-Ge (100) Schottky contacts are depicted in Fig. 7.5. The spectra were recorded for as-deposited, 100, 150, 175, 200, 225, 250, 300 and 350°C. After Ru Schottky contacts fabrication, *E*(0.38) level with capture cross section of 1.0×10^{-14} cm^{-2} is the only detectable electron trap. The defect's electronic properties were extracted from the Arrhenius plot shown in Fig. 7.6. This can be attributed to the significant injection of minority carriers into the band gap even without applying a minority carrier filling pulse because of very high barrier height of Ru SBD[27].

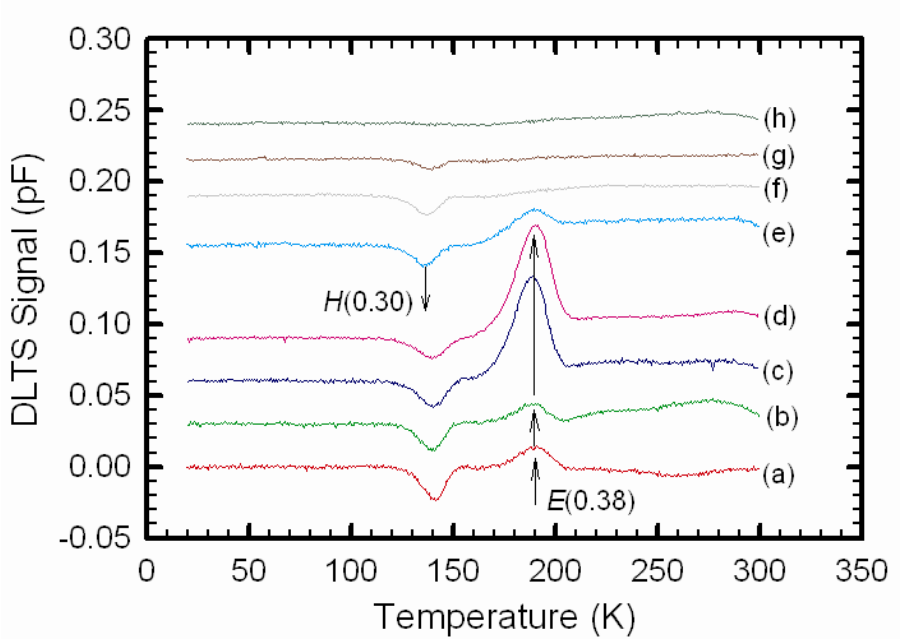


Fig. 7.5 *DLTS spectra for electron traps after electron beam deposition of Ru Schottky contacts on n-Ge (100) (a) for as-deposited, and after annealing at (b) 100°C, (c) 150°C, (d) 175°C, (e) 200°C, (f) 225°C, (g) 250°C, (h) 300°C and (i) 350°C. These spectra were recorded with a quiescent reverse bias of –2 V, at a rate window of 80 s^{-1}, a pulse voltage of –0.15 V and pulse width of 1 ms.*

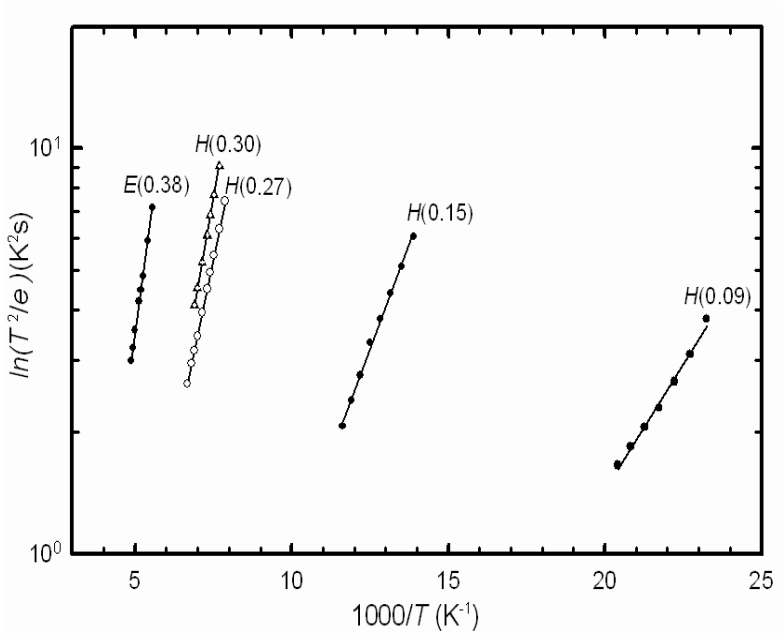


Fig. 7.6 *Arrhenius plot of an electron and hole traps (Fig. 7.5 & Fig. 7.10) introduced in n-Ge (100) after Ru Schottky contacts fabrication using EBD.*

7.3.3.2 Annealing mechanism of the E-centre (E (0.38))

The *E*-centre (*E*(0.38)) is a very important defect in Ge for its role in dopant deactivation and free carrier removal as for each V-Sb complex formation results in the removal of three free carriers [6]. It is therefore important to establish the annealing mechanism of the *E*-centre. The concentration as function of depth profile of the E-centre, measured at different isochronal annealing temperatures is shown in Fig. 7.7. It can be seen that the depth profile for as-deposited samples shows that the defect concentration decreased from the Ge surface, and this proves that the energetic particles emerging from the filament during contact fabrication creates vacancies on and beneath the semiconductor surface [28]. The defect concentration profile (Fig 7.7) shows an increase in defect concentration deeper into the bulk material as the annealing temperature is increased. This is attributed to the diffusion of the *E*- centre into the semiconductor as it become mobile at elevated temperatures. A 175°C anneal, with prolonged annealing time results in a broadened profile which shifted to lower concentration. Therefore, further investigations need to be carried out to establish defect concentration profile annealing mechanisms for prolonged time model.

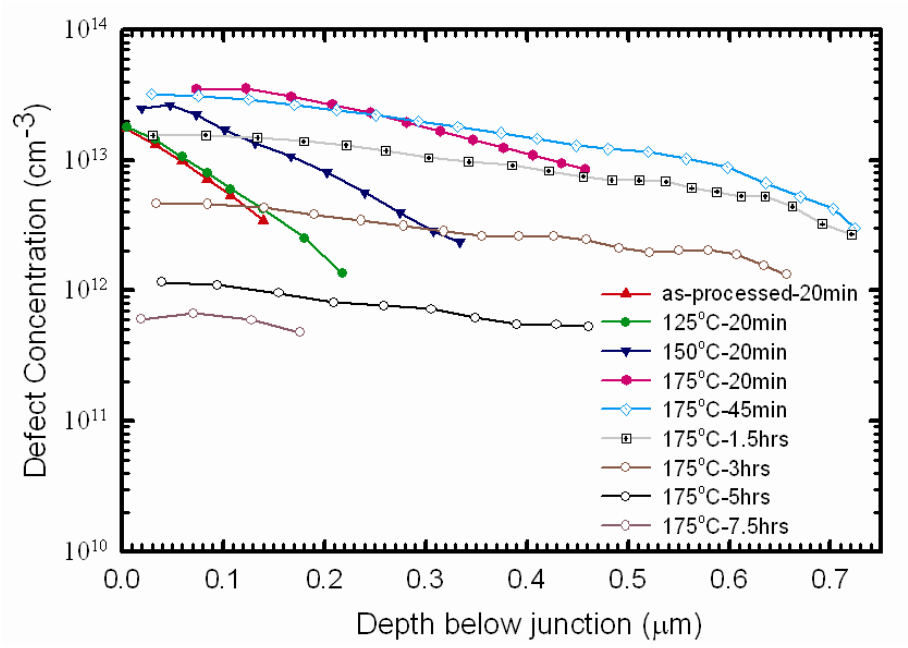


Fig. 7.7 *Depth profile for E(0.38) at different annealing temperatures. The measurements were performed by LDLTS at fixed temperature of 195 K.*

To further understand the annealing mechanism of the *E*-centre it was important to investigate the annealing kinetics of the defect and determine the activation energy for the annealing process. Fig. 7.8 (a) shows the results for the annealing kinetics at temperatures 160°C, 170°C and 175°C, from which the annealing rate (*K*) for each temperature was extracted and used for the construction of the Arrhenius plots shown in Fig 7.8 (b).

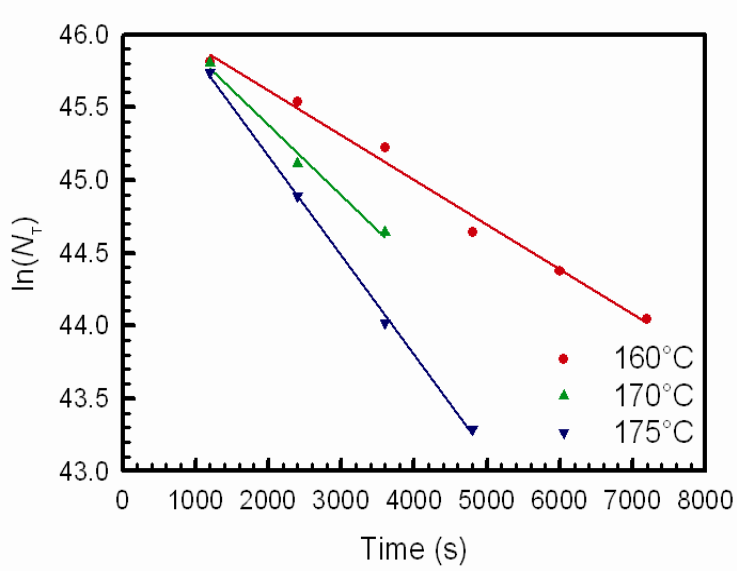


Fig. 7.8 (a) *Semi-log plot of defect concentration profiles against annealing time measured at annealing temperatures of 160°C, 170°C and 175°C from which the annealing rate constant, K is calculated.*

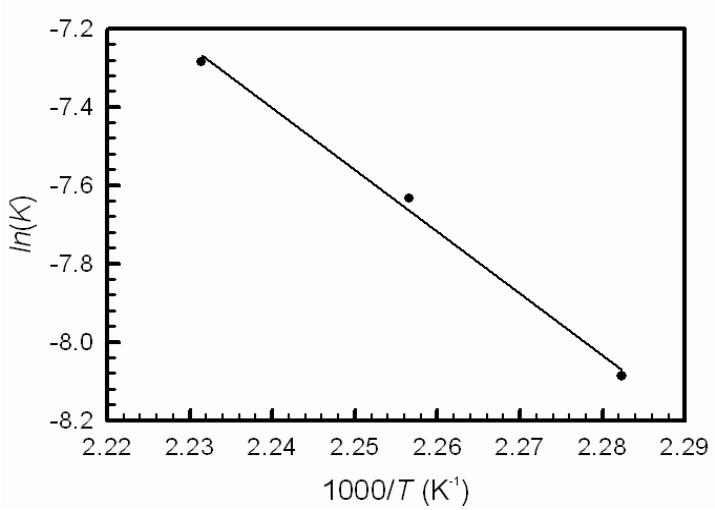


Fig. 7.8 (b) *The Arrhenius plot of ln (K) versus 1000/T*

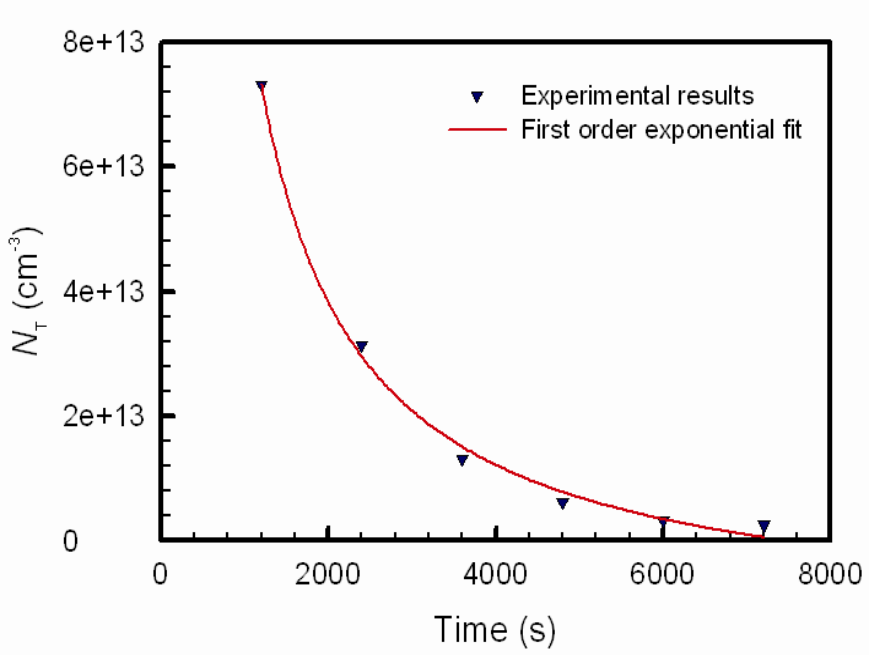


Fig. 7.8 (c) *The plot of defect concentration against annealing time at annealing temperature of 175°C*

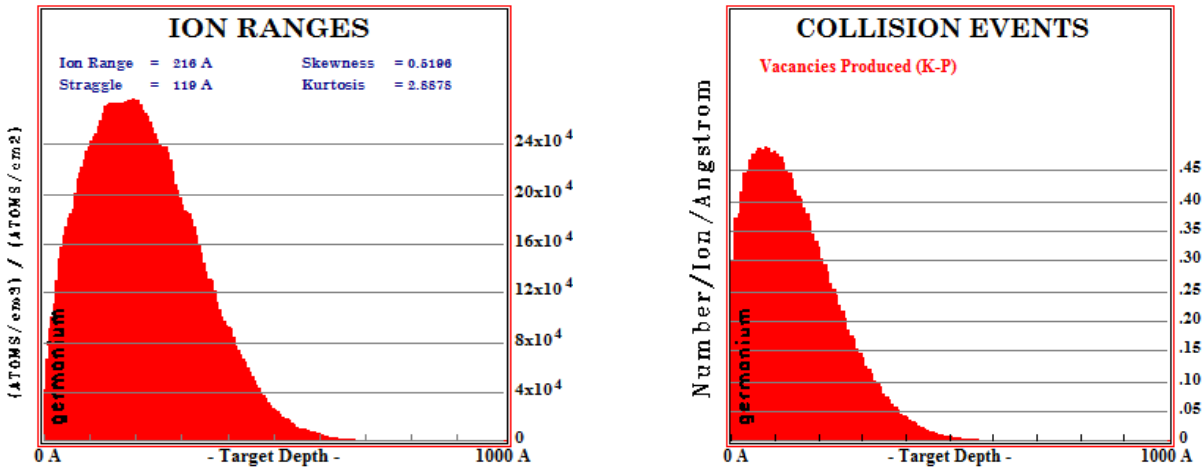
The annealing of the *E*-centre follows a first order exponential decay as depicted in Fig 7.8 (c) with activation energy E_a = 1.36 eV and pre-exponential factor $A = (1.2 \pm 0.3) \times 10^{12} s^{-1}$ extracted from the slope and vertical axis intercept of the Arrhenius plot (Fig. 7.8 (b), respectively. The value of the pre-exponential factor *A*, is just below the lower end of the purely dissociation range of $> 10^{12}$ s^{-1} [29].

7.3.3.3 Causes of EBD damage

The following energetic gaseous ions were reported by [30] to be in the chamber during the EBD process: H, H_2, C, N, O, OH, H_2O, CO, N_2, CO_2 and C_xH_y. H and H_2 are the positive ions, and negative ions are: O, OH, C and C_xH_y. Due to these energetic gaseous ions, which also reach the substrate during the EBD, vacancies are created on and beneath the semiconductor surface.

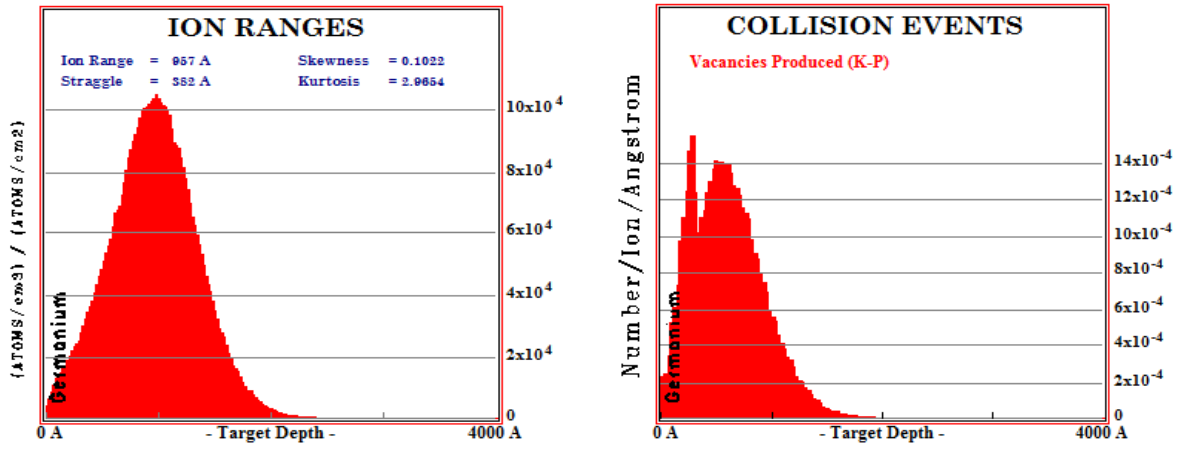
Fig. 7.9 (a & b) shows the TRIM (Transport of Ion in Matter) (version 2006.02) [31] simulation profiles for regions where vacancies are created in germanium by some residual vacuum gas ions (assuming a maximum energy of 10 keV for ions in the deposition chamber). The projected ion

range is ≈25 nm for carbon, nitrogen and oxygen ions from energy of 10 keV, each ion producing approximately 4 vacancies/nm. Hydrogen ions will create primary damage of up to a depth of ≈ 100 nm. The vacancies and interstitials created will diffuse and form stable defect complexes (e.g. *E*-centre) even deeper than the projected ion range.



(i) (ii)

Fig. 7.9 (a) *(i) TRIM simulation for the projected ion range and (ii) damage events of 10 keV oxygen ions in Ge.*



(i) (ii)

Fig. 7.9 (b) *(i) TRIM simulation for the projected ion range and (ii) damage events of 10 keV hydrogen ions in Ge*

7.3.3.1 Hole traps

Fig. 7.10 and Fig. 7.11 show conventional DLTS and Laplace DLTS spectra, respectively for hole traps introduced in Ge during Ru Schottky contacts EBD deposition. Hole trap *H*(0.30) with capture cross section 6.2×10^{-13} cm^{-2} is the prominent single acceptor level of the *E*-centre. The hole traps *H*(0.09), *H*(0.15) and *H*(0.27) with capture cross sections 7.8×10^{-13} cm^{-2}, 7.1×10^{-13} cm^{-2} and 2.4×10^{-13} cm^{-2}, respectively were also observed in as-deposited Ru Schottky contacts. The electronic properties of these defects were obtained from the Arrhenius plots shown in Fig. 7.6. Auret et al. [23] also reported the trap *H*(0.09) after metallization by EBD process. It has been proposed that this defect is the third charge state of the *E*-centre (+/0) [9].

Although the hole trap *H*(0.27) has been reported to be induced after a 200°C anneal of MeV electron irradiated Ge sample [27], in this study the defect was induced during the Ru Schottky contacts fabrication process. This may be due the fact that during EBD the substrate temperature is higher than the room temperature and thus thermally inducing the defect *H*(0.27). The measurement of the hole trap *H*(0.27) in the presence of *H*(0.30) was achieved by LDLTS which clearly separates the signals

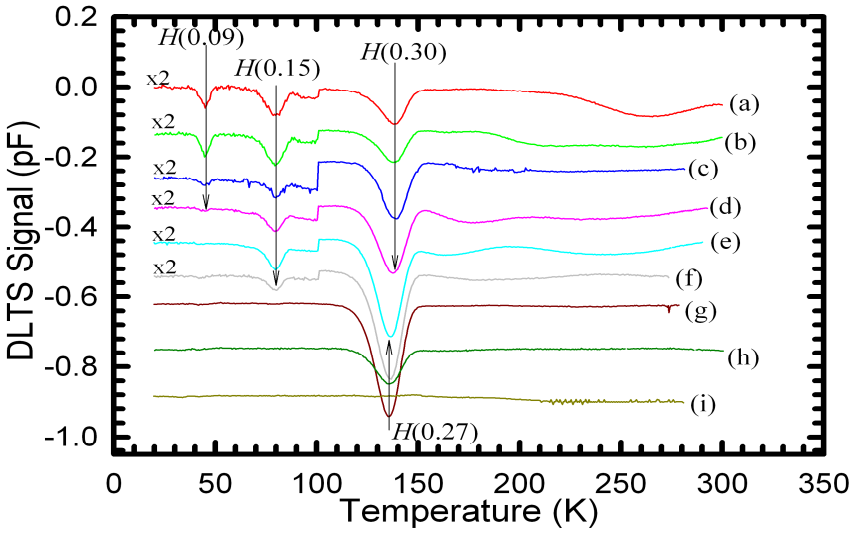


Fig. 7.10 *DLTS spectra for the hole traps induced in n-Ge (100) after electron beam deposition of Ru Schottky contacts. The spectra were recorded (a) for as-deposited, and after annealing at (b) 100°C, (c) 150°C, (d) 175°C, (e) 200°C, (f) 225°C, (g) 250°C, (h) 300°C and (i) 350°C. The spectra were recorded with a quiescent reverse bias of –1 V, at a rate window of 80 s^{-1}, a pulse voltage of 3 V and pulse width of 1 ms.*

Fig 7.11 shows that the peak concentration (peak height) for *H*(0.30) trap is much higher than that of *H*(0.27), hence much larger concentration of *H*(0.30) in the as-deposited samples. The variation of the defect concentration for the hole traps *H*(0.30) and *H*(0.27), and the electron trap *E*(0.38) as a function of annealing temperature is shown is in Fig. 7.12. The concentration of *H*(0.27) increased with annealing temperature until it reached a maximum after a 225°C anneal, at which point the *E*-centre completely vanishes. This confirms what was reported by Coutinho et al. [32] and Markevich et al. [33] that *H*(0.27) is a product of V-Sb after annealing to form a new V-Sb_2 complex which is electrically active [32,33]. After 350°C annealing temperature, all defects had completely annealed out and the annealing was carried out up to 600°C to determine whether there are any other defect levels that might be reactivated after presumably being transformed into inactive complexes during annealing. There were no other defects observed above 350°C annealing temperature.

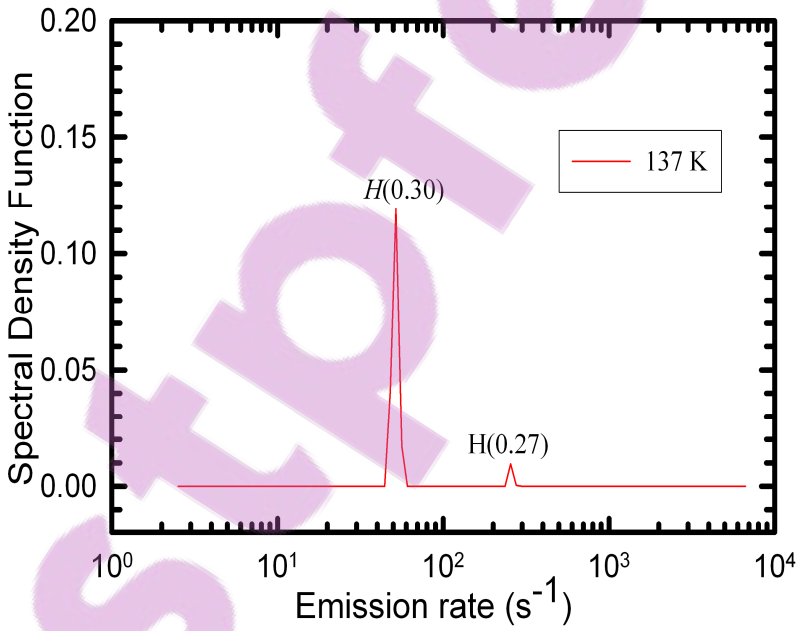


Fig. 7.11 *LDLTS spectra for H(0.27) and H(0.30) in as-deposited sample recorded at 137 K.*

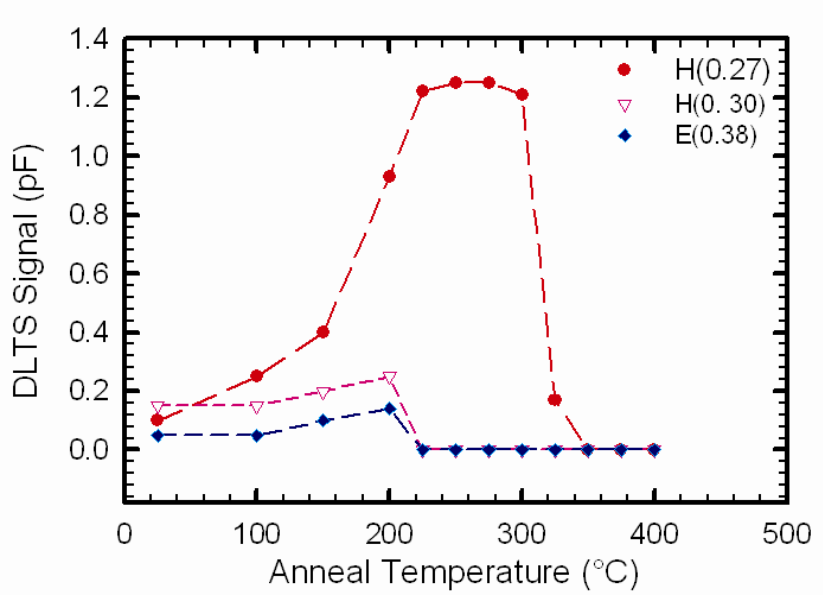


Fig. 7.12 *Variation of defect concentration for H(0.27), H(0.30) and E(0.38) with annealing temperature*

7.4 Summary and conclusions

DLTS and annealing studies of the Pd/n-Ge (100) Schottky contacts reveal the introduction of a hole trap *H*(0.33) at a temperature of 300°C. This hole trap is probably vacancy (*V*)-related defect complex. DLTS analysis on the EBD Co Schottky contacts has shown that an electron trap *E*(0.37) and a hole trap *H*(0.29) were induce in n-Ge during the fabrication of the contacts and a hole trap *H*(0.30) is induced during the annealing process. This defect is assigned to substitutional Co (Co_s) double acceptor level ($Co_s^{-/2-}$) with activation energy 0.3 eV [25].

DLTS and LDLTS revealed that the dominant defect induced by electron beam deposition is the V-Sb (*E*-centre). This depicts that during electron beam deposition vacancies are created below the semiconductor surface by particles which are ionized around the filament and then accelerated by the electric and magnetic fields towards the substrate. A hole trap *H*(0.27), induced during EBD of Ru Schottky contacts shows some reverse annealing between room temperature and 350°C (where it anneals out), reaching a maximum concentration at 225°C. This trap is reported to be due to V-Sb_2 complex. All defects induced in Ru Schottky contacts annealed out after a 350°C anneal.

References

[1] E. Simoen, K. Opsomer, C. Claeys, K. Maex, C. Detavernier, R.L. Van Meirhaeghe, and P. Clauws, J. Electrochem. Soc. **154** (2007) H857.

[2] Germanium silicon: physics and materials. In: Hull R, Bean JC, editors. Semiconductors and semimetals, vol. 56. San Diego: Academic Press; 1999.

[3] F.D. Auret, P.J. Janse van Rensburg, M. Hayes, J.M. Nel, S. Coelho, W.E. Meyer, S. Decoster, V. Matias, A. Vantomme, D. Smeets, Nucl. Instrum. Methds B **257** (2007) 169.

[4] S.J. Pearson, A.J. Tavendale, J. Appl. Phys. **54** (1983) 820.

[5] J. Fage-Pedersen, A. Nylandsted Larsen, A. Mesli, Phys. Rev. B **62** (2000) 10116.

[6] V.P. Markevich, A.R. Peaker, V.V. Litvinov, V.V. Emstev, L.I. Murin, J. Appl. Phys. **95** (2004) 4078.

[7] V.P. Markevich, I.D. Hawkins, A.R. Peaker, K.V. Emstev, V.V. Emstev, V.V. Litvinov, L. Dobaczewski, Phys. Rev. B **70** (2004) 235213-1.

[8] V.P. Markevich, I.D. Hawkins, A.R. Peaker, V.V. Litvinov, L. Dobaczewski, J.L. Lindström, Appl. Phys. Lett. **81** (2002) 1821.

[9] C.E. Lindberg, J. Lundsgaard Hansen, P. Bomholt, A. Mesli, K. Bonde Nielsen, and A. Nylandsted Larsen, Appl. Phys. Lett. **87** (2005) 172103.

[10] F.D. Auret. P.J. Janse van Rensburg, M. Hayes, J.M. Nel, W.E. Meyer, S. Decoster, V. Matias, and A. Vantomme, Appl. Phys. Lett. **89** (2006) 152123.

[11] P. Blood, J.W. Orton, The Electrical Characterization of Semiconductors: Majority Carriers and Electron States, Academic Press, London, 1992.

[12] F.D. Auret, S.M.M. Coelho, P.J. Janse van Rensburg, C. Nyamhere, W.E. Meyer, Mater.

Sci. Semicond. Process. **11** (2008) 348.

[13] F.D. Auret, W.E. Meyer, S.M.M. Coelho, M. Hayes, Appl. Phys. Lett. **88** (2006) 24110.

[14] F.D. Auret, W.E. Meyer, S.M.M. Coelho, M. Hayes, J.M. Nel, Mater. Sci. Semicond. Process, **9** (2006) 576.

[15] F.D. Auret, S.M.M. Coelho, M. Hayes, W.E. Meyer, J.M. Nel, Phys Status Solidi (a), **205** (2008) 159.

[16] F.D. Auret, S. Coelho, W.E. Meyer, C. Nyamhere, M. Hayes, J.M. Nel, J. Electron. Mater. **36** (2007) 1604.

[17] E. Simoen, K. Opsomer, C. Claeys, K. Maex, C. Detavernier, R.L. Meirhaegh et al. Appl. Phys. Lett. **89** (2006) 202114.

[18] D.V. Lang, J. Appl. Phys. **45** (1974) 3023.

[19] L. Dobaczewski, P. Kaczor, I.D. Hawkins, A.R. Peaker, J. Appl. Phys **76** (1994) 194.

[20] L. Dobaczewski, A.R. Peaker, N.K. Bonde, J. Appl. Phys **96** (2004) 4689.

[21] C.L. Churms, C.M. Comrie, R.S. Memutudi, Nucl. Instrum. Methds. B **158** (1999) 713.

[22] C. Christensen, J.W. Petersen, A. L. Nylandsted, Appl. Phy. Lett. **61** (1992) 1426.

[23] F.D. Auret, W.E. Meyer, S. Coelho, and M. Hayes, Appl. Phys. Lett. **88** (2006) 242110.

[24] C. Nyamhere, A. Chawanda, A.G.M. Das, F.D. Auret, M. Hayes, Physica B **401-402** (2007) 227.

[25] K. Opsomer, E. Simoen, C. Claeys, K. Maex, C. Detavernier, R.L. Van Meirhaeghe, S. Forment, P. Clauws, Mater. Sci. Semicond. Process. **9** (2006) 554.

[26] H.P. Sun, Y.B. Chen, X.Q. Pan, D.Z. Chi, R. Nath, Y.L. Foo, Appl. Phys. Lett. **86** (2005) 071904.

[27] C. Nyamhere, PhD Thesis, University of Pretoria, 2009.

[28] C. Nyamhere, A. Chawanda, A.G.M. Das, F.D. Auret, M. Hayes, Physica B **401-402**

(2007) 226.

[29] F.D. Auret and P.N.K. Deenapanray, Crit. Rev in Solid State and Mater. Sci. **29** (2004) 1.

[30] E.M. Sithole, MSc Thesis, University of Pretoria, 2001.

[31] J.P. Biersack and L.G. Haggmark, Nucl. Instrum. Methods. **174** (1980) 257

[32] J. Coutinho, V.J.B. Torres, S. Öberg, A. Carvalho, C. Janke, R. Jones et al. Mater. Sci. Mater. Electron. **18** (2007) 769.

[33] V.P. Markevich, S. Bernardini, I.D. Hawkins, A.R. Peaker, V.I. Kolkovsky, A. Nylandsted Larsen and L. Dobaczewski, Mater. Sci. Semicond. Process. **11** (2008) 354.

List of publications

1. A. Chawanda, C. Nyamhere, F.D. Auret, W. Mtangi, T. Hlatshwayo, M. Diale, J.M. Nel, Physica B **404** (2009) 4482.

CHAPTER 8: RESULTS

Current-Voltage Temperature characteristics of n-Ge (100) Schottky barrier diodes

8.1 Introduction

Metal-semiconductor (MS) contacts are the most widely used rectifying contacts in the electronic industry [1,2,3,4,5,6,7]. The performance and reliability of a Schottky diode is drastically influenced by the interface quality between the deposited metal and semiconductor surface [1,8,9]. It is often found that the current-voltage (*I-V*) characteristics of MS contacts usually deviate from the ideal thermionic emission (TE) current model [4,5,6,10,11,12]. The temperature dependence of barrier parameters of homogeneously doped Schottky contacts has been studied by several authors [13,14,15,16,17,18,19,20,21,22,23,24]. It was found that the barrier height (BH) extracted from *I-V* measurements using TE theory decreases and ideality factor increases with decreasing temperature. The standard TE theory fails to explain this result [19], as it expects the BH variation to be controlled only by the variation of band gap with temperature [13]. Schottky diodes (SDs) with low BH have found applications in devices operating at cryogenic temperatures, such as infrared detectors and sensors in thermal imaging [7,25,26,27]. Therefore, analysis of *I-V* characteristics of the Schottky barrier diodes (SBDs) at room temperature only does not give detailed information about their conduction process or the nature of barrier formation at the MS interface. The temperature dependence of the *I-V* characteristics allows us to understand different aspects of conduction mechanisms. Although, BH in Schottky contacts is likely to be a function of the atomic structure, and the atomic inhomogeneities at MS interface which are caused by grain boundaries, defects, multiple phases, etc. [28,29,30,31], additionally, there may be doping inhomogeneity at the MS interface and dopant clustering. Contaminants due to undesirable reaction products at the MS interface may act directly to introduce inhomogeneities [7] or they may simply promote inhomogeneity, through the generation of

defects [29,30,31,32,33]. There has been no report on the electrical transport characteristics of germanium (Ge) Schottky contacts at low temperatures. Therefore an attempt has been made to study the current transport characteristics of Pd-, Ni- and Au/n-Ge Schottky diodes in the temperature range 60-300 K. The temperature dependence of the BH and the ideality factor are discussed using TE theory.

8.2 Experimental procedures

SDs were fabricated on Sb-doped n-type Ge substrate with doping concentration of 2.5×10^{15} cm^{-3}. The substrates were sequentially degreased with organic solvents like trichloroethylene, acetone and methanol by ultrasonic agitation for 5 min in each stage followed by rinsing in deionised water. The native oxide on the surfaces was etched in a mixture of H_2O_2(30%):H_2O (1:5) for 1 min. After rinsing in deionised water the samples were blown dried using N_2. Immediately after cleaning the samples were inserted into a vacuum chamber where 100 nm thick AuSb (0.6%) was deposited by resistive evaporation as a back ohmic contact, followed by annealing at 350°C in Ar ambient for 10 min to minimize the ohmic contact's resistivity. Before Schottky contacts deposition, the samples were again chemically cleaned as described above. Palladium (Pd), gold (Au) and nickel (Ni) Schottky contacts were deposited onto Ge by vacuum resistive evaporation. These contacts were deposited under vacuum with a pressure below 10^{-6} Torr. The contacts were 0.6 mm in diameter and 30 nm thick. Following contact fabrication, current-voltage (*I-V*) measurements were performed in the temperature range 40-300 K.

8.3 Results and discussion

8.3.1 The current-voltage characteristics as a function of temperature

To understand whether or not a SD has an ideal diode behaviour, an analysis of its experimental *I-V* characteristics must be performed using the TE model [1]:

$$I(V) = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right], \tag{8.1}$$

with

$$I_0 = A^* A T^2 \exp\left(-\frac{q\Phi_B}{kT}\right), \tag{8.2}$$

where I_0 is the saturation current derived from the straight line intercept of the ln(I) – V plot at $V = 0$, V is the forward bias voltage, T is the absolute temperature, q is the electronic charge, k is the Boltzmann constant, A is the effective diode area, A^* is the effective Richardson constant, and Φ_B the zero bias effective SBH. From Eq. (8.2), we have:

$$\Phi_B = \frac{kT}{q} \ln\left(\frac{A^* A T^2}{I_0}\right), \tag{8.3}$$

and n is the ideality factor, which can be obtained accurately from the slope of the linear part of a ln (I) versus V plot, assuming pure thermionic emission can be obtained from Eq. (8.1) as

$$n = \frac{q}{kT} \frac{dV}{d(InI)}, \tag{8.4}$$

which is equal to 1 for an ideal diode and usually has a value greater than unity.

Typical forward bias I-V characteristics of Ni-/, Pd-/ and Au/n-Ge (100) Schottky contacts measured in the temperature range 60-300 K are shown in Figs. 8.1 – 8.3, respectively. These curves indicate a very strong temperature dependence of the Schottky diodes. These characteristics deviate from ideality at low temperatures (60 – 220 K), which are due to the effect of other current transport processes like the generation-recombination of carriers in space charge region [8] and tunnelling of electrons through the barrier. At temperatures above 220 K, thermionic emission becomes the dominant process. The experimental values of Φ_B and n were determined from intercepts and slopes of the forward ln (I) *versus* V plot at each temperature using the TE theory, respectively. That is, Φ_B and n were evaluated from the upper part of the temperature-dependent forward-bias I-V characteristics from 40 to 220 K .

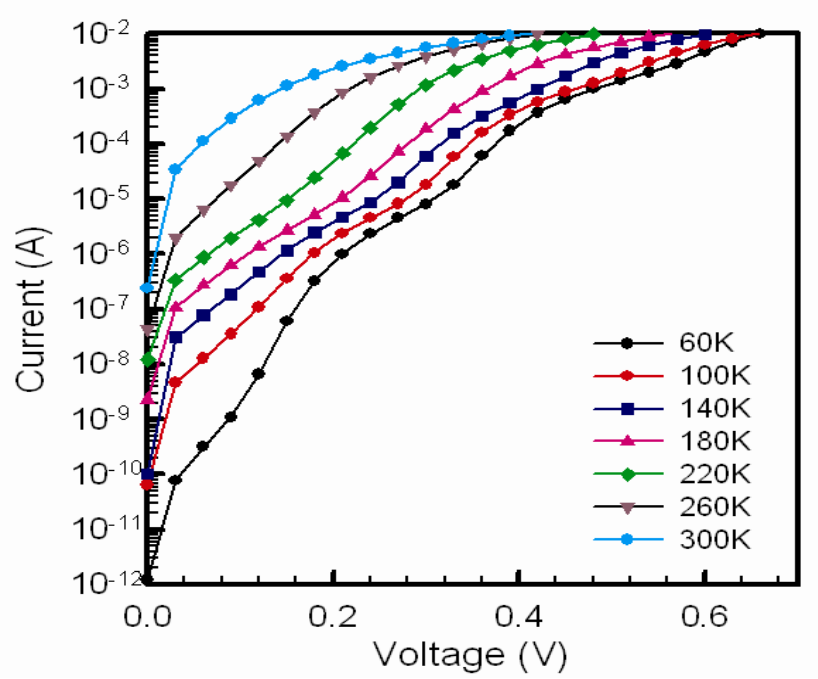


Fig. 8.1 *Experimental forward-bias current-voltage characteristics of a Ni/n-Ge (100) Schottky contact in the temperature range 60-300 K.*

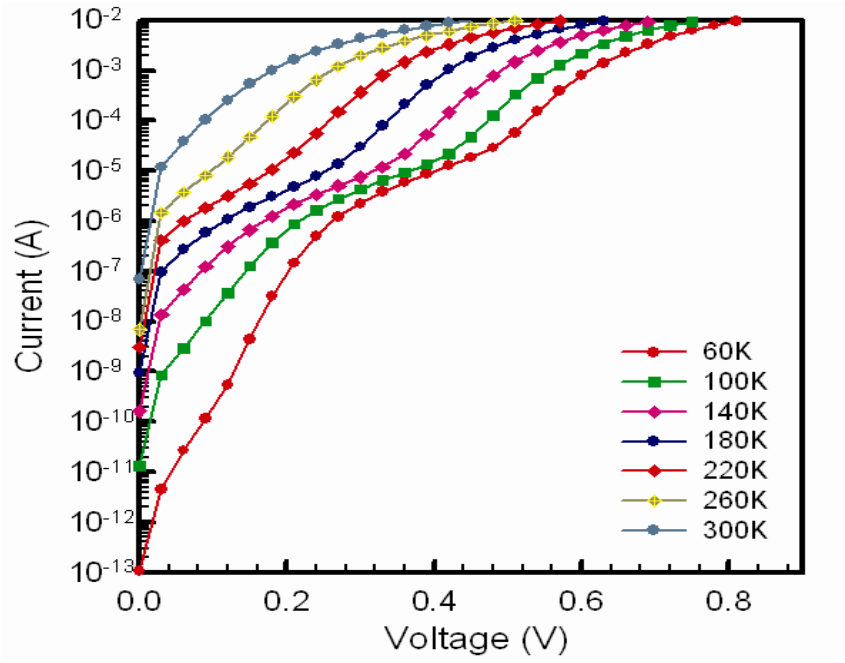


Fig. 8.2 *Experimental forward-bias current-voltage characteristics of a Pd/n-Ge (100) Schottky contact in the temperature range 60-300 K*

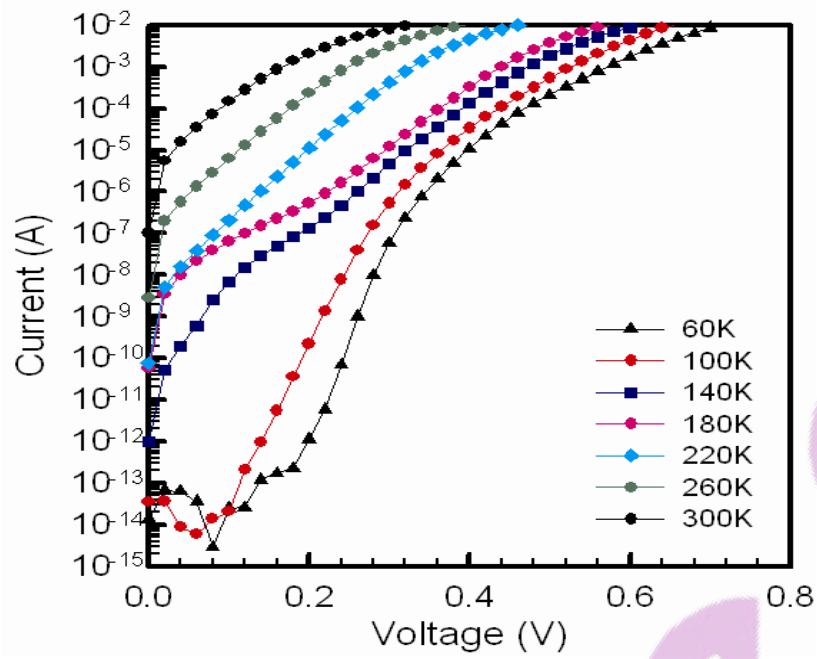


Fig. 8.3 *Experimental forward-bias current-voltage characteristics of a Au/n-Ge (100) Schottky contact in the temperature range 60-300 K*

Φ_B and n plots as a function of temperature for Ni-/, Pd-/ and Au/n-Ge (100) are presented in Figs. 8.4 – 8.6, respectively. The decrease in the barrier heights and increase in the ideality factors with decrease in temperature are observed from the *I-V* characteristics of Pd-/, Ni-/ and Au/n-Ge (100) Schottky contacts. This depicts that both parameters exhibit strong temperature dependence. This temperature dependence can be attributed to the discontinuities at the interface which may exist even for well controlled fabrication of the samples [34]. Since current transport across the MS interface is a temperature activated process, electrons at low temperatures are able to surmount the lower barriers [7], therefore, the current transport will be dominated by current flow through nanometer scale interfacial patches of small regions with lower SBH and larger ideality factors embedded in a higher background uniform barrier [31]. Because of these inhomogeneities, charge transport across the interface is no longer dominated by TE. Furthermore, many models have been evolved to explain the inhomogeneity in the barrier [31,35,36]. A potential fluctuation model was proposed by Tung [31] to explain the

inhomogeneity in BHs which show a larger deviation from the classical thermionic theory at low temperature.

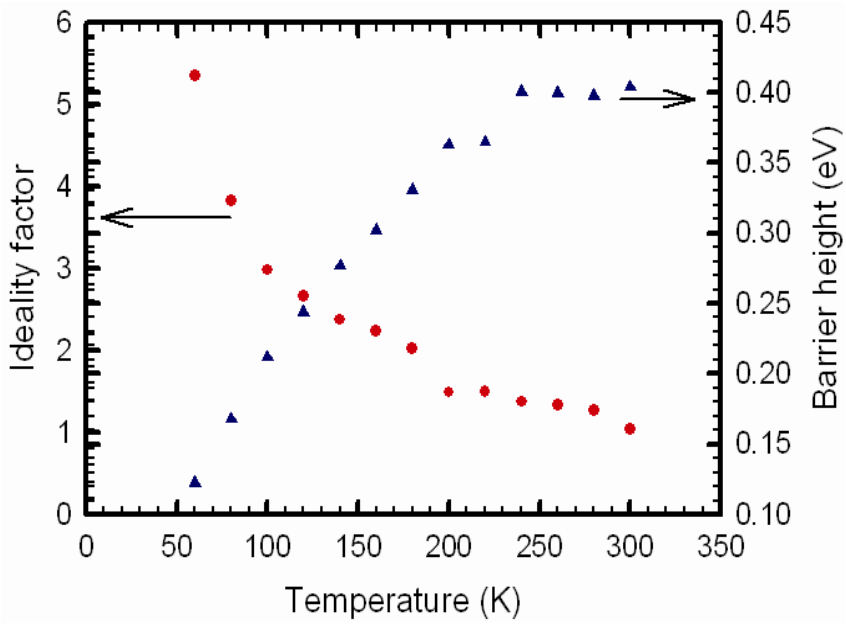


Fig. 8.4 *Temperature dependence of ideality factor and barrier height for Ni/n-Ge (100) Schottky contact in the temperature range 60-300 K*

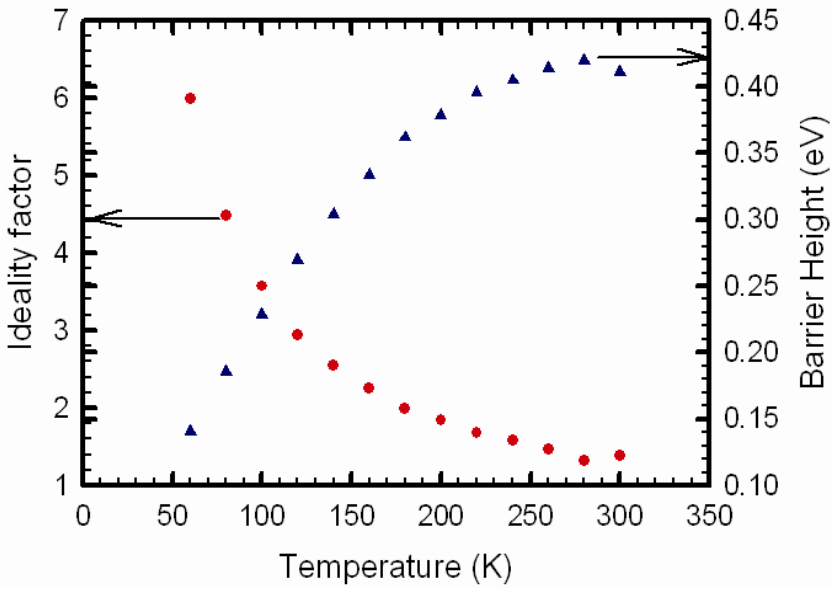


Fig. 8.5 *Temperature dependence of ideality factor and barrier height for Pd/n-Ge (100) Schottky contact in the temperature range 60-300* K

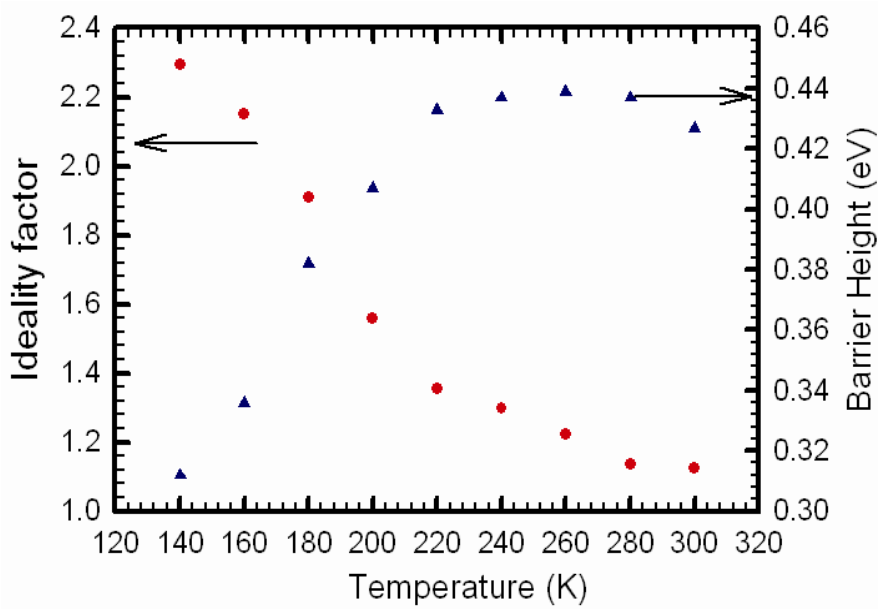


Fig. 8.6 *Temperature dependence of ideality factor and barrier height for Au/n-Ge (100) Schottky contact in the temperature range 140-300 K*

From the potential fluctuation model, at sufficiently low temperatures, a large number of patches may be present and consequently high current flowing through these patches. As the temperature increases, more electrons have sufficient energy to surmount the higher barrier [7,34]. As a result both the BH and ideality factor observed from temperature-dependent *I-V* characteristics (Figs. 8.4 – 8.6) are consistent with SBH inhomogeneity.

8.3.2 Analysis of inhomogeneous barrier height

The ideality factor is simply a manifestation of barrier uniformity [37]. BH inhomogenieties possibly originate from structural defects in semiconductors, inhomogeneous doping, interface roughness, interfacial reactions, diffusion/interdiffusion of the contaminants of deposited materials on semiconductor surfaces, inhomogeneities of thickness and composition of the layer, and non-uniformity of interfacial charges or the presence of a thin insulating layer between the metal and semiconductor [13,21,30,37,38,39]. The analysis of barrier height was also suggested and performed by Dokme et al. [40] and Karadeniz et al. [41]. The BH obtained under the flat

band condition is considered to be a real fundamental quantity which assumes that the electrical field is zero. This eliminates the effect of image force lowering that would affect the *I-V* characteristics and removes the influence of lateral inhomogeneity [40]. In order to describe the abnormal behaviours, i.e. the deviation from classical TE theory, a spatial distribution of the barrier height at the MS interface of Schottky contacts by a Gaussian distribution $P(\Phi_B)$ with a standard deviation (σ_s) around a mean SBH ($\bar{\Phi}_B$) value was suggested by Werner and Guttler [13,38] as:

$$P(\Phi_B) = \frac{1}{\sigma_s\sqrt{2\pi}} \exp\left[-\frac{(\Phi_B - \bar{\Phi}_B)^2}{2\sigma_s^2}\right], \tag{8.5}$$

where $\frac{1}{\sigma_s\sqrt{2\pi}}$ is the normalization constant of the Gaussian barrier distribution. The net current across a Schottky diode containing barrier inhomogeneities can be expressed as [40]

$$I(V) = \int_{-\infty}^{+\infty} I(\Phi_B, V) P(\Phi_B) d\Phi \ , \tag{8.6}$$

where $I(\Phi_B, V)$ is the current at a bias V for barrier height based on the ideal thermionic emission-diffusion (TED) theory and $P(\Phi_B)$ is the normalized distribution function giving the probability of accuracy for barrier height. The net current is then given by [40]

$$I(V) = I_s \exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \tag{8.7}$$

with

$$I_s = A^* A T^2 \exp\left(-\frac{q\Phi_{ap}}{kT}\right), \tag{8.8}$$

where n_{ap} and Φ_{ap} are the experimental apparent ideality factor and apparent barrier height at zero bias, respectively, and given by [38]

$$\Phi_{ap} = \bar{\Phi}_B(T=0) - \frac{q\sigma_{s0}^2}{2kT} \tag{8.9}$$

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \tag{8.10}$$

where ρ_2 and ρ_3 are the voltage coefficients that depict the voltage deformation of the barrier height distribution [37], while $\bar{\Phi}_B(T=0)$ and σ_{s0} are the mean barrier height and its standard deviation at the zero-bias ($V=0$), respectively.

The experimental Φ_B $vs\frac{1}{2kT}$ and $\left(\frac{1}{n}-1\right)vs\frac{1}{2kT}$ plots obtained by means of data from Figs. 8.1 – 8.3 for Pd-/, Ni-/ and Au/n-Ge (100) are shown in Figs. 8.7 – 8.9, respectively. The temperature dependence of the barrier height for Pd/n-Ge (100) Schottky diode (Fig. 8.7) depicts two Gaussian distributions with $\bar{\Phi}_{B1}(T=0)$ = 0.526 eV and σ_{s01} = 0.072 eV in 100 – 300 K and $\bar{\Phi}_{B2}(T=0)$ = 0.354 eV and σ_{s01} = 0.047 eV in 60 – 100 K.

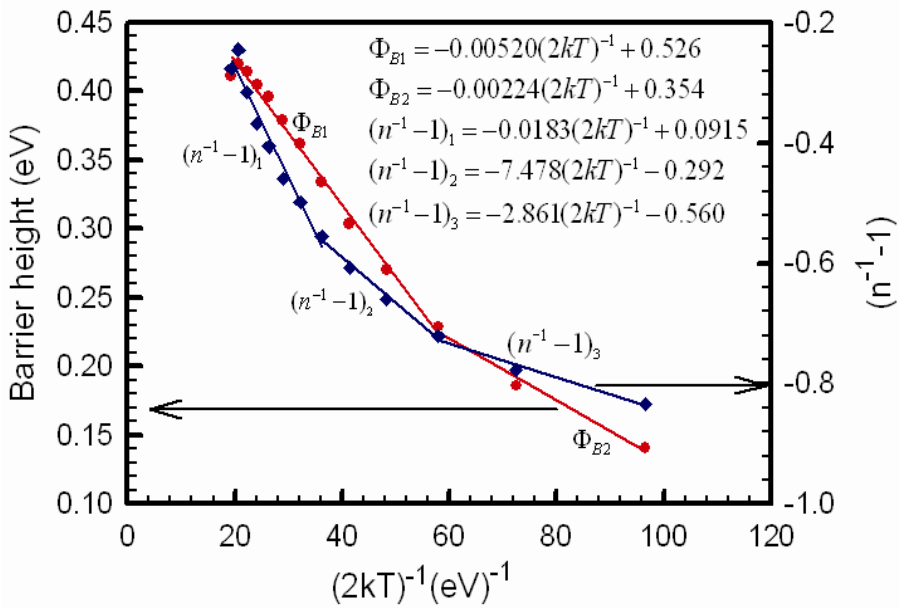


Fig. 8.7 *Temperature dependence of barrier height (Φ_B) and ideality factor (1/n −1) for Pd/n-Ge (100) Schottky diode.*

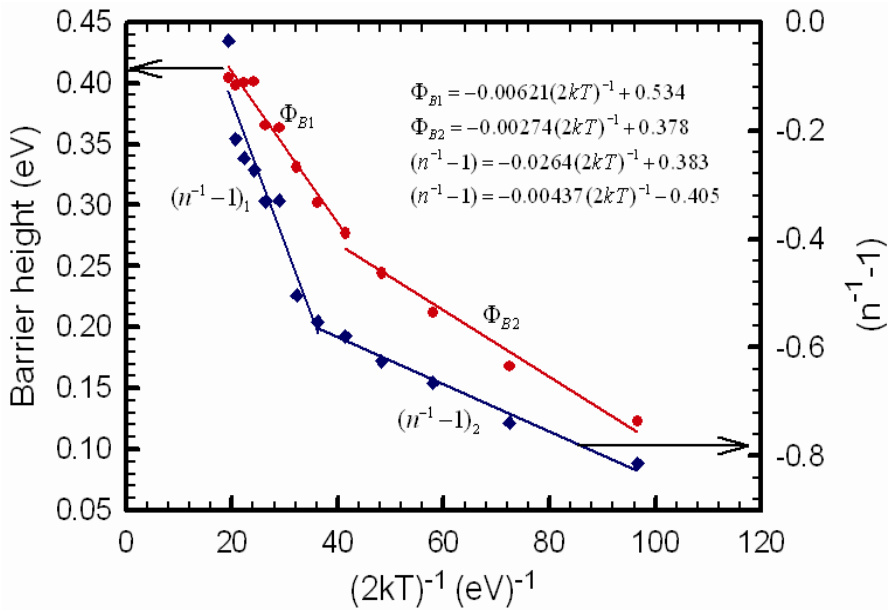


Fig. 8.8 *Temperature dependence of barrier height (Φ_B) and ideality factor (1/n −1) for Ni/n-Ge (100) Schottky diode.*

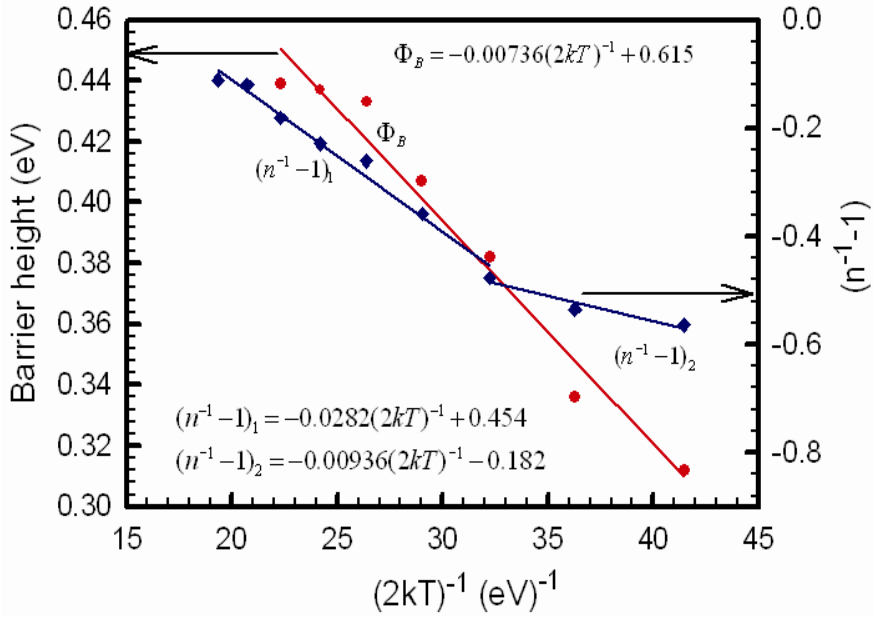


Fig. 8.9 *Temperature dependence of barrier height (Φ_B) and ideality factor (1/n −1) for Au/n-Ge (100) Schottky diode.*

The ideality factor for Pd/n-Ge (100) Schottky diode (Fig. 8.7) varies linearly with temperature in three distinct regions. The voltage coefficients have been obtained as $\rho_{21} = -0.0915$ and $\rho_{31} = -0.0183$ in 160 – 300 K range, $\rho_{22} = 0.292$ and $\rho_{32} = -7.478$ in 100 – 160 K range and $\rho_{23} = 0.560$ and $\rho_{33} = -2.861$ in 60 – 100 K range.

Fig. 8.8 shows a linear variation of barrier height and the ideality factor for Ni/n-Ge (100) Schottky contact. The data has been fitted to two regions whose Gaussian distribution parameters $\bar{\Phi}_B(T=0)$, σ_{s0} ρ_2 and ρ_3 have been extracted as $\bar{\Phi}_{B1}(T=0) = 0.534$ eV, $\sigma_{s01} = 0.0788$ eV, $\rho_{21} = -0.383$ and $\rho_{31} = -0.0264$ in 140-300 K range, and $\bar{\Phi}_{B2}(T=0) = 0.378$ eV, $\sigma_{s02} = 0.0523$ eV, $\rho_{22} = 0.405$ and $\rho_{32} = -0.0437$ in 60-140 K range.

The barrier height obtained from Au/n-Ge (100) Schottky diode is shown in Fig. 8.9. Parameters obtained for the Gaussian fit have been obtained as $\bar{\Phi}_{B1}(T=0) = 0.615$ eV and $\sigma_{s01} = 0.0858$ eV in 140-300 K. The data has been fitted to a single region. In this temperature range, the ideality factor shows some linearity with temperature in two regions. The voltage coefficients have been obtained as $\rho_{21} = -0.454$, and $\rho_{31} = -0.0282$ in 180-300 K range, $\rho_{22} = 0.182$ and $\rho_{32} = -0.00936$ in 140-180 K range.

When comparing $\bar{\Phi}_B(T=0)$ and σ_{s0} parameters, it is seen that the standard deviation is ≈ (13-15) % of the mean zero-bias barrier height. The standard deviation is a measure of barrier homogeneity. The lower value of σ_{s0} corresponds to a more homogeneous barrier height. These values of σ_{s0} are not small compared to their respective $\bar{\Phi}_B(T=0)$ and this indicates larger inhomogenieties at interface of Pd-/, Ni-/ and Au/n-Ge (100) structures. Hence, this inhomogeneity and potential fluctuations affect low temperature *I-V* characteristics. The linear behaviour of the plot from Eq. 8.10 demonstrates that the ideality factor does indeed express the voltage deformation of the Gaussian distribution of the SBH.

To determine the barrier height in another way, Eq. 8.2 can be rewritten as

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*) - \frac{q\Phi_{B0}}{kT} \tag{8.11}$$

The Richardson constant is usually determined from the intercept of $\ln\left(\frac{I_0}{T^2}\right) versus \frac{1000}{T}$ plot. Figs 8.10-8.12 show the conventional energy variation of $\ln\left(\frac{I_0}{T^2}\right) versus \frac{1000}{T}$ (labelled y_1) for Pd-, Ni- and Au/n-Ge (100) Schottky diodes, respectively. The experimental data are shown to fit asymptotically to a straight line at higher temperatures. Since the conventional Richardson plot deviates from linearity at low temperatures due to the barrier inhomogeneity, it can be modified by combining Eq. 8.8 and 8.9 as follows

$$\ln\left(\frac{I_s}{T^2}\right) - \left(\frac{q^2\sigma_{s0}^2}{2k^2T^2}\right) = \ln\left(A^*A\right) - \frac{q\bar{\Phi}_{B0}}{kT} \tag{8.12}$$

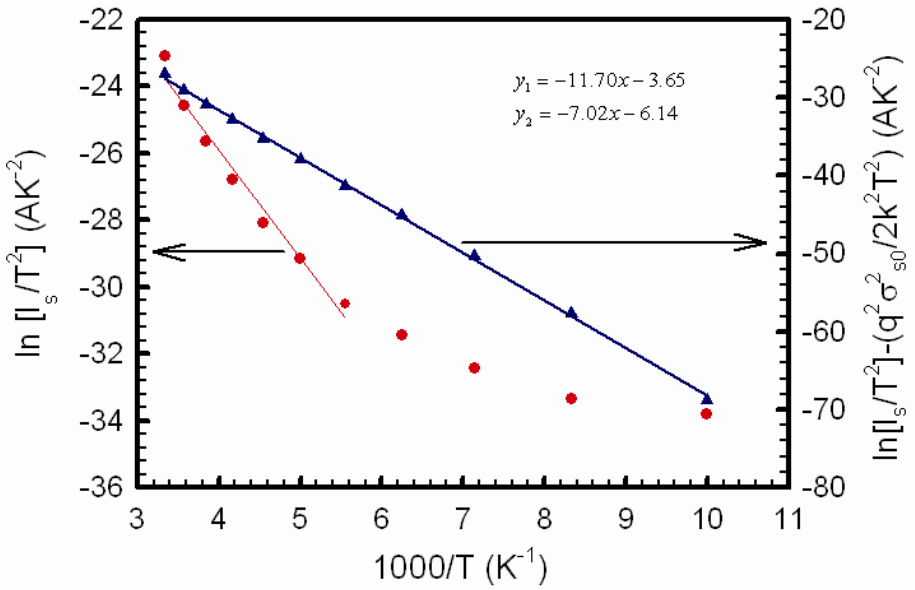


Fig. 8.10 *Richardson's plot of* $\ln\left(\frac{I_0}{T^2}\right) versus \frac{1000}{T}$ *and modified* $\ln\left(\frac{I_s}{T^2}\right) - \left(\frac{q^2\sigma_{s0}^2}{2k^2T^2}\right) versus \frac{1000}{T}$ *for Pd/n-Ge (100) Schottky diode.*

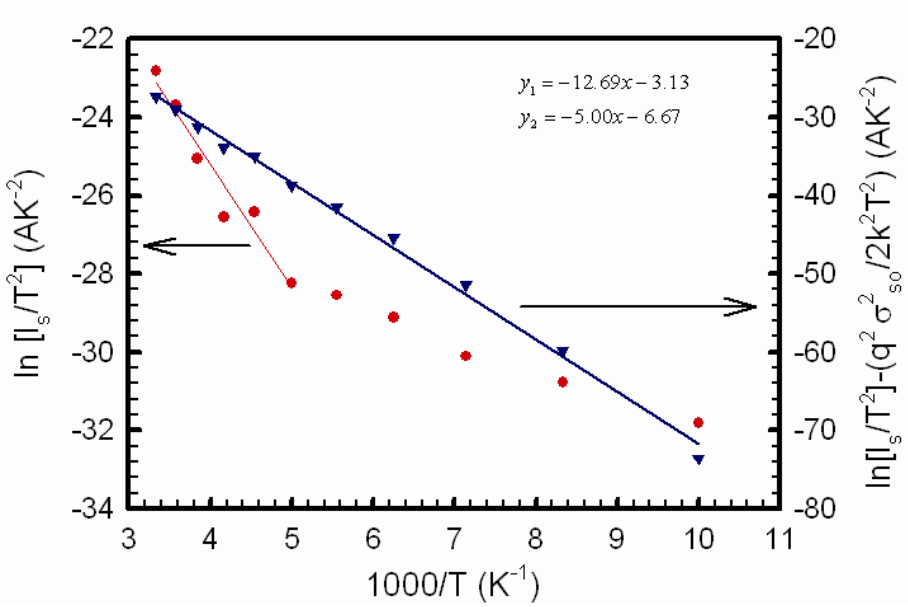


Fig. 8.11 *Richardson's plot of* $\ln\left(\frac{I_0}{T^2}\right)$ *versus* $\frac{1000}{T}$ *and modified* $\ln\left(\frac{I_s}{T^2}\right)-\left(\frac{q^2\sigma_{s0}^2}{2k^2T^2}\right)$ *versus* $\frac{1000}{T}$ *for Ni/n-Ge (100) Schottky diode.*

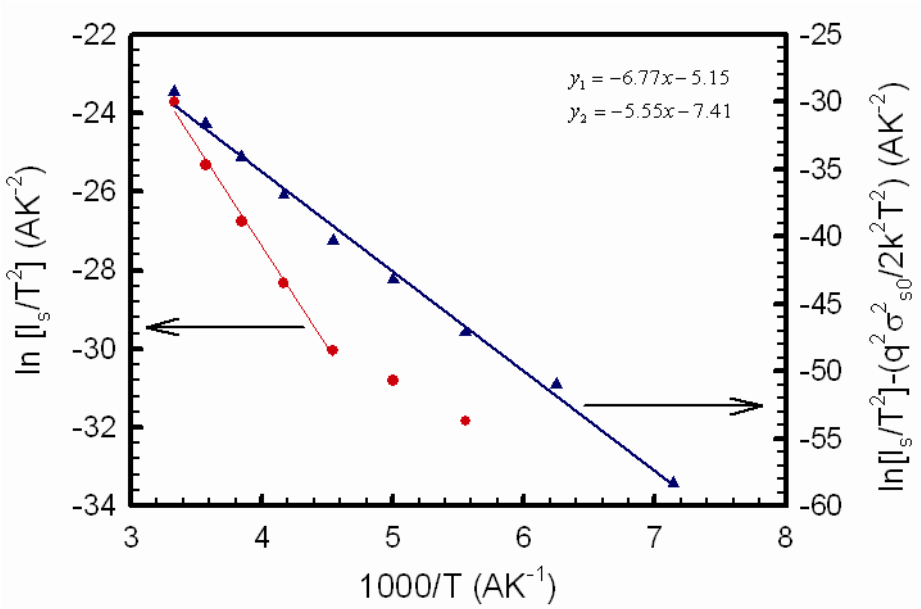


Fig. 8.12 *Richardson's plot of* $\ln\left(\frac{I_0}{T^2}\right)$ *versus* $\frac{1000}{T}$ *and modified* $\ln\left(\frac{I_s}{T^2}\right)-\left(\frac{q^2\sigma_{s0}^2}{2k^2T^2}\right)$ *versus* $\frac{1000}{T}$ *for Au/n-Ge (100) Schottky diode.*

Figs. 8.10-8.12 show the modified $\ln\left(\frac{I_s}{T^2}\right)-\left(\frac{q^2\sigma_{s0}^2}{2k^2T^2}\right) versus \frac{1000}{T}$ plot (labelled y_2) for Pd-/, Ni- and Au/n-Ge (100) Schottky diodes, respectively. The modified plot gives $\bar{\Phi}_B(T=0)=$ 0.529 eV and $A^*=$ 0.32 Acm^{-2}K^{-2} for Pd/n-Ge Schottky structures, $\bar{\Phi}_B(T=0)=$ 0.575 eV and $A^*=$ 2.38 Acm^{-2}K^{-2} for Ni/n-Ge Schottky structures and $\bar{\Phi}_B(T=0)=$ 0.639 eV and $A^*=$ 1.37 Acm^{-2}K^{-2} for Au/n-Ge Schottky structures. The values of $\bar{\Phi}_B(T=0)$ have almost the same values as the mean BHs obtained from the Φ_B *vs* $\frac{1}{2kT}$ plot at higher temperatures in Figs 8.7- 8.9. The modified Richardson constant from the modified plots ranges between 0.32 and 2.38 Acm^{-2}K^{-2}. Yao et al. [42] and Zhu et al. [43] have reported the n-type Ge Richardson constant to be 50 and 67 Acm^{-2}K^{-2}, respectively.

8.4 Summary and conclusions

The *I-V-T* characteristics of Pd-/, Ni-/ and Au/n-Ge (100) Schottky contacts fabricated using the resistive evaporation system were measured in the 40-300 K temperature range. The ideality factors were seen to increase while barrier heights decrease with decreasing temperature. These observations have been attributed to barrier inhomogeneities at the MS interface. The *I-V* characteristics of these Schottky contacts over a wide temperature range have been successfully modelled on the basis of the TE mechanism by assuming the presence of multiple Gaussian distributions of barrier heights in the 40-300 K temperature range. Chand and Kumar [44] have indicated that the existence of multiple Gaussian distributions in MS contacts can be attributed to the nature of the inhomogenieties themselves. This may involve variation in interface composition/phase, interface quality, electrical charges and non-stoichiometry, etc [45].

References

[1] E.H. Rhoderick, R.H. Williams, Metal-Semiconductor Contacts, Clarendon Press, Oxford University Press, Oxford, 1988.

[2] H. Cetin, E. Ayyildiz, Semicond. Sci. Technol. **20** (2005) 625.

[3] R.L. Van Meirhaeghe, W.H. Laflére, F. Cardon, J. Appl. Phys. **76** (1994) 403.

[4] E. Gur, S. Tuzemen, B. Kilic, C. Coskun, J. Phys. Condens. Matter. **19** (2007) 1966206.

[5] N. Rouag, L. Boussouar, S. Toumi, Z. Ounnoughi, M.A. Djouadi, Semicond. Sci. Technol. **22** (2007) 369.

[6] D.M. Kim, D.H. Kim, S.Y. Lee, Solid-State Electron. **51** (2007) 865.

[7] F.E. Cimilli, M. Sağlam, H. Efeoğlu, A. Türüt, Physica B **404** (2009) 1558.

[8] S.M. Sze, Physics of Semiconductor Contacts, 2nd .ed., Wiley, New York, 1981.

[9] R.T. Tung, Mater. Sci. Eng. R **35** (2001) 1.

[10] Dhananjay, J. Nagaraju, S.B. Krupanidhi, Physica B **391** (2007) 344.

[11] A.R. Arehart, B. Moran, J.S. Speck, U.K. Mishra, S.P. Den Baars, S.A. Ringel, J. Appl. Phys. **100** (2006) 023709.

[12] A.F. Qasrawi, Semicond. Sci. Technol. **21** (2006) 794).

[13] J.H. Werner, H.H. Guttler, J. Appl. Phys. **73** (1993) 1315.

[14] S. Chattopadhyay, L.K. Bera, S.K. Ray, K. Maiti, Appl. Phys. Lett. **71** (1997) 942.

[15] T.P. Chen, T.C. Lee, C.C. Ling, C.D. Beling, S. Fung, Solid-State Electron. **36** (1993)

949.

[16] M.K. Hudait, P. Venkatesvarlu, S.B. Krupanidhi, Solid-State Electron. **45** (2001) 133.

[17] Ş. Karataş, Ş. Altindal, A. Türüt, A. Özmen, Appl. Surf. Sci. **217** (2003) 250.

[18] T. Sawada, Y. Ito, N. Kimura, K. Imai, K. Suzuki, S. Sakai, Appl. Surf. Sci. **190** (2002) 326.

[19] J. Osvald, Zs.J. Horváth, Appl. Surf. Sci. **234** (2004) 349.

[20] N. Tuğluoğlu, S. Karadeniz, M. Şahin, H. Şafak, Appl. Surf. Sci. **233** (2004) 320.

[21] M. Soylu, B. Abay, Microelectron. Eng. **86** (2009) 88.

[22] W. Mtangi, F.D. Auret, C. Nyamhere, P.J. Janse van Rensburg, M. Diale, A. Chawanda, Physica B **404** (2009) 1092.

[23] F.E. Cimilli, M. Sağlam, H. Efeoğlu, A. Türüt, Physica B **404** (2009) 1558.

[24] Ö. Faruk Yüksel, Physica B **404** (2009) 1993.

[25] M. Pattabi, S. Krishnan, Ganesh, X. Mathew, Solar Energy **81** (2007) 111.

[26] F. Brovelli, B.L. Rivas, J.C. Bernede, J. Chilean, Chem Soc. **52** (2007) 1065.

[27] F. Yakuphanoglu, Physica B **389** (2007) 306.

[28] H.J. Im, Y. Ding, J.P. Pelz, W.J. Choyke, Phys. Rev. B **64** (2001) 075310.

[29] R.F. Schmitsdorf, T.U. Kampen, W. Mönch, J. Vac Sci. Technol. B **15** (1997) 1221.

[30] J.P. Sullivan, R.T. Tung, M.R. Pinto, W.R. Graham, J. Appl. Phys **70** (1991) 7403.

[31] R.T. Tung, Phys. Rev. B **45** (1992) 13509.

[32] W.P. Leroy, K. Opsomer, S. Forment, R.L. Van Meirhaeghe, Solid-State Electron. **49** (2005) 878.

[33] F.E. Cimilli, M. Saglam, A. Turut, Semicond. Sci. Technol. **22** (2007) 851.

[34] M.B. Reddy, A.A. Kumar, V. Janardhanam, V. R. Reddy, P.N. Reddy, Current. Appl. Phys. **9** (2009) 972.

[35] J.D. Levine,J. Appl. Phys. **42** (1971) 3991.

[36] F.A. Padovani, R. Stratton, Solid-State Electron. **9** (1996) 695.

[37] S. Zhu, R.L. Van Meirhaeghe, S. Forment, G.P. Ru, X.P. Qu, B.Z. Li, Solid State Electron. **48** (2004) 1205.

[38] J.H. Werner, H.H. Guttler, J. Appl. Phys. **69** (1991) 1522.

[39] Y.P. Song, R.L. Van Merhaeghe, W.H. Laflare, F. Cardon, Solid State Electron. **29** (1986) 633.

[40] I. Dokme, S. Altindal, M.M. Bulbul, Appl. Surf. Sci. **252** (2006) 7749.

[41] Ş. Karadeniz, M. Şahim, N. Touğluoğlu, H. Şafak, Semicond. Sci. Technol. **19** (2004) 1098.

[42] H.B. Yao, C.C. Tan, S.L. Liew, C.T. Chua, C.K. Chua, R. Li, R.T.P. Lee, S.J. Lee, D.Z. Chi, International Workshop on Junction Technology Proc (2006) 164.

[43] S. Zhu, A. Nakajima, Y. Yokoyama and K. Ohkura, International Workshop on Junction Technology Proc (2005) 85.

[44] S. Chand, J. Kumar, Semicond. Sci. Technol. **11** (1996) 1203.

[45] S. Doğan, S. Duman, B. Gürbuolak, S. Tüzemen, H. Morkoç, Physica E **41** (2009) 64.

CHAPTER 9

Conclusions

Conclusions specific to each of the experimental results are presented at the end of every chapter. In this chapter a brief summary of the results is presented.

Thermal annealing behaviour of metal Schottky contacts on n-Ge (100)

The Schottky contact behaviour was investigated under various furnace annealing conditions. The variation of Schottky barrier heights and ideality factors with annealing temperature may be attributed to interfacial reactions of the metals with germanium and phase transformation of metal-germanides during annealing. The as-deposited barrier heights near the bandgap of Ge in Pt/-, Ni/-, Ti/- and Ir/n-Ge (100) Schottky contacts imply that these metals form good Schottky source/drain contacts in p-channel Ge-MOSFETs, for hole injection from source into inverted p-channel. The results also show that Pt/n-Ge (100) and Ru/n-Ge (100) Schottky contacts are highly thermally stable over a wide range of temperature, 25 – 600°C and 25 – 550°C, respectively.

Morphological evolution of metal Schottky contacts on n-Ge (100)

SEM observations were conducted for samples annealed at different temperatures. From the SEM images, it can be concluded that the onset temperature for agglomeration in 30 nm Ni/n-Ge (100), and Pt/-, Ir/- and Ru/n-Ge (100) systems occur at 500 – 600°C and 600 – 700°C, respectively. Grain growth at the surface of these metals was evident up to 500°C, suggesting a better morphological stability.

The barrier height distribution in identically prepared Schottky contacts on n-Ge (100)

The barrier heights and the ideality factors were obtained from the individual *I-V* characteristics of the MS contacts. It has been shown that the barrier heights and the ideality factors varied from diode to diode even though they were identically fabricated. The homogeneous barrier height values were obtained for the metals on n-Ge Schottky contacts from the linear relationship between the *I-V* effective barrier heights and ideality factors, which can be explained by lateral

inhomogeneities. The agreement between experimental data and theoretical predictions on Pd/n-Ge (100), Ni/n-Ge (100) and Au/n-Ge (100) contacts were an interesting experimental illustration of the theoretical predictions [1,2,3].

Studies of defects induced in Sb doped Ge during contacts fabrication and the annealing process.

DLTS and L-DLTS have been successfully used to characterize the defects induced in n-Ge during metallization by electron beam deposition and subsequent annealing processes. These techniques have revealed that the dominant defect induced by electron beam deposition is the V-Sb (*E*-centre) complex. The source of the damage has been due to the residual vacuum gases, which were ionized around the filament and then accelerated by the electric and magnetic field towards the substrate, introducing vacancy-interstitial pairs beneath the semiconductor surface, which are mobile and form stable mainly vacancy-related defects. All defects induced during electron beam deposition and annealing were removed from Ge with very low thermal budget of between 200-350°C. This indicates low binding energies of defects in Ge.

Current-Voltage Temperature characteristics of n-Ge (100) Schottky barrier diodes.

The n-Ge Schottky contacts have revealed a strong dependence on temperature. The current transport mechanism has been shown to be predominantly thermionic emission at high temperatures (i.e. close to room temperature) while at low temperatures, the Schottky contacts have exhibited the dominance of the generation-recombination current mechanism. From the *I-V* measurements, the ideality factors were seen to increase and barrier heights decrease with decreasing temperature. This have been attributed to the presence of a wide distribution of low SBH patches at the metal-germanium interface, leading to the flow of excess current at low voltages and temperatures.

Future Work

Further studies need to be carried out to investigate the following:

(i) Identification of the composition of residual vacuum particles during electron beam metallization process.

(ii) The effects of a metal shield in the EB system to protect the Ge sample from energetic particles originating at the filament during the electron beam deposition, on the electrical properties of Ge Schottky contacts.

(iii) Structural characterization of metal germanides using XRD, XPS, AES and Raman spectroscopy techniques.

(iv) Establishment of defect concentration profile, annealing mechanisms for prolonged time: model.

References

[1] R.T. Tung, Phys. Rev. B **45** (1992) 13509.

[2] J.P. Sullivan, R.T. Tung, M.R. Pinto, W.R. Graham, J. Appl. Phys. **70** (1991) 7403.

[3] R.F. Schmitsdorf, T.U. Kampen, W. Mönch, **15** (1997) 1221.

PUBLICATIONS

Physica B 404 (2009) 4482–4484

Contents lists available at ScienceDirect

Physica B

journal homepage: www.elsevier.com/locate/physb

Thermal stability study of palladium and cobalt Schottky contacts on n-Ge (1 0 0) and defects introduced during contacts fabrication and annealing process

A. Chawanda [a,b,*], C. Nyamhere [a], F.D. Auret [a], W. Mtangi [a], T.T. Hlatshwayo [a], M. Diale [a], J.M. Nel [a]

[a] Department of Physics, University of Pretoria, 0002, South Africa
[b] Department of Physics, Midlands State University, Bag 9055, Gweru, Zimbabwe

ARTICLE INFO

PACS:
67.80.dj
68.55.ag
68.60dv

Keywords:
Schottky contacts
DLTS
Germanium

ABSTRACT

Palladium (Pd) and cobalt (Co) Schottky barrier diodes were fabricated on n-Ge (1 0 0). The Pd-Schottky contacts were deposited by resistive evaporation while the Co-contacts were deposited by resistive evaporation and electron beam deposition. Current–voltage (I–V), capacitance–voltage (C–V) and deep level transient spectroscopy (DLTS) measurements were performed on as-deposited and annealed samples. Electrical properties of Pd and Co samples annealed between 30 and 600 °C indicate the formation of one phase of palladium germanide and two phases of cobalt germanide. No defects were observed for the resistively evaporated as-deposited Pd-and Co-Schottky contacts. A hole trap at 0.33 eV above the valence band was observed on the Pd-Schottky contacts after annealing at 300 °C. An electron trap at 0.37 eV below the conduction band and a hole trap at 0.29 eV above the valence band was observed on as-deposited Co-electron beam deposited Schottky contacts. Rutherford back scattering (RBS) technique was also used to characterise the Co–Ge, for as-deposited and annealed samples.

1. Introduction

Microelectronics has been primarily a Si-based technology because of the stability and high quality of SiO_2 and its interface with a Si substrate [1]. Attempts to develop faster devices in modern microelectronics have increased the interest for alternative materials to silicon, compatible with the existing silicon-based technology [2]. Germanium (Ge) is often proposed as a potential alternative to silicon due to its high carrier mobility, low effective mass of holes [3] and relative compatibility with silicon processing. This has led to renewed interest in the complete understanding of metal–germanium interactions and dynamic properties of radiation and process-induced defects in Ge.

In this work, palladium (Pd) and cobalt (Co) Schottky contacts on n-Ge (1 0 0) were fabricated and electrical properties of the contacts were investigated. We also report the electronic properties of defects introduced during contacts fabrication and annealing process. The in-diffusion of Co–Ge was investigated by employing Rutherford backscattering spectroscopy.

2. Experimental procedure

We have used bulk grown n-type Ge with (1 0 0) crystal orientation, doped with antimony, (Sb) to a density of 2.5×10^{15} cm^{-3} supplied by Umicore. Before metallization the samples were first degreased and then etched in a mixture of H_2O_2:H_2O (1:5) for 1 min. Immediately after cleaning they were inserted into a vacuum chamber where AuSb (0.6% Sb), 120 nm thick, was deposited by resistive evaporation as back ohmic contacts. Anneal at 350 °C for 10 min in argon (Ar) to lower the barrier height and increase the ohmic behavior of the contact was performed. Before Schottky contact deposition, the samples were again chemically cleaned as described above. Pd contacts were deposited by vacuum resistive evaporation and the Co contacts were deposited by vacuum resistive evaporation and electron beam deposition. The contacts were 0.6 mm in diameter and 30 nm thick. After the contact formation the samples were characterized by current–voltage (I–V) and capacitance–voltage (C–V) measurements at room temperature to determine the quality of the diodes. The electrical characterization was repeated after every annealing cycle in Ar gas for 30 min between 30 and 600 °C. The defects introduced were characterised by DLTS [4] and LDLTS [5,6]. The '*signatures*' of induced defects (i.e. energy position in band gap relative to the conduction band and valence band for the electron traps and hole traps, respectively, E_T, and their apparent capture cross section, σ_a), were determined from Arrhenius plots of

* Corresponding author at: Department of Physics, University of Pretoria, 0002, South Africa. Tel.: +27 12 420 3508; fax: +27 12 362 5288.
E-mail address: albert.chawanda@up.ac.za (A. Chawanda).

0921-4526/$ - see front matter © 2009 Elsevier B.V. All rights reserved.
doi:10.1016/j.physb.2009.09.043

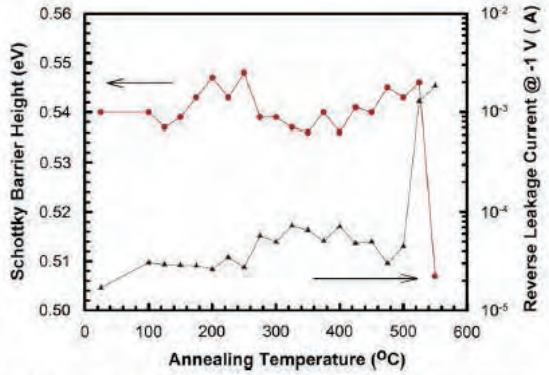


Fig. 1. (Color online) Plot of the Schottky barrier height and the Reverse leakage current at −1 V as function of annealing temperature for Pd Schottky contacts on n-Ge (1 0 0).

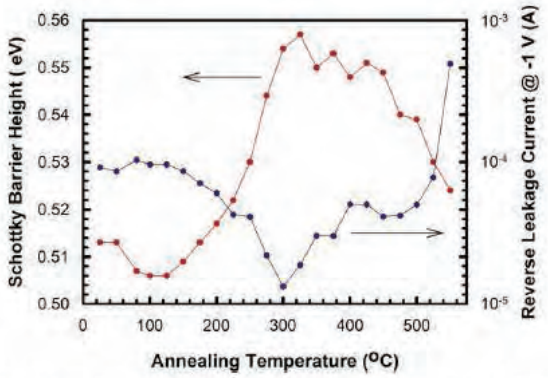


Fig. 2. (Color online) Plot of the Schottky barrier height and the Reverse leakage current at −1 V as a function of annealing temperature for Co Schottky contacts on n-Ge (1 0 0).

$\ln(T^2/e)$ vs. $1000/T$, where 'e' is either the hole or electron emission rate, and T is the measurement temperature [7].

Rutherford backscattering spectroscopy (RBS) with beam energy of 1.6 MeV He ions and a solid-state detector positioned at $\theta = 165°$ relative to the incident beam, was used to analyze the Co–Ge in diffusion in the samples, as-deposited, and after annealing at 325, 425, 500 and 600 °C.

3. Results and discussion

3.1. Germanides formation

Fig. 1 shows the variation of the Schottky barrier height and reverse current at −1 V with annealing temperature for the Pd Schottky contacts. Fig. 3(a) shows the variation of Pd Schottky contacts ideality factor with annealing temperature. From Figs. 1 and 3(a), the electrical properties of the Pd Schottky contacts between 250 and 500 °C annealing temperature, we propose that one phase of palladium germanide, PdGe is formed and is stable over a wide temperature range. This is in agreement with what was observed by Gaudet et al. [1].

The variation of the Schottky barrier height, reverse leakage current at −1 V and ideality factor with annealing temperature for the Co Schottky contacts is shown in Figs. 2 and 3(b). The variations of these electrical parameters with annealing temperature suggest that three phases of Co germanides are formed. We propose that CoGe, Co_5Ge_7 and $CoGe_2$ germanides are formed during the annealing process. The CoGe formed between 100 and 300 °C, Co_5Ge_7 formed around 300 °C and then transform to $CoGe_2$ at temperature above 425 °C [8].

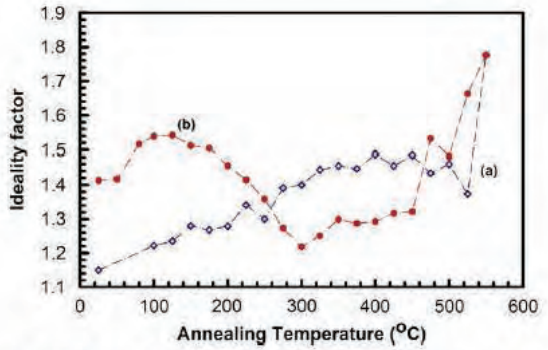


Fig. 3. (Color online) Plot of Ideality factor as a function of annealing temperature for: (a) Pd Schottky contacts on n-Ge (1 0 0) and (b) Co Schottky contacts on n-Ge (1 0 0).

3.2. DLTS analysis of fabrication and annealing process induced defects

Fig. 4 shows a conventional DLTS spectrum obtained from Pd Schottky contacts annealed from room temperature to 350 °C. It depicts that no defects are observable for the resistively evaporated as-deposited Pd Schottky contacts and a hole trap $E_V + 0.33$ eV labeled $H(0.33)$ with capture cross-section of $1.02 \times 10^{-14}\,cm^{-2}$ was observed after annealing at 300 °C. We speculate that this defect is probably Pd related.

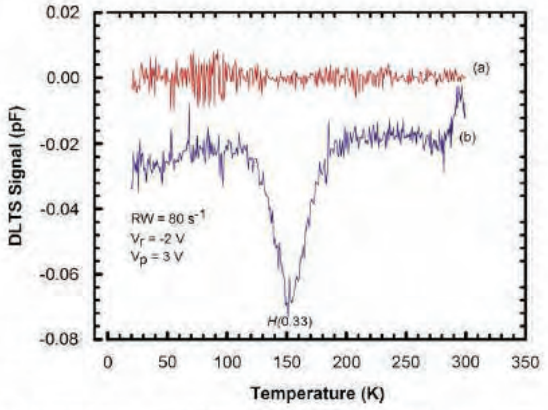


Fig. 4. DLTS spectra of the Pd Schottky contacts on n-Ge (1 0 0) (a) as-deposited and (b) after annealing at 300 °C. These spectra were recorded at a rate window of $80\,s^{-1}$ and quiescent reverse bias of −2 V with a filling pulse of 3 V.

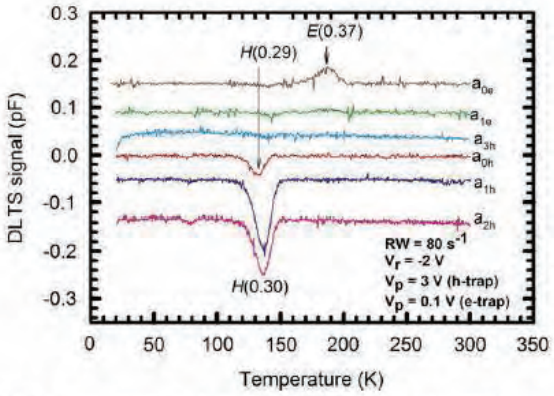


Fig. 5. DLTS spectra of the EBD Co Schottky contacts on n-Ge (1 0 0) (a_0) as-deposited and after annealing at (a_1) 200 °C, (a_2) 300 °C and (a_3) 350 °C. The subscripts 'e' and 'h' on the graph labels stand for electron and hole traps. These spectra were recorded at a rate window of 80 s^{-1} and quiescent reverse bias of −2 V with a filling pulse of 0.1 and 3 V for an electron and a hole trap, respectively.

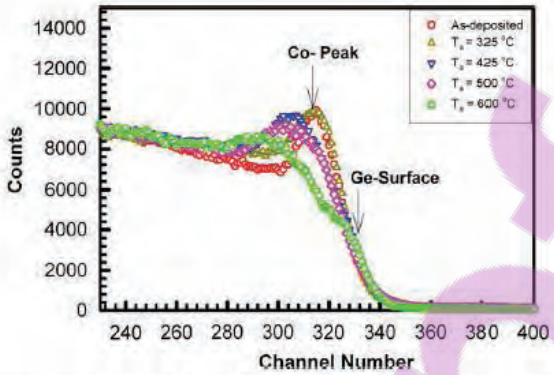


Fig. 6. (Color online) Backscattering energy spectra of 1.6 MeV He^+ ions for cobalt films deposited on germanium after isochronal thermal treatment for 30 min at different annealing temperatures: as-deposited, 325, 425, 500 and 600 °C.

An electron trap at E_C+0.37 eV labeled $E(0.37)$, and a hole trap at E_V+0.29 eV with capture cross sections of 4.03×10^{-14} cm^{-2} and 3.03×10^{-14} cm^{-2}, respectively were observed in as-deposited, Co Schottky contacts fabricated with electron beam deposition (EBD), as shown in Fig. 5. The electron trap $E(0.37)$ is the well known (=/−) charge state of the E-center (V–Sb) in Sb-doped Ge [9], whilst the hole trap $H(0.29)$ is the (−/0), the single acceptor level of the Sb–V center in Ge. The hole trap $H(0.29)$ is thermally stable up to an annealing temperature of 150 °C and anneals out at 200 °C [7]. Further annealing studies in the temperatures ranging from 200 to 350 °C, reveal a hole trap $H(0.30)$, shown in Fig. 5 with capture cross section of 7.8×10^{-14} cm^{-2} and anneals out between 300 and 350 °C. A similar defect $H(0.30)$ was also observed by Nyamhere et al. [10] during the characterization of defects introduced in antimony doped germanium by 3 keV Ar sputtering. We speculate that this hole trap is a vacancy related defect, formed when vacancies are injected into the Ge substrate during the metal germanidation process.

From the DLTS characterization of the resistively evaporated Co Schottky contacts, no defects were observed in the as-deposited samples and samples annealed up to 600 °C.

3.3. RBS analysis on the Co–Ge samples

Fig. 6 shows the RBS spectra of the Co–Ge samples; as-deposited, annealed at 325, 425, 500 and 600 °C. From Fig. 6 it is shown that Co is diffusing into Ge from the low annealing temperature (325 °C). The Co is presumed to start diffusing into Ge at a temperature of 150 °C as reported by Sun et al [8]. Co atoms will diffuse into bulk Ge at a relatively low temperature of (~150 °C). The diffusion is dominant as annealing temperature increases to 500 °C. At 600 °C, Co has significantly diffused into Ge.

4. Summary

Pd- and Co-germanides were fabricated by resistive deposition and electron beam deposition followed by an annealing process. The electrical properties of the Pd Schottky contacts show that one phase of palladium germanide, PdGe was formed. CoGe, Co_5Ge_7 and $CoGe_2$ are the three cobalt germanides we propose to have formed during the Co Schottky contacts annealing process. Annealing studies of the Pd Schottky contacts reveal the introduction of a hole trap $H(0.33)$ at a temperature of 300 °C. This hole trap is probably Pd related as a similar hole trap was not observed during the annealing studies of EBD Co-Schottky contacts. DLTS analysis on the EBD Co-Schottky contacts has shown that an electron trap $E(0.37)$ and a hole trap $H(0.29)$ were induced during the fabrication of the contacts and a hole trap $H(0.30)$ is induced during the annealing process.

Acknowledgments

This work has been made possible by financial assistance from the South African National Research Foundation. The Laplace DLTS system software and hardware used in this research has been received from Dobaczewski (Institute of Physics Polish Academy of Science) and Peaker (Centre for Electronic Materials Devices and Nanostructures, University of Manchester).

References

[1] S. Gaudet, A.J. Kellock, P. Desjardins, C. Lavoie, J. Vac. Sci. Technol. A 24 (3) (2006) 474.
[2] V.I. Kolkovsky, M. Christian Petersen, A. Nylandsted Larsen, Appl. Phys. Lett. 90 (2006) 112110.
[3] F.D. Auret, W.E. Meyer, S. Coelho, M. Hayes, Appl. Phys. Lett. 88 (2006) 242110.
[4] D.V. Lang, J. Appl. Phys. 45 (1974) 3023.
[5] L. Dobaczewski, P. Kaczor, I.D. Hawkins, A.R. Peaker, J. Appl. Phys. 76 (1994) 194.
[6] L. Dobaczewski, A.R. Peaker, K.B. Nielsen, J. Appl. Phys. 96 (2004) 4689.
[7] C. Nyamhere, A. Chawanda, A.G.M. Das, F.D. Auret, M. Hayes, Physica B 401–402 (2007) 227.
[8] H.P. Sun, Y.B. Chen, X.Q. Pan, D.Z. Chi, R. Nath, Y.L. Foo, Appl. Phys. Lett. 86 (2005) 071904.
[9] F.D. Auret, S.M. M Coelho, M. Hayes, W.E. Meyer, J.M. Nel, Phys. Stat. Sol. (c) 5 (1) (2008) 160.
[10] C. Nyamhere, et al., Physica B (2009), doi:10.1016/j.physb.2009.09.037.

Journal of Alloys and Compounds 492 (2010) 649–655

Contents lists available at ScienceDirect

Journal of Alloys and Compounds

journal homepage: www.elsevier.com/locate/jallcom

Thermal annealing behaviour of platinum, nickel and titanium Schottky barrier diodes on n-Ge (1 0 0)

A. Chawanda[a,b,*], C. Nyamhere[a], F.D. Auret[a], W. Mtangi[a], M. Diale[a], J.M. Nel[a]

[a] Department of Physics, University of Pretoria, Pretoria 0002, South Africa
[b] Department of Physics, Midlands State University, Bag 9055, Gweru, Zimbabwe

ARTICLE INFO

Article history:
Received 26 August 2009
Received in revised form
25 November 2009
Accepted 28 November 2009
Available online 5 December 2009

Keywords:
Schottky contact
Germanium
Annealing
Ideality factor
Agglomeration

ABSTRACT

Platinum (Pt) and titanium (Ti) Schottky barrier diodes were fabricated on bulk grown (1 0 0) Sb-doped n-type germanium using the electron beam whereas nickel (Ni) contacts were fabricated using the resistive evaporation system. Electrical characterization of these contacts using current–voltage (*I–V*) measurements was performed under various annealing conditions. The variation of the electrical properties of these Schottky diodes can be attributed to combined effects of interfacial reaction and phase transformation during the annealing process. The results have also revealed that Pt Schottky contacts are of a high quality, with low reverse currents in the order of (10^{-5} to 10^{-6}) A and as-deposited ideality factors as low as 1.09. Furthermore, the samples microstructural characterization was performed by scanning electron microscopy (SEM) at different annealing temperatures. From the results, it can be concluded that the onset temperature in 30 nm Ni- and Pt/n-Ge (1 0 0) systems occurs at 500–600 °C and 600–700 °C, respectively.

1. Introduction

The solid phase reaction at sub-eutectic temperatures between a thin metal film and a single-crystal semiconductor has attracted much interest because of its importance in Schottky barrier and contact formation, epitaxial growth and device reliability [1]. A good metal-semiconductor (MS) contact is essential for the successful operation of the electronic circuits and devices [2]. Contacts to very large scale integration (VLSI) circuits and interconnections require MS contacts which are thermally stable, have low resistivity and are compatible with the process technology. Due to the shrinking of the advanced Si-based complementary metal-oxide-semiconductor (CMOS) device feature size, new material and device structures to relax the physical limitation in device scaling are now required. Ge has been regarded as the replacement for Si as a channel material in future high-speed CMOS technology, because it offers two times higher intrinsic electron mobility and four times higher intrinsic hole mobility than that of Si [3]. As the possibility of using Ge in microelectronics arises, optimal implementation of germanium technology will require an understanding of metal–germanium interactions from both metallurgical and electrical standpoints.

The reactions of germanium with Pt have been studied [1,4–8], while with Ni have been reported by [4,5,9–15] and with Ti have been investigated [5,16]. The study of the solid state reaction between thin metal films and germanium to determine the phase formation sequence [1,4–6,10–13,15], microstructure of the material [4,5,7,16], growth kinetics [10,15] and electrical characteristics were analyzed by x-ray diffraction [1,4–6,10–13,15,16], Rutherford Backscattering spectroscopy [1], transmission electron microscopy [4,7,10], differential scanning calorimetry [7,10] and current–voltage (*I–V*) [4,6,11,12,14,16], techniques. Yao et al. [4] studied the *I–V* characteristics of Pt/n-Ge (0 0 1) and Ni/n-Ge (0 0 1) after subjecting the Schottky contacts to rapid thermal anneal (RTA) in N_2 ambient at 250–700 °C for 20 s. Gumeniuk et al. [6] have reported the superconductivity in Pt germanides of new skutterditelike compounds MPt_4Ge_{12}. Łaszcz et al. [7] studied the mechanisms of the Pt germanide formation by RTA processes in the Ge/Pt/Ge/SiO_2 structure at 200–600 °C range. Their results depict that, during annealing of the Ge/Pt/Ge/SiO_2 structure at 200 °C the whole Pt layer had reacted with a part of the Ge layer and after 300 °C anneal the whole Ge reacted with Pt. Ohtsu et al. [8] investigated the reactions of the samarium platinum germanides ternary system using high-pressure techniques and a simple arc-melting method. Thanailakis et al. [9] established a relationship between as-deposited Ni/n-Ge (1 1 1) Schottky barrier height value, the metal work function and the density of surface states of the germanium substrate. Peng et al. [11] reported the Ni/n-Ge (1 0 0) Schottky diodes *I–V* characteristics and the nickel germanide induced strain

* Corresponding author at: Department of Physics, University of Pretoria, Pretoria 0002, South Africa. Tel.: +27 12 420 3508; fax: +27 12 362 5288.
E-mail address: albert.chawanda@up.ac.za (A. Chawanda).

0925-8388/$ – see front matter © 2009 Elsevier B.V. All rights reserved.
doi:10.1016/j.jallcom.2009.11.202

after subjecting the Schottky contacts to RTA in the temperature range 300–600 °C. Their results show that the orthorhombic structure of NiGe induces epitaxial tensile strain on Ge substrate due to the difference in the lattice constants. They also suggested that the barrier height increases with increasing annealing temperature may be due to the conduction band edge shift by the strain after germanidation process. An et al. [12] have investigated the impact of ion implantation on nickel germanides formation with pure-Ge substrate and electrical dependence of NiGe/Ge Schottky diodes on contact size. Their results reveal that ion implantation of BF_2 before germanidation is favourable for the formation of low-resistivity monogermanide phase (NiGe). They also showed that the Schottky barrier height of Ni/n-Ge (1 0 0) Schottky diodes formed on pure-Ge substrate decreased with decreasing contact size, while the ideality factor increased remarkably, which may provide the guideline for the application to Schottky source/drain germanium transistors [12]. Peng et al. [13] have carried out micro-Raman studies on nickel germanides formed on (1 1 0) crystalline Ge. From XRD analysis, they found that Ni_5Ge_3, NiGe, and Ni_2Ge phases are formed sequentially with increasing annealing temperatures from 300 °C to 600 °C on n-Ge (1 1 0) substrate. Their results also show a strong tensile stress in the underlying Ge (1 1 0) substrate, which was attributed to the lattice mismatch between nickel germanides and Ge substrate. An et al. [14] have also successfully demonstrated the modulation of Schottky barrier height of Ni/n-Ge (1 1 1) by a germanidation-induced dopant segregation technique. Their results showed that the change of the Schottky barrier height was not attributed to the phase change of nickel germanides but to dopant segregation at the interface of germanides/germanium which causes conduction energy band bending. Perrin et al. [15] have studied both systems (Ni–Si and Ni–Ge) in order to compare their phase formation and growth kinetics. Ni thin films and armorphous semiconductor layers (a-Si and a-Ge) had been deposited on undoped (1 0 0) Si wafers. They have showed that Ni–Si system has three major phases (Ni_2Si, NiSi and $NiSi_2$) that grow sequentially while Ni–Ge system showed only two phases (Ni_5Ge and NiGe) that grow simultaneously. Dedong et al. [16] studied changes in the electrical properties of Ti- and Ni germanide Schottky contacts on n-Ge (1 0 0) substrates in the temperature range 300–500 °C.

In this work we investigate the change in the electrical properties (I–V) of Pt-, Ni- and Ti Schottky contacts on n-Ge (1 0 0) at different annealing temperatures in the temperature range 25–600 °C. Results presented here are based on the effects of thermal annealing on the current–voltage characteristics of the metal Schottky contacts at different annealing temperatures, which may be attributed to combined effects of interfacial reaction and phase transformation [17], during the annealing process.

2. Experimental procedures

To study the thermal annealing effects on the Schottky contacts, we used bulk-grown (1 0 0) oriented, n-type Ge, doped with antimony (Sb) to a density of $(2–3) \times 10^{15}$ cm^{-3} supplied by Umicore. Before metallization, the samples were first degreased and subsequently etched in a mixture of H_2O_2 (30%):H_2O (1:5) for 1 min. Immediately after cleaning they were inserted into a vacuum chamber where 120 nm of AuSb (0.6% Sb), was deposited by resistive evaporation on their back surfaces as ohmic contacts. The samples were then annealed at 350 °C in Ar for ten minutes to minimize the ohmic contact resistivity [18]. Before Schottky contact deposition, the samples were again chemically cleaned as described above. Ni Schottky contacts were resistively deposited under vacuum below 10^{-6} Torr, while Pt and Ti Schottky contacts were electron beam deposited. The contacts were 0.6 mm in diameter and 30 nm thick. The metal layer thickness and deposition rates were monitored with an INFICON XTC 751-001-G1 quartz crystal thickness monitor. After contact fabrication, the samples were characterized by I–V measurements at room temperature to determine the quality of the diodes. The Schottky contacts were then isochronally annealed in an oven under Ar ambient in the temperature range 25–600 °C in steps of 25 °C for 30 min. I–V characteristic measurements followed each annealing cycle. Characterization of the films at different annealing temperatures was accomplished using a JEOL JSM-5800LV scanning electron microscopy (SEM) system operating at 5 kV.

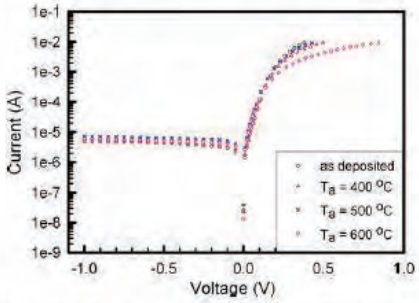


Fig. 1. Experimental forward and reverse I–V characteristics of one of the Pt/n-Ge (1 0 0) Schottky barrier diodes after isochronal thermal treatment for 30 min at different annealing temperatures: as-deposited, 400 °C, 500 °C and 600 °C.

3. Results and discussion

The barrier heights of the contacts were deduced from I–V characteristics, which were analyzed by the thermionic emission model given by the following equation [19,20]:

$$I(V) = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

where

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \quad (2)$$

is the saturation current obtained from the straight line intercept of ln$I$ at $V = 0$, A^* is the effective Richardson constant, A is the diode area, T the measurement temperature in Kelvin, k the Boltzmann constant, Φ_B is the zero bias effective Schottky barrier height (SBH), q is the electronic charge and n the ideality factor which can be determined accurately from the slope of the linear part of a ln$I$ versus V plot. Assuming pure thermionic emission, n can be obtained from Eq. (1) as

$$n = \frac{q}{kT}\frac{dV}{d(\ln(I))} \quad (3)$$

which is equal to unity for an ideal diode and usually has a value greater than unity.

We have fabricated eight Pt/-, Ni/- and Ti/n-Ge (1 0 0) Schottky barrier diodes (SBDs). Figs. 1–3 present the semilog forward and reverse bias I–V characteristics of these SBDs annealed in the 25–600 °C temperature range, together with those of as-deposited samples. The values of effective SBH were determined from the intercepts of the straight lines of the semilog-forward bias I–V characteristics with the help of Eq. (2). The effective SBHs and ideality

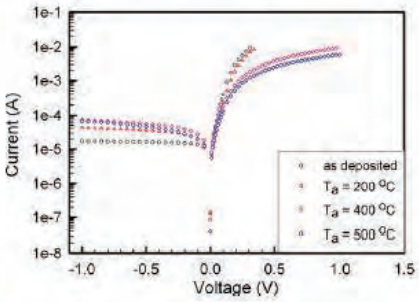


Fig. 2. Experimental forward and reverse I–V characteristics of one of the Ni/n-Ge (1 0 0) Schottky barrier diodes after isochronal thermal treatment for 30 min at different annealing temperatures: as-deposited, 200 °C, 400 °C and 500 °C.

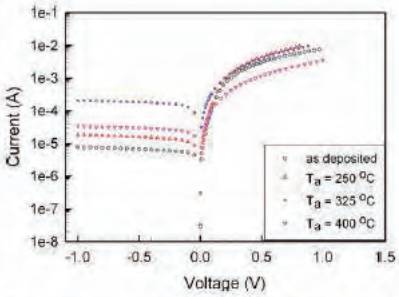


Fig. 3. Experimental forward and reverse *I–V* characteristics of one of the Ti/n-Ge (1 0 0) Schottky barrier diodes after isochronal thermal treatment for 30 min at different annealing temperatures: as-deposited, 250 °C, 325 °C and 400 °C.

factors vary from diode to diode; therefore it is common practice to take averages.

Fig. 4 shows the variation of the Schottky barrier height and reverse current at −1 V with annealing temperature for the Pt Schottky contacts. The SBH and reverse current at a bias voltage of −1 V for as-deposited Pt Schottky contacts were found to be (0.584 ± 0.005) eV and (5.46 ± 0.02) μA, respectively. The barrier height (BH) was approximately a constant within experimental error up to an annealing temperature of 350 °C. The BH then drops significantly, reaching (0.564 ± 0.005) eV after annealing at 500 °C. We suggest that there is a significant reaction between Pt and the Ge substrate. The change coincides with the initial phase formation of a germanide Ge_3Pt_2, which has been reported to form at 400 °C [1,4]. After annealing at 600 °C, the BH was found to increase to (577 ± 0.005) eV. The change in BH after the 500 °C anneal coincides with the temperature range of formation of a platinum germanide Ge_2Pt, reported by Grimaldi et al. [1] and Yao et al. [4] that forms after the 450 °C and 500 °C anneal, respectively. Throughout the annealing process the reverse current at −1 V remains in the same order of magnitude (10^{-5} to 10^{-6}) A.

Fig. 5 shows the variation of the Schottky barrier height and reverse current at −1 V with annealing temperature for the Ni Schottky contacts. The as-deposited SBH and reverse current at −1 V for Ni Schottky contacts were found to be (0.532 ± 0.005) eV and (29.20 ± 0.02) μA, respectively. The BH remains almost constant within experimental error in the tem-

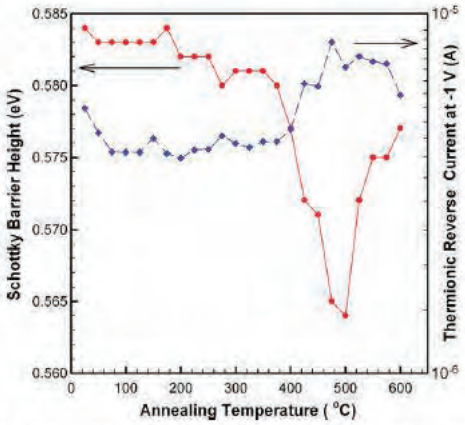


Fig. 4. Plot of the Schottky barrier height and the reverse current at −1 V as a function of annealing temperature for Pt Schottky contacts on n-Ge (1 0 0).

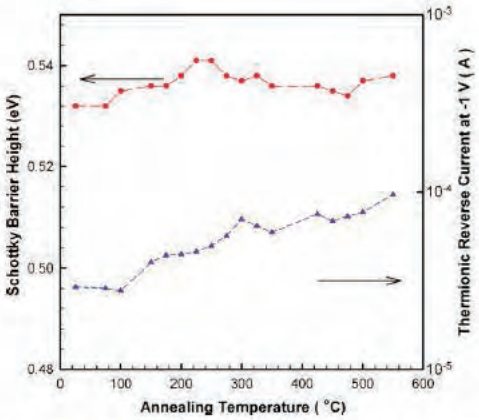


Fig. 5. Plot of the Schottky barrier height and the reverse current at −1 V as a function of annealing temperature for Ni Schottky contacts on n-Ge (1 0 0).

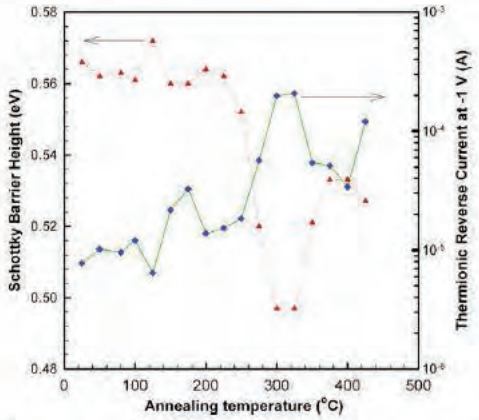


Fig. 6. Plot of the Schottky barrier height and the reverse current at −1 V as a function of annealing temperature for Ti Schottky contacts on n-Ge (1 0 0).

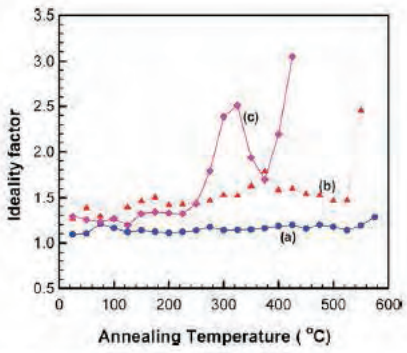


Fig. 7. Plot of Ideality factor as a function of annealing temperature for: (a) Pt Schottky contacts on n-Ge (1 0 0); (b) Ni Schottky contacts on n-Ge (1 0 0) and (c) Ti Schottky contacts on n-Ge (1 0 0).

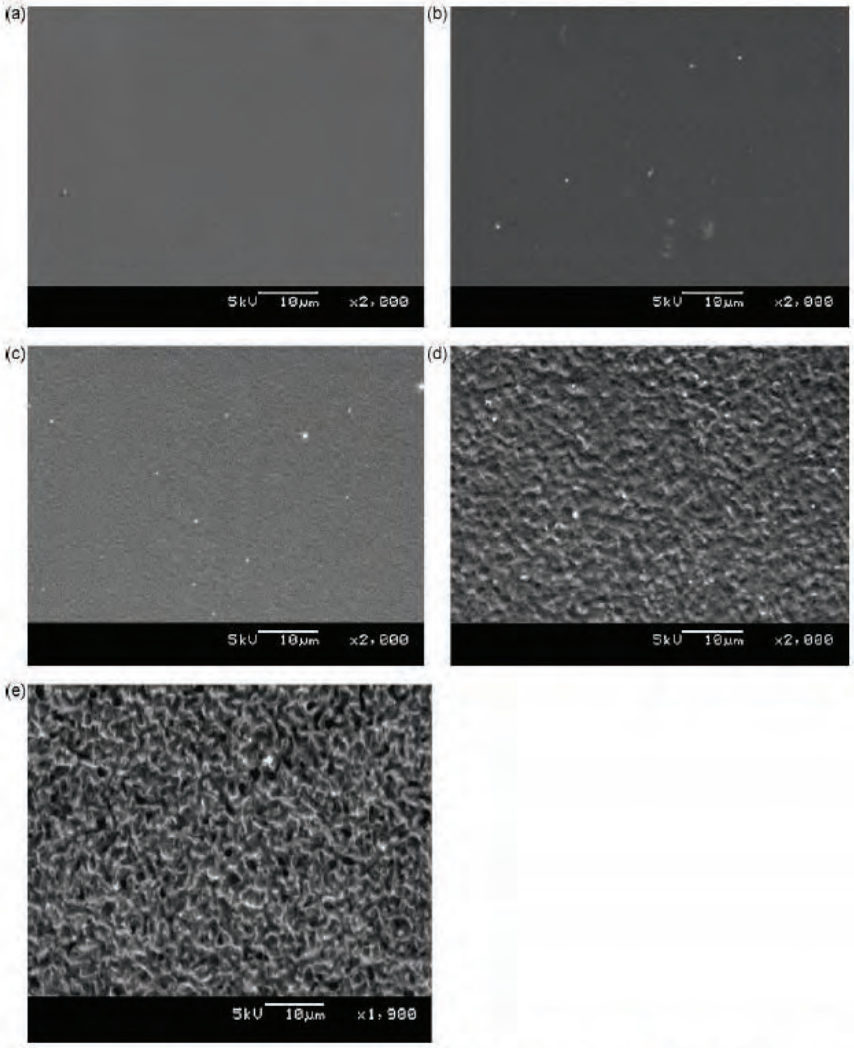


Fig. 8. SEM observation for Pt films deposited on germanium after isochronal thermal treat for 30 min at different annealing temperatures: (a) as-deposited, (b) 400 °C, (c) 500 °C, (d) 600 °C, (e) 700 °C.

perature range 100–525 °C. The near constant barrier height with annealing temperature in the Ni Schottky contacts may be attributed to the strong Fermi level pinning effect between Ni-germanide/n-Ge (1 0 0) substrates [16]. Studies by Gaudet et al. [5], Peng et al. [11] and An et al. [12] revealed the existence of only one germanide phase, NiGe for Ni in this temperature range.

The as-deposited SBH and reverse current at −1 V for Ti Schottky contacts were found to be (0.566 ± 0.005) eV and (7.76 ± 0.02) μA, respectively. Variation of barrier height and reverse current at a bias voltage of −1 V with annealing temperature for Ti Schottky contacts is shown in Fig. 6. The BH was approximately constant within experimental error up to an annealing temperature of 225 °C. After further annealing at higher temperatures the BH decreased, reaching a minimum value of (0.497 ± 0.005) eV at 300 °C. This change in BH could be associated with the phase formation of a germanide Ti_6Ge_5, which has been reported to form at 300 °C [16]. The subsequent increase in barrier height after annealing at temperatures higher than 300 °C coincides with the temperature range for the formation of the Ti_5Ge_3 germanide [16]. After a 425 °C anneal, *I–V* characteristics of the Ti Schottky contacts severely deteriorated, and the contacts became near-ohmic. Even after subjecting the Ti Schottky contacts to a temperature of 20 K, they showed no improvement in their rectifying behaviour.

It is well known that the interface states and chemical reactions between metals and semiconductors at interfaces can play an important role in the electrical properties of devices [17]. During the annealing process, metals may react with semiconductors and new compounds would form. Hence, the change of barrier heights may be attributed to the combined effects of interfacial reaction and phase transformation [17]. Furthermore, the barrier height change in Schottky contacts can be explained according to the effective work function (EWF) model [21], where the BH value is determined by the work function of microclusters of one or more phases resulting from either oxygen contamination or metal–semiconductor

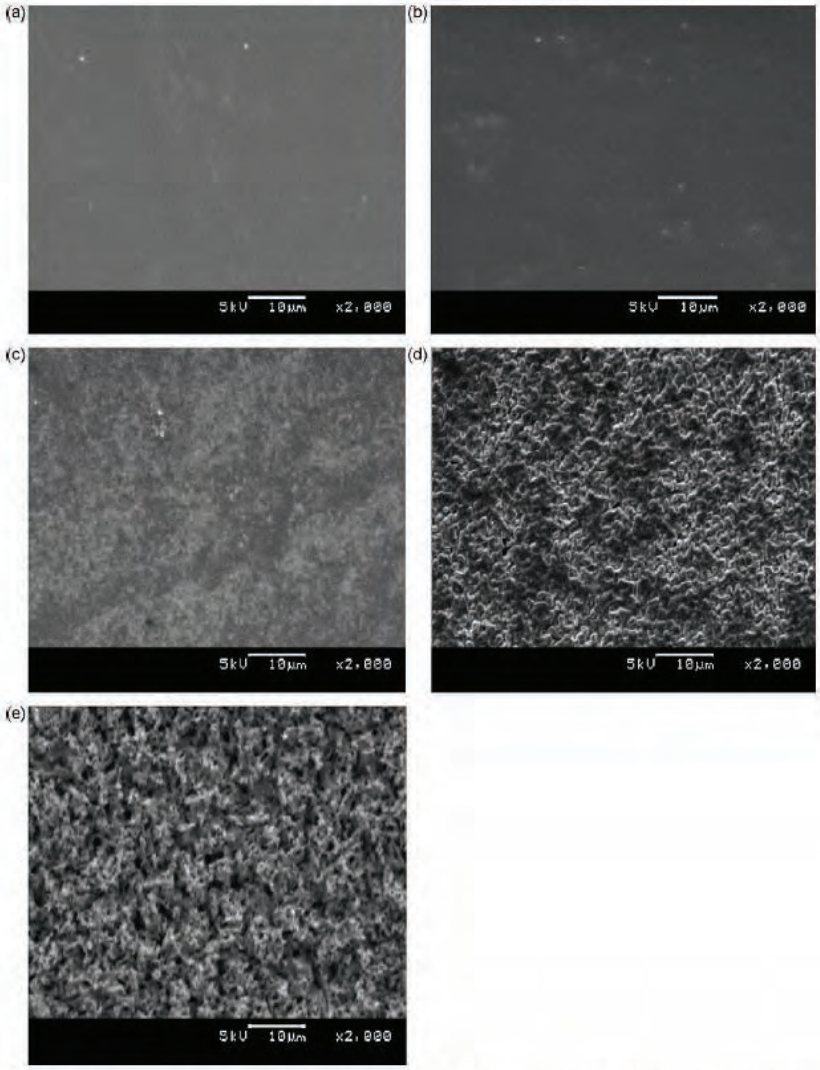


Fig. 9. SEM observation for Ni films deposited on germanium after isochronal thermal treat for 30 min at different annealing temperatures: (a) as-deposited, (b) 400 °C, (c) 500 °C, (d) 600 °C, (e) 700 °C.

reactions which occur during metallization and annealing, and each phase having its own effective work function [22].

The ideality factor was calculated from the gradient of the linear region of the experimental ln *I–V* characteristics in forward bias [2]. The variation of the Pt Schottky contacts ideality factor is shown in Fig. 7(a). The ideality factor was found to be between 1.09 and 1.30. Fig. 7(a) shows that the ideality factor is almost constant, 1.09 up to a temperature of 575 °C. It then increases to 1.30 after annealing at 600 °C.

Fig. 7(b) shows the variation of ideality factor with annealing temperature for the Ni Schottky contacts. The ideality factors were between 1.27 and 1.47 at annealing temperatures between 25 °C and 525 °C. The variation of ideality factor with annealing temperature for Ti Schottky contacts is shown in Fig. 7(c). The ideality factors were between 1.29 and 3.05 at annealing temperatures between 25 °C and 425 °C. In the case of Ni and Ti Schottky contacts, ideality factors significantly greater than 1.0 indicate that the transport properties are not well modeled by thermionic emission alone although their contacts remain rectifying [23]. Therefore, the SBH is merely a curve fitting parameter for these contacts and is not representing the true BH. The non-idealities are mostly due to the states associated with the defects near the surface of the semiconductor [2]. In a Schottky contact, even with a good surface treatment, there is an interfacial oxide layer of thickness about 1 nm with a considerable amount of surface states [2]. Interface states, inter-diffusion, chemical reaction, compound formation, defects generation, etc. can all be derived from thermodynamics due to thermal annealing [24–26]. These may lead to recombination centres [23] and SBH

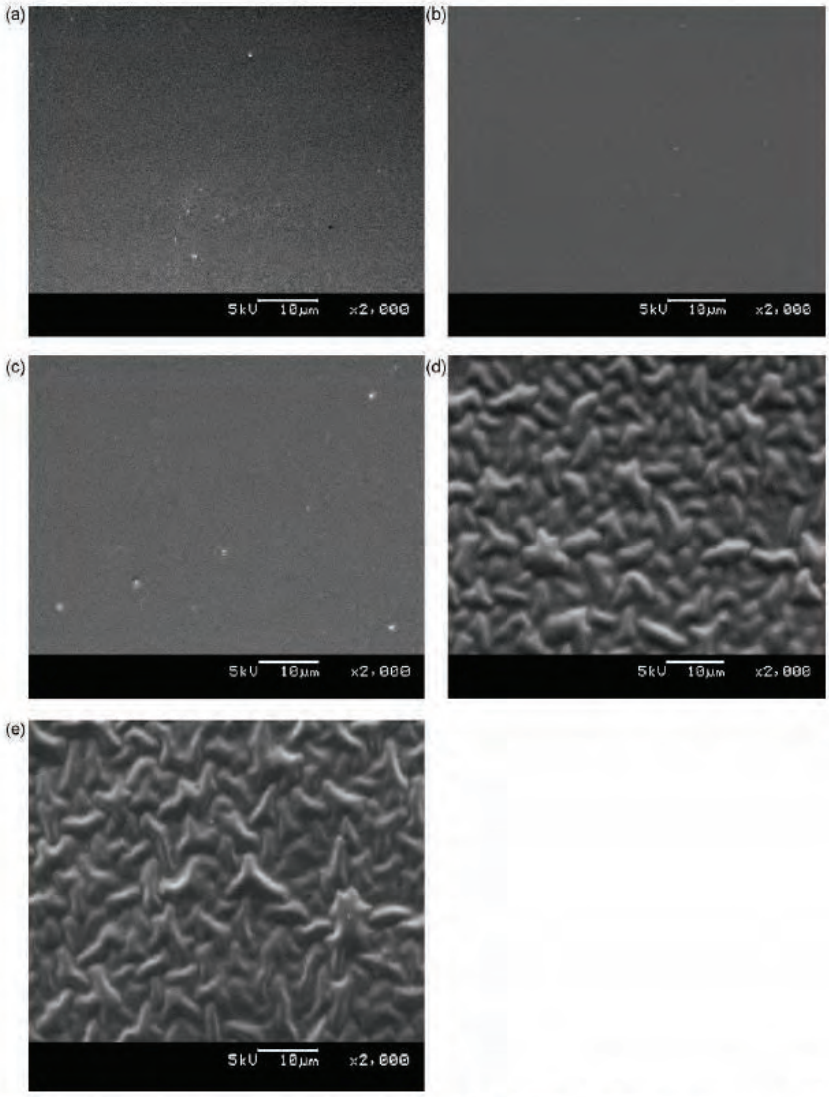


Fig. 10. SEM observation for Ti films deposited on germanium after isochronal thermal treat for 30 min at different annealing temperatures: (a) as-deposited, (b) 500 °C, (c) 600 °C, (d) 700 °C, (e) 800 °C.

inhomogeneities [27], which cause a flow of excess current leading to a deviation from the ideal thermionic emission behaviour at low voltages and temperatures.

Scanning electron microscopy (SEM) observations were conducted for Pt-, Ni- and Ti/n-Ge (1 0 0) samples, as-deposited and annealed at different temperatures. Results are shown in Figs. 8–10. The morphological evolution of Pt/n-Ge (1 0 0) is shown in Fig. 8. As seen in Fig. 8(a), (b) and (c), metal surfaces show little change when samples were annealed below 600 °C. This is in agreement with what was reported by Yao et al. [4]. The Pt-germanide exhibited no sign of agglomeration even up to 500 °C anneal, suggesting better morphological stability for Pt-germanide films [4]. At 600 °C, anneal and above (see Fig. 8(d–e)), the surface becomes rough, indicating the agglomeration of Pt, finally destroying the contact, as evidenced by the loss of rectifying properties of the Pt Schottky contacts after 625 °C anneal. From the results, it can be concluded that the onset temperature in the 30-nm Pt/Ge (1 0 0) system occurs at 600–700 °C.

Fig. 9 shows the evolution of surface morphology for Ni/n-Ge (1 0 0) with annealing temperatures. Although Zhang et al. [28] and Lee et al. [29] have reported grain growth and groove deepening at the surface at 400 °C for Ni film thickness of 15 nm, with Yao et al. [4] reporting the development of severe grain boundary grooving after 500 °C anneal (onset temperature for 15 nm Ni film agglomeration), prominent grain growth at the surface (see Fig. 9(c)) were evident up to 500 °C, indicating inception of agglomeration. Agglomeration starts with grain boundary grooving and progresses to island formation [29]. After a 600 °C anneal, we

observed development of severe grain grooving. The temperature at which grain growth and agglomeration occurs decreases with reduced film thickness [28]. This is consistent with the grooving model for agglomeration [28], as in our study the metal film thickness was 30 nm. We also observed that after 700 °C (see Fig. 9 (e)), film continuity was severely interrupted as indicated by the dark spots caused by exposed Ge regions. The agglomeration is driven by the minimization of the total surface/interface energy of the metal-germanide and germanium substrate [30]. We found the onset of the agglomeration process for 30 nm Ni/Ge (1 0 0) system to be in 500–600 °C.

Fig. 10 shows the SEM images of Ti/n-Ge (1 0 0) films at different annealing temperatures. Although Ti/Schottky contacts lost their rectifying behaviour after 425 °C anneal, the metal surface shows no change when the sample was annealed below 600 °C. Grain growth and grove deepening at the surface were evident up to 700 °C, suggesting better morphological stability.

4. Conclusions

Ni Schottky contacts were fabricated by resistive deposition. Pt and Ti Schottky contacts were fabricated by electron beam deposition. The Schottky contacts behaviour was investigated under various annealing conditions. SEM observations were conducted for samples annealed at different temperatures. The variation of Schottky barrier heights and ideality factors with annealing temperature may be attributed to interfacial reactions of metals (Pt, Ni, Ti) with germanium and the phase transformation of the metal-germanides during annealing. Ni and Ti show initial stages of reaction with Ge after annealing at 100 °C and 225 °C, respectively. The electrical properties of the metal Schottky contacts reveal that Pt Schottky contacts are of high quality with low reverse currents at −1 V of the order (10^{-5} to 10^{-6}) A and ideality factors as low as 1.09. The as-deposited BHs near the bandgap of Ge in the Pt/-, Ni/- and Ti/n-Ge (1 0 0) Schottky contacts imply good Schottky source/drain contact materials in p-channel Ge-MOSFETS, for the hole injection from source into inverted p-channel [4]. From SEM observations, it can be concluded that the onset temperature in 30 nm Ni- and Pt/n-Ge (1 0 0) systems occurs at 500–600 °C and 600–700 °C, respectively.

Acknowledgements

This work has been made possible by financial assistance from the South African National Research Foundation. The authors gratefully acknowledge SEM observation measurements by Helena Steyn.

References

[1] M.G. Grimaldi, L. Wieluński, M.-A. Nicolet, Thin Solid Films 81 (1981) 207.
[2] A.R. Saha, S. Chattopadhyay, C.K. Maiti, Mater. Sci. Eng. B 114–115 (2004) 218.
[3] R. Li, H.B. Yao, S.J. Lee, D.Z. Chi, M.B. Yu, G.Q. Lo, D.L. Kwong, Thin Solid Films 504 (2006) 28.
[4] H.B. Yao, C.C. Tan, S.L. Liew, C.T. Chua, C.K. Chua, R. Li, R.T.P. Lee, S.J. Lee, D.Z. Chi, International Workshop on Junction Technology Proceeding, 2006, p. 164.
[5] S. Gaudet, C. Detavernier, A.J. Kellock, P. Desjardins, C. Lavoie, J. Vac. Sci. Technol. A 24 (3) (2006) 474.
[6] R. Gumeniuk, W. Schnelle, H. Rosner, M. Nicklas, A. Leithe-Jasper, Yu Grin, Phys. Rev. Lett. 100 (2008) 0170021.
[7] A. Łaszcz, J. Ratajczak, A. Czerwinski, J. Kątcki, V. Srot, F. Phillipp, P.A. van Aken, N. Breil, G. Larrieu, E. Dubois, Mater. Sci. Eng. B 154–155 (2008) 175.
[8] F. Ohtsu, H. Fukuoka, S. Yamanaka, J. Alloys Compd. (2009), doi:10.1016/j.jallcom.2009.08.052.
[9] A. Thanaillakis, D.C. Northrop, Solid State Electron. 16 (1973) 1383.
[10] F. Nemouchi, D. Mangelinck, J.L. Lábár, M. Putero, C. Bergman, P. Gas, Microelectron. Eng 83 (2006) 2101.
[11] C.-Y. Peng, Y.-H. Yang, C.-M. Lin, Y.-J. Yang, C.-F. Huang, C.W. Liu, International Conference on Solid-State and Integrated Circuits Technology Proceedings (ICSICT), art. no. 4734645 (2008) 681.
[12] X. An, C. Fan, R. Huang, X. Zhang, Proceedings – Electrochemical Society, PV 1, 2008, p. 406.
[13] C.-Y. Peng, C.-F. Huang, Y.-J. Yang, C.W. Liu, ECS Trans. 16 (2008) 249.
[14] X. An, C. Fan, R. Huang, X. Zhang, Chin. Phys. Lett. 26 (2009) 0873041.
[15] C. Perrin, D. Mangelinck, F. Nemouchi, J. Labar, C. Lavoie, C. Bergman, P. Gas, Mater. Sci. Eng. B 154–155 (2008) 163.
[16] Dedong Han, Xin Wang, Yi Wang, Dayu Tian, Wei Wang, Xiaoyan Liu, Jinfeng Kang, Ruqi Han, Microelectron. Eng. 82 (2005) 93.
[17] Y. Sun, X.M. Shen, J. Wang, D.G. Zhao, G. Feng, Y. Fu, S.M. Zhang, Z.H. Zhang, Z.H. Feng, Y.X. Bai, H. Yang, J. Phys. D: Appl. Phys. 35 (2002) 2648.
[18] F.D. Auret, P.J. Janse van Rensburg, M. Hayes, J.M. Nel, S. Coelho, W.E. Meyer, S. Decoster, V. Matias, A. Vantomme, D. Smeets, Nucl. Instrum. Methpds B 257 (2007) 169.
[19] S.M. Sze, Physics of Semiconductor Devices, New York, 1981, p. 245.
[20] Baojun Li, Soo-Jin Chua, Yakovlev Nikolai, Lianshan Wang, Eng-Kee Sia, Solid State Electron. 47 (2003) 602.
[21] J.L. Freeouf, J.M. Woodall, Appl. Phys. Lett. 29 (1976) 263.
[22] E. Ayyıldız, A. Türût, Solid State Electron. 43 (1999) 521.
[23] H. Doğan, N. Yıldırım, A. Turut, Microelectron. Eng. 85 (2008) 655.
[24] T. Sands, Appl. Phys. Lett. 52 (1988) 197.
[25] S.K. Cheung, N.W. Cheung, Appl. Phys. Lett. 49 (1986) 85.
[26] J.L. Everaet, R.L. Van Meirhaeghe, W.H. Laflére, F. Cardon, Semicond. Sci. Technol. 5 (1990) 60.
[27] R.T. Tung, J.P. Sullivan, F. Schrey, Mater. Sci. Eng. B 14 (1992) 266.
[28] Q. Zhang, N.W. Wu, T. Osipowicz, L.K. Bera, C. Zhu, Jpn. J. Appl. Phys. 44 (2005) L1389.
[29] K.Y. Lee, S.L. Liew, S.J. Chua, D.Z. Chi, H.P. Sun, X.Q. Pan, Mater. Res. Symp. 810 (2004) 55.
[30] J.P. Gambino, E.G. Colgan, Mater. Chem. Phys. 52 (1998) 99.

WILEY InterScience® DISCOVER SOMETHING GREAT

Early View publication on www.interscience.wiley.com
(issue and page numbers not yet assigned;
citable using Digital Object Identifier – **DOI**)

Phys. Status Solidi C, 1–4 (2010) / **DOI** 10.1002/pssc.200982404

physica status solidi c
www.pss-c.com
current topics in solid state physics

Comparison of metal Schottky contacts on n-Ge (100) at different annealing temperatures

A. Chawanda[*,1,2], **C. Nyamhere**[2], **F. D Auret**[2], **W. Mtangi**[2], **M. Diale**[2], **and J. M. Nel**[2]

[1] Department of Physics, Midlands State University, Bag 9055, Gweru, Zimbabwe
[2] Department of Physics, University of Pretoria, Pretoria 0002, South Africa

Received 22 June 2009, revised 16 October 2009, accepted 4 December 2009
Published online 26 January 2010

PACS 68.60.Dv, 73.30.+y, 81.15.Ef, 81.40.Ef

* Corresponding author: e-mail albert.chawanda@up.ac.za, Phone: +27 12 420 3508, Fax: +27 12 362 5288.

Platinum (Pt), nickel (Ni), palladium (Pd) and cobalt (Co) Schottky barrier diodes were fabricated by vacuum resistive evaporation or electron beam deposition. We have studied the electrical characteristics of platinum, nickel, palladium and cobalt Schottky contacts on bulk grown (100) Sb-doped n-type germanium under various annealing conditions by current – voltage (*I-V*) measurements. The Schottky behaviour of the metal contacts with annealing temperatures is compared. Results obtained from the electrical properties of the Schottky contacts have revealed that Pt contacts are highly thermally stable over a wide range of temperature compared to Pd, Ni and Co contacts. Furthermore, Pt Schottky contacts are of highest quality, with low reverse currents of the order (10^{-6}- 10^{-5} A) and as-deposited ideality factor as low as 1.09, compared to Pd, Ni, and Co Schottky contacts.

1 Introduction Thin film reactions of metal on semiconductor have been of interest for the past 30 years for their applications in microelectronic devices [1]. In the manufacturing of semiconductor devices, metal contacts have always played a pivotal role, especially in MOSFET and CMOS devices. A good metal-semiconductor (MS) contact is essential for the successful operation of the electronic circuits and devices [2]. Contacts to very large scale integration (VLSI) circuits require MS contacts, which are thermally stable, have low resistivity and are compatible with the process technology. Schottky contacts play an important role in controlling the electrical performances of semiconductor devices [2]. The attempts to develop faster devices in modern microelectronics have increased the interest for alternative materials to silicon, compatible with the existing silicon-based technology [3]. Germanium (Ge) has been regarded as the replacement for silicon due to its high carrier mobility, low effective mass of holes [4] and relative compatibility with silicon processing. This has led to renewed interest in the complete understanding of metal-germanium interactions and electronic properties of radiation and process-induced defects in Ge.

The reactions of germanium with Pt[5,6,7], Ni [8,9,10,11,12], Pd [6,9,13,14,15] and Co [9,13,16,17] have also been investigated previously. Study of the solid state reaction between the metal films and germanium to determine the phase formation sequence [5,9,11,13,15,17], microstructure of material [9,10,12], growth kinetics[11,16] and electrical characteristics [9,10,12],were analyzed by x-ray diffraction, Rutherford backscattering spectroscopy, transmission electron microscopy, differential calorimetry and current-voltage (*I-V*) techniques respectively. Thanailakis *et al.* [8] established a relationship between as-deposited Pd/n-Ge (111) and Ni/n-Ge (111) Schottky barrier height values, the metal work functions and the density of surface states of germanium substrate. Yao *et al.* [10] studied the *I-V* characteristics of Pt/n-Ge (001) and Ni/n-Ge (001) after subjecting the Schottky contacts to rapid thermal anneal (RTA) in N_2 ambient in the temperature range 250-700 °C for 20 s. Han *et al.* [12] has reported the changes in the electrical properties of Ni germanide Schottky contacts on n-Ge (100) in the temperature range 300-500 °C.

The aim of this paper is to report the change in the electrical properties and give a comparative study of ther-

physica status solidi c

mal stability of the Pt, Ni, Pd and Co Schottky contacts on n-Ge (100), in the temperature range 25-600 °C. Results presented here are based on the thermal annealing effects on the *I-V* characteristics of the Pt, Ni, Pd and Co Schottky contacts, which may be attributed to combined effects of interfacial reaction and phase transition [18], during the annealing process.

2 Experimental procedures Bulk-grown, (100) oriented, n-type Ge samples, doped with antimony, (Sb) to a density of (2-3) x 10^{15} cm^{-3} supplied by Umicore, were degreased in successive trichloroethylene, acetone and methanol ultrasonic baths and subsequently etched in a mixture of H_2O_2 30%: H_2O (1:5) for 1 minute. Immediately after cleaning they were inserted into a vacuum chamber where AuSb (0.6% Sb), 120 nm thick, was deposited by resistive evaporation on their back surfaces as ohmic contacts. The samples were then annealed at 350 °C in Ar for 10 minutes to minimize the contact resistivity of the ohmic contacts [19]. Before Schottky contact deposition, the samples were again chemically cleaned as described above. Ni and Pd Schottky contacts were deposited by vacuum resistive evaporation and the Pt and Co Schottky contacts were deposited by electron beam deposition. The vacuum was maintained at below 1×10^{-6} Torr during the depositions. These Schottky contacts were deposited through a mechanical mask resulting in an array of 0.6 mm diameter contacts. After the contacts fabrication the samples were characterized by current-voltage (*I-V*) measurements at room temperature to determine the quality of the diodes. The Schottky contacts were then isochronally annealed in an oven under Ar gas from 25 °C to 600 °C in steps of 25 °C for 30 min. *I-V* measurements followed each annealing cycle.

3 Results and discussion The *I-V* characteristics are widely used to study the performance of the Schottky contacts since they offer many important device parameters. The barrier heights of the contacts were deduced from *I-V* characteristics which were analyzed by using the thermionic emission model given by the following equation [20,21]:

$$I(V) = A^{*}AT^{2}\exp(-q\Phi_{B}/kT)[\exp(qV/nkT)-1] \quad (1)$$

where A^{*} is the effective Richardson constant, A is the diode cross-sectional area, T the measurement temperature, k the Boltzmann constant, Φ_B the Schottky barrier height (SBH), and n the ideality factor which can be determined accurately from the linear part of the forward bias ln I versus V plot, and assuming pure thermionic emission can be obtained as:

$$n = \frac{q}{kT}\frac{dV}{d(\ln(I))} \quad (2)$$

The SBH values were determined using the intercepts of the straight lines of semi log-forward bias *I-V* characteristics with help of equation

$$\Phi_B = \frac{kT}{q}\ln\left(\frac{A^{*}AT^{2}}{I_0}\right) \quad (3)$$

Table 1 Electrical parameters for as-deposited Pt, Pd, Ni and Co Schottky contacts on n-Ge (100).

metal	Work function (eV)[a]	SBH (eV)	Ideality factor	Reverse current density at −1V(A/cm^2)
Pt	5.65	0.584±0.005	1.09±0.02	1.93 x 10^{-3}
Pd	5.12	0.540±0.005	1.15±0.02	6.00 x 10^{-3}
Ni	5.15	0.532±0.005	1.27±0.02	10.30 x 10^{-3}
Co	5.00	0.513±0.005	1.41±0.02	32.4 x 10^{-3}

[a]Ref. [22,23,24,25],which give the currently accepted values of the work functions for the metals, Pt, Pd, Ni and Co.

Figure 1 shows a linear correlation of the as-deposited SBH values and work functions for the metals Pt, Pd, Ni and Co, cornfirming the Effective Work Function model.

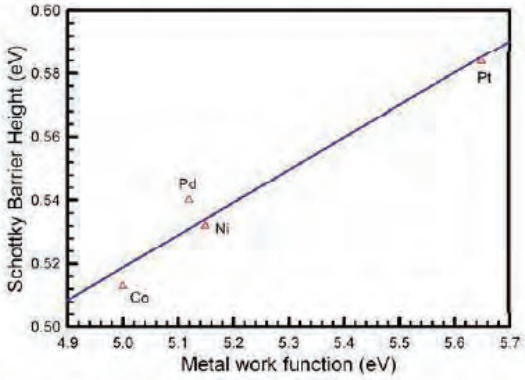


Figure 1 Plot of the as-deposited Schottky barrier heights against published values of metals Pt, Pd, Ni and Co work function.

From Table 1 we see that the as-deposited electrical parameters for Pt and Pd Schottky contacts reveal relatively better quality compared to the Schottky contacts of Ni and Co. It has been shown that the electrical properties and stability of semiconductor devices are strongly influenced by contaminants inadvertently introduced during the many processing steps involved during device fabrication [26]. It is also known that the interface states and chemical reactions between metals and semiconductors at interface also play an important role in the electrical properties of devices.

Figure 2 shows the variation of the Schottky barrier height with annealing temperature. The as-deposited Pt Schottky contacts barrier height is the highest due to the

Contributed Article

fact that its work function (Table 1) is significantly higher than that of other metals investigated here. Although four Pt germanide phases are reported to form during annealing between 25-600 °C [5], Fig. 2 and Fig. 3 depict that Pt contact electrical parameters are approximately constant up to 350 °C. The change coincides with the initial phase formation of a germanide Ge_3Pt_2, reported by Grimaldi *et al.* [5] and Yao *et al.* [10] to form at an annealing temperature of 400 °C. The Pt SBH then increases to 0.578 ± 0.005 eV after annealing the sample at a temperature of 600 °C. The SBH change after a 500 °C anneal coincides with the temperature range of formation of a platinum germanide Ge_2Pt, reported to form after a 450 °C anneal [5,9,10].

The variation in the electrical parameters of Co Schottky contacts (Fig. 2 and Fig. 3) coincide with the temperature ranges of Co germanide phases formed by annealing as reported by Hsieh *et al.* [7] and Sun *et al.* [27], CoGe forming between 100-300 °C, Co_5Ge_7 forming around 300 °C and $CoGe_2$ forming at temperatures above 425 °C. The variation of Ni and Pd Schottky contacts barrier height between 100-525 °C annealing temperatures is approximately constant within experimental error of ±5 %. According to Gaudet *et al* [9], only one germanide phase exists for both Ni (NiGe) and Pd (PdGe) in this temperature range.

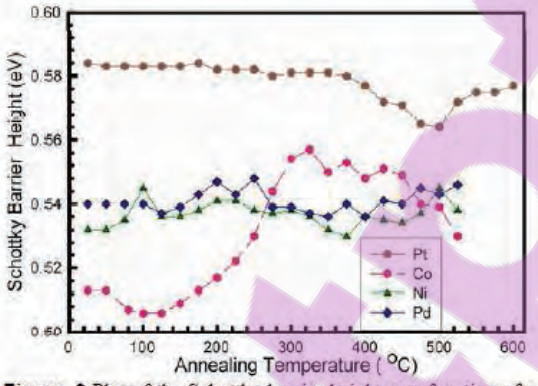


Figure 2 Plot of the Schottky barrier height as a function of annealing temperature for Co, Ni, Pd and Pt Schottky contacts on n-Ge (100).

During the annealing process, metals may react with germanium, forming new compounds. The change of barrier heights may be attributed to the combined effects of interfacial reaction and phase transition [18]. The SBH is also temperature dependent, due to the fact that the measured current across a Schottky junction is a combination of thermionic emission and recombination currents [2]. Furthermore, the barrier height change in Schottky contacts can be explained according to the effective work function (EWF) model [28], where the value of barrier height is determined by the work function of microclusturs of one or more phases resulting from either oxygen contamination or metal-semiconductor reactions which would occur during metallization and annealing, each phase having its own effective work function [29].

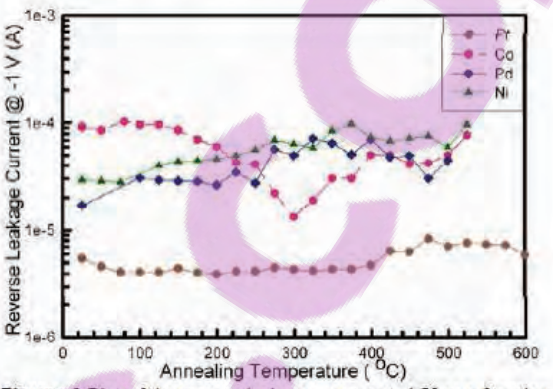


Figure 3 Plot of the reverse leakage current at -1 V as a function of annealing temperature for Pt, Pd, Ni and Co Schottky contacts on n-Ge (100).

Figure 3 shows the variation of reverse leakage current at -1 V with annealing temperature for the Pt, Pd, Ni and Co Schottky contacts. Throughout annealing process the reverse leakage current at -1 V for Pt Schottky contacts was the lowest, in the range (10^{-6}-10^{-5}) A. The variation of the Pt electrical properties during the annealing process reveal that, Pt Schottky contacts are highly thermally stable over a wide range of temperature, as after 525 °C anneal the Pd, Ni and Co Schottky contacts lost their rectifying behaviour.

The ideality factor was calculated from the gradient of the linear region of the experimental ln (I) - V characteristics in forward bias [2]. The variation of the Pt, Ni, Pd and Co Schottky contacts ideality factor with annealing temperature is shown in Fig. 4. The Pt Schottky contacts ideality factor was found to be between 1.09 and 1.19, in the temperature range 25-550 °C. It then increased after 575 °C anneal. The ideality factors for Ni, Pd and Co are found to be greater than 1.1, indicating that the transport properties are not well modeled by thermionic emission alone although their contacts remain rectifying [30]. The deviation from ideality is mostly due to the states associated with the defects near surface of the semiconductor [2]. These interface states, and inter-diffusion, chemical reaction, compound formation, defects generation, etc. can all be derived by thermodynamics due to thermal annealing [31,32,33], may lead to recombination centers [30] and Schottky barrier inhomogeneities [34], giving rise to excess current, which causes deviation from the ideal thermionic emission behaviour at low voltages and temperature.

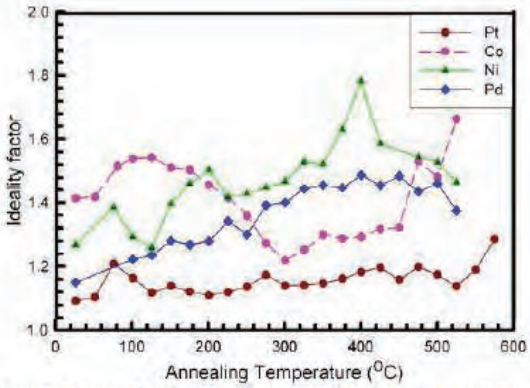


Figure 4 Plot of the Ideality factor as a function of annealing temperature for Pt, Pd, Ni and Co Schottky contacts on n-Ge (100).

4 Summary Ni and Pd Schottky contacts were fabricated by resistive deposition. Pt and Co Schottky contacts were fabricated by electron beam deposition. These Schottky contacts electrical properties were investigated under various annealing conditions and results compared. The variation of barrier heights and ideality factors with different annealing temperatures may be attributed to interfacial reactions of metals (Pt, Ni, Pd and Co) with germanium and phase transition of the metal-germanides during annealing. The results show that Pt Schottky contacts are highly thermally stable over a wide range of temperature compared to the Ni, Co and Pd Schottky contacts, and Pt Schottky contacts have best quality with lowest reverse leakage currents of the order (10^{-5}-10^{-6}) and as deposited ideality factors as low as 1.09.

Acknowledgements This work has been made possible by financial assistance from the South African National Research Foundation.

References

[1] F. Nemouch, D. Mangelinck, J.L LáBár, M. Putero, C. Bergma, and P. Gas, Microelectron. Eng. **83**, 2101-2106 (2006).
[2] A.R. Saha, S. Chattopadhyay, C.K. Maiti, Mater. Sci. Eng. B **114/115**, 218 (2004).
[3] V.I. Kolkovsky, M. C. Petersen, and A. N. Larsen, Appl. Phys. Lett. **90**, 112110 (2006).
[4] R. Hull and J. C. Bean (Eds.), Germanium Silicon: Physics and Materials, Semiconductors and Semi-metals, Vol. 56 (Academic, San Diego, 1999).
[5] M.G. Grimaldi, L. Weiluński, and M. A. Nicolet, Thin Solid Films **81**, 207 (1981).
[6] E.D. Marshall, C.S. Wu, C.S. Pai, D.M. Scott, and S.S. Lau, Thin Films: The Relationship of Structure to Properties, MRS Symposia Proceeding (Material Research Society, Pittsburg, PA, 1985), pp. 161-166.
[7] Y.F. Hsieh and L.J. Chen, J. Appl. Phys. **63**, 1177 (1988).
[8] A. Thanailakis and D.C. Nortrop, Solid-State Electron. **16**, 1383 (1973).
[9] S. Gaudet et al., J. Vac. Sci. Technol. A **24**(3), 474 (2006).
[10] H.B. Yao, C.C. Tan, S.L. Liew, C.T. Chua, C.K. Chua, R. Li, R.T.P. Lee, S.J. Lee, and D.Z. Chi, Proc. International Workshop on Junction Technology (2006), p. 164.
[11] F. Nemouchi, D. Mangelinck, J.L. Lábár, M. Petero, C. Bergman, and P. Gas, Microelectron. Eng. **83**, 2101 (2006).
[12] D. Han, X. Wang, Y. Wang, D. Tian, W. Wang, X. Liu, J. Kang, and R. Han, Microelectron. Eng. **82**, 93 (2005).
[13] M. Wittmer, M.A. Nicolet, and J.W. Mayer, Thin Solid Films **42**, 51 (1977).
[14] G. Ottaviani, C. Canali, G. Ferrari, G. Majni, M. Prudenziati, and S.S. Lau, Thin Solid Films **47**, 187 (1977).
[15] Y.F. Hsieh and L.J. Chen, Thin Solid Films **162**, 295 (1988).
[16] Y.F. Hsieh, L.J. Chen, L.J. Marshall, and S.S. Lau, Appl. Phys. Lett. **51**, 1588 (1987).
[17] S.P. Ashburn, M.C. Öztürk, G. Harris, and D.M. Maher, J. Appl. Phys. **74**, 4455 (1993).
[18] Y. Sun, X.M. Shen, J.Wang, D.G. Zhao, G.Feng, Y.Fu, S.M. Zhang, Z.H. Zhang, Z.H. Feng, Y.X. Bai, and H. Yang, J.Phys. D: Appl. Phys. **35**, 2648 (2002).
[19] http://ece-www.colorado.edu/bart/book/surfstart.htm.
[20] S.M. Sze, Physics of Semiconductor Devices (New York, 1981), p. 245.
[21] Baojun Li, Soo-Jin Chua, N. Yakovlev, Lianshan Wang, and Eng-Kee Sia, Solid-State Electron. **47**, 601 (2003).
[22] http://environmentalchemistry.com/yogi/periodic/Pt.html (12.10.2009)
[23] http://environmentalchemistry.com/yogi/periodic/Pd.html (12.08.2009)
[24] http://environmentalchemistry.com/yogi/periodic/Ni.html (12.10.2009)
[25] http://environmentalchemistry.com/yogi/periodic/Co.html (12.10.2009)
[26] B. Şahin, H. Çetin, and E. Ayyildiz, Solid State Commun. **135**, 490 (2005).
[27] H. P. Sun, Y.B. Chen, X. Q. Pan, D.Z. Chi, R. Nath, and Y. L. Foo, Appl. Phys. Lett. **86**, 071904 (2005).
[28] J. L. Freeouf and J.M. Woodall, Appl. Phys. Lett. **29**, 263 (1976).
[29] E.Ayyilidz and A.Türüt, Solid-State Electron. **43**, 521 (1999).
[30] H. Doğan, N. Yildirim, A. Türüt, Microelectron. Eng. **85**, 655 (2008).
[31] T. Sands, Appl. Phys. Lett. **52**, 197 (1988).
[32] S.K. Cheung and N.W. Cheung, Appl. Phys. **49**, 85 (1986).
[33] J.L. Everaet, R.L. Van Meirhaeghe, W.H. Laflére, and F. Cardon, Semicond. Sci. Technol. **5**, 60 (1990).
[34] R.T. Tung, J.P. Sullivan, and F. Schrey, Mater. Sci. B **14**, 266 (1992).

