TABLE OF CONTENTS

LIST OF ABBREVIATIONS

III-V	Periodic table group 3-4
AC	Alternating current
ACLR/ACPR	Adjacent channel leakage ratio/Adjacent channel power ratio
AM-AM	Amplitude-to-amplitude conversion
AM-PM	Amplitude-to-phase conversion
ADBPD	Adaptive digital baseband predistortion
ADC	Analogue-to-digital converter
ADRFPD	Adaptive digital RF predistortion
AMS	Analog Mixed Signal
APD	Adaptive predistortion
BEOL	Back-end-of-line
BV_{CBO}	Breakdown voltage collector base (open base)
BV_{CEO}	Breakdown voltage collector emitter (open emitter)
BV_{CER}	Breakdown voltage collector emitter (open emitter) with resistor
BiCMOS	Bipolar and CMOS
BJT	Bipolar junction transistor
CAD	Computer aided design
CE	Common emitter
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analogue converter
DC	Direct current
DRC	Design rule check
DSP	Digital signal processor
DBPD	Digital baseband predistortion
EER	Envelope elimination and restoration
EVM	Error vector magnitude
FET	Field effect transistor
GaAs	Gallium arsenide
GSG	Ground-signal-ground
HBT	Heterojunction bipolar transistor
HiCuM	High current model
HB	High breakdown
HP	High performance
IBM	International Business Machines

IC	Integrated circuit
IF	Intermediate frequency
IIP_3	Input third-order intercept point
$IP_{1\ dB}$	Input power 1 dB compression point
IM	Inter-modulation
LINC	Linear amplification with non-linear components
LUT	Look-up table
LVS	Layout versus schematic
MESFET	Metal semiconductor field effect transistor
MIM	Metal insulator metal
MOSFET	Metal oxide semiconductor field effect transistor
MOSIS	Metal Oxide Semiconductor Implementation Service
mm-wave	Millimetre-wave
MPW	Multi-project wafer
NDA	Non-disclosure agreement
N/PFET	N/P-type field effect transistor
OFDM	Orthogonal frequency division multiplexing
QAM	Quadrature amplitude modulation
RF	Radio frequency
Si	Silicon
SiGe	Silicon-germanium
p-cells	Parametric cells
PA	Power amplifier
PAC	Periodic AC
PAE	Power added efficiency
PCB	Printed circuit board
PDK	Process design kit
PSS	Periodic steady state
IMD3	Third-order intermodulation distortion
RFC	RF choke
TL	Transmission line
VBIC	Vertical bipolar intercompany
VGA	Variable gain amplifier
VNA	Vector network analyser
XOR	Exclusive OR

CHAPTER 1 INTRODUCTION

1.1 BACKGROUNG TO THE RESEARCH

In today's information-dependent world, there is an increase in demand for faster communication speeds and larger bandwidth. Current microwave frequency bands have become saturated and recent advancements in technology, especially in silicon-germanium (SiGe) technology, has resulted in a growing necessity to use new frequency spectrums such as the millimetre-wave (mm-wave) frequency band. In particular, the 60 GHz band is very useful for wireless communication. It offers a very wide frequency and higher transmission speed and it is unlicensed [1].

The wireless transmitter needed for mm-wave communication comprises many building blocks, as shown in Figure 1.1, and of particular interest is the power amplifier (PA). The purpose of the PA is to amplify the input signal to an acceptable power level so that the signal can be transmitted from the transmitter to the receiver through the air interface. PAs are the final subsystems prior to the antenna in the transmitter and directly affect the performance of the transmitter.

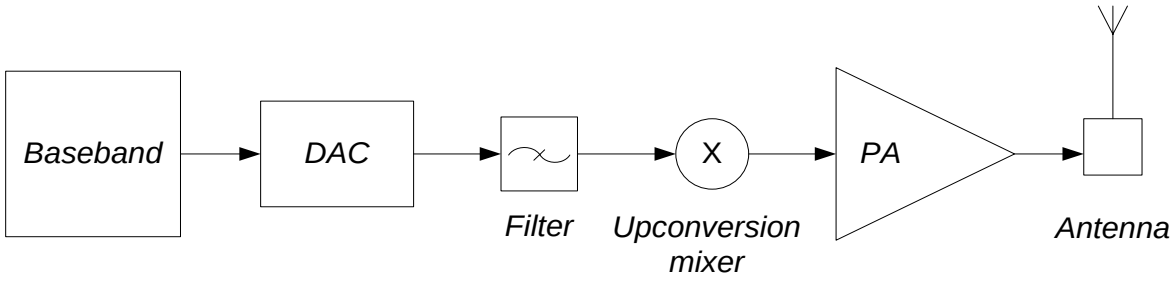


Figure 1.1. Wireless transmitter.

Unlike wired line communications, wireless systems must share a common transmission medium. The available spectrum is therefore limited. The demand for greater spectral efficiency has resulted in orthogonal frequency division multiplexing (OFDM) being considered as the modulation scheme for communication systems in the mm-wave frequency band [2]. This modulation scheme results in amplitude and phase modulated signals with large peak-to-average ratios.

These signals are very sensitive to disturbances that affect the amplitude and phase of the signal, such as non-linear amplification, which causes distortion in the output signal. This distortion causes the signal to expand to the other adjacent channels, resulting in interference, and deteriorates the performance of the communication system. For this reason it is important for a PA to operate linearly. Linearity and efficiency are mutually exclusive. Designing linear PAs is possible, but most linear PAs are not efficient [3]. The PA efficiency is a very important factor especially in mobile communications. The design of linear and efficient mm-wave PA presents one of the most challenging design problems.

Therefore, in order to achieve good linearity with sufficient efficiency, some kind of linearisation technique has to be implemented [4]. This research focuses on improving the linearity of PAs for mm-wave frequencies using adaptive predistortion (APD) as the linearisation technique. Predistortion's chief attribute is its conceptual simplicity and it does not suffer from bandwidth limitations, which makes it suitable for wideband PAs.

1.2 RESEARCH PROBLEM AND HYPOTHESIS

The primary research question addressed in this thesis:

How can a low-complexity, high-performance APD be integrated with a PA and reduce distortion and improve the linearity of PAs at 60 GHz?

The distortion makes it difficult for the receiver to detect the information correctly. Reducing distortion components will improve the linearity of the PA and also the overall transmitter performance. Existing predistortion linearisation techniques using digital and analogue predistortion methods have been implemented. The analogue predistortion is the simplest predistortion technique and can be realised using a diode or a cubic predistorter at the input of the PA. Digital predistortion is mostly found in an adaptive form in the baseband region where the predistortion is applied with a look-up table (LUT) using a digital signal processor (DSP). Table 1.1 shows the current existing predistortion linearisation methods and their performance in terms of either the adjacent channel leakage ratio/adjacent channel power ratio (ACLR/ACPR), error vector magnitude (EVM) or third-order intermodulation distortion (IMD3) reduction.

Table 1.1. Summary of existing predistortion linearisation techniques implemented.

Reference	Frequency [GHz]	Predistortion	Linearity improvement	Impact factor (2012)	Cited half-life (2012)
[5]	2.14	Analogue	16.1 dB †	1.784	5.2
[6]	1.96	Digital	15 dB †	2.229	9.0
[7]	1.8	Analogue	20 dB #	-	-
[8]	2.14	Analogue	16.4 dBc †	1.784	5.2
[9]	60	Digital	*	-	-
[10]	60	Analogue	25 dB #	1.784	5.2
[11]	1.95	Analogue	**	2.229	9.0
[12] This Work	60	Analogue	10 dB #	0.585	5.6

† Reduction in ACLR/ACPR.

* Linearity improvement of -28 dB in EVM.

Optimum IMD3 reduction.

** A minimum input third-order intercept point (IIP_3) of 7.5 dBm.

As shown in Table 1.1, few predistortion linearisation techniques are implemented at 60 GHz. Furthermore, few of these on-chip predistortion linearisation techniques have been fabricated using the International Business Machines (IBM) SiGe bipolar and complementary metal oxide semiconductor (BiCMOS) process. The proposed research is focused on an APD linearisation technique at 60 GHz using SiGe BiCMOS technology.

The research hypothesis can be stated by means of the following:

If the linearity of PAs is related to the distortion in PAs, then if APD is used to reduce the distortion in PAs, this will improve the linearity in PAs.

Based on the hypothesis, the following secondary research questions are asked:

- How can the APD circuit be realised and integrated with PAs at mm-wave frequencies?
- Determine the distortion reduction and linearity improvement that can be achieved by using APD for PAs at mm-wave frequencies.
- How can the overall PA performance be influenced by using APD?

To validate the hypothesis and to address the above questions, different APD options and PA architectures and performance metrics were evaluated and their trade-offs were investigated. The optimal solution for the PA and APD was then designed and simulated at 60 GHz using circuit models separately and then integrated. The PA and APD performance was then evaluated in terms of linearity improvement. After the optimisation of the PA and APD design, both the PA and APD were fabricated onto an integrated circuit (IC). Measurement results were performed on the prototyped solution to determine the performance and feasibility of the design and validate the hypothesis practically.

1.3 JUSTIFICATION FOR THE RESEARCH

The huge bandwidth around 60 GHz is one of the largest unlicensed bandwidth allocations available. This band provides at least 3 GHz (59-62 GHz) overlap that is available worldwide, offering high data-rate communications. Even though this band suffers from severe attenuation of 10 dB/km due to oxygen absorption, this further justifies its use for short-range communication.

The IEEE 802.15.3c and the WirelessHD task teams have defined standards for the 60 GHz band with 30 dBi gain for the antennas and 10 dBm output power for the PA [13]. In addition, OFDM has strict requirements for linearity. Therefore designing a PA at this frequency is challenging, as these PAs must deliver high linear output power and be efficient.

Linearisation techniques can be used to improve the linearity of PAs and meet the demands of mm-wave communications. Not much attention has been focused on linearisation techniques of PAs at 60 GHz. Therefore there is a need to investigate and characterise these linearisation techniques to determine their ability to improve the linearity of 60 GHz PAs.

In addition there is an increasing demand for PAs to be reliable and cost-effective and to yield high performance to satisfy the mm-wave requirements. SiGe BiCMOS technology provides low cost and superior performance and can be used as the building blocks to realise these demands of mm-wave systems.

1.4 METHODOLOGY

The initial step in the research was conducting a thorough literature study focusing on linearity limitations on PAs, the semiconductor building blocks realising PAs at 60 GHz and techniques to improve the linearity of PAs specifically focusing on predistortion, as it provides low complexity and yields good performance in improving the linearity of PAs. The literature study was done to locate a gap in the current research in order to formulate and define a hypothesis.

The optimal PA and APD solution was determined by simulating the design on a schematic level. The PA and APD were then fabricated and prototyped to obtain measurement results. The PA and APD were therefore critically evaluated on a practical level to determine realistically the performance of the PA and APD and the PA separately, therefore validating the hypothesis.

1.5 OUTLINE OF THE THESIS

This thesis is organised as follows:

- Chapter 1: Introduction

This chapter highlights the research problem, the hypothesis and the motivation for the research. The research is also placed into context with other research conducted in PA linearisation using predistortion.

- Chapter 2: Literature Review

The existing body of knowledge in this area of research is presented and analysed in this chapter. The chapter describes the fundamentals of PAs, the non-linear phenomena in PAs that result in distortion, the semiconductor technologies available for PAs and methods to reduce the distortion in PAs using current linearisation techniques focusing specifically on using predistortion at mm-wave frequencies.

- Chapter 3: Research Methodology

The method and procedures used to validate the hypothesis and answer the research questions are explained in this chapter. An overview of the software package used for simulation is also presented. The fabrication process in the design of the PA and APD is discussed, as well as the details of the measurement equipment used on the prototyped IC. Finally a set of measurement tests is presented that was conducted to validate the hypothesis practically.

- Chapter 4: Mathematical Analysis

The distortion components in the SiGe heterojunction bipolar transistor (HBT) are analysed in this chapter with the use of the Volterra series analysis. The mathematical analysis describes the effects of the IMD3 component on the fundamental signal and provides techniques to overcome this problem.

- Chapter 5: PA and APD Design and Results

The detailed design of the PA and the APD is described in this chapter. The chapter is divided into the following main sections, viz. the PA design, APD design and implementation and results. All the subsystems are designed from first principles using mathematical analysis and then optimised during system integration.

- Chapter 6: Conclusion

This chapter concludes the thesis and provides the critical evaluation of the hypothesis. The challenges and limitations experienced during this research work are also mentioned, as well as possible future work and improvements on this research work.

1.6 DELIMITATIONS OF THE SCOPE OF THE RESEARCH

The scope of this research is limited to reducing the distortion caused by non-linearities found in PAs at mm-wave frequencies, especially at 60 GHz using APD. The PA was designed and fabricated to integrate with the APD to determine the linearity improvement that can be obtained at 60 GHz, therefore validating the hypothesis.

Since no prior experimental data were available for the PA and APD, both these systems were designed using first principles. Approximations were made from literature and from the limitations set by the process models (operating ranges of the transistors and the dimensions of the passive and active models) from the foundry.

For the APD, different types and configurations are available. The chosen APD focuses on amplitude non-linearity and the IMD3 components and this choice is justified in chapters 4 and 5. The end result is a low-complexity, high-performance APD in terms of linearising the PA and ease of integration with the PA. Although this APD design can easily be integrated with a PA to provide sufficient linearity improvement, because of the limited space available on the multi-project wafer (MPW) run and complexity of the PA, additional PA designs could not be fabricated. Therefore the APD with different PA designs could not be evaluated.

1.7 CONTRIBUTION TO THE FIELD

A new predistortion method using APD for the linearity improvement of PAs has been proposed for use in mm-wave frequencies (specifically 60 GHz). A detailed list of the resulting contributions to the body of knowledge is given here.

- Non-linearity has been identified as a major source of transmitter degradation especially at 60 GHz where efficient and linear PAs are required. The main contribution of this research is the identification and characterisation of these non-linear properties (the IMD3 components) found in HBTs. This research also provides a new solution to reduce the IMD3 components for PAs at 60 GHz.
- The proposed solution followed a thorough literature study on existing PA linearisation techniques. This allowed to find the current trends, performance, strengths and weaknesses of these techniques which are discussed below and in chapter 2.

    - The use of spectral efficient modulation schemes such as OFDM at mm-wave frequencies, results in a need for highly linear PAs at 60 GHz. Previously, linearity analysis in PAs were focused at lower frequencies

(< 5 GHz) using mostly algorithms in DSPs in the baseband region to apply the linearisation techniques. Baseband linearisation is not a true PA linearisation technique but more a transmitter linearisation technique. Only recently has attention been given to the linearity of PAs at 60 GHz [9, 10, 14]. The proposed linearisation technique is a true PA predistortion linearisation technique that can be implemented completely on-chip not requiring any auxiliary circuitry such as in [9, 14].

- The current radio frequency (RF) predistortion linearisation technique at 60 GHz shown in [10] provides a non-adaptive predistortion function to the PA and therefore does not optimise the linearity improvement. It has been shown that using an adaptive predistortion technique approach can improve the linearity of the PA as it provides greater control of the predistortion function.
- Previous 60 GHz predistortion techniques have looked at CMOS transistors [9, 10]. This research analyses the SiGe HBT which is known to have better performance at mm-wave frequencies than CMOS transistors and reduced cost compared to gallium arsenide (GaAs) technologies.

- The non-linearity components were analysed and characterised using the Volterra series analysis. This mathematical analysis identified the major contributors to the non-linearity phenomena in HBTs. The large signal analysis of the PA was also investigated separately. Using these analyses, a solution was derived to reduce IMD3 components in the HBT.
- The proposed solution was enhanced further making it adaptable using an on-chip power detector, analogue-to-digital converter (ADC), control logic, digital-to-analogue converter (DAC) and dynamic bias circuitry. This is the first time a complete APD has been implemented on-chip to improve the linearity of PAs at 60 GHz.
- The APD design provides full control to the user allowing the PA to be optimally linearised. Although the APD in this research was integrated with a three-stage single-ended common emitter (CE) PA, it can be applied to any PA topology. This is because the adaptation is applied to the bias circuitry of the PA.

- The mathematical analysis has been verified by analysing the linearity performance of the HBT using simulations. It was observed that by increasing the bias current up to 23 mA, the IIP_3 increased for the 0.12 µm × 16 µm SiGe HBT therefore validating that the linearity of the HBT based PA can be improved.
- The APD proposed in this research has been demonstrated successfully through the design and simulation of a non-linear and linear PA at 60 GHz. The PAs were designed from first principles. Both the non-linear and linear PAs were submitted for fabrication. The non-linear PA achieves a P_{SAT} of 11.97 dBm, an input power 1 dB compression point ($IP_{1\,dB}$) of -10 dBm and a peak power added efficiency (PAE) of 12.6 %. When the APD is applied, the PA has an improved $IP_{1\,dB}$ of -6 dBm, a peak PAE of 11.8 % and an optimum IMD3 reduction of 10 dB is achieved. The linear PA also has an improved linear output power of 2.5 dBm compared to the non-linear PA.
- The mathematical model can be applied easily into any computer aided design (CAD) software as this analysis is independent of the CAD software. This thesis also presents a complete design and implementation of a three-stage 60 GHz PA and the APD subsystems. The use of the BiCMOS process from IBM allowed the integration of both SiGe HBT and CMOS technology nodes.

1.8 PUBLICATION LEADING FROM THIS RESEARCH

The following peer-reviewed journal article related to this work has been accepted:

- J. Valliarampath and S. Sinha, "Linearity Improvement Analysis for PAs at mm-Wave Frequencies", *Microwave and Optical Technology Letters*, vol. 56, no. 3, pp. 743-748, March 2014.

The journal is listed by Thomson Reuters Web of Knowledge (formerly ISI).

1.9 CONCLUSION

This chapter laid the foundation for this thesis. The background of the research was presented and the need to characterise and minimise the IMD3 components for PAs at 60 GHz was emphasised in this chapter. This allowed the identification of the research problem and the formulation of the hypothesis. The methodology to validate the hypothesis, as well as the organisation of the thesis, was also outlined to indicate how the research was conducted.

CHAPTER 2 LITERATURE REVIEW

2.1 INTRODUCTION

The 3 GHz overlap unlicensed bandwidth allocation at 60 GHz has made this mm-wave spectrum lucrative for fast gigabit applications. This has resulted in numerous RF transceivers currently being developed to operate within the 60 GHz band. One of the most challenging functional blocks in the transceiver at 60 GHz is the PA [15]. Its function is to amplify the input signal and deliver high output linear power while being efficient, but its performance is severely affected by the scaled semiconductor technology and the operating frequency. It is for this reason that PA linearisation techniques should be investigated to improve the linearity and maintain efficiency, enhancing the performance of the PA.

The first part of this chapter focuses on the fundamental concepts, parameters and figures of merit for PAs. The current semiconductor technologies as the building blocks of the PA are also discussed. The second part of this chapter analyses the various distortion components in the PAs. This important property contributes to the understanding of non-linearity in PAs. The last part investigates several linearisation techniques, evaluating their trade-offs and specifically concentrating on the predistortion linearisation technique for mm-wave PAs.

2.2 POWER AMPLIFIERS

The PA usually consumes the largest amount of static power of the transmitter. It is therefore desirable to operate the PA in the saturation region to achieve maximum power efficiency of the PA. The trade-off is that all real PAs have non-linear characteristics and this is most noticeable in the saturation region. This trade-off becomes even more stringent at 60 GHz, where desirable Si-based technology for low-cost production cannot provide sufficient output power in PAs while maintaining high linearity [16]. PAs are therefore designed and evaluated on several trade-offs, each trying to accomplish a conflicting requirement such as linearity versus efficiency or high output power versus minimum

distortion. Consequently understanding the characteristics and operation of PAs is essential to ensure PAs are correctly designed to meet the requirements [17].

2.2.1 PA CLASS OF OPERATION

The performance of any PA will be influenced by how the PA is biased. There are several groups of classes; each has been well documented and is briefly discussed here. The most common group is the biasing class, which can be defined as Class A, B, AB or C. The choice of PA class determines the amount of distortion and the power efficiency of the output signal. The class of operation to use is determined by the linearity and efficiency requirements of the system using the PA [17]. Table 2.1 summarises the biasing classes from Class A to Class C.

Table 2.1. Comparison of PA biasing classes [17].

Class	Current Conduction Angle θ	Bias Point	Maximum Theoretical Efficiency (%)
A	360 °	Midway between device pinch-off and saturation.	50
B	θ = 180 °	Device pinch-off.	78.5
AB	180 ° < θ < 360 °	Above pinch-off.	50 – 78.5
C	θ < 180 °	Below pinch-off.	78.5 - 100

As shown in Table 2.1, the Class A PA operates in the linear region of the transistor's *i-v* curve and is on 100 % of the time. The output therefore experiences minimum distortion but offers the least amount of efficiency. Class B PAs are on 50 % of the time and therefore the output is not as linear; however, they do provide improved efficiency compared to Class A. The Class AB PA is a compromise between the Class A and B PA in terms of linearity and efficiency, while the Class C PA is most efficient, but suffers most distortion, as its bias point is below the pinch-off region. Class AB PAs produce distortion components that are considered low enough to use an external linearisation technique to improve the linearity of these PAs. However, Class C PAs produce such a large amount of distortion that they are not ever considered for use with external linearisation techniques [18].

2.2.2 PA TOPOLOGIES

Three basic PA topologies exist, viz. single-ended, balanced and differential. The criteria for choosing the particular topology depend on the PA requirement. Table 2.2 provides a comparison between these PA topologies and Figure 2.1 shows the circuit configurations of these topologies.

Table 2.2. Comparison of PA topologies.

Topology	Advantages	Disadvantages
Single-ended	Low complexity. Reduced cost.	Reduced performance compared to other PA topologies.
Balanced	Higher output saturated power and 1 dB compression point. Excellent impedance matching. Improved reliability and stability.	Additional components required. Losses of couplers reduce overall PA performance. Increased costs.
Differential/Push-pull	Higher output saturated power and 1 dB compression point.	Consumes more static power than single-ended. Increased cost.

As shown in Table 2.2 and in Figure 2.1 (a), the single-ended topology is the least complex PA topology and is commonly used in either the CE/common source or cascode configuration. The cascode typically provides higher gain and improved efficiency and can be operated above the breakdown voltage that usually restricts the CE configuration [19]. The single-ended has the smallest chip area and is the most cost-effective PA topology [13].

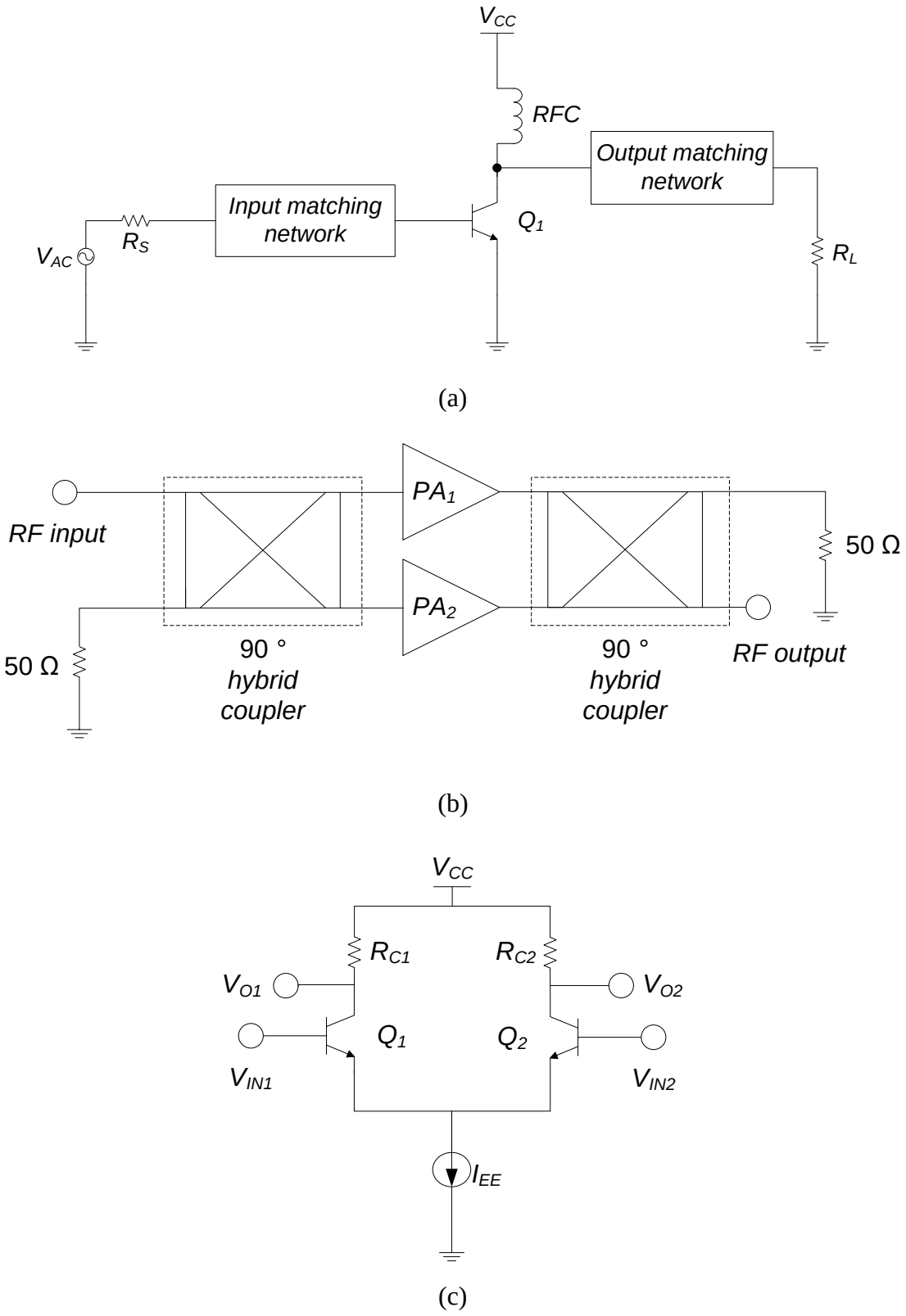


Figure 2.1. PA topologies viz. **(a)** general single-ended PA **(b)** balanced PA using 90 ° hybrid couplers **(c)** differential CE PA.

The balanced and differential PA topology is able to obtain higher output saturated power and a 1 dB compression point compared to the singled-ended PA topology. The balanced topology shown in Figure 2.1 (b) provides improved input and output matching capability as long as the amplifier cells are identical and also results in improved stability. In case one of the single-ended transistors fails, the PA is still able to function; however, the gain will be reduced by 6 dB. The major drawback of the balanced topology is the use of couplers because it introduces losses into the system and also consumes a large chip area as shown in [20], therefore increasing the cost of the design. The disadvantage of the differential topology is that it consumes 50 % more static power compared to the singled-ended PA topology. It also occupies a larger chip area because it consists of two singled-ended PAs as shown in Figure 2.1 (c) and therefore increases the cost as well [13].

2.2.3 OUTPUT POWER

The primary goal of the PA is to deliver maximum power to the load. The output power can be determined from the power supply voltage and the load for a single-ended PA, as shown in Figure 2.1 (a). This PA consists of the transistor Q_1, the input and output matching networks, the RF choke (RFC), in the form of an inductor and the source (R_S) and load resistors (R_L). The transistor Q_1 is usually constrained by the breakdown voltage and the collector saturation current and this must be taken into account when designing the PA. The maximum power delivered to the load for a Class A PA can be determined using (2.1),

$$P_{OUT} = \frac{{V_{CC}}^2}{2R_L}, \tag{2.1}$$

where V_{CC} is the power supply voltage.

2.2.4 POWER MATCHING

The maximum power theorem states that the maximum power transfer occurs when the PA is conjugately matched and is given by (2.2) and (2.3):

$$\Gamma_S = S_{11}^*, \tag{2.2}$$

$$\Gamma_L = S_{22}^*, \tag{2.3}$$

where Γ_S and Γ_L are the source and load reflection coefficients respectively. The above equations are only valid when the PA is unilateral.

This theorem is valid only for low input power, i.e. small-signal operation where the PA is linear and can only be used on the input side and not at the output side of the PA. For large-signal operation the load-line/load-pull approach is used instead to obtain maximum output power, which transforms the output load to a Γ_{OPT}. The load-line maximises the output power by using the maximum current and voltage swings, while the load-pull determines Γ_{OPT} using an exhaustive search approach. The results of the load-line/load-pull approach and the conjugately match method are shown in Figure 2.2.

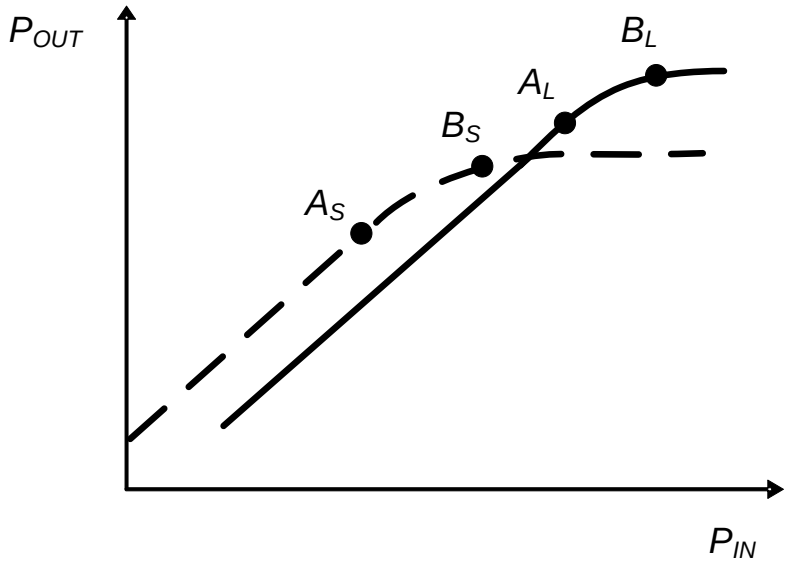


Figure 2.2. Optimal matching versus small-signal matching [21].

As shown in Figure 2.2, the dashed line and solid line are the small-signal matching and optimal matching approaches respectively. Points A_S, A_L and B_S, B_L are the small-signal and optimal matching maximum uncompressed power and 1 dB gain compression points respectively. Although higher output power is achieved using the load-line/load-pull approach, it does come at the cost of reduced gain.

2.2.5 POWER EFFICIENCY

Efficiency is a key performance metric of mm-wave PAs and is a measure of the RF output power to the direct current (DC) input power. Efficiency is either defined as the drain efficiency (η_D) or collector efficiency (η_C) and is given by (2.4)

$$\eta_{D/C} = \frac{P_{OUT}}{P_{DC}}. \tag{2.4}$$

Another key performance metric is the PAE. This metric is the ratio of the output RF power minus the input RF power to the DC input power and is calculated using (2.5)

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}}. \tag{2.5}$$

2.2.6 MODULATION SCHEMES

There has been a growing trend in utilising complex digital modulation schemes that are bandwidth efficient for mm-wave applications. The IEEE 802.15.3.c and WirelessHD have developed a modulation scheme standard for the 60 GHz frequency band focusing mainly on OFDM because of its high spectral efficiency [2]. Using OFDM results in a stronger and clearer signal because the signal is split into several narrowband channels at different frequencies, which reduces wireless interference. The use of an OFDM modulation scheme is known as an effective way to mitigate selective multipath fading effects in wireless channels [22]. However, OFDM is more complex and expensive because it requires the analysis of many frequencies and the characteristics of those frequencies.

Typically with OFDM, quadrature amplitude modulation (QAM) is employed, which uses both amplitude and phase for encoding data for higher data rates. It has been reported that using an OFDM 16-QAM modulation is sufficient to achieve a 3.8 Gbps data rate [23]. These modulation schemes require high linearity PAs in order to maximise system performance and satisfy the increasing demand for higher data rates at 60 GHz.

2.2.7 NON-LINEAR PHENOMENA IN PA

In order to achieve high efficiency output power, PAs have to operate in the non-linear area near the saturation region. This increases the PA's non-linearity, which affects the spectrum of the signal. One way to model this non-linearity and to calculate the spectral components is by using a memory-less polynomial model. The output of a system modelled using a third-degree polynomial is given by (2.6),

$$I = aV(t) + bV(t)^2 + cV(t)^3, \tag{2.6}$$

where *a*, *b* and *c* are real coefficients. Assume the input signal, $V(t)$ is of the form as shown in (2.7):

$$V(t) = V_1\, cos(\omega_1 t) + V_2\, cos(\omega_2 t). \tag{2.7}$$

Substituting (2.7) into (2.6), results in three terms, as shown in (2.8) to (2.10):

$$i_1(t) = aV_1\, cos(\omega_1 t) + aV_2\, cos(\omega_2 t), \tag{2.8}$$

$$i_2(t) = \frac{b}{2}\{V_1^2 + V_2^2 + V_1^2\, cos(2\omega_1 t) + V_2^2\, cos(2\omega_2 t) + 2V_1V_2[cos\big((\omega_1 + \omega_2)t\big) + cos\big((\omega_1 - \omega_2)t\big)]\}, \tag{2.9}$$

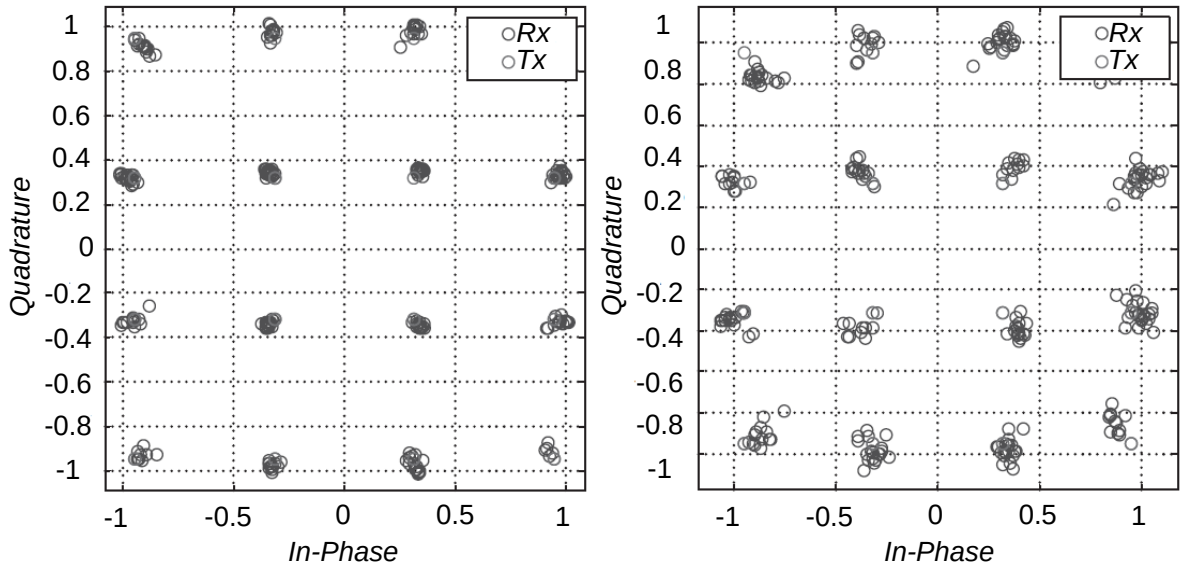
$$i_3(t) = \frac{c}{4}\{V_1^3\, cos(3\omega_1 t) + V_2^3\, cos(3\omega_1 t) + 3V_1^2V_2[cos\big((2\omega_1 + \omega_2)t\big) + cos\big((2\omega_1 - \omega_2)t\big)] + 3V_1V_2^2[cos((\omega_1 + 2\omega_2)t) + cos((\omega_1 - 2\omega_2)t)] + 3(V_1^3 + 2V_1V_2^2)cos(\omega_1 t) + 3(V_2^3 + 2V_1^2V_2)cos(\omega_2 t)\}. \tag{2.10}$$

From (2.8) to (2.10), the generated frequencies all occur at a linear combination of the two excitation frequencies (2.11),

$$\omega_{m,n} = m\omega_1 + n\omega_2, \tag{2.11}$$

where *m*, *n* = ..., *–3*, *–2*, *–1*, *0*, *1*, *2*, *3*, ...

The current or the voltage components at the mixing frequency, $\omega_{m,n}$, result in many non-linear problems such as harmonics, intermodulation (IM), amplitude-to-amplitude conversion (AM-AM) and amplitude-to-phase conversion (AM-PM) distortion. The non-linear effect on the 16-QAM signal is shown in Figure 2.3.



(a) (b)

Figure 2.3. 16-QAM constellation before and after non-linear amplification under **(a)** 3 dB and **(b)** 1 dB output back-off [16].

The non-linear effect results in a distorted QAM constellation, as shown in Figure 2.3. The modulation data points lie outside their correct decision areas. This increases the probability that the receiver will misinterpret these values, thus increasing the bit error rate.

2.2.8 HARMONIC DISTORTION

One obvious result from the non-linear PA is the generation of harmonics shown in (2.8) to (2.10) at $m\omega_1$ and $n\omega_2$. Generally harmonics are not a serious problem because these components are situated far from the desired signals and are removed using filters.

2.2.9 IM DISTORTION

Two or more tones added in (2.8) to (2.10) are called IM components. IM components pose a very serious problem, because these components can be mistaken for the desired signals.

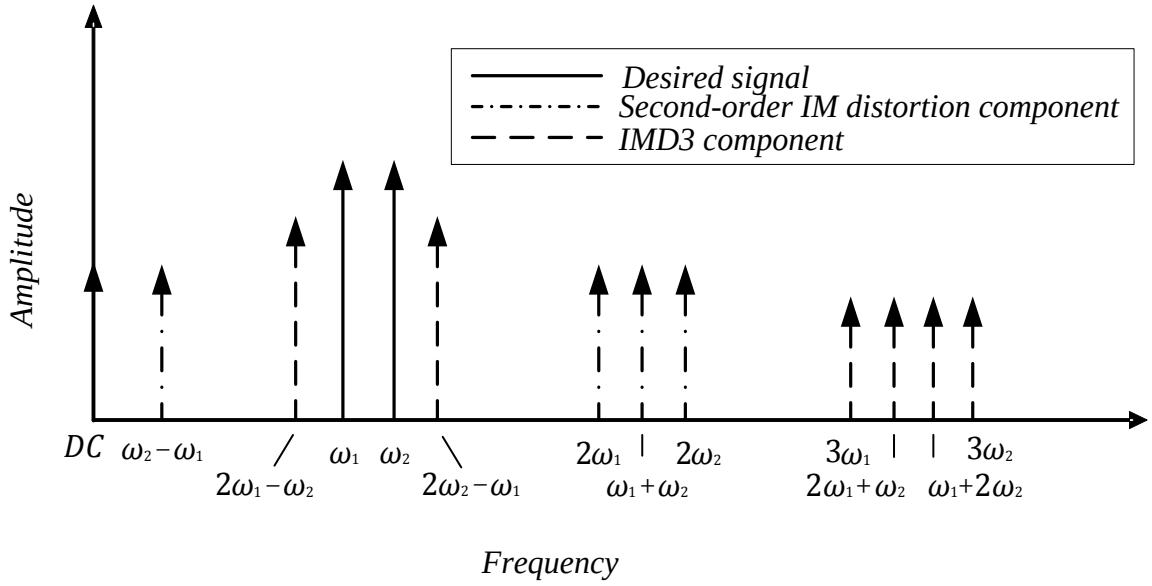


Figure 2.4. Second-order IM distortion and IMD3 components.

Even-order IM products are often of little concern because they occur at frequencies that are situated well above or below the desired signals. The odd-order IM products are of greatest concern, especially the third-order ones that occur at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, as shown in Figure 2.4. The IMD3 components are the strongest of all odd-order products and lie very close to the desired signals. These IMD3 components also fall both on the signal band and out of the signal band, resulting in spectral regrowth, and cannot easily be rejected by filters.

The IM distortion components (predominately the IMD3 and fifth-order IM distortion) are used to calculate the ACPR. This is a ratio between the power in the main channel and the power in the adjacent channels. It is a measure of the amount of spectral regrowth within the PA. The lower the ACPR value, the better the linearity of the PA.

2.2.10 GAIN COMPRESSION

The non-linear phenomenon known as gain compression occurs when the output gain decreases with increased input power due to the PA's physical limits. This effect results in the output power of the PA saturating at a certain point, as shown in Figure 2.5.

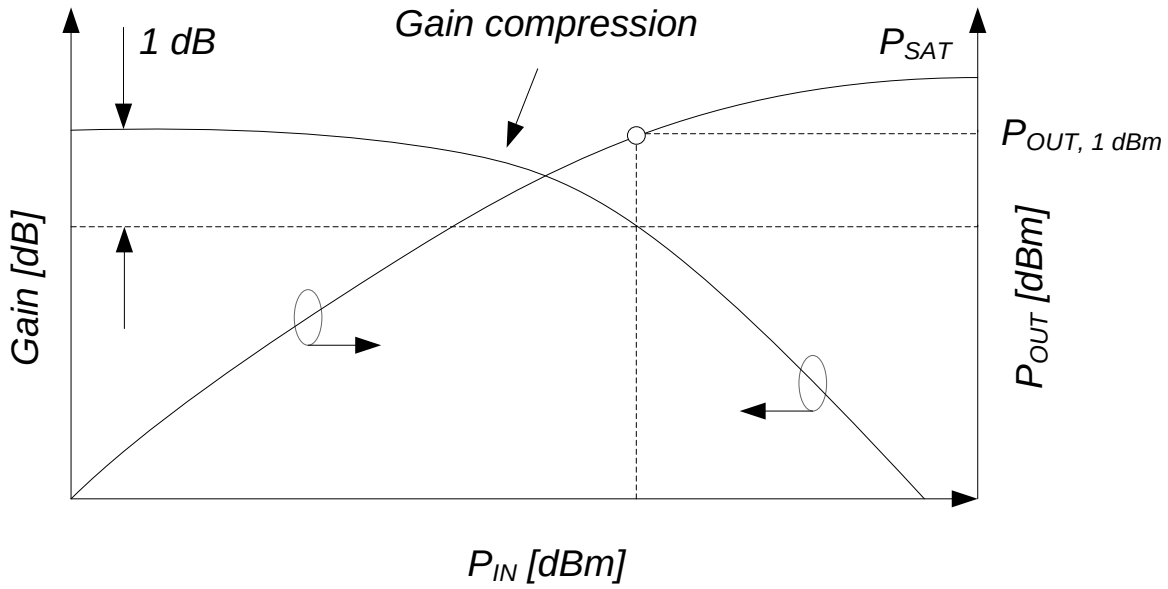


Figure 2.5. A typical PA experiencing gain compression.

The point where the output power level deviates by 1 dB from the linear output power characteristic is known as the 1 dB compression point as shown in Figure 2.5. This point separates the almost linear output power from the non-linear output power.

2.2.11 AM-AM AND AM-PM DISTORTION

AM-AM and AM-PM distortion will occur in a memory reactive non-linear circuit owing to amplitude distortion and phase difference with the input signal only. If the distortion components are dependent on the current input signal as well as the previous input signal, then these distortion components will be affected by memory effects [16]. The effect of these distortions is illustrated in Figure 2.6.

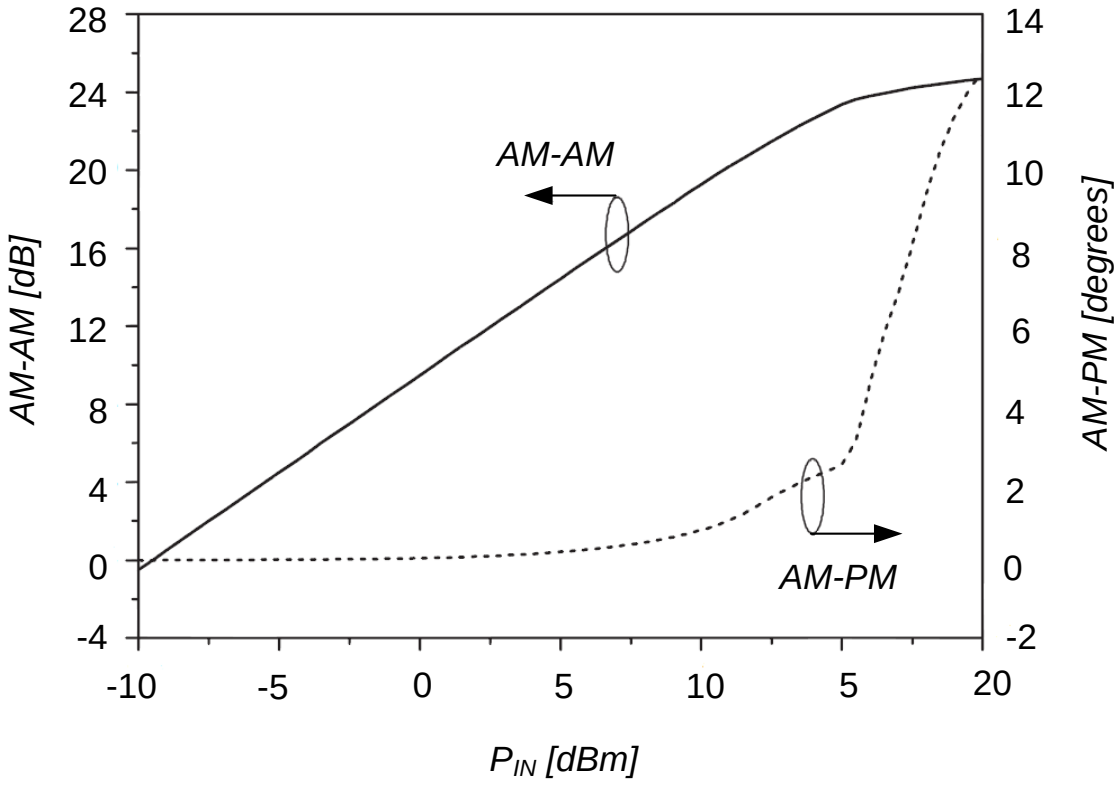


Figure 2.6. AM-AM and AM-PM distortion due to PA non-linearities [17].

In Figure 2.6, the AM-AM distortion indicates non-linearity only in the amplitude and is associated with gain compression. To avoid AM-AM, the amplifier can be operated in the output back-off region, but this will reduce the power efficiency of the PA. AM-PM conversion occurs when changes in the amplitude of a signal applied to a PA cause a phase shift and affect the linearity of the PA. AM-PM often begins to affect the linearity of the PA at several dBs below the compression point [24]. Ideally, the amplitude and phase shift should be linear and constant respectively as input power is increased, resulting in little amplitude and phase distortion with increasing input power levels.

2.3 NON-LINEARITY COMPONENTS IN SIGE HBT

The dominant *i-v* and C-V non-linearities found in the SiGe HBT result in the following non-linearity components [25]:

- The collector current, I_C, is a non-linear function of the control voltage, v_π, and relates to a non-linear transconductance.
- The base current, I_B, is also a non-linear function of v_π and therefore follows the non-linear characteristics of the transconductance.
- The diffusion capacitance, C_{diff}, is directly proportional to I_C and is therefore inherently non-linear.

2.4 SEMICONDUCTOR TECHNOLOGIES

The performance achieved by the mm-wave PA and APD is highly dependent on the semiconductor building blocks. These include both active and passive devices. Several semiconductor technologies are available to fabricate mm-wave PAs. Accurate active and passive models are necessary to predict the real performance of the PA during the design process.

2.4.1 ACTIVE DEVICES

The requirements to integrate analogue and digital circuits and extend the capabilities of the same PA chip have become very important. Historically metal oxide semiconductor field effect transistor (MOSFET) and metal semiconductor field effect transistor (MESFET) devices were used in PAs. However, owing to higher gains and current densities required at microwave and mm-wave frequencies, bipolar devices have been the preferred choice at higher frequencies [26]. Bipolar junction transistor (BJT) devices based on Si and periodic table group 3-4 (III-V) compound technologies such as GaAs are now found in microwave and mm-wave PA designs.

GaAs technology has a significant performance advantage due to the higher electron drift mobility and semi-insulating substrate compared to Si. This was the reason for GaAs being favoured for RF applications. However, recent advancements in Si-based technologies, particularly the SiGe HBTs, offer a significant challenge to III-V technologies. SiGe HBT technology reduces manufacturing costs as well as power consumption compared to semiconductor technologies based on GaAs and indium phosphide [15], [26].

Germanium has a bandgap of 0.66 eV compared to Si, which has a bandgap of 1.12 eV. However SiGe has a narrower bandgap than Si, where Ge is graded across the otherwise Si base, forming the SiGe HBT. This results in the overall bandgap of the base region being reduced. This bandgap difference between the emitter and the base in the HBT results in a higher CE current gain [27]. Semiconductor device performance is shown for SiGe HBT and GaAs HBT in Table 2.3.

Table 2.3. Process parameters for SiGe HBT and GaAs HBT technologies [28].

	SiGe HBT	GaAs HBT
f_T (GHz)	44	46
Forward gain, β	200	120
Base-emitter voltage, V_{be} (V)	0.8	1.33
Early voltage, V_A (V)	100	1223
Collector-emitter breakdown voltage, V_{ce} (V)	6	14.3
Collector-base breakdown voltage, V_{cb} (V)	12	26
Emitter-base breakdown voltage, V_{eb} (V)	5	6.9
Power density (mW/μm^2)	2	0.9
Thermal conductivity (W/cm-°C)	1.5	0.49
Base-emitter capacitance, C_{be} (fF)	10	2.4
Base-collector capacitance, C_{bc} (fF)	3.3	1
Possibility of N-type and P-type metal oxide semiconductor integration	Yes	No

As shown in Table 2.3, HBTs based on III-V semiconductors are currently the fastest devices and offer better performance than SiGe HBTs because of their superior breakdown voltage and smaller parasitic capacitances. Nevertheless, recently higher f_T and f_{max} values (which determine the ultimate circuit speed) of 230 GHz and 280 GHz respectively have been reported for SiGe HBTs [29]. An advantage of SiGe HBTs over GaAs HBTs, where PA is concerned, is represented by the higher linearity of the former. Table 2.4 [30] shows the comparison of the linearity efficiency of the SiGe BiCMOS HBT technology against different semiconductor device technologies.

Table 2.4. Comparison of different semiconductor technologies in terms of linearity [30].

Technology	OIP_3 (dBm)	P_{DC} (mW)	Linearity efficiency
IBM SiGe HBT	25	27	12
GaAs HBT	25	29.1	11
GaAs high electron mobility transistor	31.5	240	6
GaAs MESFET	28	60	10.5
Si BJT (high f_T)	17	14	4

The linearity efficiency in Table 2.4 is calculated by dividing the power at the output third-order intercept point (OIP_3) by the DC power (P_{DC}). It shows that the SiGe HBT has the highest linearity efficiency compared to the other technology processes. Based on the trends in linearity efficiency, the current SiGe HBT technology with its reduced cost and improved performance, as compared to GaAs HBT technology, makes it favourable for high-linearity circuit designs.

The availability of HBTs and MOSFETs in SiGe BiCMOS technologies offer increased design flexibility in PA circuits. SiGe HBTs are generally integrated with MOSFETs in a BiCMOS technology. The SiGe HBTs are used in the mm-wave circuits and the MOSFETs are used in the digital CMOS circuits. BiCMOS technologies incorporating SiGe HBTs are therefore well suited for producing mm-wave PAs.

2.4.1.1 Breakdown voltage

The continuous scaling down of the SiGe HBT technology has achieved cut-off frequencies greater than 300 GHz. The higher operating frequencies are achieved by increasing the collector doping, which increases the operating current density. This in turn leads to high electric fields at the collector-base junction. However, improvements in the transit frequencies lead to a reduction in the collector-emitter breakdown voltage (BV_{CEO}) [31]. Another breakdown voltage also exists and is the result of the breakdown of the collector-base junction, which is known as collector-base breakdown voltage (BV_{CBO}). Both these circuit configurations are shown in Figure 2.7.

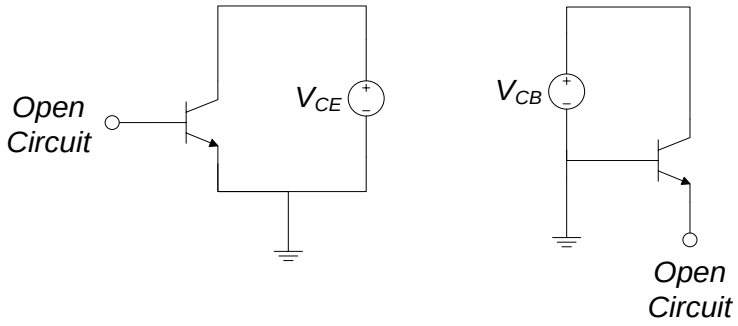


Figure 2.7. Transistor in the open base and open emitter configurations [32].

The CE and common base configurations that result in BV_{CEO} and BV_{CBO} respectively are shown in Figure 2.7. Impact ionisation is the main cause of the breakdown voltages and results in the generation of electron-hole pairs by accelerated electrons, resulting in the necessary base recombination current. This effect reduces the transistor's BV_{CEO}. Operation above BV_{CEO} is possible if an external base resistor is used, which will extract the generated majority carriers from the base. In [33] a base resistance of 300 Ω was used, extending the BV_{CEO} limit from 1.7 V to 4 V (BV_{CER}) for the IBM BiCMOS8HP SiGe HBT. The BV_{CBO} is higher than the BV_{CEO} [34] and is the maximum limit of operating the transistor and BV_{CER} is bounded between BV_{CBO} and BV_{CEO}.

2.4.1.2 Transistor device models

There are different device models such as the Ebers-Moll, Gummel-Poon, vertical bipolar intercompany (VBIC), most exquisite transistor model and high current model (HiCuM) to describe BJTs and HBTs. The Eber-Moll and the Gummel-Poon are simple transistor models and suffer from limitations especially in transistor modelling at very high frequencies. VBIC has several improvements compared to the previous two models; however, there are still some shortcomings in this model. While the HiCuM has proven to be the most accurate model, correlating closely with the measured results [35], the VBIC model is still widely used and is used to describe the IBM BiCMOS8HP SiGe HBT. The schematic of this model is shown in Figure 2.8.

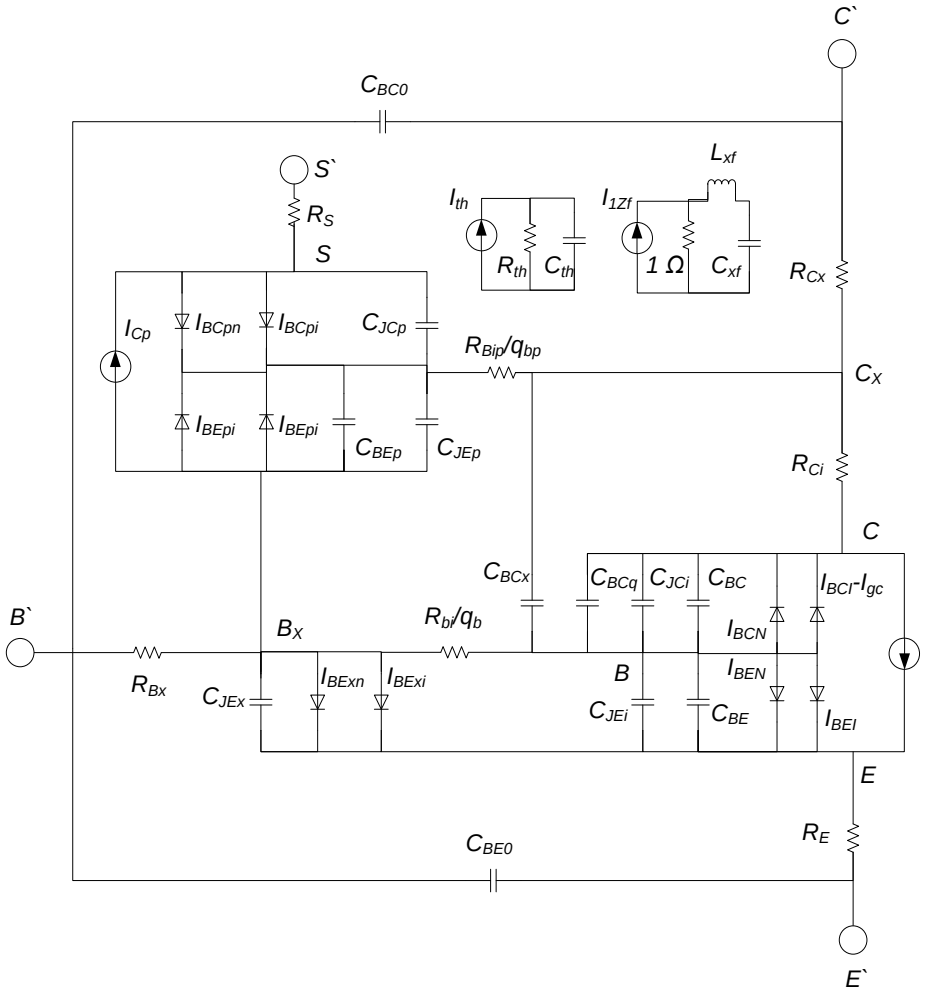


Figure 2.8. Equivalent circuit for the VBIC model [36].

As shown in Figure 2.8, the following important parameters are included and computed by the VBIC model:

- The base resistance, R_B, is calculated using R_{Bi}/q_b and R_{Bx}, where R_{Bi}, R_{Bx} and q_b are the intrinsic base resistance, the extrinsic base resistance and the normalised base charge respectively.
- A quasi-saturation effect is achieved using the constant extrinsic resistance, R_{Cx} and variable intrinsic resistance, R_{Ci}.
- The substrate model consists of a parasitic substrate transistor and is computed using a simplified Gummel-Poon model.
- The weak avalanche current is applied to the *b-c* component of the base current to model avalanche multiplication.

- A subcircuit is added to model self-heating.
- Non-ideal and ideal current sources are used to calculate the *b-c* and the *b-e* component of the base current.

2.4.2 PASSIVE DEVICES

Passive device elements consist of distributed transmission lines (TLs) and lumped components such as capacitors and resistors at mm-wave frequencies. Semiconductor Si substrates with 1-20 Ω.cm resistivity have been used to manufacture mixed signal RF-ICs and the conductive substrate is well known to cause signal loss in passives [37]. Although the Si substrate is lossy, passive elements with *Q* factors above 10 at 60 GHz are still feasible [13]. The shorter wavelengths at mm-wave frequencies make it possible to integrate these devices on-chip. Owing to the low resonance frequency of lumped components, distributed TLs are preferred in mm-wave designs [38].

By adjusting the lengths of the TLs, various passive components can be realised as follows:

- Inductors can be realised if the length, L, is less than $\lambda/4$.
- RFC can be obtained if the L equals $\lambda/4$.
- A capacitor can be formed if $\lambda/4 < L < \lambda/2$.

The cross-section of a typical microstrip TL implemented with a Si substrate is shown in Figure 2.9.

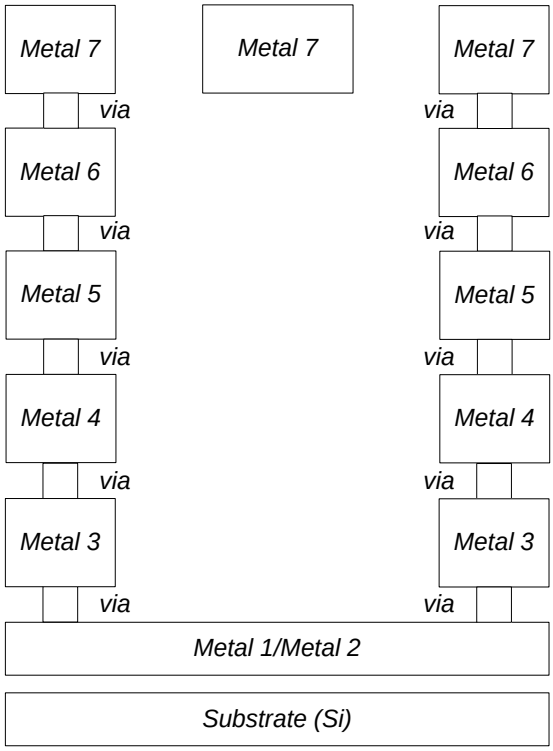


Figure 2.9. Cross-section of a typical microstrip line with side shielding.

As shown in Figure 2.9, the microstrip line is constructed using various metal levels. Depending on the technology process, usually the top metal level is used as the signal path with either the metal-1 or metal-2 as ground planes [39]. Side shielding can also be used and is connected to the ground plane using vias.

Lumped metal insulator metal (MIM) capacitors are also commonly used in mm-wave frequencies. These capacitors can achieve high Q factors and are typically realised by inserting an intermetal dielectric in the higher metal levels [13].

Transformers are also found in mm-wave designs and can be used for AC coupling, impedance matching and as baluns. A typical transformer can be constructed using two spiral inductors. One way to increase the output power of a PA is to use additional PAs and sum the output power using either parallel or series power combiners.

In [40], a transformer was implemented in a 60 GHz PA design using stacked coupled wires. This transformer provided power combining and efficient impedance transformation simultaneously. Transformers if implemented correctly can also achieve a compact layout

size. The challenge with using transformers is that as the frequency increases, the inductance of the primary coil should decrease, therefore it becomes more sensitive to parasitic values.

2.4.3 LAYOUT AND PARASITICS

At mm-wave frequencies, system performance is affected by the device layout. The designer can actually change the device performance by changing the device layout. This allows the designer more freedom in modifying the device performance. The layout of the circuit will also introduce parasitics especially in the interconnects. These parasitics can be defined as resistive, capacitive or inductive parasitics and become more prominent as the frequency increases resulting in severe degradation of the system.

It is important to incorporate these parasitics in the design of the circuit. To model the parasitic effects, *S*-parameter characterisation as well as modelling the impedance mismatches and losses are required. Some process design kits (PDKs) include parasitic effects based on experimental data in their device models. The designer can therefore measure the parasitic effects for different conditions. Another method in predicting the effect of parasitic impedances is through the use of an electromagnetic simulator. This is especially useful in analysing interconnects. Post-layout simulations can provide further insight into the layout, highlighting the effect of parasitics and device performance. The design can then be further optimised using these data.

2.5 PA MODELLING

To understand the non-linear behaviour of PAs, behavioural models, viz. memory-less non-linear and memory non-linear PA models, are used. These two models are described in the following subsections.

2.5.1 QUASI-MEMORY-LESS NON-LINEAR MODEL

This model characterises the current AM-AM and AM-PM non-linearities only. As stated in [16], at 60 GHz the transmitter power is usually around 10 dBm and memory effects can be neglected. Assuming an input signal given by (2.12),

$$x(t) = G[A(t)]\cos[\omega_f t + \theta(t) + \varphi[A(t)]], \tag{2.12}$$

where $G[A(t)]$ and $\varphi[A(t)]$ are the AM-AM and AM-PM non-linearities respectively. The Rapp model, which describes the SiGe HBT, can provide the small-signal gain G shown in (2.13),

$$G[A(t)] = \frac{G|A(t)|}{(1+(\frac{G|A(t)|}{V_{SAT}})^{2p})^{1/2p}}, \tag{2.13}$$

where V_{SAT} and p are the saturation voltage and smoothing factor respectively, while a modified Rapp model provides the AM-PM effects given by (2.14),

$$\varphi[A(t)] = \frac{\alpha|A(t)|^q}{1+(\frac{|A(t)|}{\beta})^q}, \tag{2.14}$$

where α, β and q are fitting parameters.

2.5.2 MEMORY EFFECT NON-LINEAR MODEL

As stated previously, if the AM-AM and AM-PM non-linearities are affected by both the current and previous input values, then the PA suffers from memory effects. There are two main types of memory effects, viz. electrical and thermal memory effects [41], and these will be discussed in the following subsections.

2.5.2.1 Electrical memory effects

This form of memory effect is caused by non-constant node impedances within the frequency bands. The node impedance is the impedance level at the node. The CE BJT amplifier is shown in Figure 2.10.

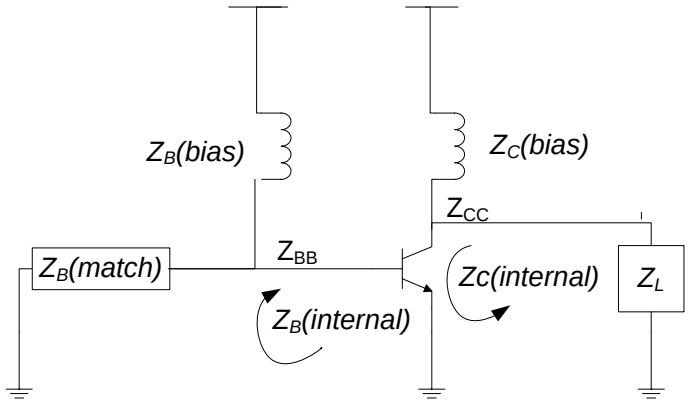


Figure 2.10. CE BJT amplifier schematic [41]. © 2003 Artech House, Inc.

In Figure 2.10, $Z_B(match)$ is the matching impedance, $Z_B(internal)$ is the internal base impedance and $Z_B(bias)$ is the base bias impedance. The total impedance at the base is shown in (2.15):

$$Z_{BB} = Z_B(match)||Z_B(internal)||Z_B(bias). \quad (2.15)$$

$Z_C(bias)$ is the collector bias impedance, $Z_C(internal)$ is the internal collector impedance and Z_L is the load impedance. The total impedance at the collector is shown in (2.16):

$$Z_{CC} = Z_L||Z_C(internal)||Z_C(bias). \quad (2.16)$$

By analogy, the node impedance at the gate and drain for a MESFET amplifier can be calculated with (2.17) and (2.18) respectively,

$$Z_{GG} = Z_G(match)||Z_G(internal)||Z_G(bias), \quad (2.17)$$

$$Z_{DD} = Z_L||Z_D(internal)||Z_D(bias). \quad (2.18)$$

These non-constant impedances are due to the bias networks of the transistors that cannot be made wideband and therefore these impedances change with frequency. Electrical memory effects mostly affect wideband systems [41]. In [8], memory effects were reduced using a high drain bias voltage, as well as a wide bias line and several decoupling capacitors.

2.5.2.2 Thermal memory effects

Thermal memory effects are generated by the junction temperature [42]. The junction temperature of the transistor can be expressed in (2.19):

$$T_j = T_{amb} + R_{th}.P_{dissip} + Z_{th}(\omega_1 - \omega_2).P_{dissip}(\omega_1 - \omega_2). \quad (2.19)$$

The temperature at the junction consists of three components, viz. the ambient temperature, the thermal resistance multiplied by the DC power dissipation and the envelope signal multiplied by the thermal impedance at the same frequency [42]. This shows that the temperature fluctuates as a function of the bandwidth of the signal and changes the electrical characteristics of the transistors and other components, resulting in variations in the generated distortion components. Thermal memory effects generally affect systems using narrowband signals [41, 42].

2.5.2.3 Volterra series analysis

The Volterra series analysis is an extension of the Taylor series analysis and is a powerful tool used for modelling and calculating the distortion components of weakly non-linear systems with memory effects. Weakly non-linear systems can be defined quite accurately up to the first three terms. The analysis can be described in both the time domain and frequency domain for RF behavioural models of PAs. The frequency domain is preferred because the non-linearity components can be analysed better. The non-linearities are described as polynomials on the *i-v* and *Q-V* functions and the method is independent of semiconductor physics.

The Volterra time series model that describes the distorted output signal is shown in (2.20):

$$D(t) = \sum_{n=0}^{\infty} D_n(t), \quad (2.20)$$

where $D_n(t) = \int_{-\infty}^{\infty} \dots \int_{-\infty}^{\infty} h_n(\tau_1, \dots, \tau_n) x(t - t_n) d\tau_1 \dots d\tau_n$.

The functions $h_n(\tau_1, \dots, \tau_n)$ are the *n*-th order Volterra kernels. The Fourier series is then applied to the time domain to transform (2.20) into the frequency domain, as shown in (2.21):

$$H_n(\omega_1, \dots, \omega_n) = F\{h_n(\tau_1, \dots, \tau_n)\}, \tag{2.21}$$
$$= \int_{-\infty}^{\infty} \dots \int_{-\infty}^{\infty} h_n(\tau_1, \dots, \tau_n)\, x(t - t_n) e^{-(s_1\tau_1 + \dots + s_n\tau_n)} d\tau_1 \dots d\tau_n,$$

where H_n is the frequency domain Volterra kernel and $F\{\cdot\}$ is the Fourier transformation.

These kernels can completely characterise a system. The disadvantage of the Volterra series analysis is that for strong non-linear systems such as Class C PAs, the sum may begin to diverge and a solution may not be possible. Therefore the Volterra series analysis can only be used for weakly non-linear systems.

There are other simpler non-linear models that take into account memory effects such as the Wiener, Hammerstein and memory polynomial non-linear models. These models are variations of the Volterra series model and have limitations because of their simplified approach in characterising the system.

2.6 REDUCING DISTORTION IN PAS

In many applications, the distortion at full output power should be minimised. One approach is to reduce the PA's output power, which is known as back-off. This improves the linearity of the PA and reduces the distortion at the expense of efficiency [15, 17]. At mm-wave frequencies this should be avoided, as efficient PAs are needed. To reduce distortion, an external linearisation technique is needed. The basic idea is to operate the PA as close to saturation as possible to maximise its power efficiency, and then use some linearisation technique to suppress the distortion generated at the saturated region. Many linearisation techniques are used in practice, such as feedback, feedforward, linear amplification with non-linear components (LINC), envelope elimination and restoration (EER), digital and analogue predistortion.

Feedback is the simplest method of reducing PA distortion. It uses the difference between the PA's input and output signal to compensate for the distortion components. Feedback linearisation can reduce the distortion as long as the feedback loop has sufficient loop gain. The feedback technique can be divided into four categories, viz. envelope, Cartesian, polar and RF feedback [43]. Cartesian feedback is widely used in PA linearisation; it is a

baseband feedback linearisation technique and strictly speaking should be referred to as a transmitter linearisation technique. Current Cartesian feedback techniques have been able to achieve 8.2 dB ACLR suppression [44] and 10 dB distortion reduction in [45].

Feedforward linearisation is similar to feedback, but instead subtracts the difference between the PA input and output signal from the PA output signal. Feedforward has the ability to linearise a wide bandwidth and it is unconditionally stable. The disadvantage of feedforward is the complexity of the system. However, current feedforward techniques have tried to reduce this complexity by performing the feedforward function in a DSP, resulting in ACLR improvement of 10 dB [46].

The LINC technique decomposes the amplitude varying signal into two out-phased constant envelope signals. These two signals are then amplified using high-efficiency switching mode PAs and then combined to generate a linear amplified version of the input signal. The LINC system in [47] has reported a 15 dB reduction in ACPR. The EER technique separates the input signal into two signals, viz. the amplitude and the phase. The phase signal is passed through a non-linear amplifier while the amplitude is removed. The amplitude is then returned onto the carrier by modulating the power supply of the PA. Similar to LINC, the drawback of EER is managing the synchronisation between the amplitude and the phase signals. A PA with a carrier frequency of 100 MHz using the EER technique has obtained an attenuation of the IMD3 component by 40 dB [48].

Among the various linearisation techniques discussed, predistortion is the most attractive and promising linearisation technique in mm-wave frequencies because of the advantages of small size, low complexity and low cost. The predistortion technique generates the inverse characteristic function of the PA to extend the linear output power region [10]. The disadvantage is that accurate modelling of the PA is needed in order to generate the inverse transfer function of the PA. However, with the use of proper behavioural models, accurate characterisation of the PA can be obtained. The use of APD can also be used to control the PA better.

2.6.1 PREDISTORTION LINEARISATION OPERATION

The predistortion linearisation technique can successfully correct the distortion of the output signal from a PA. The predistorter generates a linear amplified amplitude and constant phase output, as shown in (2.22) and (2.23):

$$A_{PD}(v_{in}) \cdot A_{PA}(v_{pd}) = C, \tag{2.22}$$

$$\emptyset_{PD}(v_{in}) + \emptyset_{PA}(v_{in}) = P, \tag{2.23}$$

where v_{in} and v_{pd} are the input signals to the predistorter and PA respectively and A_{PD} and A_{PA} are the amplitude transfer functions of the predistorter and the PA respectively. $\emptyset_{PD}$ and $\emptyset_{PA}$ are the phase transfer functions of the predistorter and PA respectively. C and P are the linear amplitude and phase constants respectively. The amplitude predistortion linearisation operation is graphically shown in Figure 2.11.

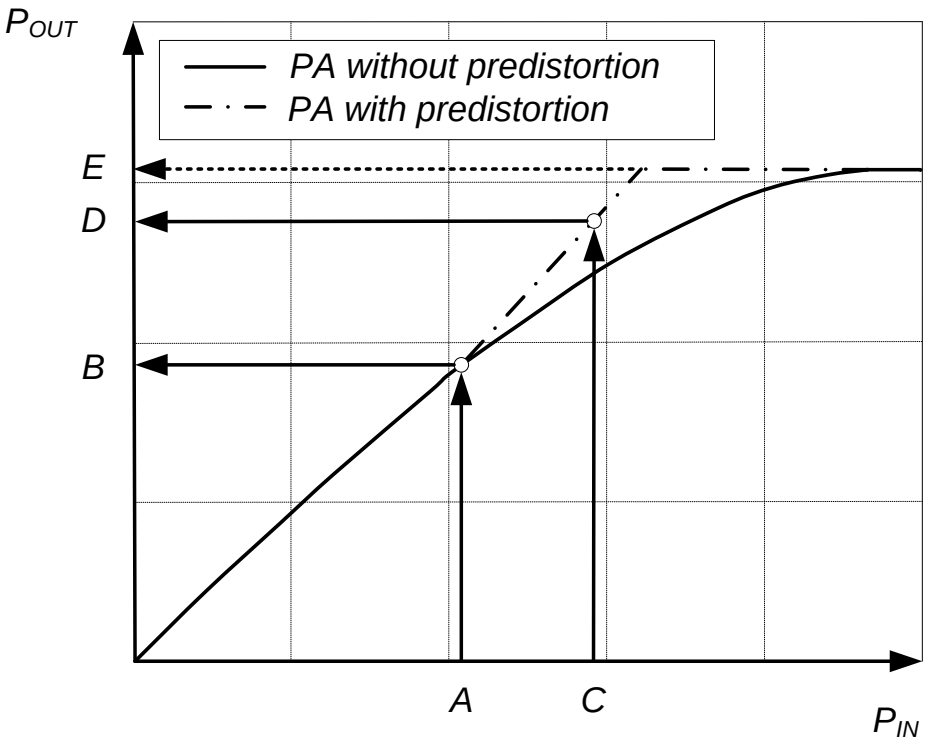


Figure 2.11. Predistortion operation.

In Figure 2.11, points *A* and *B* are the input and output power of the PA respectively without predistortion. The PA cannot operate in the non-linear region, as this will generate distortion in the output. With predistortion applied, the PA can operate at a much higher

operating point (point *C*), resulting in output power at point *D*. The distortion in the output signal can be corrected up to the saturation level. The intersection between the linear response and the saturation limit (*E*) is the maximum allowable input power for correction with predistortion [49].

2.6.2 TYPES OF PREDISTORTION

Predistortion linearisation can be divided into two techniques: digital and analogue predistortion. Analogue predistortion can be applied to the baseband or the intermediate frequency (IF)/RF signal. Baseband analogue predistortion implementations have been rare because the accuracy and matching of the predistortion function are difficult to achieve [41, 43]. Both IF and RF predistortion operate similarly, the only difference being the location of the predistorter. In the IF predistortion system, the predistorter is located before up-conversion while in RF, the predistortion circuit is located after up-conversion.

Analogue predistortion uses a non-linear device that aims to produce inverse non-linearity components to cancel the non-linearity of the PA. Existing models of on-chip analogue predistortion use a cubic predistorter or a diode to generate the distorted signal. There are quite a few types of analogue predistortion circuits; however, most of them are variations of these two general types of predistortion circuits. A typical cubic predistorter is shown in Figure 2.12.

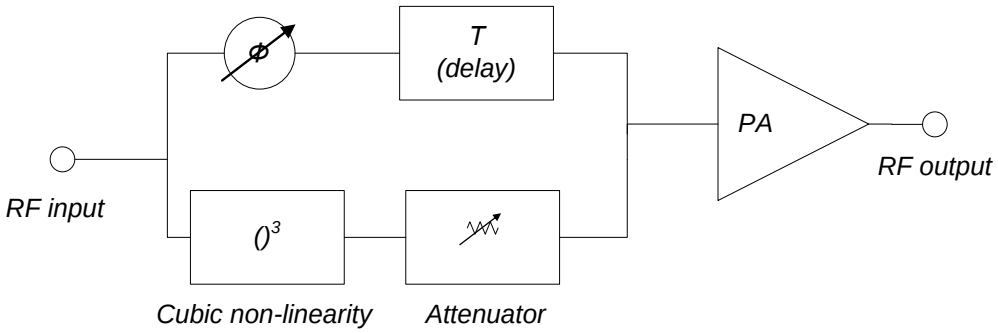


Figure 2.12. A general cubic predistorter.

The general form of the cubic predistorter is shown in Figure 2.12. It uses diodes in an anti-parallel form to generate the IMD3 components [5, 50]. The input signal is split into two paths using a directional coupler. The one path consists of the distortion generator and

attenuator. In the other path, the input signal is phase-shifted and delayed, so that the original signal and the distorted signal are 180 ° out of phase, but synchronised. The two signals are then recombined and passed through the PA. Much work [5, 8, 51] has been done on enhancing the cubic predistorter to extend its linearisation capabilities to include multi-order distortion components. Typical ACLR reductions with multi-order predistortion linearisers are 16.1 dB [5] and 16.4 dBc [8].

Another approach used for analogue predistortion is the use of the cold-mode MOSFET lineariser. The cold-mode MOSFET is a passive device and requires large input power to drive the transistor for gain expansion. It has been implemented with a 60 GHz PA, and an optimum improvement of 25 dB is achieved for the IMD3 component [10].

Traditional digital predistortion uses algorithms in a DSP to adjust the transmitted baseband signal to reduce the distortion in the PA. These algorithms correct the non-linearities of the PA by using a LUT. The advantage of digital baseband predistortion (DBPD) is that it is fully implemented in the digital domain and this offers great flexibility for the predistortion algorithms.

The disadvantage of using DBPD is that in its signal path there are up-conversion functions, quadrature modulators and mixers. Therefore the DBPD has to take into account and compensate for the non-linearities of the oscillators, mixers, filters and other non-linear analogue components, as well as the PA. Existing DBPDs [52] and [53] have reported an ACPR improvement of 19.3 dB (using the memory polynomial method) and an ACLR improvement of 15 dB respectively.

2.6.2.1 APD

The typical predistorter operates in an open-loop approach and applies the inverse transfer function of the PA to the PA. To have better control of the predistortion, feedback from the PA to update the predistortion function is needed. Similar to the non-adaptive DBPD, the adaptive DBPD (ADBPD) is a complete transmitter lineariser technique because the input signal is baseband and the predistortion includes an additional receiver for down-conversion and a signal processor for the algorithm to update the predistortion function [9, 54]. It is unnecessarily complex because it has to compensate for the non-linearity of all the transmitter subsystems. In [9], the authors have demonstrated a 60 GHz

PA with ADBPD, achieving an EVM of -28 dB with 7 dB back-off power. On the other hand, the adaptive digital RF predistortion (ADRFPD) focuses only on the RF signal and on the PA. Figure 2.13 shows the block diagram of the ADRFPD.

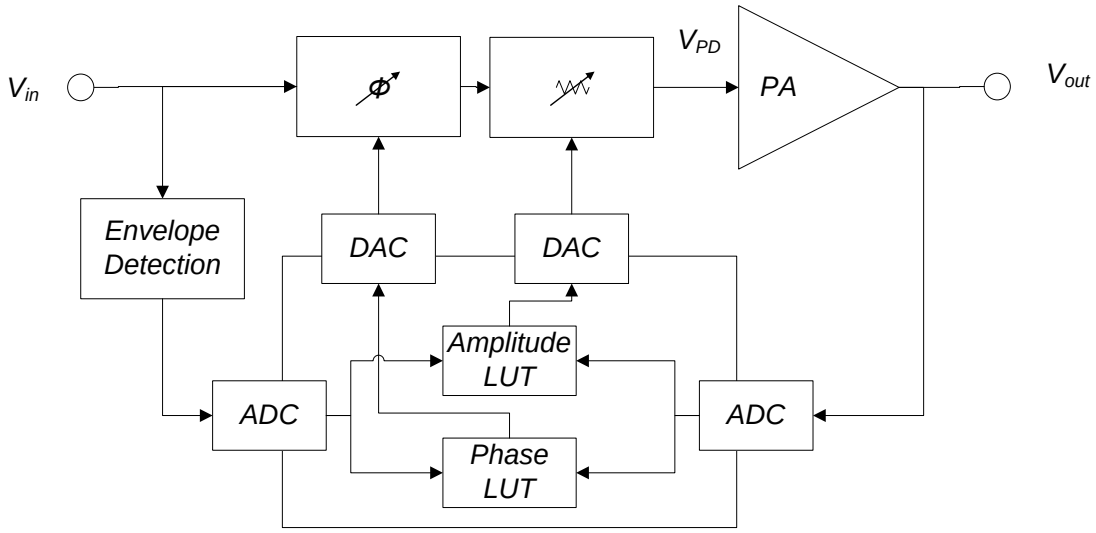


Figure 2.13. ADRFPD using amplitude and phase modulators.

The feedback is implemented in such a way that the predistortion output is updated slowly, reducing instability. The predistorter can consist of amplitude and phase modulators, as shown in Figure 2.13, or quadrature modulators. In Figure 2.13, the input signal passes through an envelope detector and is down-converted and converted into digital format using the ADC. At the output of the PA, the output signal is fed back to a predistortion function using another ADC. Both the input and output signals are usually compared and a predistortion algorithm is applied to the amplitude and phase separately and converted into analogue format and upconverted. This signal is then applied to the PA.

This adaptation process is usually implemented in the digital domain using a LUT. The performance of this adaptation is dependent on the size and indexing of the LUT and adaptation methods used by the LUT. The size is a very important aspect of the LUT-based predistorter. The larger the LUT, the more data entries it can hold, therefore more linearity can be achieved. However, this increases the physical size of the LUT.

Existing ADRFPDs have shown excellent PA linearity improvements. [7] showed a 20 dB ACPR improvement, while [6] reported a 15 dB ACPR improvement. Another form of ADRFPD is the use of a variable gain amplifier (VGA) to realise the predistortion function. The gain expansion characteristic of a PA can be controlled using a dynamic biasing circuit to provide the inverse PA transfer function to the PA. Recently, [11] showed that a minimum IIP_3 of 7.5 dBm can be achieved using this approach for a 1.95 GHz PA. To the author's knowledge no adaptive RF predistortion linearisation techniques have been used at 60 GHz.

2.7 CONCLUSION

Spectral efficient modulation schemes such as OFDM require stringent linear PAs in order to increase data rates. PA linearity performance is heavily dependent on the distortion components. Distortion components such as IMD3 have proven to degrade the performance of the PA severely, resulting in spectral regrowth.

Reducing distortion in order to improve the linearity in PAs is becoming a key area of focus. Various linearisation techniques currently exist, with APD linearisation being the most attractive because of its ability to control the predistortion function. The control circuitry in the digital domain is a challenge with APD. However, the use of the SiGe BiCMOS process allows the flexibility of designing digital elements with analogue components, making the APD possible at mm-wave frequencies.

CHAPTER 3 RESEARCH METHODOLOGY

3.1 INTRODUCTION

This chapter details the methodology used to investigate and improve the linearity of a PA specifically at 60 GHz using an APD linearisation technique. A PA with APD at 60 GHz was implemented using the SiGe BiCMOS process. Testing and verifying the hypothesis was done throughout the design process.

3.2 JUSTIFICATION FOR THE PARADIGM AND METHODOGOLY

In any PA designed at mm-wave frequencies, the importance of optimising the key metrics such as output power, gain, linearity and efficiency cannot be over-emphasised, specifically linearity, as it is directly related to the output power, gain and efficiency of the PA. Predistortion has been proven to be a very effective way to reduce the non-linearities, especially IMD3 components, in PAs. APD is an improvement on the existing analogue predistortion linearisation technique, as it is able to optimise the predistortion function. This approach alleviates the problem that is associated with conventional analogue predistortion circuits, which have a static predistortion function.

Careful analysis and investigation of the PA therefore needs to be conducted, as the design of the APD circuit is be based on the characteristics of the PA. A prototype of the complete PA and APD has also been fabricated to analyse and verify the measurement performance with the mathematical and simulated results. Subsequently the hypothesis was tested in practice.

3.3 OUTLINE OF THE METHODOLOGY

The research methodology used in this thesis is shown in Figure 3.1.

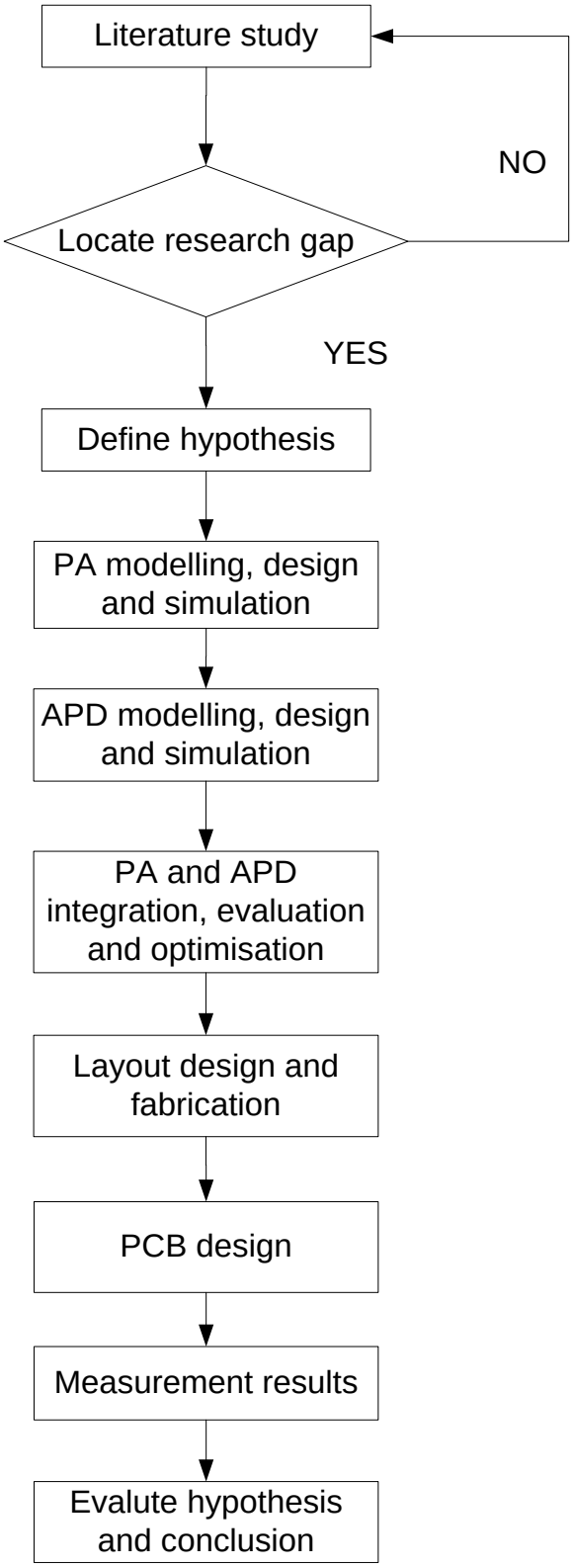


Figure 3.1. Flowchart illustrating the research methodology.

The research methodology shown in Figure 3.1 can be grouped into theoretical background, mathematical modelling and simulation, layout, testing and hypothesis evaluation. These are described in more detail below:

- Theoretical background: The initial part of the research methodology process involved the literature study that looked at the current body of knowledge and challenges in improving the linearity of PAs. This was then extended to applications at 60 GHz. Once a research gap had been found, a hypothesis was formulated to address this research gap.
- Mathematical modelling and simulation: The next stage focused on the modelling, design and simulation of the PA and APD. Mathematical models of the components together with manual calculations were used to obtain an initial estimate of the performance of the PA and APD. At mm-wave frequencies and with the scaling down of components, especially transistors, this led to certain assumptions and approximations being invalid. This resulted in models becoming more complex and at a certain point manual calculations becoming cumbersome. Simpler mathematical models, e.g. small-signal models, were therefore used to obtain initial estimates of output power, gain and stability of the PA. These models were then improved upon using the process parameters from the PDK in the CAD tools (which are discussed below) and further investigations and analysis were performed and compared to the mathematical results. Once satisfactory results from the PA had been achieved, the APD was designed. The function of the APD is to improve the linearity of the PA and it was therefore integrated with the PA. Once the entire system had been evaluated and verified, the layout was performed.
- Layout: As this research is focused at 60 GHz, poor floor planning will introduce unnecessary, additional parasitics and hinder the overall performance of the system. To minimise these effects, careful planning of the layout of the components was performed. Design rule check (DRC), layout versus schematic (LVS), pattern density (local and global) and antenna checks were done and passed successfully. The completed layout was then sent for fabrication to obtain measurement results.

The prototyped IC was then wirebonded onto a custom printed circuit board (PCB) to perform measurements. The measurement results were used to evaluate and verify the

hypothesis on a practical level. In essence, to test the hypothesis, the following data were needed:

- PA and APD: A PA was designed and integrated with the APD. This was fabricated on an MPW run to evaluate the performance of the PA with the APD together.
- PA: An identical PA as the one mentioned above was also fabricated on the same MPW run, but completely isolated from the PA and APD system. This was done to characterise and evaluate the performance of the PA only and to provide a comparative analysis of the PA and APD results.

The hypothesis for this thesis is the effectiveness of the APD in improving the linearity of the PA at mm-wave frequencies. The theoretical, simulation and measurement results all test the linearity of the PA as well as other metrics and therefore test the hypothesis as well.

3.4 PA AND APD DESIGN METHODOLOGY

The fundamental function of the PA in this research (and in general) is to deliver highly linear output power at mm-wave frequencies. Apart from this key metric, there are other metrics that are important and are inter-related, as shown in Figure 3.2.

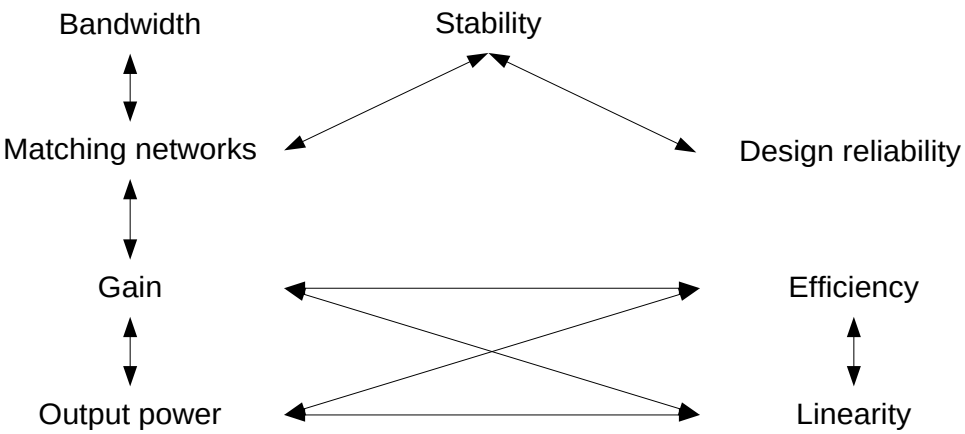


Figure 3.2. Key PA metrics.

Each of these metrics shown in Figure 3.2 should be optimised to achieve the best performance of the PA. This makes the design of the PA a challenging task. Some metrics, such as linearity, are best improved upon using an external linearisation technique and in this research the APD is used to fulfil this task. This therefore allows some PA design requirements to be relaxed, such as class of operation, matching network topology and PA architecture. The design flow for the PA in this thesis is shown in Figure 3.3.

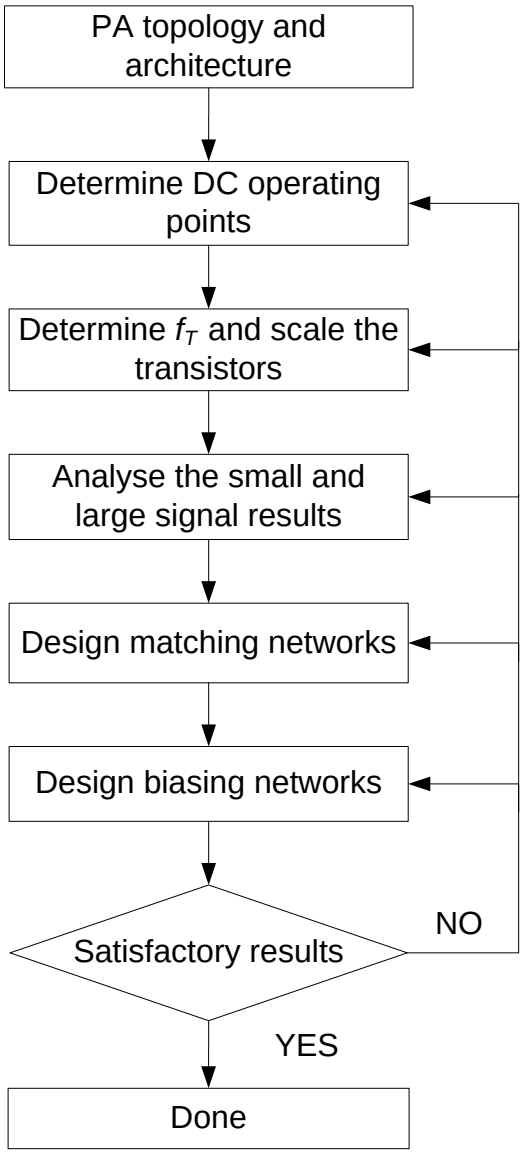


Figure 3.3. PA design process.

The circuit topology and the class of operation of the PA were selected before the design commenced as illustrated in Figure 3.3. A CE and a single-ended PA were used, as this would provide sufficient gain and meet the measurement requirements. The Class AB

operating class was chosen to address the efficiency trade-off while compromising linearity and gain, which would eventually be compensated for by the APD.

The PA performance is directly related to the capabilities and limitations of the models provided by the foundry. The initial output power of the PA was determined using the load-line approach. The output power determines the bias current and voltages, i.e. the DC bias conditions. The transistors were then scaled according to their current output capabilities.

Hybrid-π and -T transistor models can be used to roughly approximate the two-port parameters of the input and output matching networks using the component values provided from the foundry. The foundry does not provide data for every transistor size, as this can become impractical. A more useful and accurate method of determining these impedance values was performed using the load-pull and source-pull analysis, as explained in [33]. From these analyses, the optimal output power of the PA and DC bias conditions were also obtained. The next step was to conduct small-signal and large-signal simulations and from this it was realised that additional gain stages were needed. Each stage was therefore optimally matched using the results from the load-pull, source-pull, small-signal and large-signal results. The bias networks were finally added at the end of the design process. The entire design was then evaluated and the design process was optimised until satisfactory results were obtained.

The predistortion design used in this thesis is an APD solution. The APD measures the output power of the PA and provides a feedback voltage control signal to the VGA located in the PA. As the input power increases, so does the output power until saturation is reached. The APD slowly increases the gain of the PA as the input power increases, until the point of saturation. This results in higher linear output power.

3.5 SIMULATION SOFTWARE

The main software package used in the modelling and simulation of all the subsystems of the PA and APD was Cadence Virtuoso. The Cadence suite is a complete simulation and

layout software suite. Additional software tools were used to realise the entire system practically. Each of these software tools is presented in Table 3.1.

Table 3.1. Summary of software packages used.

Package Name	Functionality
Cadence Virtuoso Schematic Editor	Circuit schematic design.
Analog Mixed Signal (AMS)	Simulation program with integrated circuit emphasis and spectre simulator.
Cadence Virtuoso Layout Editor	Circuit layout design.
Cadence Assura	DRC, LVS, pattern density (local and global), antennas checks.
MATLAB	Initial mathematical modelling and post-simulation analysis.
Double CAD XT and Eagle	PCB design and layout.

The modelling and design of the PA and APD were initially done using manual analysis and MATLAB (Table 3.1). MATLAB provided a first-round performance analysis of the PA, specifically modelling the matching networks using the two-port approach. These mathematical models were then translated into schematic models using Cadence's schematic editor. The technology files provided by the foundry, which contained physics-based models, process parameters and DRC, were extracted and integrated into the Cadence software suite. This allowed the ideal components to be replaced with the PDK components using the Cadence schematic editor.

The AMS simulator within Cadence allowed various simulations to be conducted, viz. DC, parametric, transient, periodic steady state (PSS), periodic alternating current (PAC) and frequency simulations. Once all the simulations had been completed, the layout of the entire IC was compiled using the layout editor in Cadence. Since the functionality and performance of the entire system depends on the circuit layout, DRC and LVS checks were conducted. The DRC was performed to verify that all the component models adhered to the foundry's requirements. The LVS checks ensured that the layout matched the schematic net lists accurately. Pattern density and antenna checks were performed in accordance with the design manual to ensure chip reliability. All these tests and checks were done using the Assura tool in Cadence and after passing successfully, the layout of the IC was submitted for fabrication.

Double CAD XT and Eagle were used in the design of the PCB. The PCB provides a placement for the prototyped IC to allow measurements to be done.

3.6 MANUFACTURING PROCESS

The technology process used in this thesis is the IBM 0.13 µm SiGe (BiCMOS8HP) technology. All the models in this process are physics-based, scalable compact models allowing the designer a great deal of flexibility and excellent model accuracy [55]. Process parameters are protected by a non-disclosure agreement (NDA).

All the simulation models were based on the PDK and associated process parameters from this technology. The BiCMOS8HP technology process provides a complete suite of devices and allows the use of both HBT and CMOS active devices in the simulation models. The features of this technology process are listed below.

BiCMOS8HP technology features:

- SiGe HBT:
  - High performance HBT: $f_T = 210$ GHz, $BV_{CEO} = 1.7$ V.
- CMOS transistor:
  - $V_{DD} = 1.2$ V (thin triple-well N-type field effect transistor (NFET)).
  - Dual gate oxide with physical thickness of 2.2 nm and 5.2 nm.
- Resistors: p+ poly and NS.
- Bondpads: C4 and wirebond.
- TLs.
- Seven metal layers of Cu and Al metal:
  - Four layers of thin 1x Cu.
  - One layer of thick 2x Cu.
  - Two layers of thick Al.
- Wiring layer vias: V1, V2, V3, VL, VY and AV.
- CMOS transistor:
  - → $V_{DD} = 2.5$ V (thick oxide triple-well NFET).
- MIM capacitors.

- Hyper-abrupt junction varactors.
- High value poly and TaN back-end-of-line (BEOL) resistors.

Apart from the technology files, the following files were provided by the foundry and are listed in Table 3.2:

Table 3.2. List of files used in Assura.

Filename	Purpose
drc.rul	Design rule check.
float.rul	Floating gate, NW, Pwell, pad and antenna rules.
global.rul	Global pattern density check.
local.rul	Local pattern density check.
extract7.rul	Parasitic extraction and LVS check for the 7 metal levels.

These files listed in Table 3.2 were needed to verify that the models used were within their specifications and design rules when validating the circuit layout. The foundry also provided the accurate parametric cells (*p*-cells) for each of the devices. The *p*-cell for each device is updated according to the device configuration, size or geometry and is accessed in the layout. This provides design flexibility. Seven metal layers are available in this particular technology process and were used in the simulation models and layout.

3.6.1 SIGE HBTS

The SiGe HBT used in the design has a f_T > 200 GHz and is well suited for PA applications at 60 GHz. The major design constraint with SiGe HBTs is the low breakdown voltage, which reduces the available output power. The process parameters of the SiGe HBT cannot be provided due to the NDA.

The RF power gain decreases with increasing emitter size. Therefore a multistage PA was needed to increase the overall power gain. The largest HBT size was used in the last stage of the PA to ensure maximum output power. In terms of linearity, the SiGe HBTs have the best performance, as mentioned in chapter 2, and this metric was improved upon in the PA using the APD.

3.6.2 MIM CAPACITORS

MIM capacitors are used throughout the design of the PA and APD. The structure of the MIM capacitor is shown in Figure 3.4.

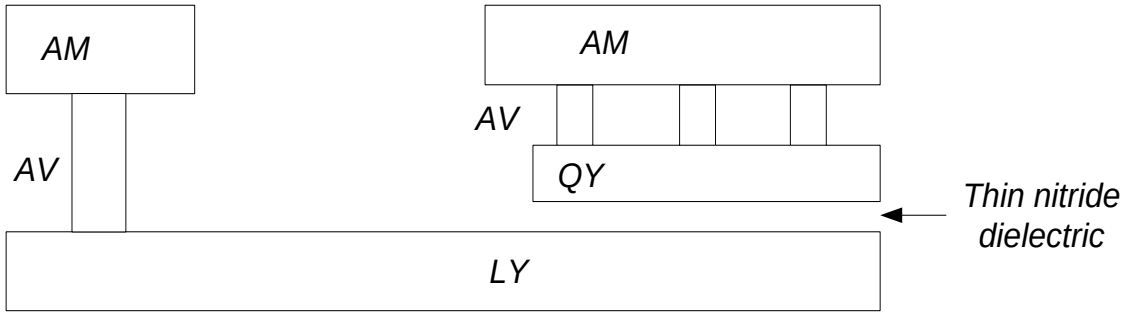
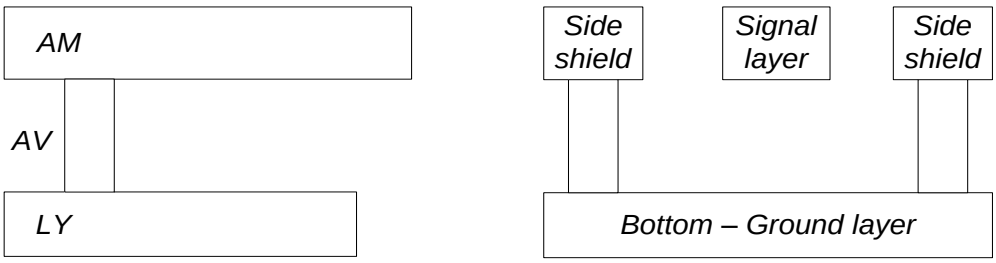


Figure 3.4. Cross section of the MIM capacitor.

This capacitor is formed by placing a thin nitride dielectric layer between the metal layer QY and LY as shown in Figure 3.4. The QY layer is the top plate of the capacitor. The widths and lengths of the MIM capacitor are design variables and the aspect ratio must adhere to the design specification which is protected by the NDA.

3.6.3 TLS

TLs form part of the matching and DC biasing networks. The PDK provides many forms of TLs, such as microstrip TLs (single and coupled wires), as well as co-planar waveguide TLs (single and coupled wires). Single-wire microstrip TLs with side shielding were used in the design to satisfy the matching and biasing requirements. The structure of this microstrip TL is illustrated in Figure 3.5.



(a) (b)

Figure 3.5. The AM/LY microstrip TL showing **(a)** the BEOL conducting and interlevel film thickness (protected by the NDA) and (**b)** the cross-section.

From Figure 3.5 it can be seen that only two metal layers with side shields were used in the microstrip TL, viz. AM (signal layer) and LY (bottom shield layer). The length, width and side shield width of the TLs are design variables.

3.7 MEASUREMENT EQUIPMENT

Fabrication of the design was conducted to obtain additional data in terms of actual measurement information to validate the hypothesis. The prototyped IC in this thesis was part of an MPW run provided by Metal Oxide Semiconductor Implementation Service (MOSIS). The IC is designed to operate at mm-wave frequencies and therefore all measurements were done at 60 GHz. This poses a problem because typical IC packaging such as the ones used at lower frequencies cannot be used at 60 GHz. The reason is that additional parasitics resulting from unmatched impedances due to the wirebonds will severely affect the performance of the PA at 60 GHz. Instead, on-wafer measurements need to be conducted. This entails the use of an on-wafer probe station and high-fidelity measurement equipment. A custom PCB was manufactured to provide the DC bias from an external power supply to the IC. The custom PCB is shown in Figure 3.6.

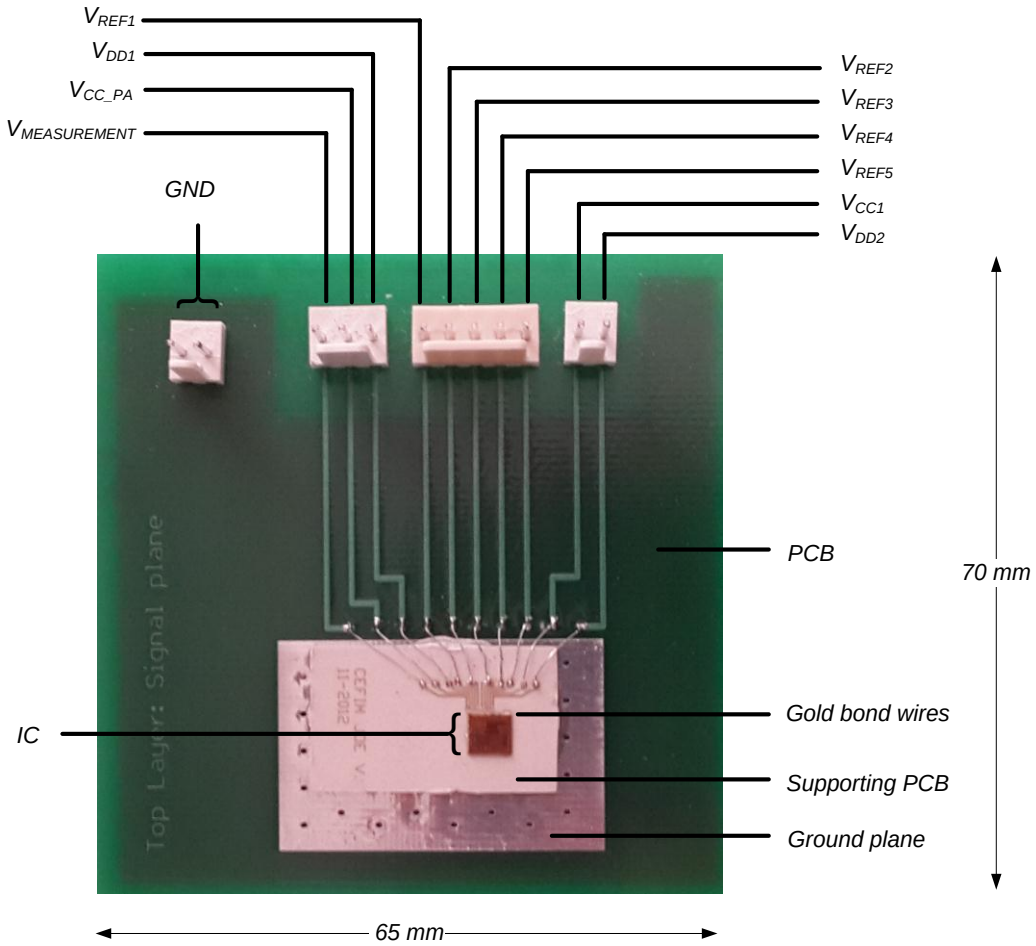


Figure 3.6. Custom PCB.

Three PCBs were manufactured with dimensions of 70 mm by 65 mm, as shown in Figure 3.6. The IC was first baked onto a supporting PCB and gold wirebonds were used to connect the PCB pads to the bondpads on the IC. The supporting PCB was then placed onto a larger PCB.

The on-wafer probe station consists of wafer probes that are lowered onto the RF input and output contact points, i.e. the bondpads on the IC. The layout of the bondpads is therefore crucial to allow the wafer probes to connect correctly and interface to the rest of the IC. Square bondpads were placed around the IC. The bondpads on the left and right of the IC are meant for the wafer probes. The bottom bondpads are for the DC connections. This orientation was used to prevent the wafer probes and DC wirebonds from coming into contact with each other, which can damage the wafer probes and wirebonds.

The wafer probes have a ground-signal-ground (GSG) format. This meant that each RF input and output contact needed three bondpads to satisfy the wafer probe GSG format. Another important requirement set out by the probes was the probe pitch, which effects the RF input and output bondpad's size and position. These bondpads cannot be very large, as this will introduce unnecessary parasitics and also cannot be too small, as they must meet the minimum requirement of probe pitch. The bondpads used were 100 µm by 100 µm in size and were positioned to meet the requirement of the probe pitch. The parasitics associated with this size were included in the design of the matching networks of the PA. The probes used for the measurement are shown in Figure 3.7.

Figure 3.7. The i110 GSG Infinity probe.

The probe shown in Figure 3.7 is the i110 probe from Infinity Technologies in GSG format. It can operate between DC and 110 GHz and has a probe pitch of 150 µm. The vector network analyser (VNA) and wafer probe station used for the measurements are shown in Figure 3.8.

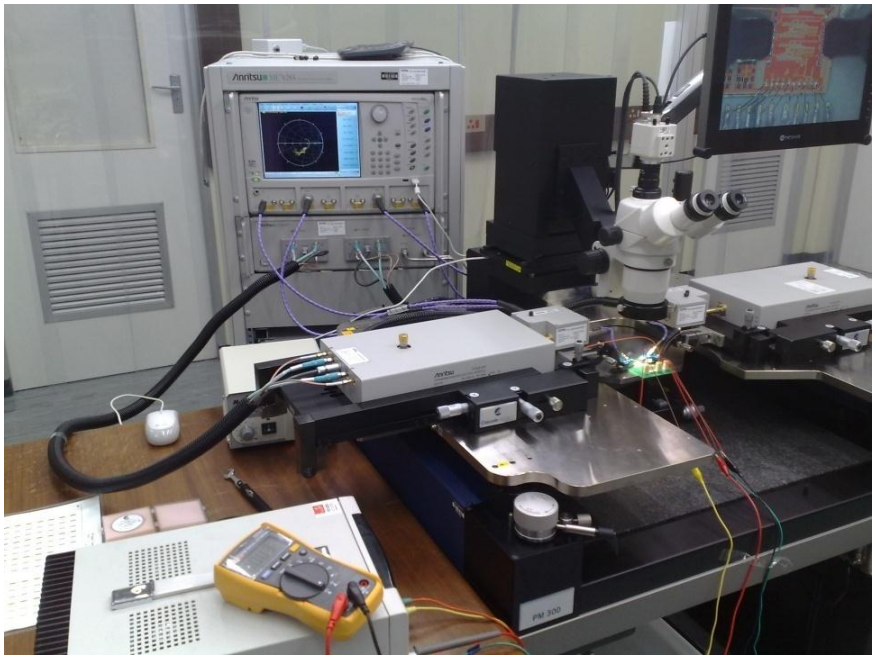


Figure 3.8. The Anritsu VectorStar ME7828A VNA and the PM 300 Cascade Microtech wafer probe station.

The measurement equipment used is the Anritsu VectorStar ME7828A VNA, which has an operating frequency range between 70 kHz and 110 GHz. The VNA is interfaced to the PM 300 Cascade Microtech wafer probe station as shown in Figure 3.8. The PS2-56-450/15S power divider from Pulsar Microwave Corporation was used to perform the two-tone linearity tests and is shown in Figure 3.9.

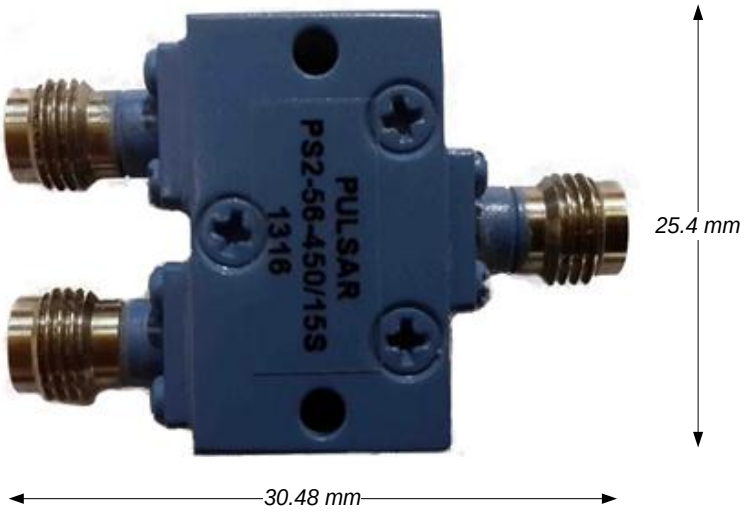


Figure 3.9. The PS2-56-450/15S power combiner.

The power combiner in Figure 3.9 operates between 8 GHz and 60 GHz and has a maximum insertion loss of 4 dB. The Topward 6303D power supply shown in Figure 3.10 was used to provide the bias voltages.

Figure 3.10. Topward 6303D power supply.

The power supply shown in Figure 3.10 was sufficient to provide the required bias conditions and was interfaced to the IC through the custom PCB.

3.8 MEASUREMENT SETUP

This section discusses the type of measurements and the procedures that were followed for each of the measurements. Before actual measurements could be done, the VNA, probe station and wafer probes were first calibrated using the contact substrate provided by Cascade Microtech. The measurement equipment was calibrated from 1 GHz to 80 GHz using the WinCal XE software with the short, open, load and through calibration technique. The measurement setup procedure for the PA and APD is described in Figure 3.11.

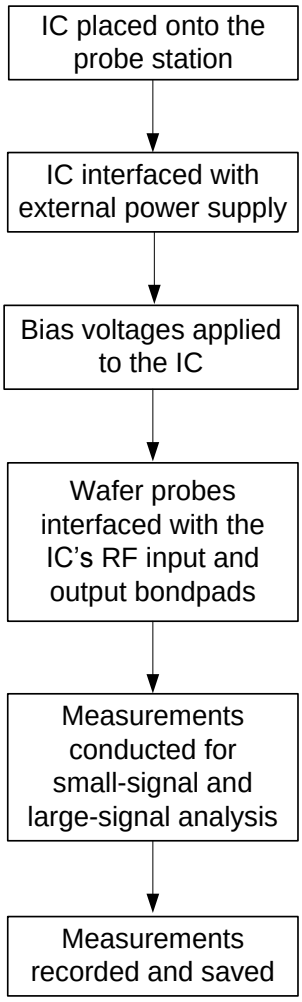


Figure 3.11. Measurement procedure for the PA and APD.

Once the IC had been placed on the probe station, an external power supply was interfaced to the IC through the custom PCB interface and then bias connections were applied to the IC as illustrated in Figure 3.11. After the correct bias voltages had been applied, the wafer probes were aligned with the IC's RF input and output bondpads and lowered onto these bondpads. Depending on the type of measurement, the relevant data were extracted, recorded and displayed on the VNA. The tests that were performed on the IC in order to validate the hypothesis are shown in Table 3.3.

Table 3.3. Measurement for PA only and PA with APD.

Measurement	Procedure	Expected results	
Large-signal analysis	To measure output power, sweep the input power range and measure the output power	PA Only:	Gain in dB, output power in dBm and efficiency of the PA

Measurement	Procedure	Expected results	
	at the load.		should be obtained.
		PA with APD:	Improvement when compared to the PA measurement.
Small-signal analysis	Measure *S*-parameters.	PA Only:	S_{21} > 0 dB, S_{11} < 0 dB, S_{12} < 0 dB, S_{22} < 0 dB.
		PA with APD:	Improvement when compared to the PA measurement.
Stability	Measure *S*-parameters.	PA Only:	k_f > 1 and B_1 > 0.
		PA with APD:	k_f > 1 and B_1 > 0.
Linearity	Sweep input power and measure output power. Note the 1 dB compression point.	PA Only:	Output power 1 dB compression point should be obtained.
		PA with APD:	Improvement when compared to the PA measurement.
IMD3	Two-tone test.	PA Only:	IMD3 should increase as RF input power increases.
		PA with APD:	Improvement when compared to the PA measurement.

The five measurements shown in Table 3.3 are the full suite of measurements required to evaluate the PA and the PA with the APD and therefore test and validate the hypothesis. Each of these measurements was conducted on the PA and on the PA with APD separately. The large-signal analysis measurements were done in order to determine the gain, output power and efficiency using the power meter connected to the VNA. Small-signal analysis

was done using the VNA to obtain the *S*-parameters and analyse the stability of the two systems. The first linearity measurement was done by determining the 1 dB compression point. The second linearity measurement was done using a two-tone signal to measure the IMD3 component. Once all the tests had been completed, the measured results were compared to the expected results and the hypothesis was evaluated.

3.9 CONCLUSION

Chapter 3 discussed the research methodology followed in this thesis to validate the hypothesis. Each step in the design and fabrication of the PA and APD is critical to ensure successful realisation of the design practically and correlate with the simulated results. A PA and APD were designed and simulated using the IBM 0.13 µm technology node on the schematic level with the Cadence software suite. The measurement equipment used, the measurement setup and the various tests to validate the hypothesis were also discussed in this chapter.

CHAPTER 4 MATHEMATICAL ANALYSIS

4.1 INTRODUCTION

The literature study in chapter 2 illustrated the dominant non-linear components of the HBT. In order to design the predistortion linearisation technique, a mathematical understanding of these non-linear components and how they relate to the IM distortion components should be obtained.

4.2 MATHEMATICAL ANALYSIS

The input signal is presumed to be small and therefore the non-linear components are described as weakly non-linear. To understand the behaviour of these non-linear components, Volterra series analysis is performed on the CE HBT model shown in Figure 4.1.

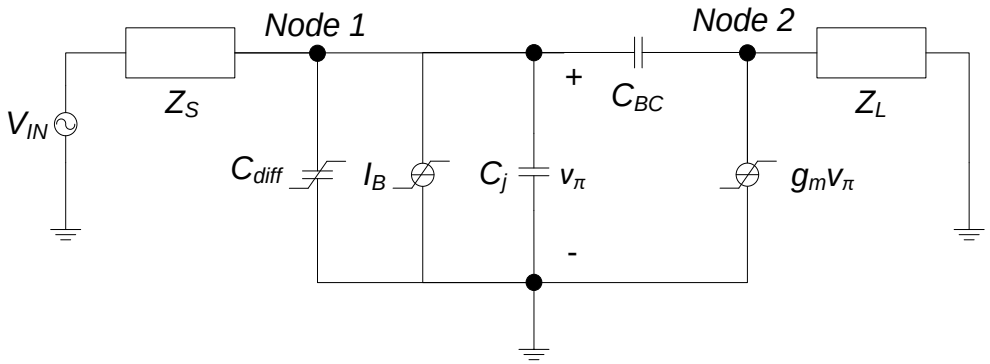


Figure 4.1. Non-linear model of a CE HBT.

As mentioned in chapter 2 and shown in Figure 4.1, I_C and I_B are both functions of the non-linear v_π and C_{diff} is assumed to be proportional to I_C. It is assumed that the base-collector capacitance, C_{BC}, and the base-emitter depletion capacitance, C_j, are linear.

The collector current is given by (4.1),

$$I_C = I_Q e^{\frac{v_\pi}{V_T}}, \tag{4.1}$$

where I_Q is the saturation current.

Using the Taylor series expansion, (4.1) can be represented in (4.2)

$$I_C = I_Q[\frac{v_\pi}{V_T} + \frac{1}{2}\left(\frac{v_\pi}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_\pi}{V_T}\right)^3 + \cdots]. \tag{4.2}$$

The Taylor coefficients are defined in (4.3) to (4.5):

$$g_{m1} = \frac{I_C}{V_T}, \tag{4.3}$$

$$g_{\pi 1} = \frac{g_{m1}}{\beta_f}, \tag{4.4}$$

$$C_{diff1} = \tau_F g_{m1}, \tag{4.5}$$

where $\beta_f = \frac{I_C}{I_B}$, $\tau_F = \frac{Q_{diff}}{I_C}$, Q_{diff} is the diffusion charge, C_{diff1} is the first order (linear) diffusion capacitance and V_T is the thermal voltage.

The non-linearity components can therefore be written in (4.6) to (4.8),

$$i_c(t) = g_{m1}v_\pi(t) + g_{m2}{v_\pi}^2(t) + g_{m3}{v_\pi}^3(t), \tag{4.6}$$

$$i_b(t) = g_{\pi 1}v_\pi(t) + g_{\pi 2}{v_\pi}^2(t) + g_{\pi 3}{v_\pi}^3(t), \tag{4.7}$$

$$q_{diff}(t) = C_{diff1}v_\pi(t) + C_{diff2}{v_\pi}^2(t) + C_{diff3}{v_\pi}^3(t). \tag{4.8}$$

Following Kirchhoff's current law in Figure 4.1 and converting the impedances to admittances result in the following matrix (4.9) [56]:

$$\begin{bmatrix} Y_S(s) + g_{\pi 1} + s(C_{diff1} + C_j + C_{BC}) & -sC_{BC} \\ g_{m1} - sC_{BC} & Y_L(s) + sC_{BC} \end{bmatrix} \begin{bmatrix} V_{11}(s) \\ V_{12}(s) \end{bmatrix} = \begin{bmatrix} Y_S(s)V_{IN} \\ 0 \end{bmatrix}, \tag{4.9}$$

where $V_{11}(s)$ and $V_{12}(s)$ refer to the first order Volterra kernels at nodes 1 and 2 respectively. With $V_{IN} = 1$, and using Cramer's rule to solve the above matrix, $V_{12}(s)$ can be obtained in (4.10):

$$V_{12}(s) = \frac{-Y_S(s)[g_{m1} - sC_{BC}]}{\det(Y(s))}, \tag{4.10}$$

where $\det(Y(s)) = (Y_L(s) + sC_{BC})[Y_S(s) + g_{\pi 1} + s(C_{diff1} + C_j + C_{BC})] + sC_{BC}(g_{m1} - sC_{BC})$ and $s = j\omega$.

The second-order non-linear components of the SiGe HBT are shown in Figure 4.2.

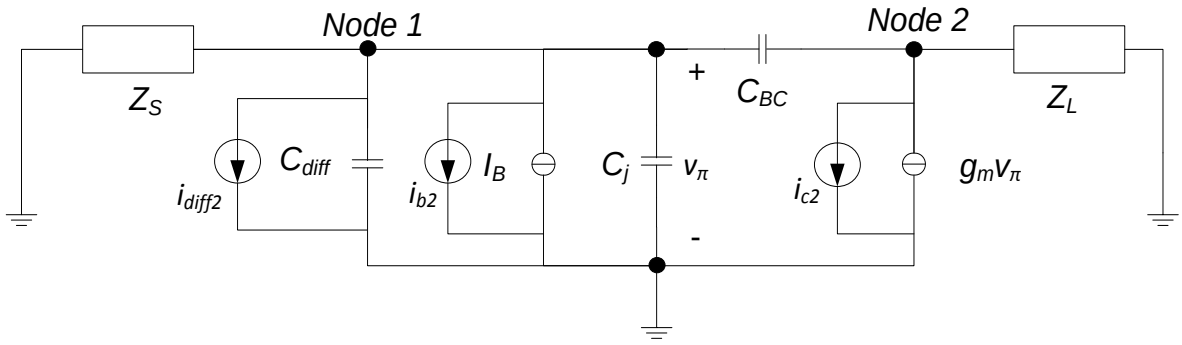


Figure 4.2. Second-order non-linear equivalent model.

The second-order Volterra kernels are obtained by placing the second-order non-linear currents and capacitors in parallel to the linear current sources and capacitors, as shown in Figure 4.2. The input voltage V_{IN} in Figure 4.1 is now shortened. The second-order non-linear diffusion current, i_{diff2}, the second-order non-linear collector current, i_{c2}, and the second-order non-linear base current, i_{b2}, as shown in Figure 4.2, are defined in (4.11) to (4.13):

$$i_{c2} = g_{m2}V_{11}(s_1)V_{11}(s_2), \tag{4.11}$$

$$i_{b2} = g_{\pi 2}V_{11}(s_1)V_{11}(s_2), \tag{4.12}$$

$$i_{diff2} = C_{diff2}V_{11}(s_1)V_{11}(s_2)(s_1 + s_2). \tag{4.13}$$

The second-order Volterra kernels are then obtained using Cramer's rule and are shown in (4.14) to (4.15):

$$V_{21}(s_1, s_2) = \frac{-(Y_L(s_1+s_2)+(s_1+s_2)C_{BC})(i_{b2}+i_{diff2})-(s_1+s_2)C_{BC}i_{c2}}{\det(Y(s_1+s_2))}, \quad (4.14)$$

$$V_{22}(s_1, s_2) = \frac{-(Y_S(s_1+s_2)+g_{\pi 1}+(s_1+s_2)(C_{diff1}+C_j+C_{BC}))i_{c2}+(g_{m1}-(s_1+s_2)C_{BC})(i_{b2}+i_{diff2})}{\det(Y(s_1+s_2))}. \quad (4.15)$$

Similar to the non-linear second components, the third-order non-linear components are placed in parallel to their linear components, as shown in Figure 4.3. The input voltage V_{IN} in Figure 4.1 is once again shortened.

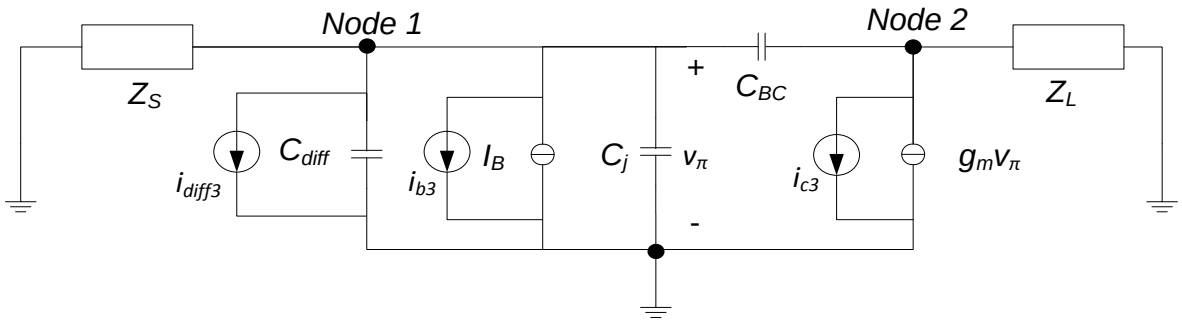


Figure 4.3. Third-order non-linear equivalent model.

The third-order non-linear collector current, i_{c3}, third-order non-linear base current, i_{b3}, and third-order non-linear diffusion current, i_{diff3}, as shown in Figure 4.3, are defined in (4.16) to (4.18):

$$i_{c3} = g_{m3}V_{11}(s_1)V_{11}(s_2)V_{11}(s_3) + 2g_{m2}\overline{V_{11}V_{21}}, \quad (4.16)$$

$$i_{b3} = g_{\pi 3}V_{11}(s_1)V_{11}(s_2)V_{11}(s_3) + 2g_{\pi 2}\overline{V_{11}V_{21}}, \quad (4.17)$$

$$i_{diff3} = (C_{diff3}V_{11}(s_1)V_{11}(s_2)V_{11}(s_3) + 2C_{diff2}\overline{V_{11}V_{21}})(s_1+s_2+s_3), \quad (4.18)$$

where $\overline{V_{11}V_{21}} = \frac{V_{11}(s_1)V_{21}(s_2,s_3)+V_{11}(s_2)V_{21}(s_1,s_3)+V_{11}(s_3)V_{21}(s_1,s_2)}{3}$.

The third-order Volterra kernel is shown in (4.19):

$$V_{32}(s_1,s_2,s_3) = \frac{-(Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j+C_{BC}))i_{c3}+(1-\frac{(s_1+s_2+s_3)C_{BC}}{g_{m1}})(i_{b3}+i_{diff3})(g_{m1})}{\det(Y(s_1+s_2+s_3))}, \quad (4.19)$$

where $\det(Y(s_1+s_2+s_3)) = [Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j+C_{BC})](Y_L(s_1+s_2+s_3)+(s_1+s_2+s_3)C_{BC})+(s_1+s_2+s_3)C_{BC}(g_{m1}-(s_1+s_2+s_3)C_{BC})$.

The intermodulation distortion ratio is given by (4.20):

$$IMD3 = \frac{3}{4}{V_{IN}}^2\left|\frac{V_{32}(s_1,s_2,s_3)}{V_{12}(s_1)}\right|, \quad (4.20)$$

$$= \frac{3}{4}{V_{IN}}^2\left|\frac{-(Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j+C_{BC}))i_{c3}+(1-\frac{(s_1+s_2+s_3)C_{BC}}{g_{m1}})(i_{b3}+i_{diff3})(g_{m1})}{[Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j+C_{BC})](Y_L(s_1+s_2+s_3)+(s_1+s_2+s_3)C_{BC})+(s_1+s_2+s_3)C_{BC}(g_{m1}-(s_1+s_2+s_3)C_{BC})} \times \frac{(Y_L(s_1)+s_1C_{BC})[Y_S(s_1)+g_{\pi 1}+s_1(C_{diff1}+C_j+C_{BC})]+s_1C_{BC}(g_{m1}-s_1C_{BC})}{-Y_S(s_1)[g_{m1}-s_1C_{BC}]}\right|,$$

where $s_1 = s_2 = j\omega_1$ and $s_3 = -j\omega_2$.

By letting $C_{BC} = 0$ [56, 57], (4.20) can be simplified to (4.21):

$$IMD3 = \frac{3}{4}{V_{IN}}^2\left|\frac{(\frac{(Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j))i_{c3}}{g_{m1}}-(i_{b3}+i_{diff3}))}{[Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j)](Y_L(s_1+s_2+s_3))} \times \frac{Y_L(s_1)[Y_S(s_1)+g_{\pi 1}+s_1(C_{diff1}+C_j)]}{Y_S(s_1)}\right|. \quad (4.21)$$

As shown in (4.3) and (4.21), increasing the bias current and the gain will reduce the IMD3 component and improve linearity [25,57]. The point at which the IMD3 component equals the fundamental component is known as the IIP_3. The IIP_3 for increasing bias current is shown in Figure 4.4.

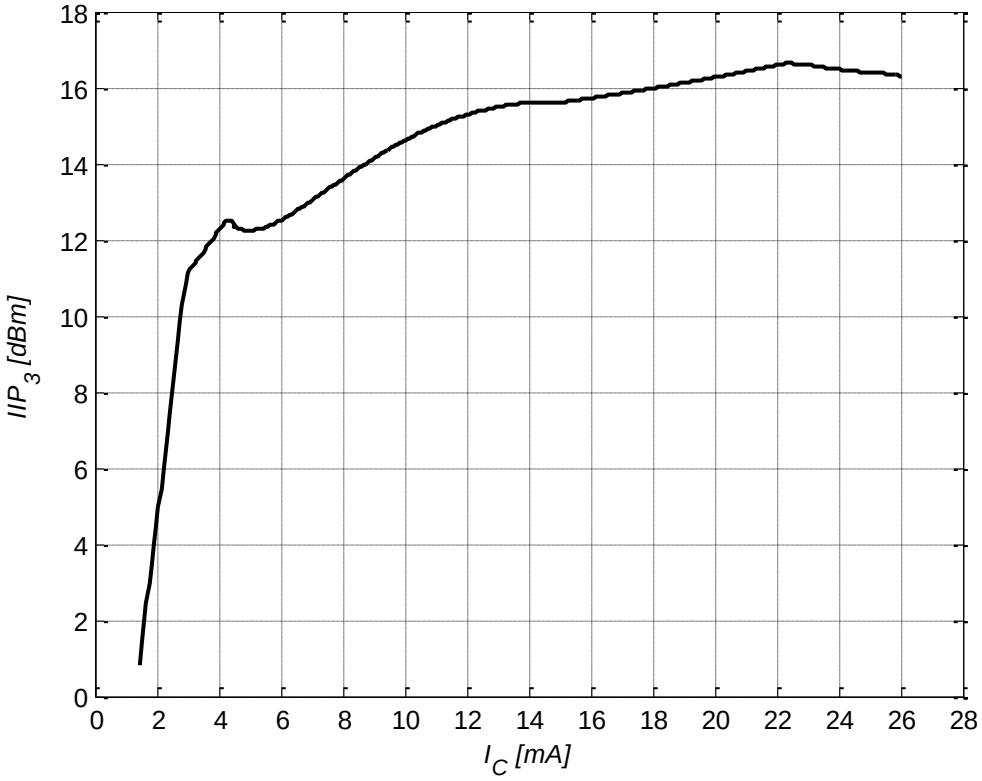


Figure 4.4. IIP_3 for a CE SiGe HBT.

A transistor size of 0.12 µm × 16 µm was used to simulate the IIP_3. As shown in Figure 4.4, the linearity increases sharply for small bias currents and is then followed by a gradual increase in the linearity as the bias current increases. The IIP_3 begins to taper off for bias currents > 23 mA.

In terms of the large signal analysis, the output power of the PA is defined using (4.22):

$$P_{OUT}[dBm] = G[dB] + P_{IN}[dBm]. \quad (4.22)$$

However, all PAs suffer from the non-linear effect of saturation where the gain begins to decrease with increasing input power known as gain compression. One cause of this

phenomenon is due to device heating because of the power dissipation by the transistors resulting in self-heating. This is most noticeable at high current densities. However, the main cause of gain compression is the overdriving of the RF signal away from the device's linear region of operation and into the device's ohmic region. The result of this, is that the output RF signal is now clipped. Therefore the gain compression is directly linked to the quiescent bias point of the transistor. By providing an increasing gain at certain measured output power levels will ensure a constant overall gain such that the output power remains linear until the saturation limit has been reached, at which point no further linearity improvement can be achieved.

4.3 CONCLUSION

This chapter presented the mathematical analysis that was required to understand the non-linearities in the CE SiGe HBT and therefore provided a suitable solution to reduce these non-linearity components. The Volterra series analysis was performed on the CE SiGe HBT to derive the fundamental, second-order and third-order non-linearity distortion components.

A means of reducing the IMD3 component was also discussed in this chapter using theoretical and simulation results. This allowed a way of implementing a predistortion system that can reduce the IMD3 component and thus improve the linearity of the PA.

CHAPTER 5 PA AND APD DESIGN AND RESULTS

5.1 INTRODUCTION

At mm-wave frequencies the PA has to be efficient, operate optimally and reduce the output distortion. However, its design features are limited by the scaled-down active devices and by the parasitic substrate losses, especially of the passive components at this desired frequency. These factors have a huge impact on the overall performance of the PA and pose an extremely challenging task in designing the PA at mm-wave frequencies. Not only does the PA need to operate at such high frequencies, but the linearity of the system should be improved. The mathematical analysis done in chapter 4 provided a foundation for implementing a predistortion system. The APD designed in this chapter was based on this mathematical analysis to improve the linearity of the PA at 60 GHz.

The PA and the APD circuits were designed using the IBM PDK. Both CMOS transistors and SiGe HBTs were used in the design of the complete system. This was made possible by the BiCMOS technology that is supported in the IBM PDK, allowing the integration of CMOS and SiGe, as explained in chapter 2. All the subsystems were simulated to validate their functionality. These subsystems were integrated into a complete system and were prototyped in order to obtain measurement results. The PDK includes the parasitics and process tolerance for each device. The design guideline also provides a detailed analysis of each device's performance including their parasitic values under various simulated and measured conditions for comparative purposes. This chapter will present the design process, circuit architecture and simulation results of each of these subsystems of the PA and the APD, as well as the measured results.

5.2 PA AND VGA

The initial design of the PA was a three-stage CE Class AB PA. The first stage was then converted to a VGA. The last stage was designed for maximum output power while the

first stage was designed for maximum gain. The input and output ports of the PA were designed for 50 Ω to match the measurement equipment's input and output ports. A single-ended PA configuration was chosen to simplify the measurement equipment requirements. The SiGe transistors have two transistor options, viz. the high performance (HP) and high breakdown (HB) transistors. The HP transistor has two layout configurations, CBEBC and CBE, while the HB transistor has only the CBEBC layout configuration. All the power transistors have an emitter width of 0.12 µm. The HP transistors have a higher f_T than the HB transistors. Since the frequency of operation for this design is 60 GHz, the HP transistors were chosen as the power transistors. The CBEBC layout configuration was chosen, as it is the recommended layout configuration from the foundry for performance and reliability.

5.2.1 PA AND VGA DESIGN

The initial manual calculation of the output power of the PA provided a starting point for the design of the PA. The output stage was designed first and the output power was determined using (5.1):

$$P_{OUT} = \frac{1}{2} V_{swing} \times I_c. \tag{5.1}$$

The major problem with SiGe bipolar transistors is the low breakdown voltage. The breakdown voltage should always adhere to the condition shown in (5.2):

$$v_{SWING} + V_{CE} < BV_{CEO}. \tag{5.2}$$

The inequality in (5.2) states that the sum of the voltage swing and the voltage at the CE must be smaller than the open-base CE breakdown voltage, BV_{CEO}. BV_{CEO} is the maximum voltage where breakdown occurs when the base of the transistor is open. The breakdown voltage of the transistors provided by the IBM PDK is 1.7 V. This breakdown voltage is quite small and is caused by impact ionisation. However, this breakdown voltage can be overcome by using a 300 Ω resistor at the base of the transistor. This results in the breakdown voltage being extended from 1.7 V (BV_{CEO}) to approximately 4 V (BV_{CER}), as explained in chapter 2.

The final V_{CE} and bias current that were chosen from the simulations were 1.8 V and 25 mA respectively. The transistor was then scaled according to its current capabilities, as shown in Figure 5.1.

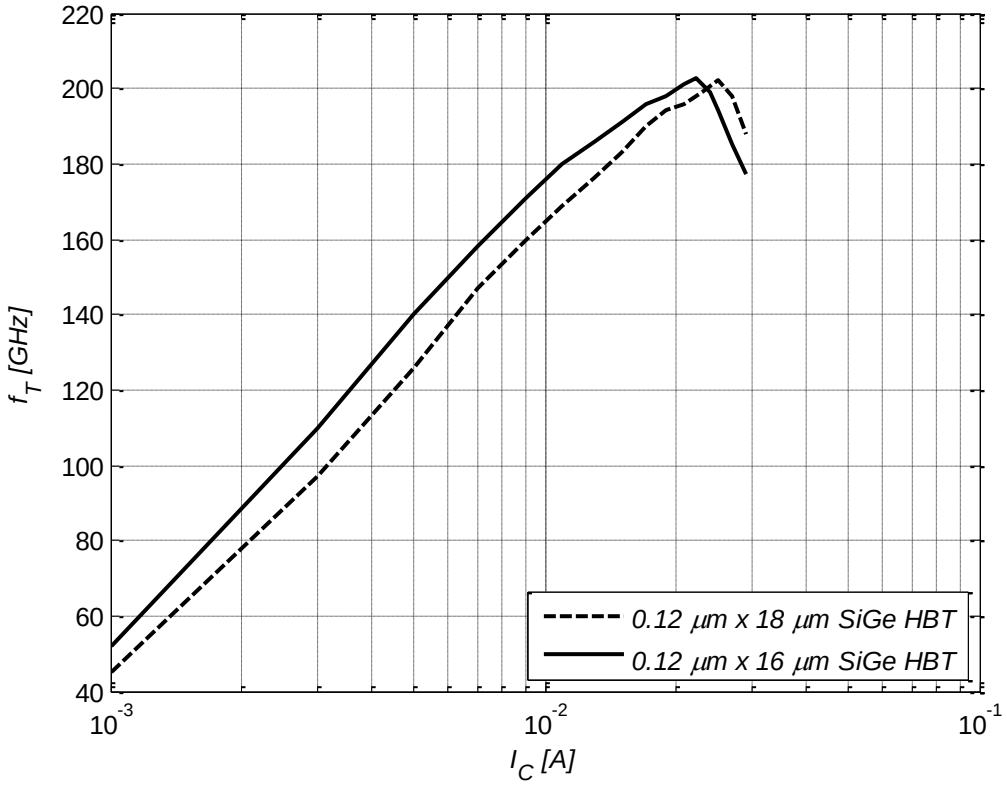


Figure 5.1. f_T vs I_C for the 18 µm and 16 µm transistors.

The two HP transistor sizes have a peak f_T greater than 200 GHz, as shown in Figure 5.1. For the output stage, the emitter length was set to 18 µm, which results in the transistor being biased near its f_T at the collector bias current.

An important factor in PA design is stability. Under certain conditions, such as high gain, the PA may start to oscillate and become unstable. The PA should be designed to be always unconditionally stable for all conditions. For a PA to be unconditionally stable it should satisfy the following two conditions in (5.3) and (5.4):

$$k_f = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1, \tag{5.3}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2 > 0. \tag{5.4}$$

In a multistage power amplifier, each of the stages as well as the overall PA needs to be checked for stability [58]. Small-signal analysis was performed at the operating points to determine the stability and gain of the output stage of the PA at 60 GHz. The output stage of the PA is unconditionally stable with a minimum *k*-factor and B_1 of 1.22 and 0.64 respectively. The gain of this stage is 5.1 dB.

5.2.2 MATCHING NETWORKS

To achieve high gain and output power in the CE PA configuration, the base and the collector of the power transistor need to be matched to the source impedance and the load impedance, respectively. The design of the output stage was designed using the load-line technique and load-pull simulations and not by using the output impedance of the transistor. The objective of load-pull measurements is to obtain the optimal output load impedance in order to maximise the current and voltage swings at the collector of each stage. This results in the optimum output power and efficiency being achieved. The measurements begin by fixing the voltage bias and input signals. The output impedance is then varied at the output port of the transistor using an output tuner. Using a similar approach, the source-pull measurements can be done at the input port of the transistor by varying the input impedance, using an input tuner. The source-pull measurements provide the optimal gain and noise figure results.

The matching network requires the use of reactive components. Therefore care must be taken in designing and implementing these matching networks, as they will influence the frequency of operation of the PA. Capacitors and TLs were used in the design of all the matching networks. The capacitors were realised using MIM capacitors with seven metal layers. The TLs were designed with a characteristic impedance of 50 Ω and were realised using a single-wire structure. Side shielding was implemented within the TLs to minimise the coupling between adjacent structures [33]. The initial optimum load impedance was obtained using (5.5)

$$R_{OPT} = \frac{v_{SWING}^2}{2 \times P_{OUT}}, \quad (5.5)$$
$$= 24.2\ \Omega,$$

where v_{SWING} and P_{OUT} are 1.1 V and 0.025 W respectively. It is clear from (5.5) that matching networks were needed to convert the 50 Ω load to the optimal load resistance. These calculations were used as a starting point for the design of the matching networks. Further iterations and simulations were then performed in particular load-pull simulations. These simulations were done to obtain the optimal load impedance for maximum output power and PAE from the simulation software. The optimum load impedance is Z_{L3OPT} = 15 + j30 Ω, which results in an output power of 13 dBm and a PAE of 12 %.

The optimum load impedance is matched to the 50 Ω load resistance. Because of the parasitic capacitance of the bondpad, the load termination is not purely resistive and therefore the parasitic capacitance of the bondpad must be included. The bondpads were chosen to be 100 µm by 100 µm as recommended by the foundry. This bondpad size also eases the contact requirements of the measurement equipment. This bondpad size has a parasitic capacitance of approximately 45 fF [55]. This parasitic capacitance is parallel to the 50 Ω load resistance, resulting in a total load impedance of Z_L = 29 – j24 Ω. All the impedances were normalised to 50 Ω and placed on the Smith chart. The matching of the optimum load-line impedance to the load impedance is shown in Figure 5.2.

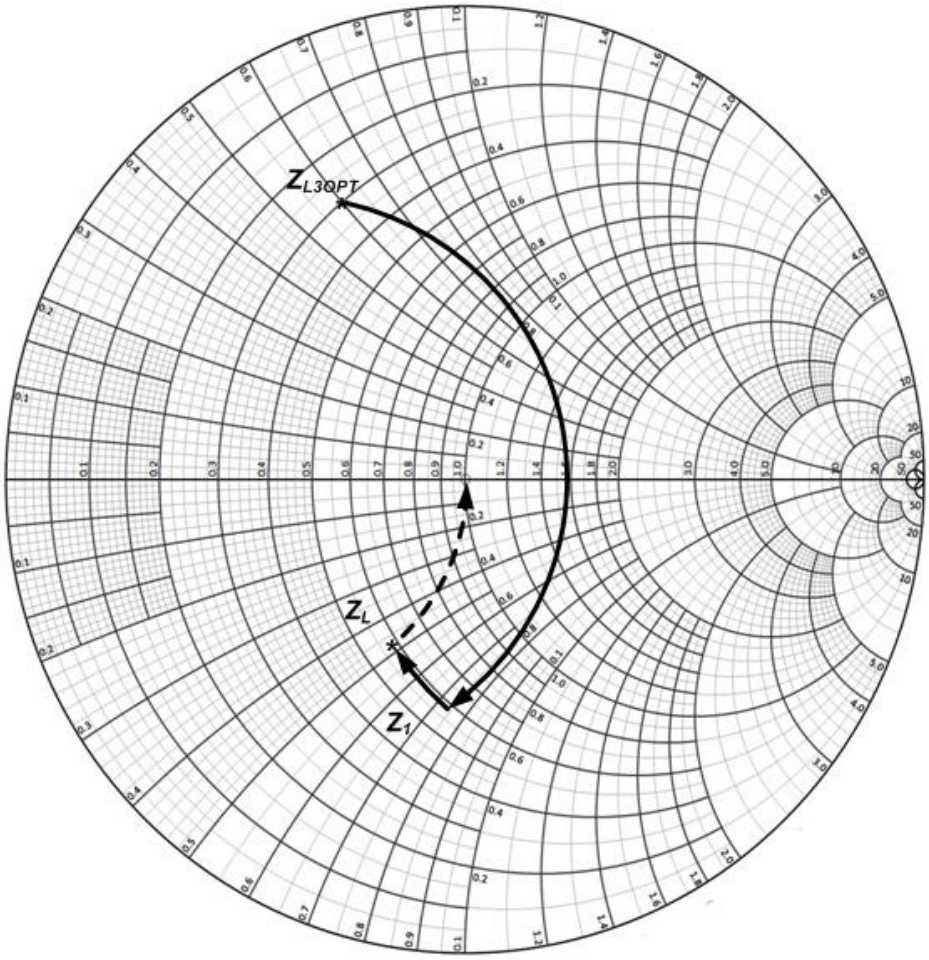


Figure 5.2. The output matching using the Smith chart.

To realise the matching of the optimum load impedance to 50 Ω, three movements were used on the Smith chart, as shown in Figure 5.2. The movement from Z_{L3OPT} to Z_1 was realised using a short stub TL. The length of the TL was calculated using (5.6) and (5.7):

$$\lambda_g = \frac{c}{freq\sqrt{\epsilon_{eff}}}, \tag{5.6}$$

$$TL_{O1} = \frac{\theta \times \lambda_g}{360^\circ}, \tag{5.7}$$

$$= 171\ \mu m,$$

where c, speed of light, $\approx 3 \times 10^8$ m/s, $freq$ is the frequency (i.e. 60 GHz) and ϵ_{eff} is the effective permittivity of Si. The following movement from Z_1 to Z_L was achieved using a series capacitor. The capacitor value was determined using the Smith chart in Figure 5.2 and (5.8)

$$C_{O1} = \frac{1}{2\pi freq(50)(0.216)}, \quad (5.8)$$
$$= 245 \text{ fF}.$$

The final movement (patterned line) was to cancel the parasitic capacitance of the bondpad and resulted in a matched load of 50 Ω. The schematic of the output matching network is shown in Figure 5.3.

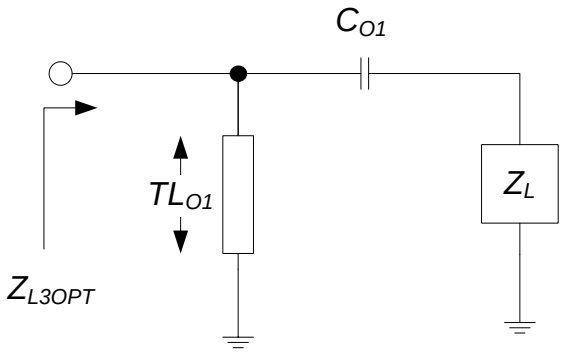


Figure 5.3. Output matching network.

A two-element L network as shown in Figure 5.3 was used to realise the output matching network of the PA. The calculated values obtained from (5.7) and (5.8) were optimised as shown in Table 5.1.

Table 5.1. Recalculated and simulated output matching component values.

Component	Value
Z_{L3OPT}	25 + j33 Ω
C_{O1}	300 fF
TL_{O1}	200 µm

The final design values for the short stub TL, TL_{O1}, and the series capacitor, C_{O1}, shown in Table 5.1, were finalised with the use of the PDK equivalent components that included parasitics and operational restrictions.

To obtain the required gain of the PA, two additional gain stages were needed. It is important to note that when designing multistage PAs, one must ensure that the previous stage's output power does not saturate before the next stage's output power. The second stage was designed using the simulation results of the output stage and the DC operating

points chosen from the simulation results were 1.8 V and 22 mA. This meant a transistor with emitter length of 16 µm being chosen, which was biased at the peak f_T, as shown in Figure 5.1. The second stage was proven to be unconditionally stable with a minimum *k*-factor and B_1 of 1.57 and 0.9 respectively. The gain of the second stage is 7.2 dB.

Interstage matching was performed in order to transform the input impedance of the output stage to the optimum load of the second stage. These impedances were obtained using load-pull and source-pull simulations. The final optimum load impedance of the second stage and input impedance of the output stage are Z_{L2OPT} = 28 - *j*21 Ω and Z_{IN3} = 13 - *j*3 Ω respectively. The impedance matching schematic is shown in Figure 5.4.

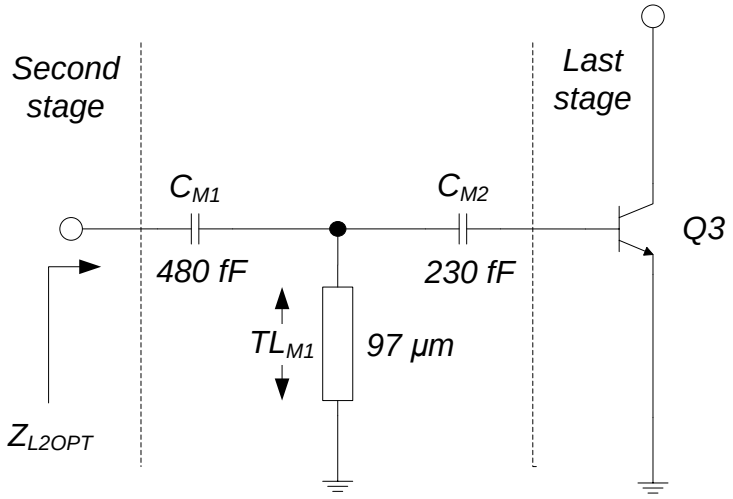


Figure 5.4. Interstage matching between second stage and output stage.

The final design values for each of the components are shown in Figure 5.4. The impedance matching network was realised using a three-element T matching network with two series capacitors and a short TL.

Similar to the design of the second stage, the first stage was designed so that its output power did not saturate before the second stage's output power. The first stage is part of the driver stage of the PA. It was later changed into a VGA for the APD circuit. The bias voltage and the maximum bias current for the VGA are 1.8 V and 22 mA respectively. An emitter length of 16 µm was chosen to coincide with the maximum bias current and the peak f_T, as shown in Figure 5.1. The minimum bias current was set to 16 mA and it was decided that this bias current would be the default bias current for the VGA. Choosing

16 mA and 22 mA as the minimum and maximum bias currents for the VGA provided sufficient gain variation to realise the predistortion function and ensured that the PA operated within the Class AB mode. Biasing the PA below the minimum or above the maximum bias currents resulted in the PA operating towards the Class B or Class A mode respectively. Small-signal analysis revealed that the first stage was unconditionally stable with a minimum *k*-factor of 1.38 and B_1 of 0.8. At the default bias current, the gain of the amplifier is 4.2 dB and it increases to 7 dB at the maximum bias current.

Similar to the previous stage, the input impedance of the second stage was transformed to the optimum load impedance of the first stage. According to load-pull and source-pull simulations the final optimum load and input impedances are Z_{L1OPT} = 42 – *j*35 Ω and Z_{IN2} = 10.4 – *j*1.8 Ω respectively. The circuit schematic of the interstage matching network is shown in Figure 5.5.

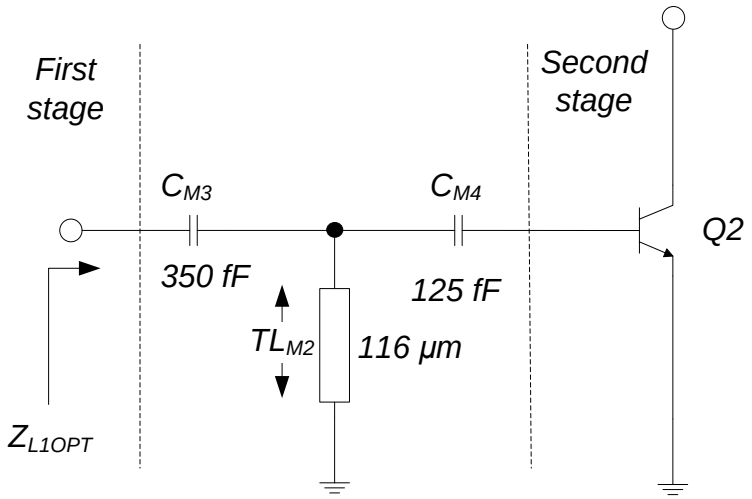


Figure 5.5. Matching network between the first and second stage.

The matching network between the first and second stage of the PA was realised using a T network with two series capacitors and a short TL, as shown in Figure 5.5. The final component values in Figure 5.5 were optimised using the equivalent components from the PDK.

The input power is much smaller than the output power, therefore *S*-parameter analysis was used for the input matching network. The input impedance was determined as 10.4 – *j*1.8 Ω. The source impedance is the 50 Ω input port in parallel with the parasitic

bondpad, viz. 29 – j24 Ω. The input matching of the first stage was designed for maximum gain. Therefore the source impedance was conjugate matched to the input impedance of the first stage, as shown in Figure 5.6.

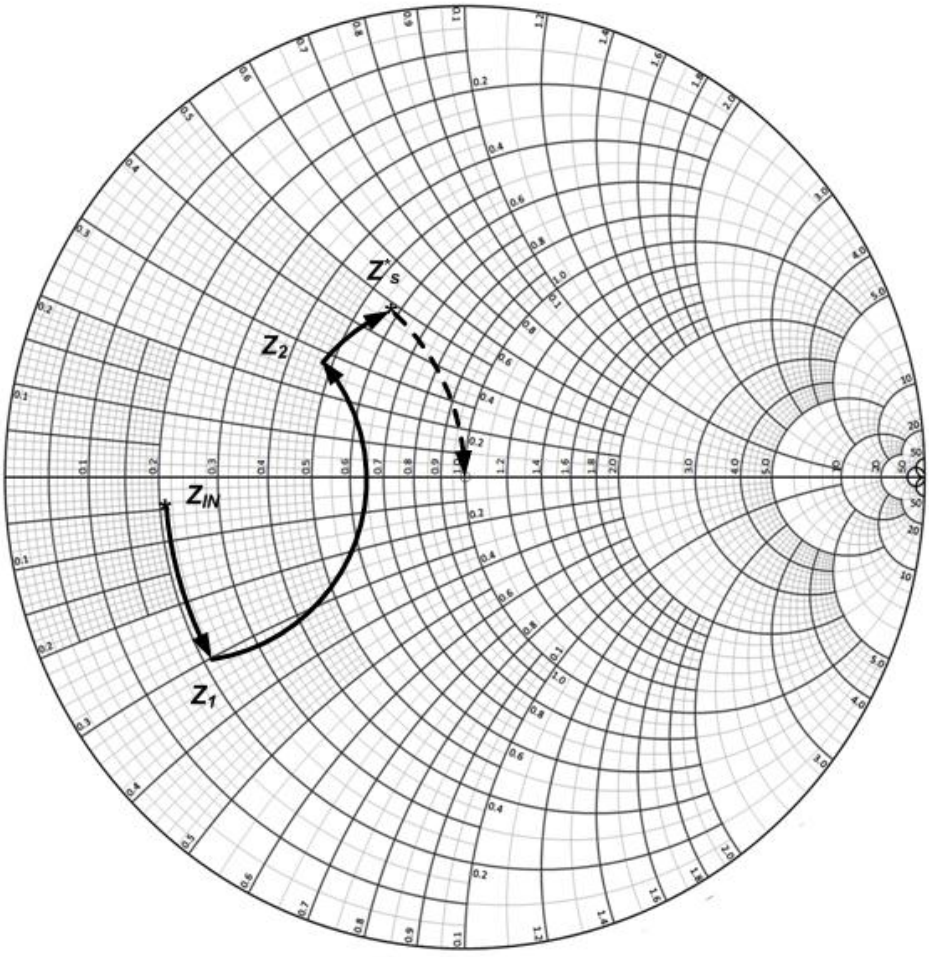


Figure 5.6. Input matching network using the Smith chart.

The input matching was performed using three movements, as shown in the Smith chart in Figure 5.6. The movements from Z_{IN} to Z_1, from Z_1 to Z_2 and from Z_1 to Z_S^* were done using a capacitor, a shunt stub and a series stub respectively. The final movement marked by the patterned line was done to cancel the effect of the parasitic capacitance of the bondpad. The schematic of the input matching network is shown in Figure 5.7.

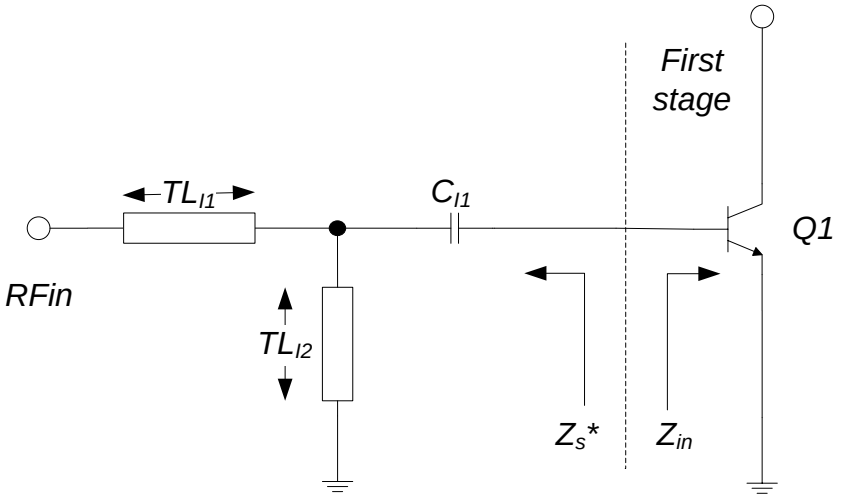


Figure 5.7. Input matching network.

A three-element T matching network was used to realise the input matching network, as shown in Figure 5.7. The final recalculated values of the components in Figure 5.7 are shown in Table 5.2.

Table 5.2. Recalculated and simulated component values for input matching network.

Component	Value
Z_{in}	9.5 – j6.5 Ω
C_{I1}	248 fF
TL_{I1}	40 µm
TL_{I2}	120 µm

Table 5.2 shows the optimised component values using the components from the PDK. These values were used in the final design of the input matching network of the PA.

5.2.3 BIASING NETWORK

Biasing circuits are applied to each stage of the PA. The chosen bias network provides three important functions viz. biasing the power transistors at the correct bias point, extending the BV_{CEO} limit and providing temperature compensation. Bypass capacitors were used extensively in the bias circuits to provide good AC grounding. The bypass capacitors were carefully chosen not to operate above their self-resonating frequencies. The bias circuit for the VGA stage is shown in Figure 5.8 (a) and (b).

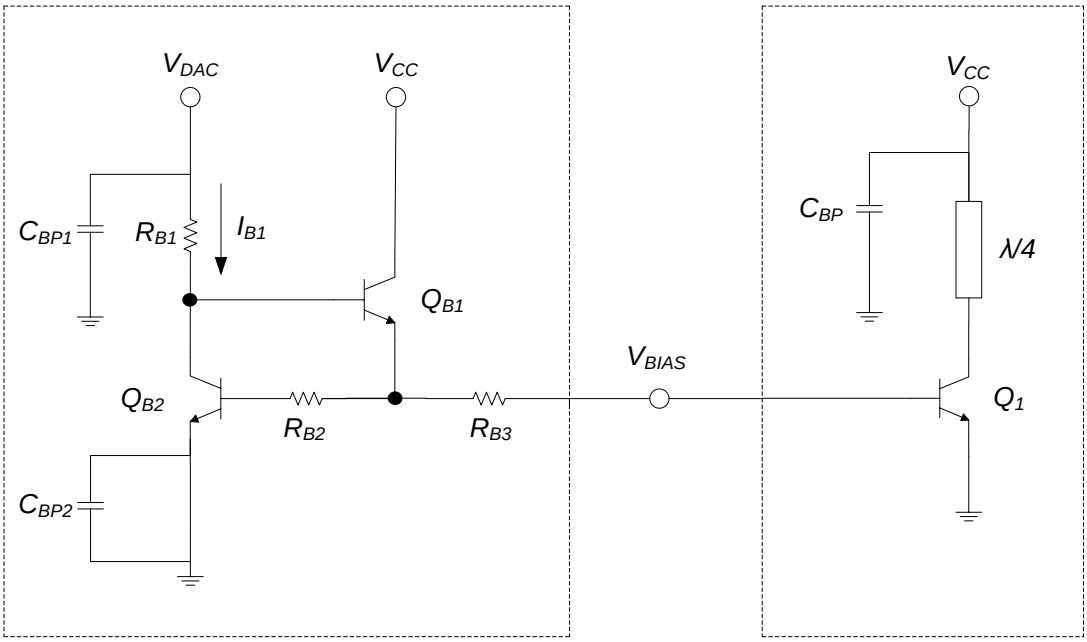


Figure 5.8. Biasing circuit for the VGA stage consisting of **(a)** the dynamic biasing circuit and **(b)** the biasing circuit for the power transistor.

The VGA is biased dynamically using the DAC. As shown in Figure 5.8 (a), the current, I_{B1}, is controlled by resistor, R_{B1}, and the control voltage, V_{DAC}, is supplied from the output of the DAC. The BV_{CEO} limits the output power of the PA. To improve the output power and to enable the power transistor to operate above BV_{CEO}, the bias circuit was designed so that the base of the power transistor sees a 300 Ω resistance. Therefore reducing the generated avalanche currents caused by impact ionization, from the base.

The circuit of Figure 5.8 also provides temperature compensation. V_{BE} is a function of junction temperature. In response to temperature variations, V_{BE} changes and this can lead to a change in the class of operation of the PA. Therefore ballasting resistors R_{B2} and R_{B3} were added, which reduced variations in V_{BE} by minimising the effect of the base voltage on V_{BE} using a negative feedback approach [59]. Owing to the large base current requirement of the power transistor, a current driver transistor, Q_{B1}, was used to increase the current-driving capacity into the base of the power transistor, Q_1.

A biasing circuit is also applied to the collector node of Q_1, as shown in Figure 5.8 (b). These biasing circuits are applied to each of the power transistors and include a bypass capacitor and a $\lambda/4$ TL. At DC, the above circuit provides a short circuit from the supply lines and an open circuit at mm-wave frequencies. The $\lambda/4$ TLs are used as RFCs and at 60 GHz, the length of these $\lambda/4$ TLs is $\approx$ 620 µm.

5.2.4 FINAL PA SCHEMATIC

The three-stage PA schematic is shown in Figure 5.9.

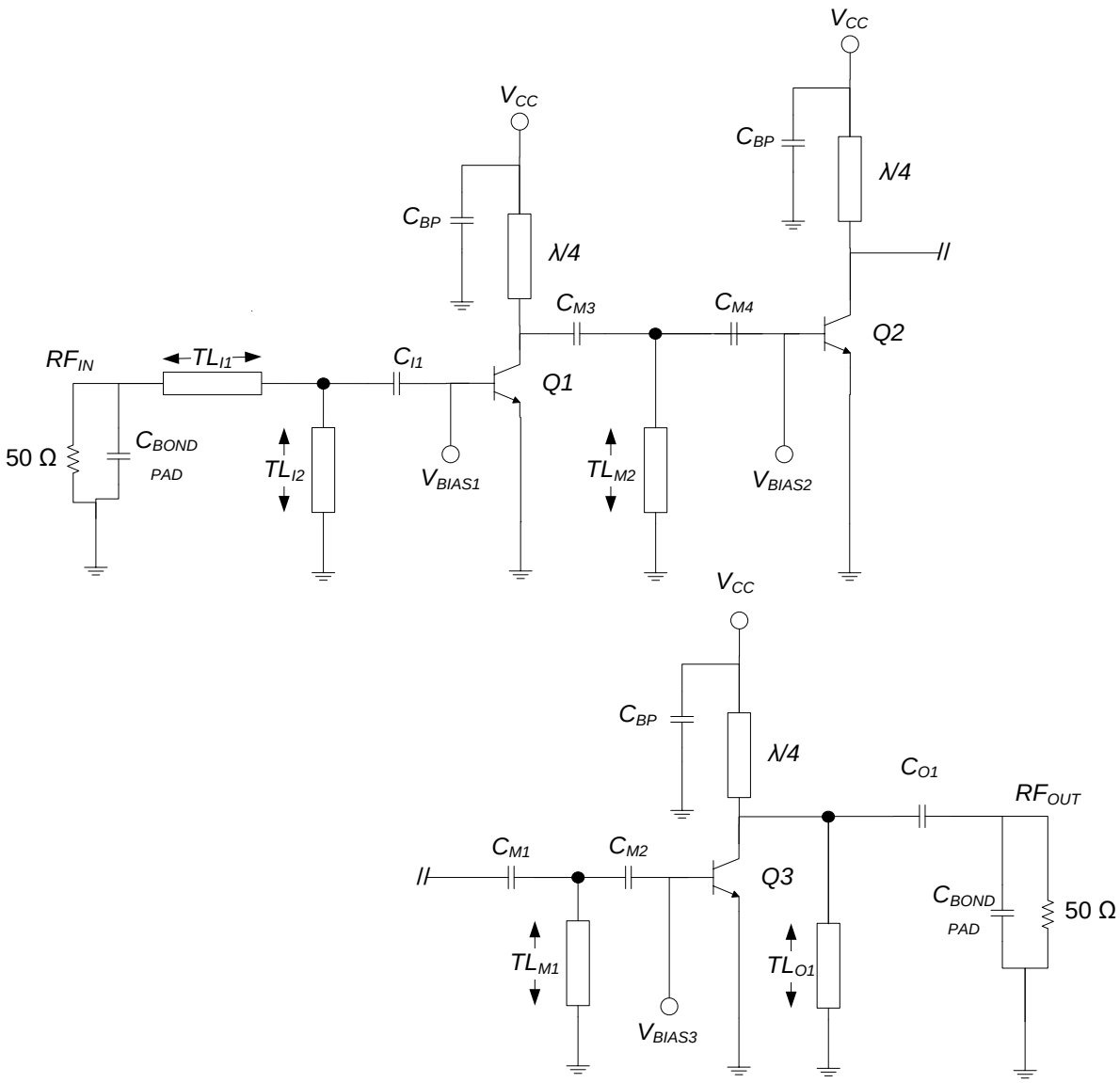


Figure 5.9. Final PA schematic.

In Figure 5.9 each stage of the PA was optimally biased and matched to obtain the maximum output power, gain and stability. The capacitive bondpads and the 50 Ω input and output ports of the PA are also shown in Figure 5.9.

5.3 POWER DETECTOR

An on-chip power detector is used in this design and forms part of the first subsystem of the APD circuit. The power detector circuit is a mean square detector, as shown in Figure 5.10.

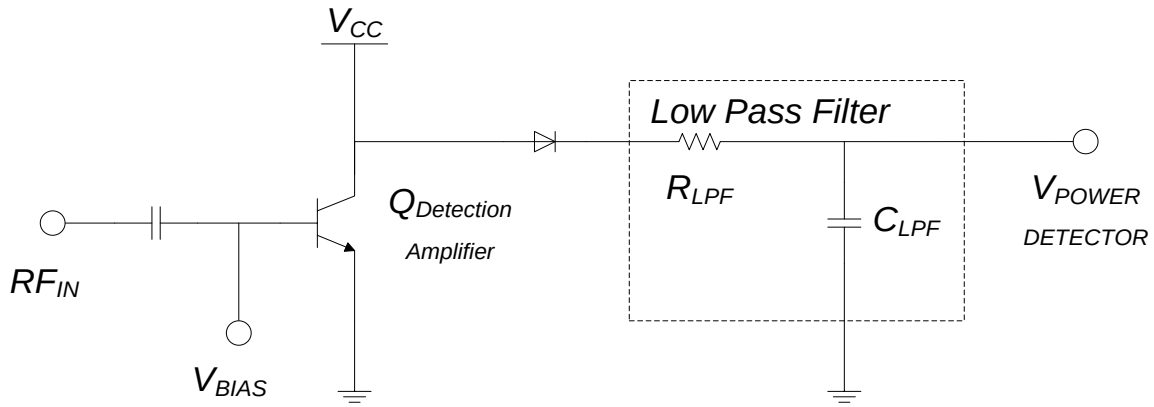


Figure 5.10. Power detector schematic.

In Figure 5.10, the power detector uses a detection amplifier, a diode and a low pass filter. The power detector is connected to the output of the PA. A high input impedance at the power detector minimises the leakage of power from the PA to the power detector. As the input signal increases, an increasing RF signal enters the power detector. However, this signal is still too small and therefore the detection amplifier is used to amplify the input signal and provide a more representative output with regard to the PA. The output of the detection amplifier is therefore a function of the output power of the PA.

Since only the DC component is of interest, a first order low pass filter was designed with a cut-off frequency given by (5.9),

$$f_c = \frac{1}{2\pi R_{LPF} C_{LPF}}, \approx 30 \text{ MHz}, \quad (5.9)$$

where R_{LPF} = 8.2 kΩ and C_{LPF} = 650 fF.

It was decided to use a cut-off frequency of 30 MHz, as it provided sufficient RF attenuation and also enough dynamic range. The power detector output is shown in Figure 5.11.

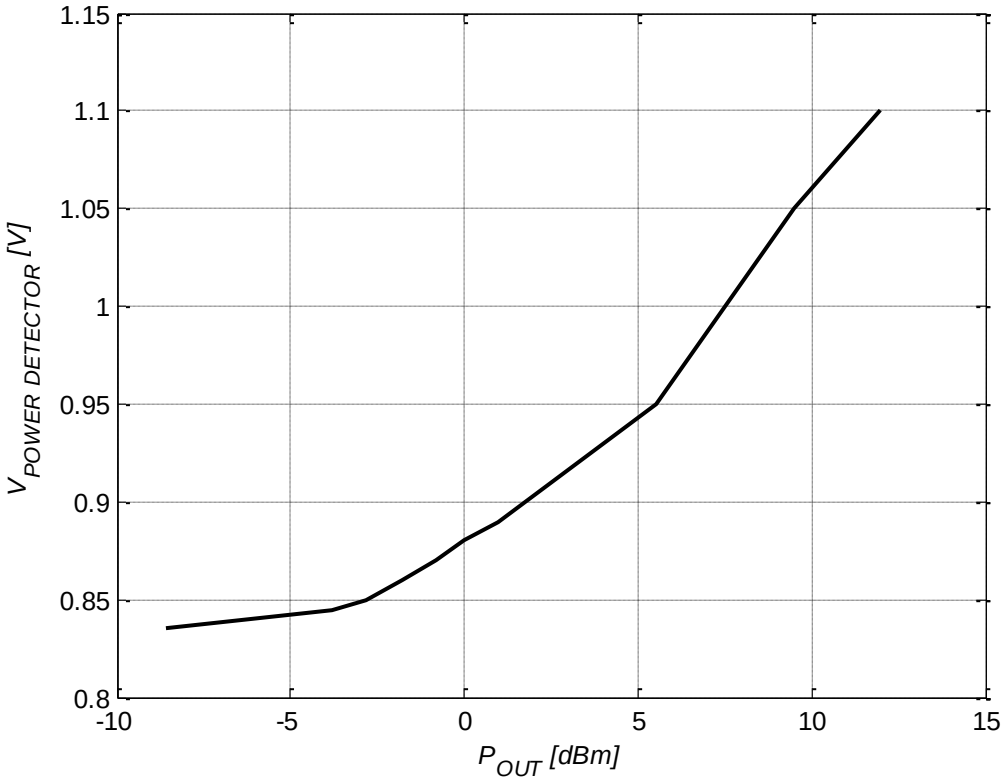


Figure 5.11. Power detector output.

After filtering the high-frequency components, the DC output voltage of the power detector, $V_{POWER\ DETECTOR}$, is proportional to the square of the amplitude of the input AC voltage, as shown in (5.10):

$$V_{POWER\ DETECTOR} \propto V_{RF_{IN}}^2. \quad (5.10)$$

Therefore with increasing output power, $V_{POWER\ DETECTOR}$ increases, as shown in Figure 5.11. These detected voltages are the inputs to the ADC. Its dynamic range of operation is between 0.84 V and 1.1 V for detected output power between -8 and 12 dBm. The predistortion function was applied to this dynamic range.

5.4 ADC

The ADC is the second subsystem of the predistortion circuit. The purpose of the ADC is to convert the detected voltage from the power detector to a digital signal for the control logic subsystems. The input signal is presumed to be slowly varying, therefore a simple flash ADC was designed. The flash ADC usually consists of a sample-and-hold circuit and comparators. The sample-and-hold circuit was omitted because of the slow varying input. Therefore the flash ADC only consisted of comparators. The major drawback of flash ADCs is that for higher resolution *Nbits*, $2^{Nbits} - 1$ comparators are needed. In this design only six output combinations were required. Therefore only five comparators were needed. The flash architecture was therefore used in this ADC. The flash ADC compares the input signal with a set of reference signals and follows the logic as shown in (5.11) and (5.12):

$$V_{IN} > V_{REF} \rightarrow V_{OUT} = 1, \tag{5.11}$$

$$V_{IN} < V_{REF} \rightarrow V_{OUT} = 0. \tag{5.12}$$

As the input signal exceeds the reference signal at each comparator, the output moves from a low state to a high state. The flash ADC is composed of CMOS transistors and its main function block, i.e. the comparator, is described in the next subsection.

5.4.1 COMPARATOR

The comparator consists of a differential amplifier, a latch and an output buffer, as shown in Figure 5.12. One of inputs to the comparator is the detected voltage, which is a slow varying signal from the power detector. The other input to the comparator is the reference signal, which is a non-varying voltage signal that is supplied and controlled off-chip. The

important properties of a comparator, viz. gain, input offset voltage and response time, were analysed in the design of the comparator.

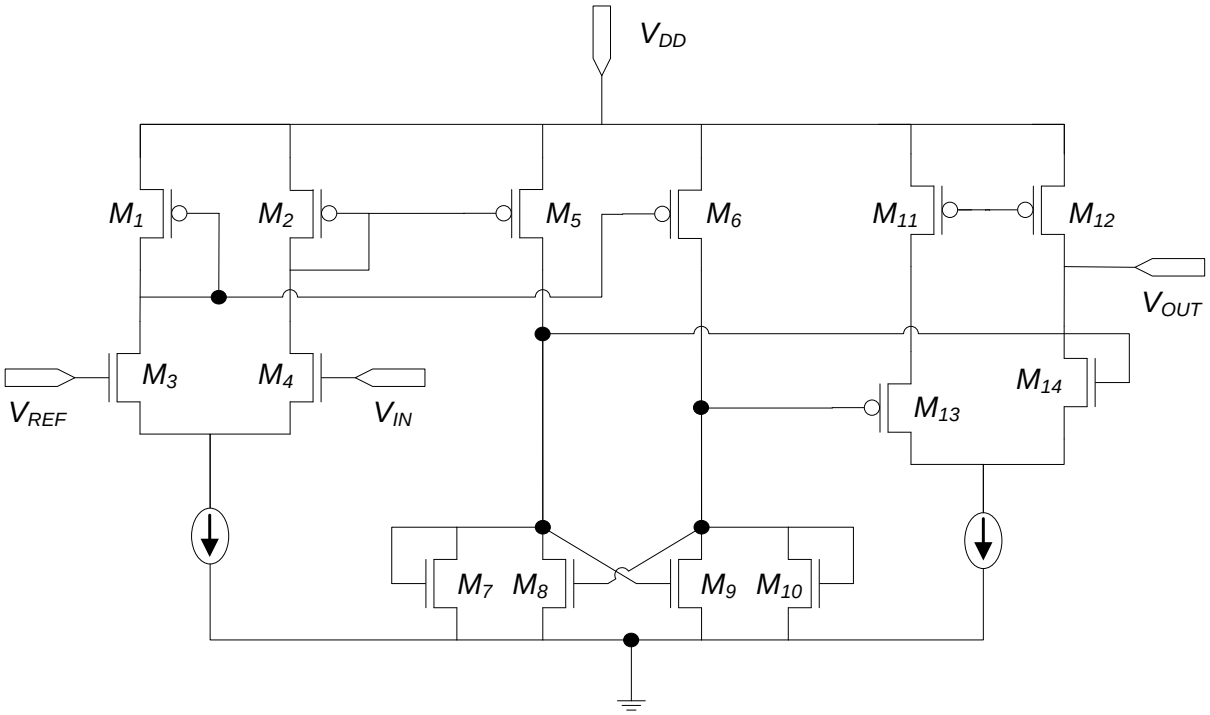


Figure 5.12. The comparator schematic.

The output of the differential amplifier is fed to the p-type field effect transistor (PFET) current mirrors (M_5 and M_6) and is multiplied by the $K \times \frac{W}{L}$ ratio of the current mirror as shown in Figure 5.12. The NFET pair (M_8 and M_9) have their gates cross-connected and therefore form the latch. The latch is the crucial part of the comparator because of its role as the decision circuit. The output of the latch is then fed into an output buffer, which is a single-ended differential amplifier.

The gain of the comparator is an important characteristic, as it defines the minimum amount of input voltage needed to change the output state from low to high and vice versa. The gain of the comparator is given by (5.13) and is shown in Figure 5.13.

$$A_v = \frac{V_{OH}-V_{OL}}{V_{IH}-V_{IL}}, \quad (5.13)$$
$$= 50 \text{ V/V}.$$

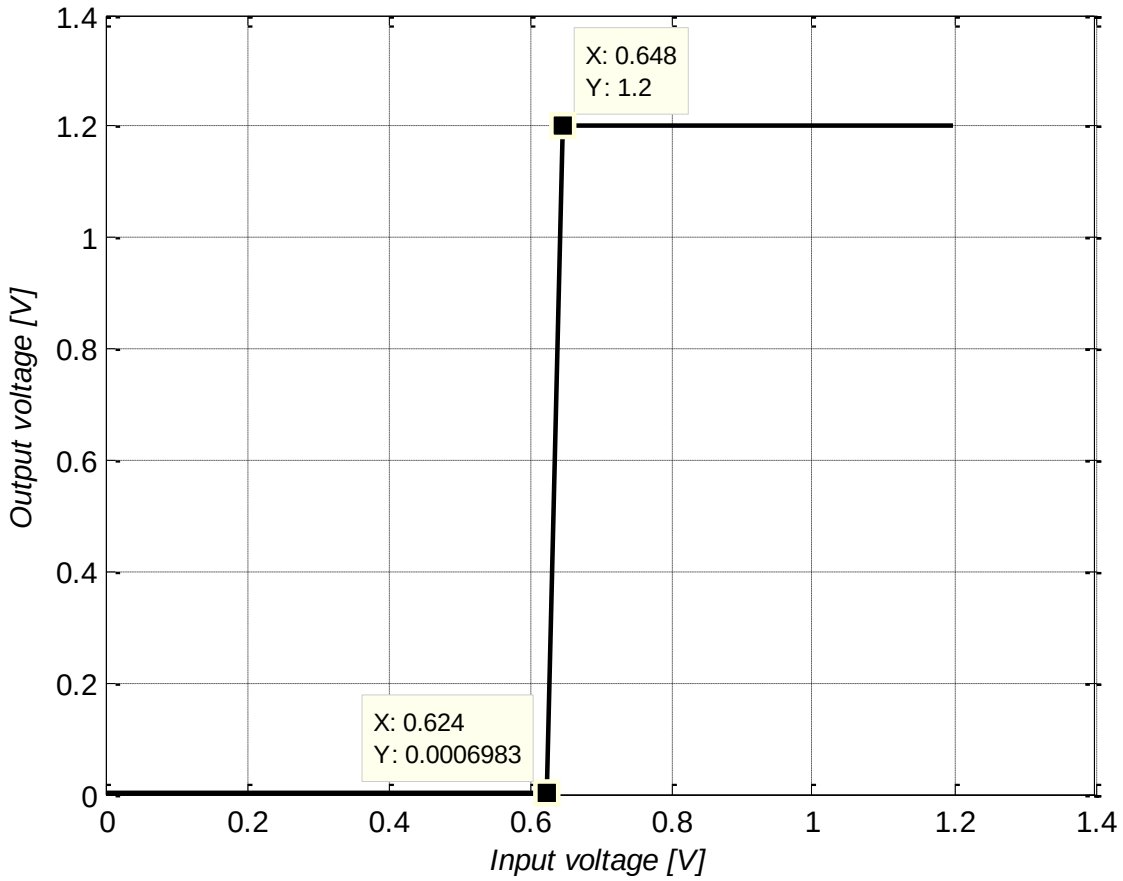


Figure 5.13. Gain of the comparator.

The offset voltage was calculated using (5.14) and can also be seen in Figure 5.13.

$$\Delta V_{IN} = \frac{V_{OH}-V_{OL}}{A_V}, \quad = 24 \text{ mV}. \tag{5.14}$$

Therefore the output does not change from logic 0 to logic 1 until the input voltage is greater than 0.624 V. The dynamic characteristic of the comparator, i.e. propagation delay, was calculated from Figure 5.14 and (5.15)

$$Propogation\ Delay = \frac{Rise\ time+fall\ time}{2}, \quad \approx 0.95 \text{ ns}. \tag{5.15}$$

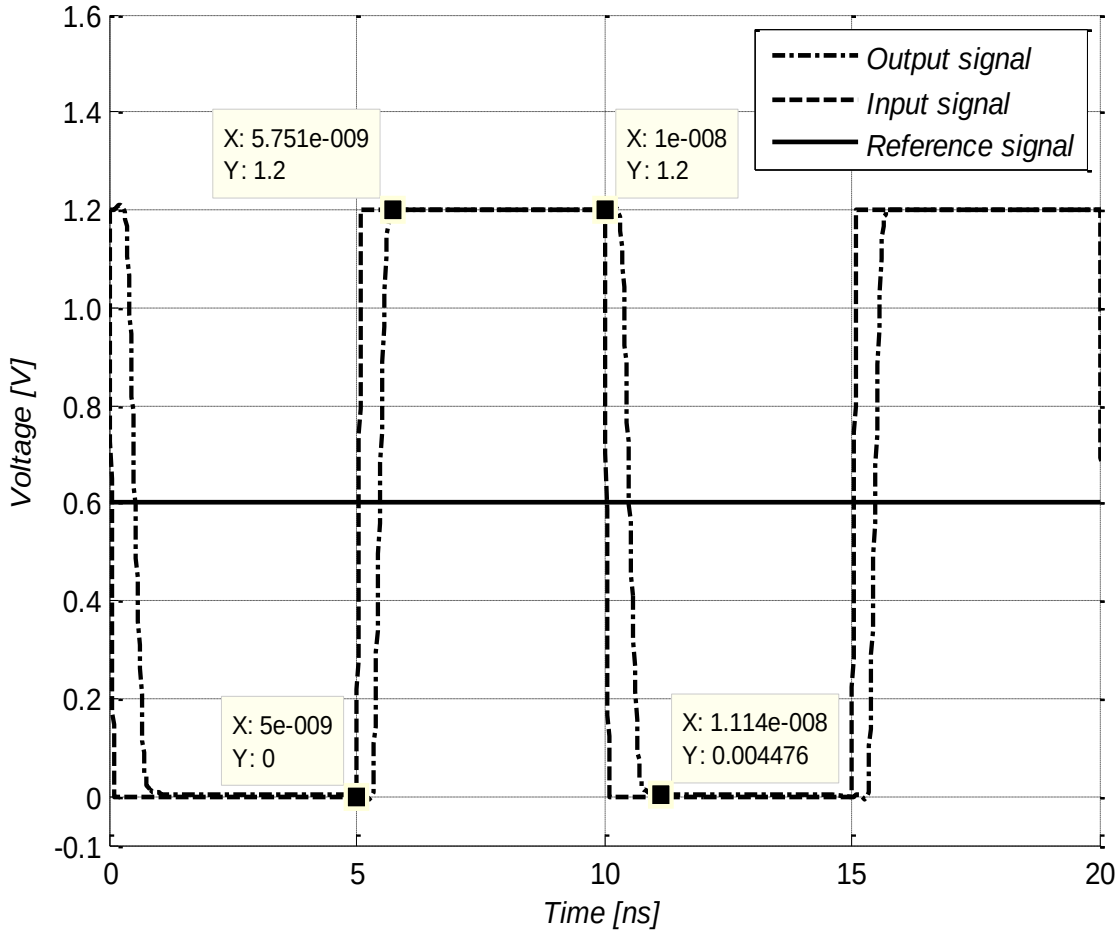


Figure 5.14. Dynamic response of the comparator.

The dynamic characteristic of the comparator yields excellent results, as shown in Figure 5.14. It has a response time of less than 1 ns as well as a very small overshoot for the rising and falling edges. The outputs of the comparators are fed into the control logic subsystem, which is discussed in the next section.

5.5 CONTROL LOGIC SUBSYSTEMS

The control logic subsystem is the third subsystem of the APD circuit and consists of exclusive OR (XOR) gates and inverters. It was designed taking into account the performance of the flash ADC.

5.5.1 XOR GATES

The XOR gates generate the encoding scheme, which is at the heart of the control logic circuit. The inputs to the XOR gates are received from the comparators. The connection between the comparators and XOR gates and the schematic for a single XOR gate are shown in Figure 5.15.

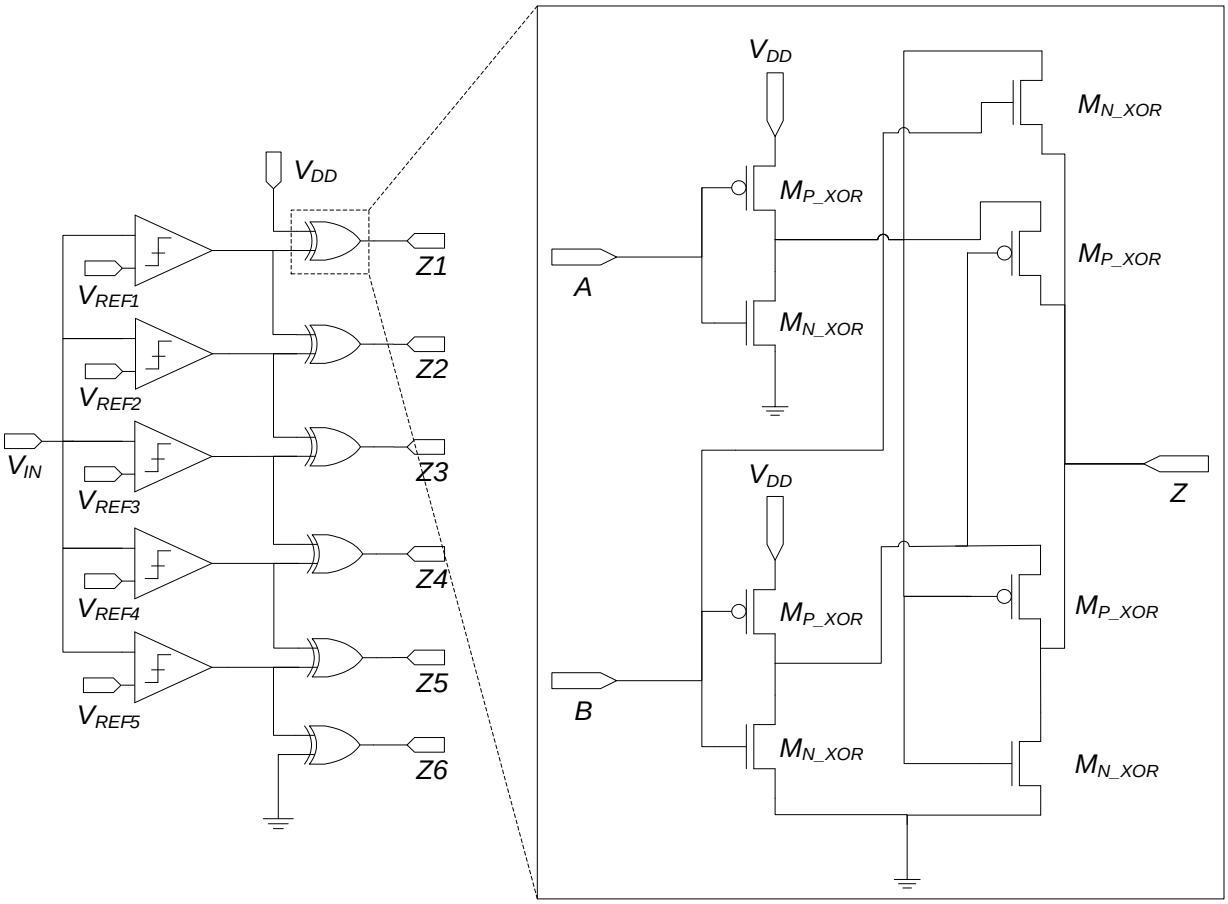


Figure 5.15. Comparator-XOR connection and single XOR schematic.

The XOR gate makes use of both PFETs and NFETs, as shown in Figure 5.15. The design follows a typical CMOS XOR gate design. Each of the PFETs and NFETs has a length of 120 nm. To achieve a propagation delay of less than 2 ns, the widths of the PFETs and NFETs were scaled to 1.97 µm and 1.57 µm respectively.

5.5.2 INVERTERS

The maximum output voltage of the XOR gate from the control circuit is 1.2 V when its output logic is 1. Therefore it cannot be directly used with the DAC because the VGA requires a minimum bias voltage of 1.52 V. To overcome this problem an inverter circuit was implemented. There are six inverters and each one of these is connected to the output of each of the six XOR gates in the control logic circuit. The inverters consist of three-stages. The schematic of a single inverter is shown in Figure 5.16.

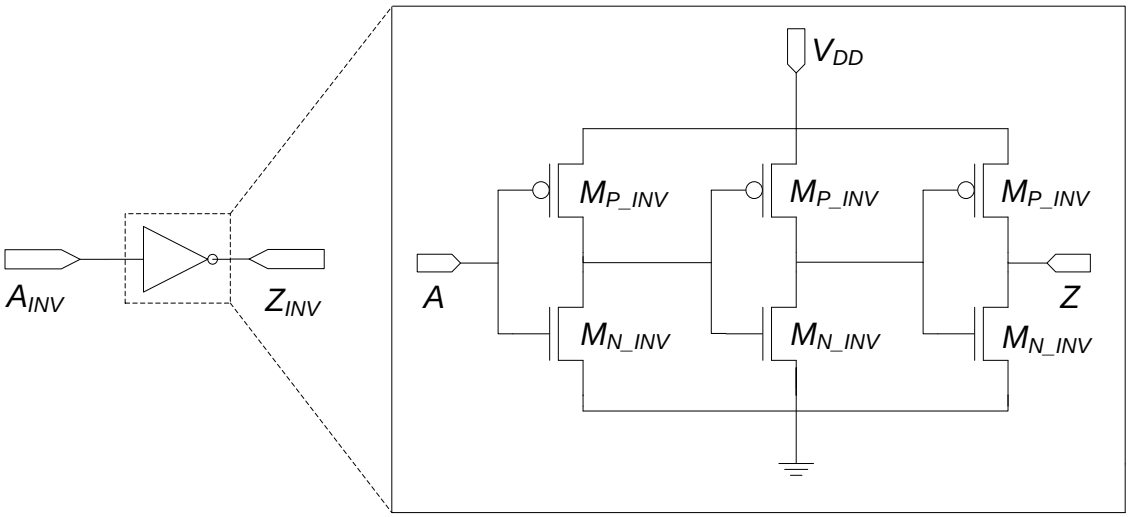


Figure 5.16. Schematic of the three-stage inverter.

The inverters were designed using the thin gate regular FETs. The length of each of the transistors is 120 nm. The transistor sizes of the PFETs in Figure 5.16 were calculated using (5.16) to obtain an inversion point of ½V_{DD}, where V_{DD} is 1.2 V,

$$(W/L)_P = 2(W/L)_N, \qquad (5.16)$$
$$= 14.$$

The operation of the comparators, XOR gates and inverters is shown in Figure 5.17.

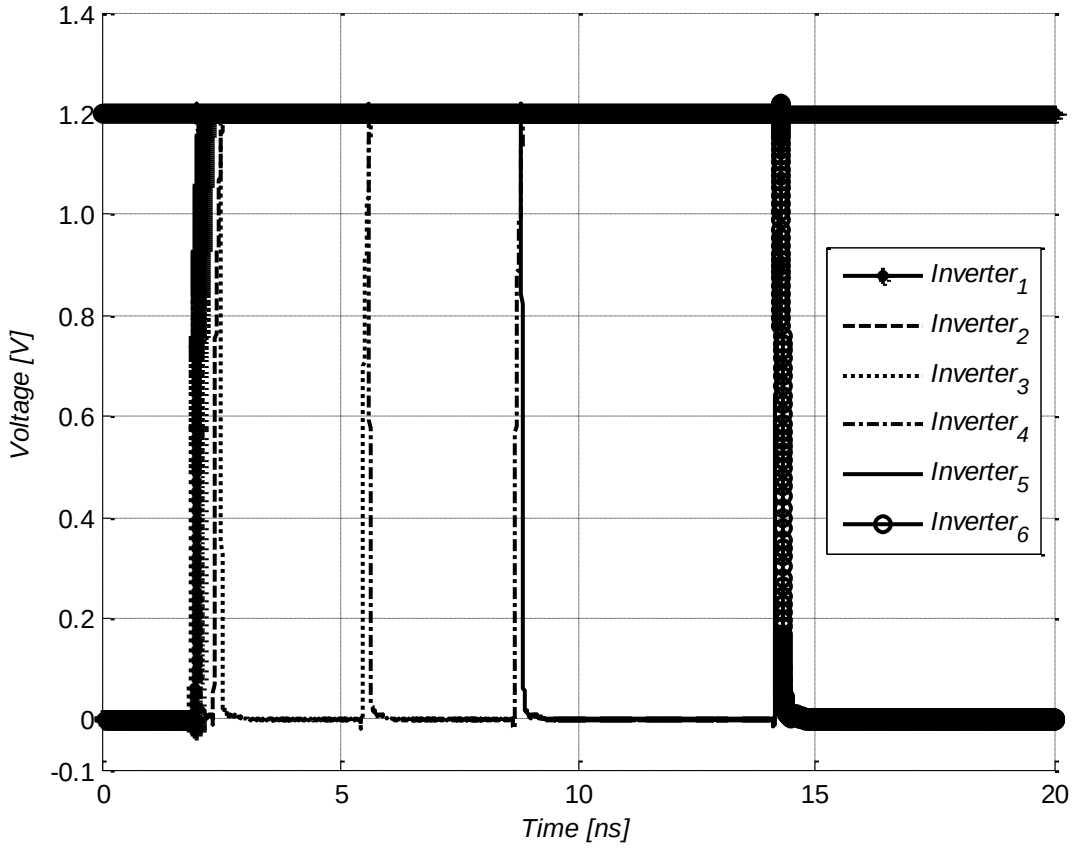


Figure 5.17. Operation of the comparators, XOR gates and inverters at the output of the inverters.

As shown in Figure 5.17, by increasing the input power the detected power (from the power detector) V_{IN} in Figure 5.15 increases; each incrementing inverter is switched on and the previous inverter is switched off. In Figure 5.17, the input power was increased until the detected power resulted in $V_{IN} > V_{REF5}$ and this switched on $Inverter_6$.

5.6 DAC

The DAC is the fourth and final subsystem of the predistortion circuit. Its function is to output a control voltage that will drive the VGA. By varying the VGA using only six voltages, the predistortion function can be achieved. Therefore the DAC was designed to output these six different voltages.

The design of the DAC consists of inverters, diodes and a simple voltage buffer, as shown in Figure 5.18. The required output voltages do not increase monotonically, therefore each diode was scaled to obtain the required output voltage. The preceding subsystem to the

DAC is the inverter from the control logic. This inverter will always output logic 0 when the corresponding XOR gate outputs logic 1. Because of the minimum and maximum voltage requirement of the VGA being 1.52 V and 1.7 V respectively, the thick gate oxide FETs that are available in the PDK were used in the inverter design located in the DAC. The thick gate oxide FETs are much slower than the thin gate oxide FETs; however, because the transitions vary only with output power from the PA, which is presumed to be slow, they are suitable for use in the inverter design. The thick gate oxide FETs operate at a nominal voltage of 2.5 V. However, only 1.8 V is required to realise the input voltages for the operation of the VGA. This inverter is cascaded with the inverter from the control logic.

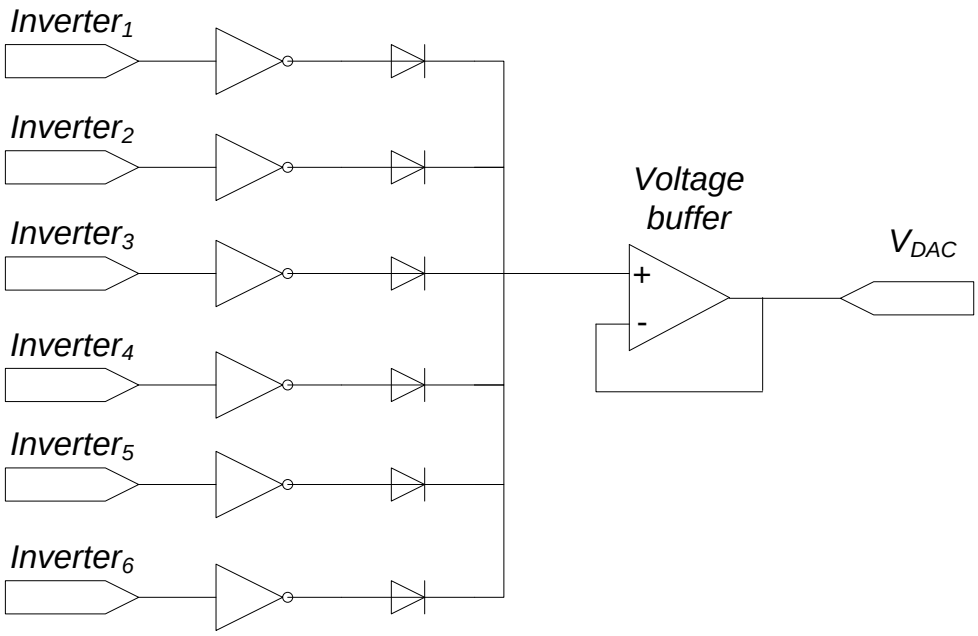


Figure 5.18. DAC circuit.

The implementation of the DAC circuit is shown in Figure 5.18. A similar three-stage inverter as shown in Figure 5.16 was used in the design of the thick gate oxide FET inverters. The length of each of the PFETs and NFETs is 240 nm. In order to realise the inversion point at $\frac{1}{2}V_{DD}$ where V_{DD} is 1.8 V, the PFET was scaled using (5.17). The transfer characteristic of the inverter is shown in Figure 5.19.

$$(W/L)_P = 4(W/L)_N, \qquad (5.17)$$
$$= 8.$$

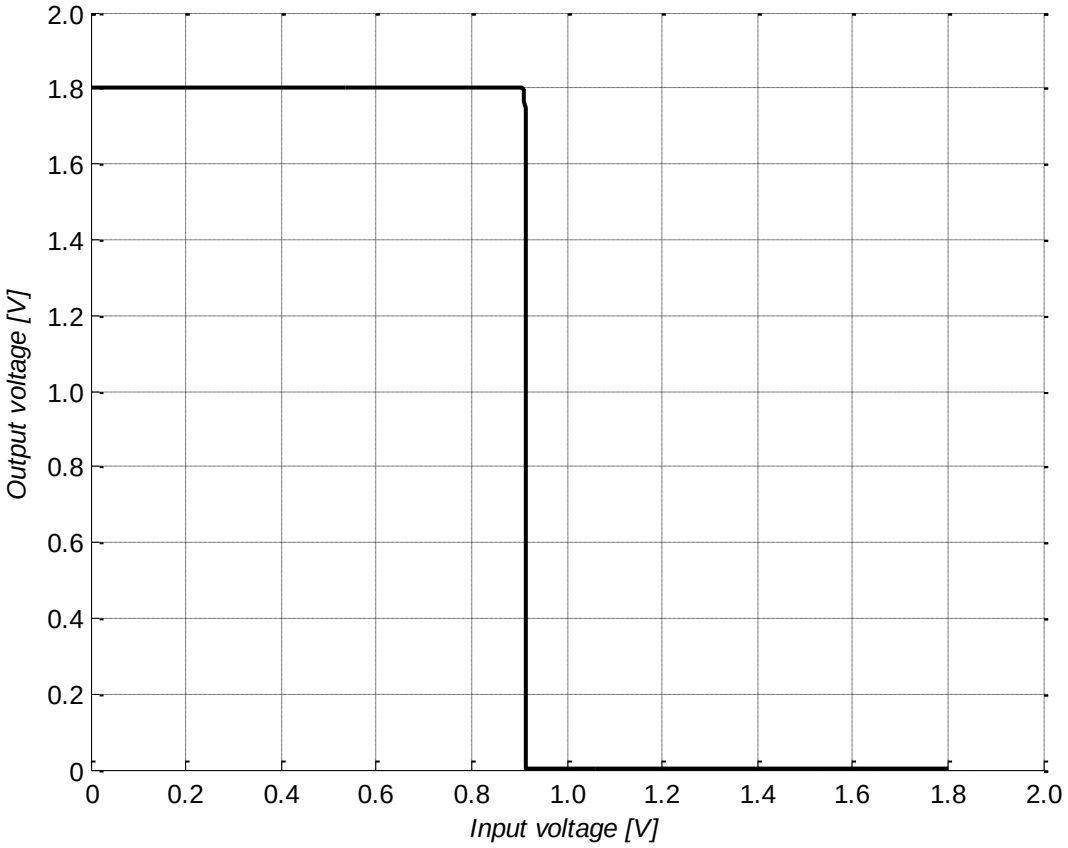


Figure 5.19. Transfer function of the thick gate oxide FET inverter.

As shown in Figure 5.19, an input of 1.2 V from the previous inverter stage is enough to trigger the transistors to output 0 V. With this design, only one inverter can output a logic 1 at a time and trigger its corresponding diode. When the input is 0 V to this inverter stage, i.e. a logic 0 from the previous inverter stage, the output is 1.8 V and is sufficient to bias the diode and output the required voltage. The output buffer maintains this required voltage and supplies it as an input to the VGA.

5.7 COMPLETE SYSTEM INTEGRATION

The complete system includes the entire APD circuit and the three-stage PA. The complete system is shown in Figure 5.20 where the patterned and solid rectangle blocks are the APD system and PA respectively.

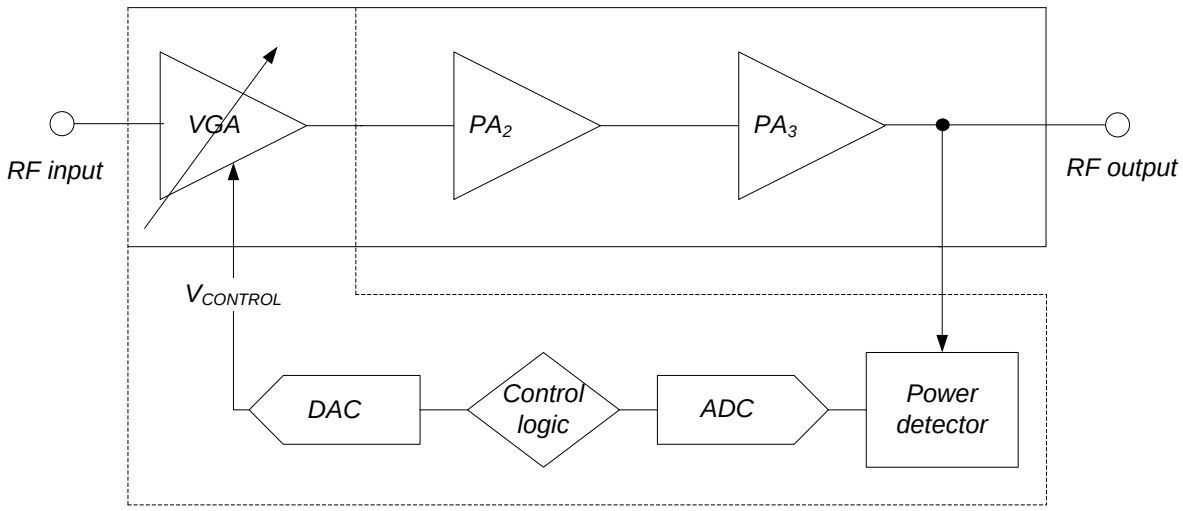


Figure 5.20. APD circuit with PA.

The feedback path from the output of the PA to the power detector and back to the input of the PA makes the predistortion system adaptable as shown in Figure 5.20. The entire system is designed to be fabricated on-chip. The only section that is off-chip is the reference voltage circuits of the ADC. It was decided to keep these off-chip in order to control the reference voltages externally and not to rely on on-chip voltage dividers. The operation of the APD system and the PA is shown in Table 5.3.

Table 5.3. Operation of the complete system.

P_{OUT} [dBm]	Condition	Comparator output	XOR output	$V_{CONTROL}$ [V]
< -7.8	$V_{IN} < V_{REF1}$	00000	100000	1.52
> -7.5	$V_{IN} > V_{REF1}$	10000	010000	1.55
> -2.75	$V_{REF2} < V_{IN} < V_{REF3}$	11000	001000	1.57
> 5	$V_{REF3} < V_{IN} < V_{REF4}$	11100	000100	1.59
> 7.5	$V_{REF4} < V_{IN} < V_{REF5}$	11110	000010	1.62
> 9.5	$V_{IN} > V_{REF5}$	11111	000001	1.7

As shown in Table 5.3, a corresponding digital signal is generated (XOR output) when the detected output power of the PA satisfies the condition set out in Table 5.3. This digital signal then commands the DAC to output the desired control voltage, which then drives the VGA.

5.8 SIMULATION RESULTS

Two separate systems were evaluated, one with only the PA and the other with an identical PA connected to the APD. This was done in order to measure and analyse their performance separately.

5.8.1 PA WITHOUT PREDISTORTION

The small-signal and large-signal simulations were performed on the PA. The results of these simulations are described below.

5.8.1.1 Small-signal simulations

The small-signal parameters were simulated using the two-port analysis method in Cadence Virtuoso. The simulated *S*-parameters of the non-linear PA are shown in Figure 5.21. The small-signal parameters were simulated from 1 Hz to 100 GHz to analyse the behaviour of the PA at various frequencies.

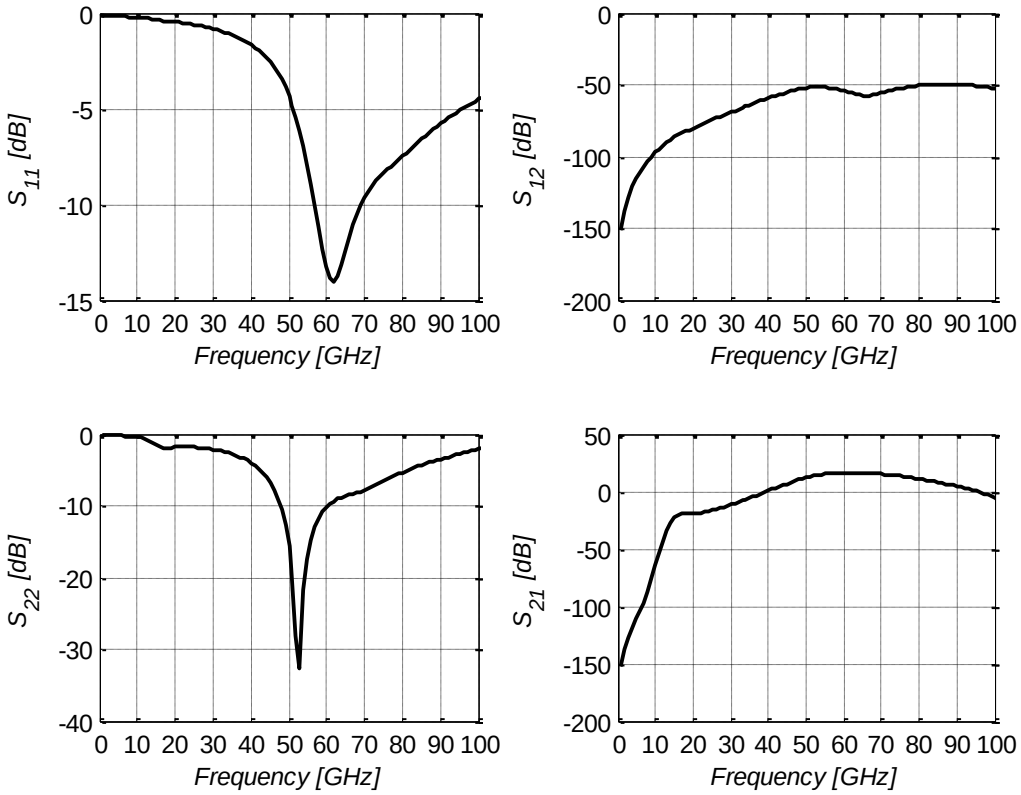
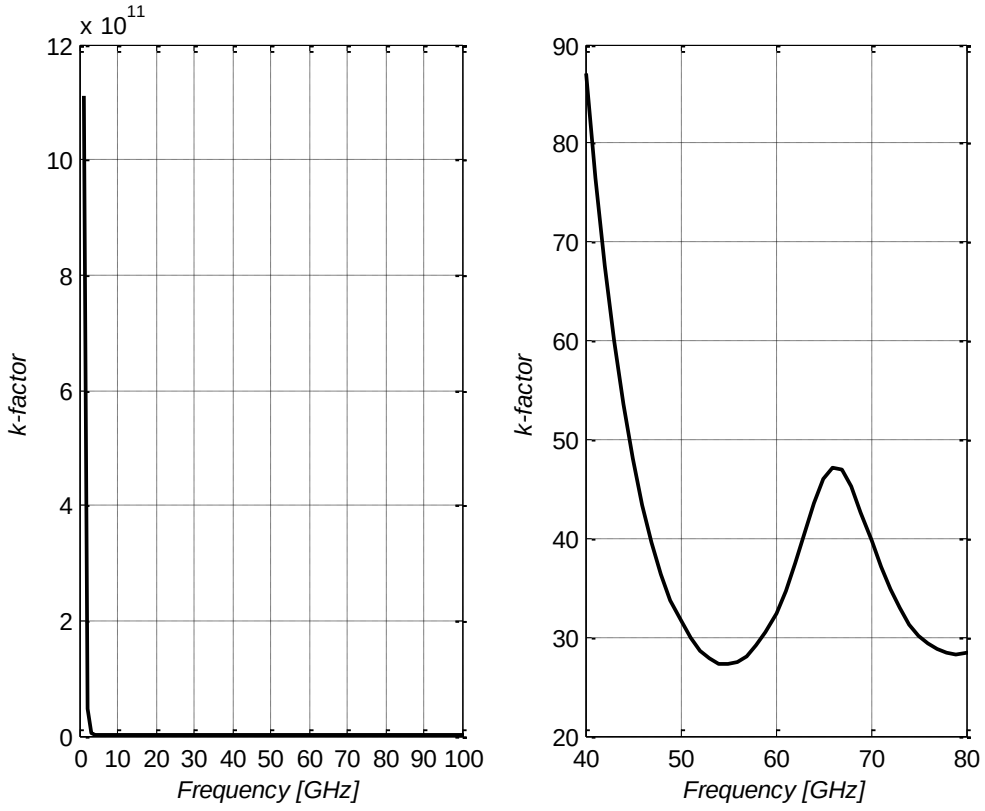


Figure 5.21. *S*-parameters for the non-linear PA.

Figure 5.21 shows that the S_{11} has a notch of -14.02 dB at 62 GHz and -13.27 dB at 60 GHz, indicating that the input of the PA is well matched. The S_{22} has a notch of -32.73 dB at 53 GHz and -10.22 dB at 60 GHz. The reason for the output match not occurring at 60 GHz is because of the load-pull approach being implemented instead of the conjugate match method at the output of the PA. The S_{12} parameter is -54.08 dB at 60 GHz. The peak small-signal gain, S_{21}, is 16.56 dB at 60 GHz.

The *k*-factor and the B_1 for the non-linear PA are shown in Figure 5.22 and 5.23 respectively. Each stage of the PA was proved to be unconditionally stable, as described previously.



(a) (b)

Figure 5.22. The overall *k*-factor for the non-linear PA consisting of **(a)** the *k*-factor from 1 Hz to 100 GHz and **(b)** the *k*-factor zoomed in at the minimum value.

The overall *k*-factor from 1 Hz to 100 GHz for the three-stage non-linear PA is shown in Figure 5.22 (a), showing that it is always greater than 1. Figure 5.22 (b) shows the *k*-factor zoomed in at the minimum, which is 27.22 at 55 GHz and 32.37 at 60 GHz.

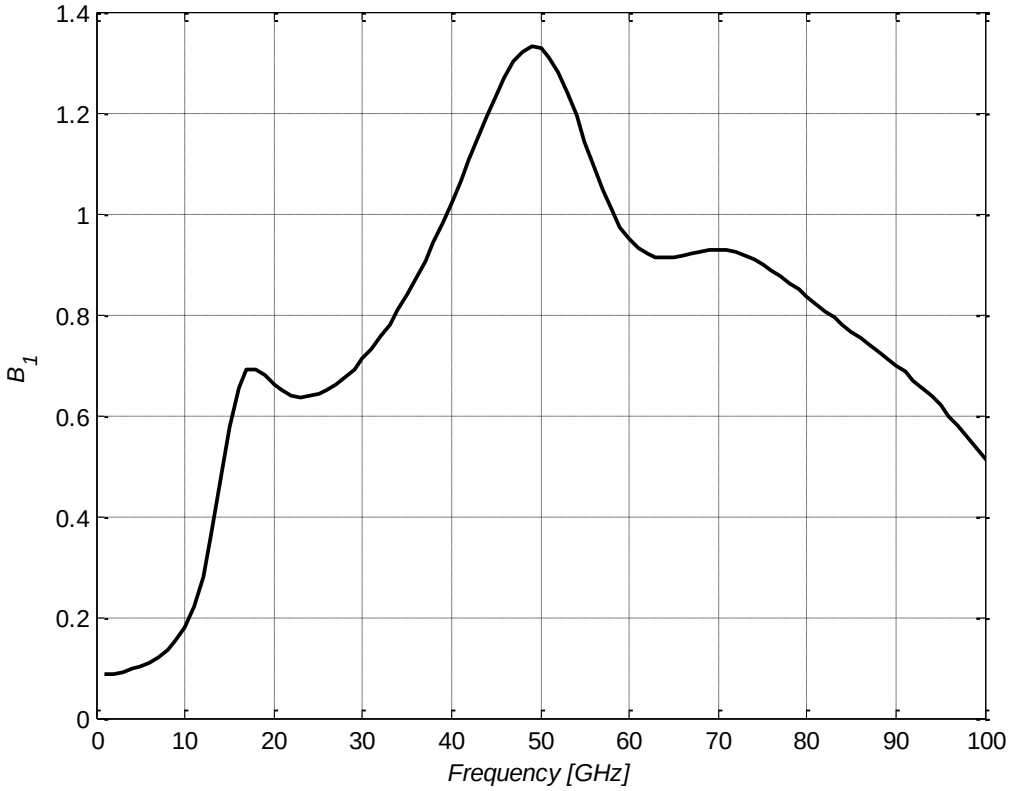


Figure 5.23. B_1 for the non-linear PA.

B_1 is 0.95 at 60 GHz, as shown in Figure 5.23. Figures 5.22 and 5.23 show that the overall *k*-factor and B_1 are greater than 1 and 0 respectively and therefore the three-stage non-linear PA is unconditionally stable from 1 Hz to 100 GHz.

5.8.1.2 Large-signal simulations

The large-signal simulations were performed using the PSS simulation in Cadence Virtuoso. The large signal gain and output power versus input power of the non-linear PA are shown in Figure 5.24 and the PAE of the non-linear PA is shown in Figure 5.25.

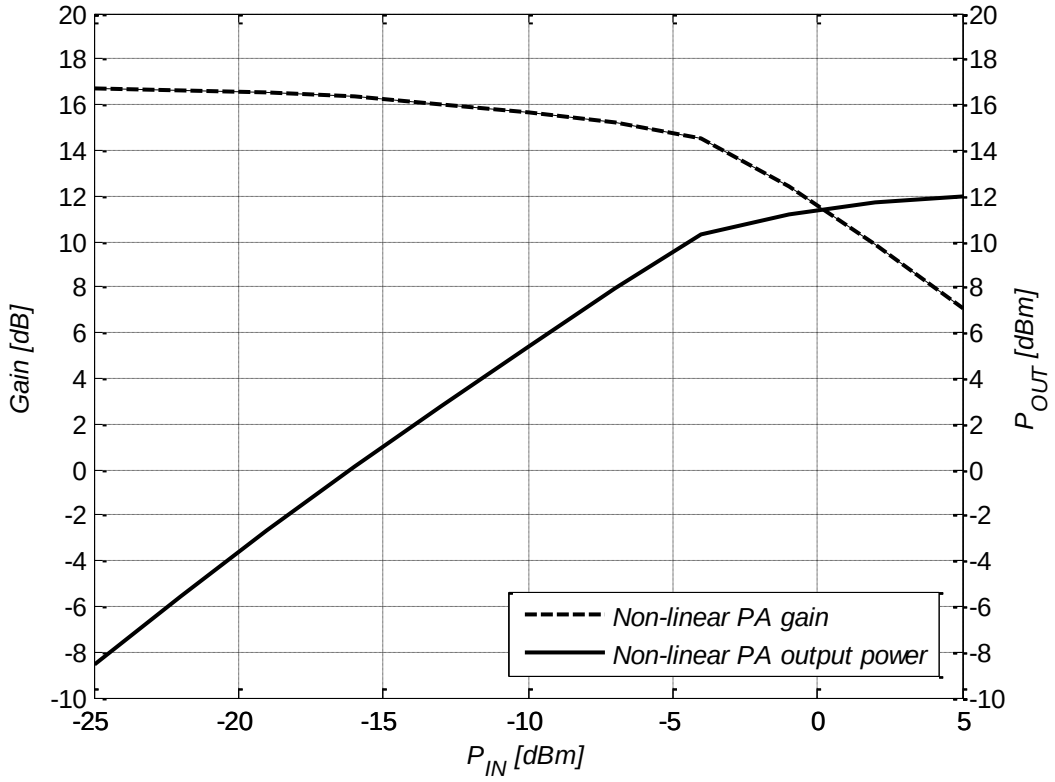


Figure 5.24. Non-linear PA gain and output power.

As shown in Figure 5.24, the gain and output power were simulated from an input power of -25 dBm to 5 dBm, resulting in a maximum gain of 16.5 dB for the non-linear PA. The saturated output power is approximately 12 dBm. The $IP_{1\,dB}$ of the non-linear PA occurs at -10 dBm.

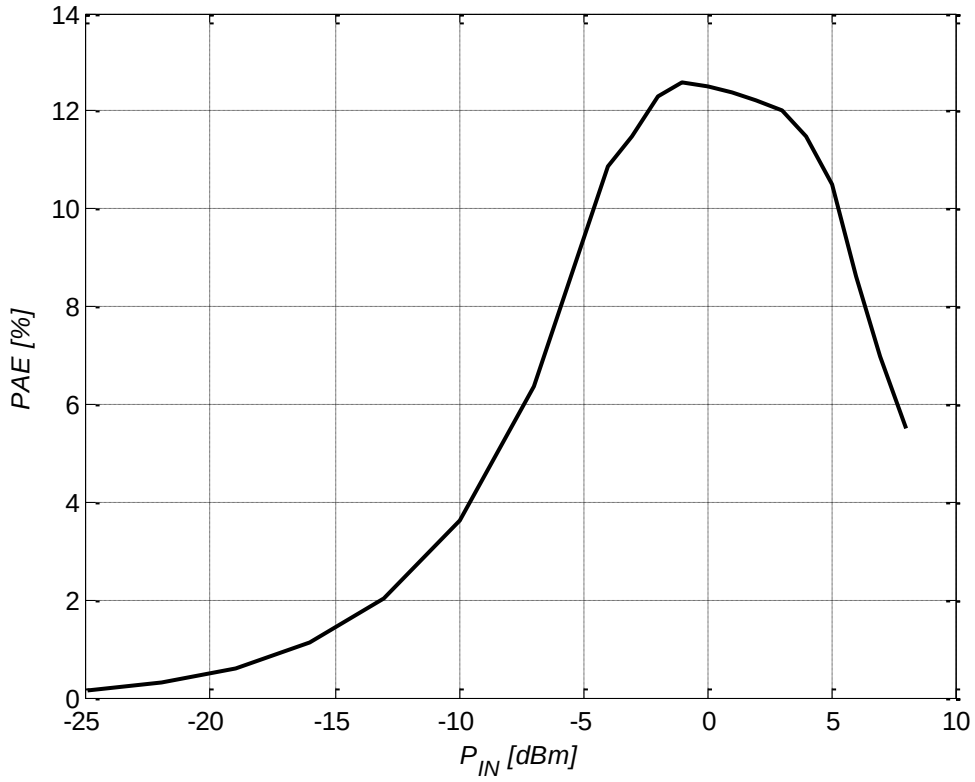


Figure 5.25. PAE for the non-linear PA.

Similar to the large-signal gain and output power simulations, the PAE of the non-linear PA was simulated. The peak PAE of the non-linear PA as shown in Figure 5.25 is 12.6 % at an input of power of -1 dBm.

5.8.2 PA WITH PREDISTORTION

Similar simulations were performed with the PA integrated with the APD. The non-linear PA results are redrawn with the PA with the APD results for comparison purposes.

5.8.2.1 Small-signal simulations

The small-signal results for each bias voltage are shown in Figures 5.26 to 5.27. To measure the *S*-parameters and stability factors, each of the bias voltages (1.52 V to 1.7 V) was kept constant and the frequency was varied from 1 Hz to 100 GHz.

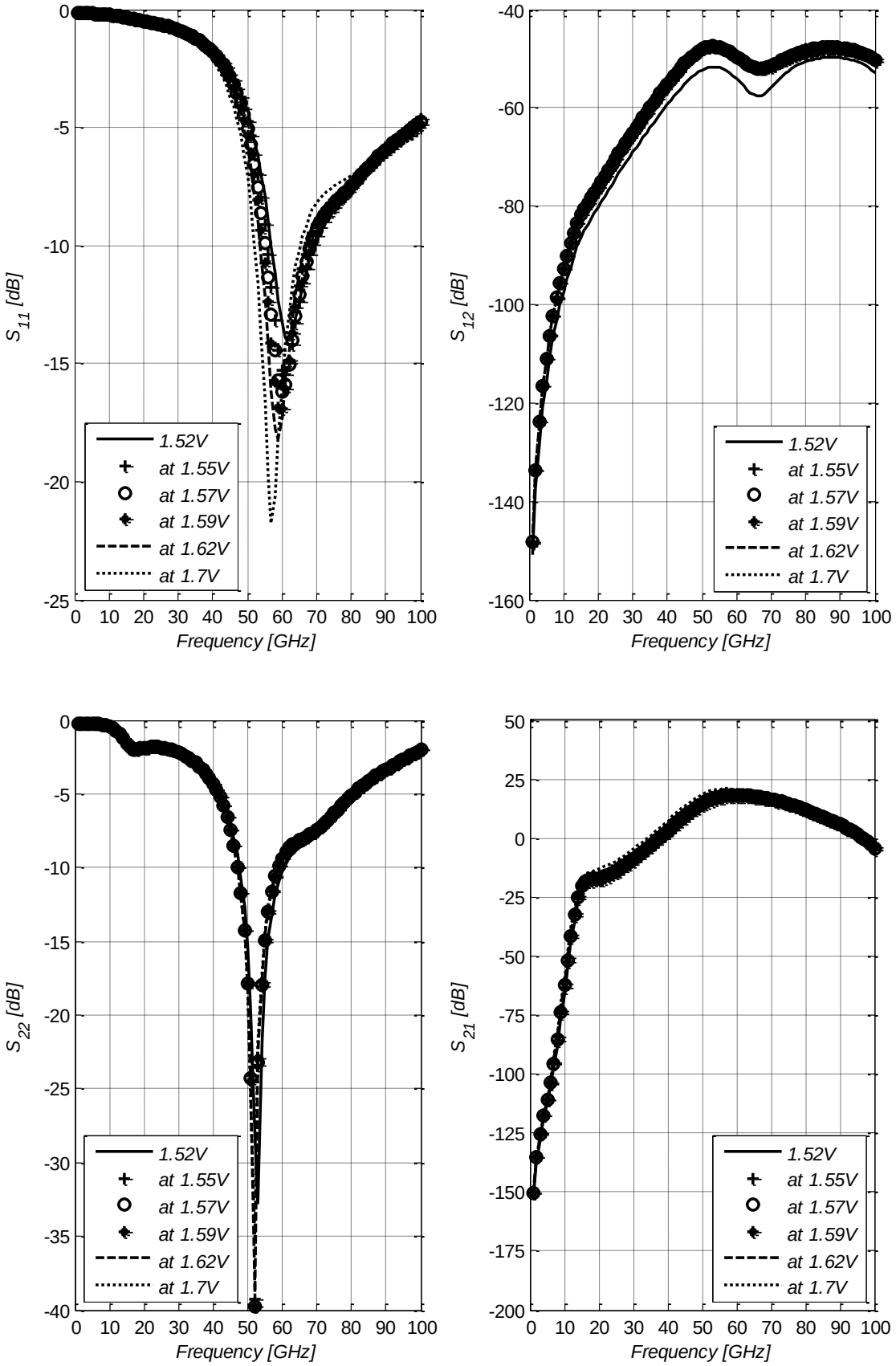
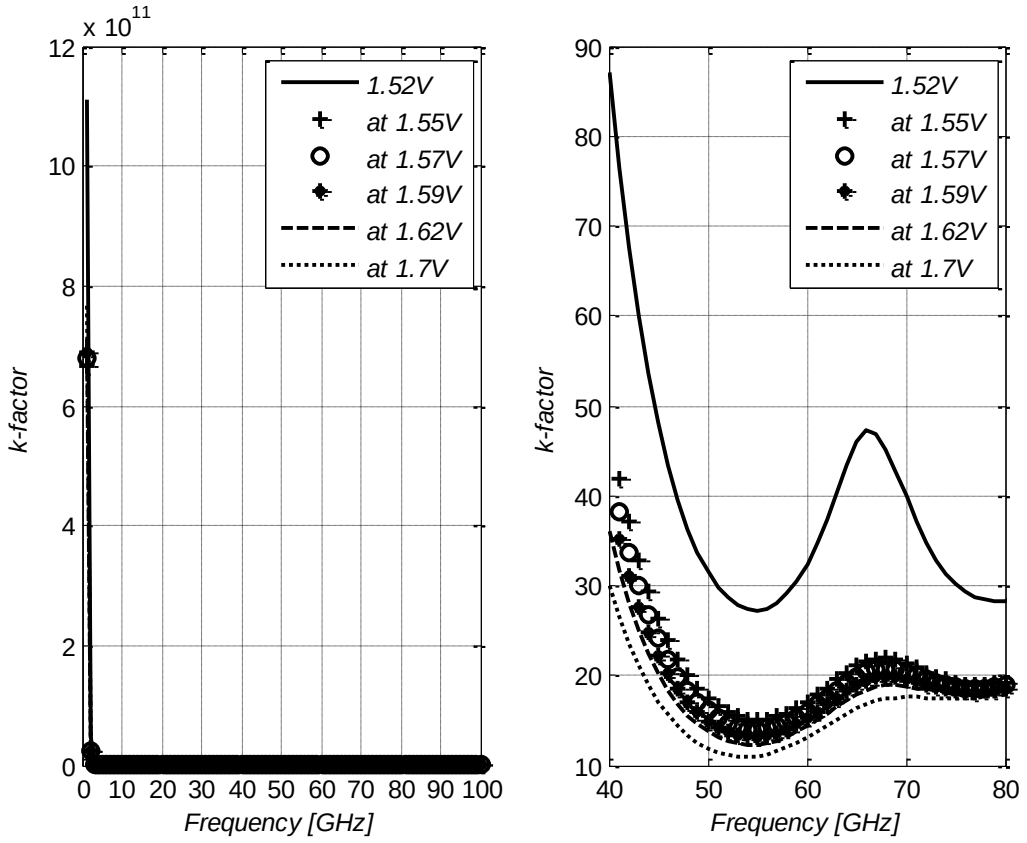


Figure 5.26. *S*-parameters for bias voltages 1.52 V to 1.7 V.

In Figure 5.26 the notch of the S_{11} parameter varies between -14.02 dB at 62 GHz when the bias voltage is 1.52 V to a minimum of -21.74 at 57 GHz when the bias voltage is 1.7 V. This indicates that the input matching network remains well matched as the bias voltage increases. The S_{12} parameter increases slightly from -54.08 dB to -50.35 dB at 60 GHz when the bias voltage changes from 1.52 V to 1.7 V. However, the input and output ports of the PA still remain well isolated. The S_{22} achieves a minimum of -39.71 dB at 52 GHz. As mentioned in section 5.8.1.1, this is because of the load-pull matching technique being used at the output stage of the PA. The small-signal gain, S_{21}, increases from 16.56 dB to 20.66 dB because of the bias voltage increase from 1.52 V to 1.7 V.

5.8.2.2 Stability analysis

The *k*-factor and B_1 parameters for each bias voltage from 1.52 V to 1.7 V are shown in Figures 5.27 and 5.28 respectively. For each of the bias voltages it can be seen that the PA is unconditionally stable from 1 Hz to 100 GHz.



(a) (b)

Figure 5.27. The overall *k*-factor for bias voltages from 1.52 V to 1.7 V consisting of **(a)** the *k*-factor from 1 Hz to 100 GHz and (**b)** the *k*-factor zoomed in at the minimum value.

As shown in Figure 5.27 (a) and Figure 5.27 (b), the overall *k*-factor for the three-stage PA is always greater than 1 for bias voltages 1.52 V to 1.7 V. The zoomed in minimum *k*-factor value shown in Figure 5.27 (b), decreases with increasing bias voltage. The lowest *k*-factor value of 10.98 occurs at 54 GHz when the bias voltage is 1.7 V. At 60 GHz the *k*-factor value is 13.09.

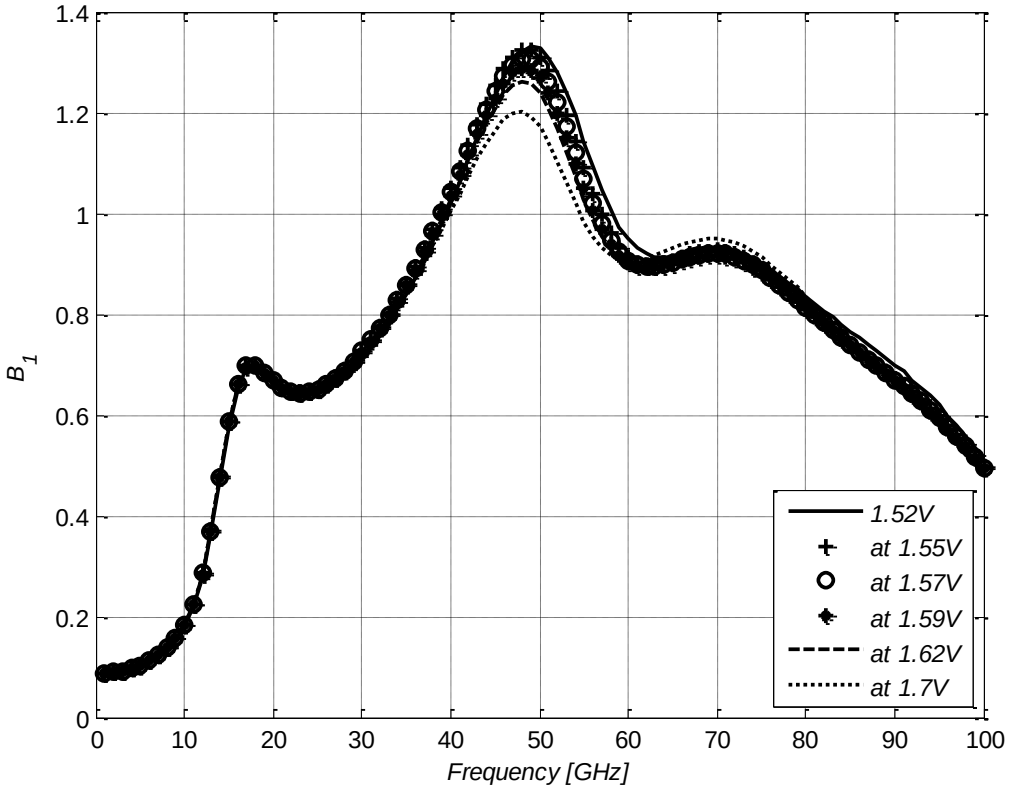


Figure 5.28. Overall B_1 factor for bias voltages 1.52 V to 1.7 V from 1 Hz to 100 GHz.

The B_1 factor shown in Figure 5.28 has the lowest set of values for the bias voltage of 1.7 V with 0.9 at 60 GHz. However, B_1 is always greater than zero for bias voltages 1.52 V to 1.7 V from 1 Hz to 100 GHz. Therefore from Figure 5.27 and 5.28, it can be seen that the PA is unconditionally stable for bias voltages 1.52 V to 1.7 V from 1 Hz to 100 GHz.

5.8.2.3 Large-signal simulations

Figure 5.29 plots the non-linear and linear gain and output power of the PAs. The PAE of both the non-linear and linear PAs is shown in Figure 5.30.

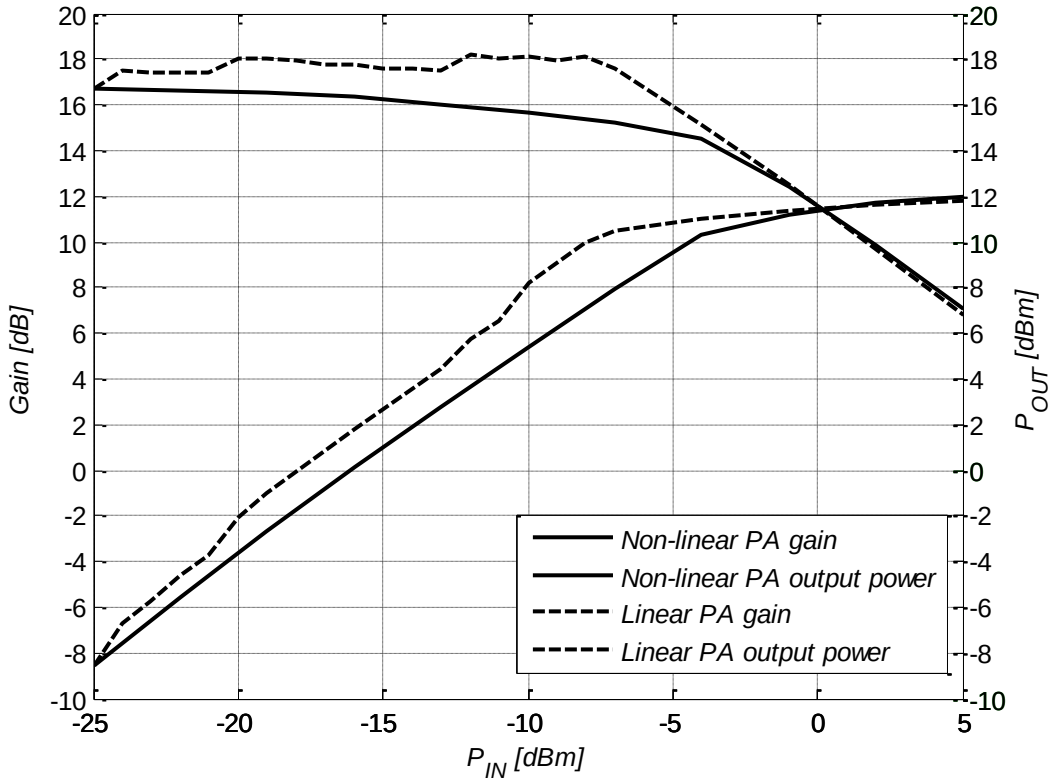


Figure 5.29. Gain and output power for the non-linear and linear PAs.

Using the control logic as described in Table 5.3, the results for the gain and output power of the linear PA are shown in Figure 5.29. As shown in Figure 5.29, increased gain and linear output power of the PA are achieved when APD is applied to the PA. The gain of the linear PA is fixed around 18 dB, resulting in an increased $IP_{1\,dB}$ of -6 dBm and improved linear output power. The linear PA shows an improvement of 2.5 dBm, at which point no further linearisation can be applied and the linear PA begins to saturate.

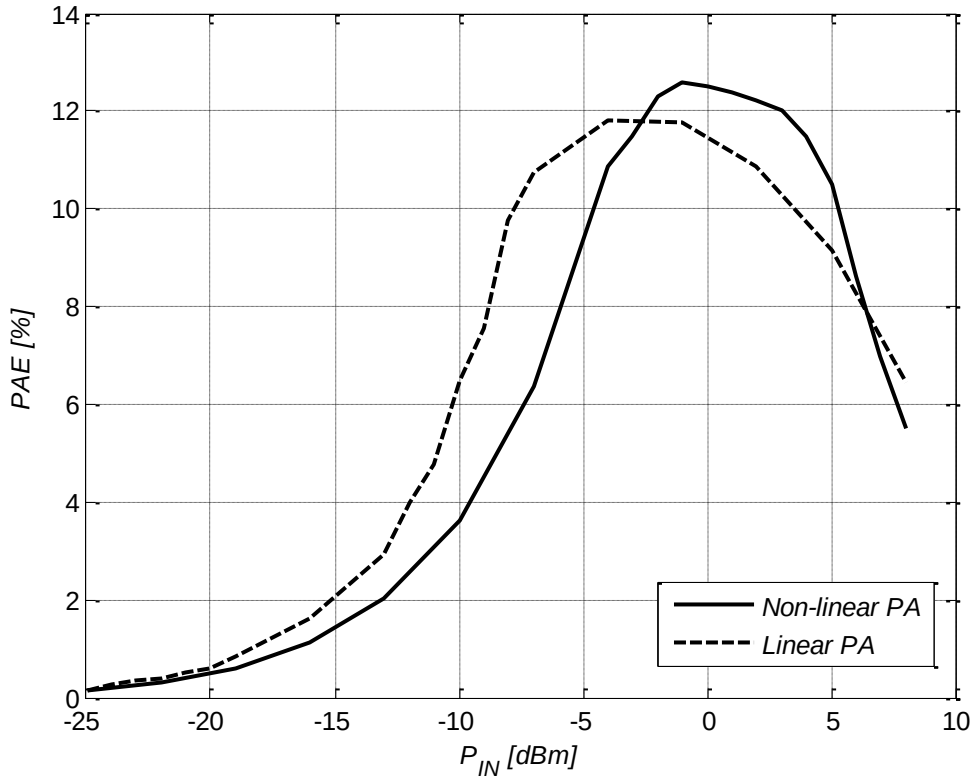


Figure 5.30. PAE of the non-linear and linear PA.

The peak PAE of the linear PA is 11.8 % and 11 % at the $IP_{1\,dB}$ compared to the non-linear PA with a peak PAE of 12.6 % and 3.63 % at its $IP_{1\,dB}$ as shown in Figure 5.30. The reduced PAE of the linear PA (as defined in (2.5)) is expected because of the increased P_{DC} due to the dynamic bias mechanism.

5.8.3 IMD3 SIMULATIONS

The IMD3 simulations were done using the PSS in conjunction with the PAC analysis simulations in Cadence Virtuoso. The results and comparison of the non-linear and linear PAs are shown in Figure 5.31.

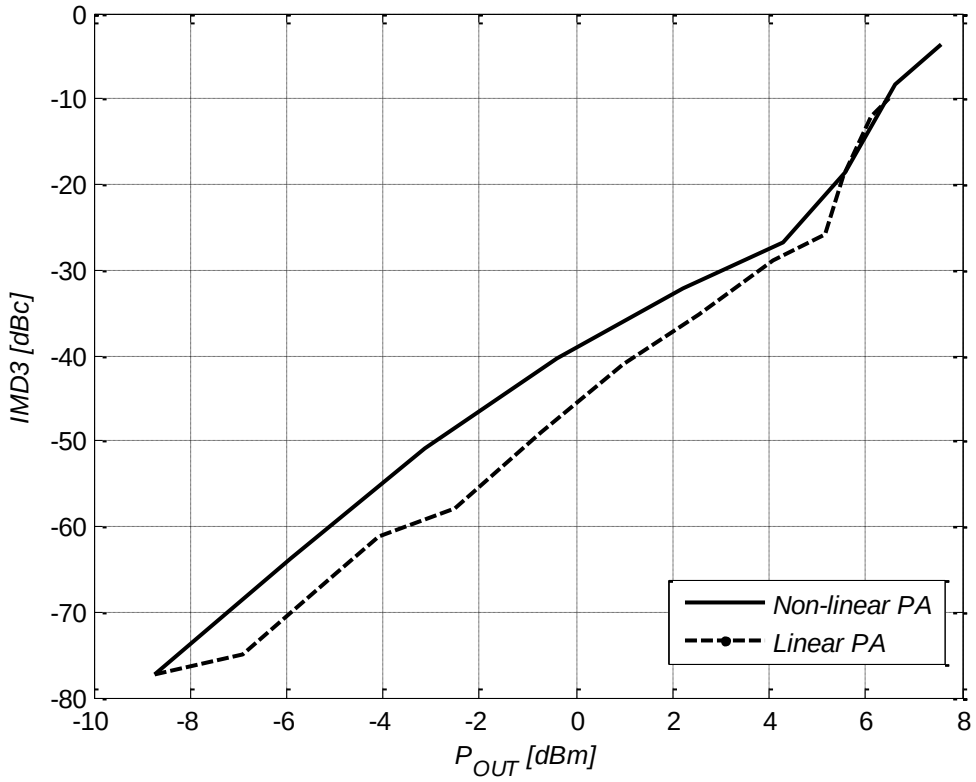


Figure 5.31. IMD3 components for non-linear and linear PA.

The IMD3 components are shown in Figure 5.31. A 100 MHz tone spacing was used in the two-tone test to analyse the IMD3 components. The use of the APD linearisation technique results in a reduction of the IMD3 component. Optimum reduction is achieved for output power between -7 and 3 dBm with a maximum IMD3 improvement of 10 dB being achieved.

5.9 MEASUREMENT RESULTS

The prototyped IC for this research work is shown in the micrograph in Figure 5.32. The circuit layouts of the PA and APD with their subsystems are shown in Appendix A. This IC was part of an MPW run sponsored by MOSIS, which included two additional subprojects.

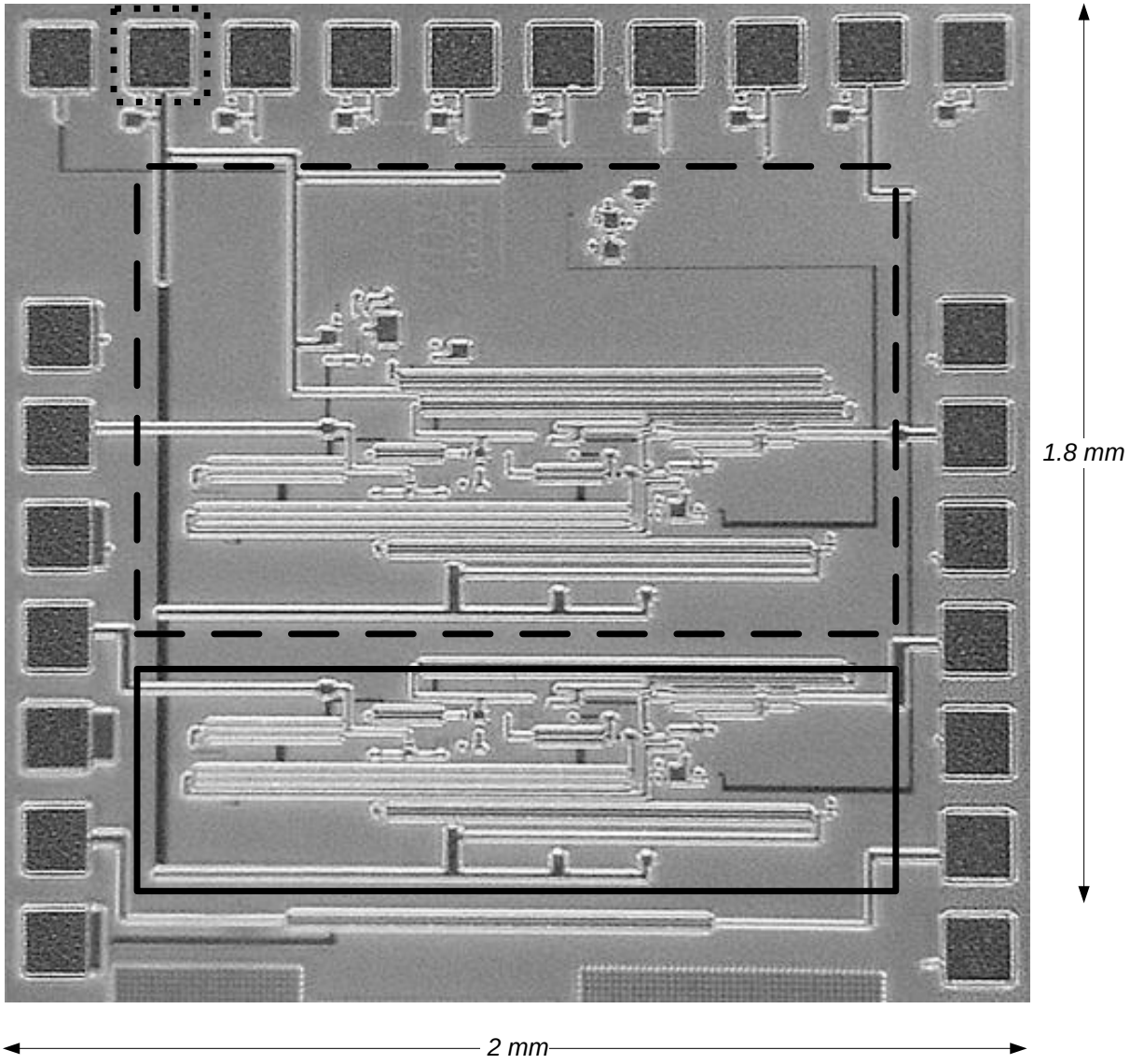


Figure 5.32. Prototyped IC consisting of the non-linear PA and linear PA with APD.

As shown in Figure 5.32, the complete IC consists of the non-linear PA in the black rectangle and linear PA and APD with their subsystems in the patterned rectangle. The entire IC occupies an area of 2 mm × 1.8 mm. Three ICs were mounted onto three PCBs in order to conduct the measurements.

5.9.1 DC BIASING PROBLEM

As mentioned in chapter 3, the measurement equipment included the VNA, probe station and an external power supply. The external power supply was used to provide the required

bias and reference voltages for the IC. Because of layout restrictions there is only one bondpad to provide the bias voltage, V_{BIAS}, for both the non-linear and linear PAs, as shown by the dotted square on the top left of Figure 5.32. V_{BIAS} was applied to the three PCBs separately and the total current for each PCB was measured, as shown in Figure 5.33.

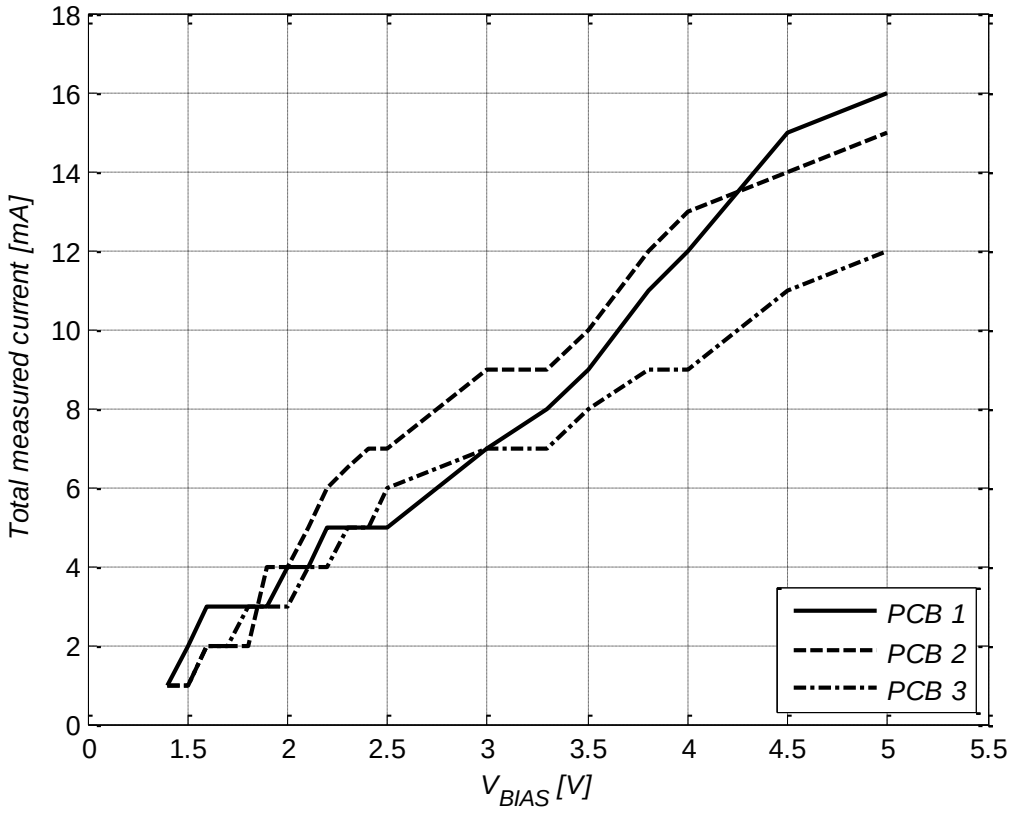


Figure 5.33. Total measured current for different V_{BIAS} voltages and PCBs.

As shown in Figure 5.33, after supplying the correct bias voltage (1.8 V) it was noticed that the total current being drawn was too small. This meant that the power transistors were not correctly biased. To measure the effect of increasing V_{BIAS}, V_{BIAS} was increased to 5 V, as shown in Figure 5.33, and the total current was measured for each of the three PCBs.

The reasons for the low total measured current are:

- The biasing networks with temperature compensation technique for each stage of the PA were designed and implemented on-chip. The bias voltage, V_{BIAS}, for these biasing networks for both the non-linear and linear PAs was supplied from one

bondpad connection because of layout restrictions. Therefore only the total current being drawn by all three stages of the non-linear and linear PAs could be measured. If the biasing networks had been placed off-chip, the current being drawn to each stage could have been analysed; however, this was not possible, as the VGA required an on-chip biasing network to function.

- Increasing V_{BIAS} results in an increase in the total measured current, as shown in Figure 5.33, for each of the PCBs. For *PCB 1*, the total measured current is 2 mA at V_{BIAS} of 1.5 V (effective resistance, R_{EFF} = 750 Ω). Although the total measured current increases with V_{BIAS}, R_{EFF} is still too large and the power transistors are still not correctly biased. With the power transistors not being correctly biased at the design bias values, no meaningful measurements can be conducted.
- R_{EFF} can be attributed to the resultant parasitic resistance from each contact, via and metal level length. Multiple vias were used in the design. From the process parameter design guide, a worst case parasitic resistance can be as much as 30 Ω between a single top metal level via and a contact coupled with the metal length resistance.
- Many, long interconnects were used between the DC connections from the single bondpad to the bias nodes and between the TLs and each power transistor owing to layout and size restrictions. The current carrying capability of the interconnects depends on the metal level type and on the width of these interconnects. The top metal level has the highest current carry capability (> 10 mA at minimum width) and was used in most of the interconnects between the DC bondpad and PA biasing points. Although these interconnects were made as wide as possible to carry the required current, these many, long interconnects introduced additional parasitics. Also, with each interconnect vias were required to interface between different metal layers, increasing the parasitics. These parasitics reduced the current-carrying capabilities of the interconnects.
- The design used a seven metal stack layer instead of a five metal stack layer to ensure that the IC used the same metal stack layers as the other subprojects. This resulted in additional vias (metal 5 to 6 via and metal 6 to 7 via) being included in the design, adding more parasitics.

The bondpad restrictions were laid out by the RF probe interfacing and wirebonding requirements. It was recommended that the RF signal and DC bondpads be separated for the following reasons:

- The RF input and output bondpads should be located on the left and right side of the chip area respectively.
- Sufficient clearance between the DC wirebonds and RF pads should be provided. The minimum clearance distance set out by the Infinity probes is 200 μm. This is to prevent the RF probes and wirebonds coming into contact. Any additional DC bondpads would interfere with the RF probes.
- Wirebonding was done on the DC bondpads. The wirebonding process required that all the DC bondpads be located in one line either on the top or bottom of the die area. Otherwise the wirebonds might touch and connecting it to the PCB contact would have been difficult.
- The DC bondpads took the maximum available space and no additional space was available (in a single line format) for additional DC bondpads. Even if additional bondpads were available, long interconnects would still have been required.

Because of the complexity of the entire system, each of the subsystems had to be tested separately to identify where the exact problem(s) could be located. However, owing to the space restrictions of the MPW run, this was not possible. The problems mentioned above severely degraded the performance of the IC and therefore no further measurements could be performed.

5.9.2 FUTURE DESIGN IMPROVEMENTS

In the circuit design, some of the subsystems can be placed off-chip especially the digital circuitry. Although this would not be a complete on-chip solution, it would provide additional space for the analogue circuitry. Also in future with the availability of DC probes, on-wafer DC biasing can be done, eliminating the need for the supporting PCB and wirebonding.

5.10 CONCLUSION

Each of the subsystems to realise the PA and the APD was designed, simulated and evaluated in this chapter. All the subsystems were designed from first principles in order to integrate these systems on-chip.

HBTs were used in the design of the PA, while CMOS transistors were used in the design of the APD system. A three-stage PA was designed, with the first stage being converted to a VGA in order to realise the predistortion function. The predistortion circuit was then designed and integrated with the PA. This chapter also discussed the integration of the entire system and the decision criteria of the APD circuit. The PA with the predistortion circuit was integrated on-chip and was fabricated.

The HBTs, MOSFETs and passive models all include parasitic modelling and were included in the optimised design values. The parasitics for the active device models included a set of parasitic resistors and capacitors and were determined through design guidelines.

The simulation results were also presented in this chapter. Both the non-linear and linear PAs are unconditionally stable. Without any linearisation the PA achieves a P_{SAT} of 11.97 dBm, an $IP_{1\,dB}$ of -10 dBm and a peak PAE of 12.6 %. With linearisation, the predistortion is applied to the PA by varying the gain of the PA through its VGA. After linearisation the PA has an improved $IP_{1\,dB}$ of -6 dBm and a peak PAE of 11.8 %.

The literature study, theoretical and mathematical analysis as discussed in the previous chapters and the simulation results in this chapter, have shown that APD is able to reduce the distortion components and improve the linearity of the PA. Previous works have shown that APD can be used for linearity enhancement, however these were based on different technologies but still focusing on linearity improvement using predistortion. Although the hypothesis could not be completely evaluated practically, the design methodology and simulations provide sufficient evidence thus proving the hypothesis. The primary and secondary research questions were also answered, viz.:

- A low-complexity, high-performance APD circuit can be realised to reduce the distortion of PAs at 60 GHz using a voltage signal based on the output power of the PA to increase the gain of the VGA, thereby realising the predistortion function.
- With the use of APD, an optimum IMD3 reduction of 10 dB is achieved. The linear PA has an improved linear output power of 2.5 dBm compared to the non-linear PA.

Because of DC biasing problems, the power transistors in the PA were not correctly biased. Therefore no meaningful measurements could be performed on the prototyped IC.

CHAPTER 6 CONCLUSION

6.1 INTRODUCTION

This chapter provides a summary of the entire research work covered in this thesis to evaluate the hypothesis critically. The research problem addressed in this work is the distortion experienced by PAs at mm-wave frequencies. This results in degradation in the transmitter's performance. APD was proposed as the external linearisation technique to solve this research problem. A complete APD solution and PA were designed and implemented in a 0.13 μm SiGe IBM BiCMOS process to test and validate this hypothesis.

This chapter also provides discussions on the challenges and limitations of this research work. Suggestions for future work and improvements to this research are also presented at the end of the chapter to conclude this thesis.

6.2 CRITICAL HYPOTHESIS EVALUATION

The hypothesis and research questions were presented in chapter 1. The hypothesis is repeated here for the reader's convenience:

If the linearity of PAs is related to the distortion in PAs, then if APD is used to reduce the distortion in PAs, this will improve the linearity in PAs.

The hypothesis and the research questions were proven and answered successfully through the design, simulation and prototyping of the PA and APD system. The following important aspects of the research are described below:

- From the literature review it was observed that not enough attention had been paid to addressing the linearity of PAs at mm-wave frequencies. Most of the current work was dedicated to improving the PA's output power and gain. Spectral efficient modulation schemes proposed at mm-wave frequencies require PAs to output minimal distortion, therefore linearity in PAs cannot be ignored.

- The PA was designed using the 0.13 μm SiGe IBM process. The PA was designed for maximum output power using the load-line approach at the output stage instead of the complex conjugate method. There were three-stages; each of these was optimally matched using lumped capacitors and TLs. Bypass capacitors and RFCs were used extensively to isolate the DC and AC signals.
- The SiGe HBT inherently suffers from distortion, the most severe being the IMD3 components. The Volterra series analysis characterised these distortion components, showing the contribution of the IMD3 component to the fundamental signal. It was observed that the IMD3 component can be reduced by increasing the bias current up to a certain value.
- To overcome these distortions, an external linearisation technique needs to be applied to the PA. Of the many linearisation techniques currently available, predistortion was proposed. Using predistortion, the inverse characteristic function of the PA was applied at its input. Predistortion provided the advantage of low complexity, low cost and good linearisation performance in reducing the PA's IMD3 component. These qualities make predistortion very attractive for on-chip implementation at mm-wave frequencies.
- The predistortion was applied at the input of a three-stage PA, therefore modifying the first stage of the PA into a VGA by varying its bias current and thus its gain. The predistortion was made adaptive as a function of the PA's output power. This allowed the linearity of the PA to be optimised. The APD provided a stable gain until the saturation point, therefore maximising the output power of the PA.
- The adaptation implementation included a power detector, ADC, control logic circuit, DAC and VGA. The APD solution occupied a chip area of approximately 1.04 mm^2. The ADC, control logic and DAC were implemented in CMOS.
- The user can select at which PA output power level to apply the predistortion, using the external comparator reference voltages. There are five reference voltages, providing sufficient control of the APD to the user. Once the reference voltages have been set by the user, the system is completely independent of any user input and will apply the predistortion automatically.
- All the subsystems were simulated and tested individually as well as on a systems level in Cadence Virtuoso using the PDK components provided by the foundry. Layout of the entire circuit and prototyping of the IC were also performed.

- Two identical PAs were evaluated at 60 GHz, one without any linearisation applied to it and the other with APD applied. The simulations revealed that the $IP_{1\,dB}$ increased by 4 dBm for the linear PA and an optimal reduction in IMD3 of 10 dB was achieved with the APD.

6.3 CHALLENGES AND LIMITATIONS

PAs need to operate efficiently and with minimal distortion, two conflicting requirements. Improving the linearity of PAs at mm-wave frequencies is consequently an extremely difficult task. This is further constrained by the scaled transistor size and breakdown voltages adding further restrictions on the gain and output power of these PAs. The APD linearisation technique can only be applied up to the saturation limit of the PA, at which point no further linearity improvement can be achieved. This is a physical limitation of the PA itself.

The limited sponsored chip area resulted in an MPW run with other subprojects. The entire circuit (PA with APD and PA alone) was placed on the sponsored chip area with the other subprojects aligned next to it. As mentioned in chapter 5, each of the subsystems could not be separated and tested on a unit level for functionality and performance. This made it very difficult to probe and debug where a fault might lie in the practical evaluation of the IC.

Once again owing to the area restrictions, the bondpads and components had to be optimally positioned for space rather than for ideal performance. This resulted in a reduced number of bondpads, especially DC bondpads, where some were feeding many subsystems.

The DC wirebond connections and the custom PCBs introduced additional parasitic effects that negatively affected the performance of the system. Although these effects can be de-embedded from the measured results, the performance of the system will still be degraded. The use of on-chip DC probes can help reduce these unknown and unwanted effects.

6.4 SUGGESTED FUTURE WORK

The use of other simulation environments such as Agilent ADS (with foundry support) can be investigated in future. These simulation environments can be used to verify the simulation and layout results from Cadence Virtuoso. This will provide greater confidence in the simulation and layout of the circuit to the designer.

Characterisation of the active and passive devices for the IBM BiCMOS8HP process using measurement equipment can be also investigated. This will provide invaluable information such as parasitic effects on the performance of these devices. Modular testing of each subsystem in the PA and APD system can also be investigated in future.

This work focused on improving the linearity of a single-ended PA at 60 GHz. PAs at higher frequencies such as 77 GHz and above can be investigated. Although operating PAs at higher frequencies using the IBM BiCMOS8HP process will result in reduced performance, it can highlight the current limitations and provide data for future improvements of the technology. As mentioned in chapter 2, Class B and C PAs are not recommended for use with an external linearisation technique due to the large amount of distortion that they produce. However these PAs are more efficient than Class AB PAs. Therefore to improve the efficiency of Class AB PAs, the use of other dynamic biasing methods such as *switched* dynamic biasing can also be investigated.

The linearity improvement through the use of the APD in this research work focused on the amplitude aspect of the IMD3 component and not on the phase of this distortion component. Further work can be done on investigating and incorporating both amplitude and phase linearity improvement for PAs at 60 GHz and above.

The APD can be further improved upon in order to make the PA's linearity less sensitive to process, voltage and temperature variations. This can be done by using neural networks with LUTs to learn and update themselves automatically.

REFERENCES

[1] S. Xiao, M. Zhou, and Y. Zhang, *Millimeter Wave Technology in Wireless PAN, LAN, and MAN*, Auerbach Publications, Boca Raton, FL, 2008.

[2] R. C. Daniels, J. N. Murdock, T. S. Rappaport, and R. W. Heath, "60-GHz Wireless: Up Close and Personal", *IEEE Microwave Magazine*, vol.11, no. 7, pp. 44–50, December 2010.

[3] S. Cripps, *Advanced Techniques in RF Power Amplifier Design*, Artech House, Norwood, MA, 2002.

[4] F. M. Ghannouchi, "Power Amplifier and Transmitter Architectures for Software Defined Radio Systems", *IEEE Circuits Systems Magazine*, vol. 10, no. 4, pp. 56–63, December 2010.

[5] Y.-S. Lee, S.-Y. Lee, K.-I. Jeon, and Y.-H. Jeong, "Highly Linear Predistortion Power Amplifiers With Phase-Controlled Error Generator", *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 12, pp. 690-692, December 2006.

[6] S. Boumaiza, J. Li, M. Jaidane-Saidane, and F.M. Ghannouchi, "Adaptive Digital/RF Predistortion Using a Nonuniform LUT Indexing Function With Built-In Dependence on the Amplifier Nonlinearity", *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 12, pp. 2670-2677, December 2004.

[7] P. B. Kenington, S. J. Gillard, and A. E. New, "An Ultra-Broadband Power Amplifier using Dynamically-Controlled Linearisation", *IEEE MTT-S International Microwave Symposium Digest*, Anaheim, pp. 355–358, 13-19 June 1999.

[8] Y.-S. Lee, M.-W. Lee, S.-H. Kam, and Y.-H. Jeong, "A High-Linearity Wideband Power Amplifier With Cascaded Third-Order Analog Predistorters", *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 2, pp. 112–114, February 2010.

[9] E. Cohen, S. Ravid, and D. Ritter, "60 GHz 45nm PA for linear OFDM signal with predistortion correction achieving 6.1% PAE and −28dB EVM", *Radio Frequency Integrated Circuits Symposium*, Boston, pp. 35-38, 7-9 June 2009.

[10] J.-H. Tsai, C.-H. Wu, H.-Y. Yang, and T.-W. Huang, "A 60 GHz CMOS Power Amplifier With Built-in Pre-Distortion Linearizer", *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 12, pp. 676-678, December 2011.

[11] Y.-Y. Huang, W. Woo, H. Jeon, C.-H. Lee, and J. S. Kenney, "Compact Wideband Linear CMOS Variable Gain Amplifier for Analog-Predistortion Power Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 1, pp. 68-76, January 2012.

[12] J. Valliarampath and S. Sinha, "Linearity Improvement Analysis for PAs at mm-Wave Frequencies", *Microwave and Optical Technology Letters*, vol. 56, no. 3, pp. 743-748, March 2014.

[13] Y. Jin, M. A. T. Sanduleanu, and J. R. Long, "A Wideband Millimeter-Wave Power Amplifier With 20 dB Linear Power Gain and +8 dBm Maximum Saturated Output Power", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1553-1562, July 2008.

[14] J.Y.-C. Liu, R. Berenguer, and M.-C. F. Chang, "Millimeter-Wave Self-Healing Power Amplifier With Adaptive Amplitude and Phase Linearization in 65-nm CMOS", *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 5, pp. 1342-1352, May 2012.

[15] V.-H. Do, V. Subramanian, W. Keusgen, and G. Boeck, "A 60 GHz SiGe-HBT Power Amplifier With 20% PAE at 15 dBm Output Power", *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 3, pp. 209-211, March 2008.

[16] S.-K. Yong, P. Xia, and A. V. Garcia, *60 GHz Technology for Gbps WLAN and WPAN: From Theory to Practice*, John Wiley & Sons Ltd, Chichester, West Sussex, 2011.

[17] P. Colantonio, F. Giannini, and E. Limiti, *High Efficiency RF And Microwave Solid State Power Amplifiers*, Wiley, Chippenham, Wiltshire, 2009.

[18] J. S. Love, *RF Frontend: World Class Designs*, Elsevier, Burlington, MA, 2009.

[19] U. R. Pfeiffer and D. Goren, "A 20 dBm Fully-Integrated 60 GHz SiGe Power Amplifier With Automatic Level Control", *IEEE Journal of Solid-State Circuits*, vol. 42, no. 7, pp. 1455-1463, July 2007.

[20] H. Jeon, Y. Park, Y.-Y. Huang, J. Kim, K.-S. Lee, C.-H. Lee, and J. S. Kenney, "A Triple-Mode Balanced Linear CMOS Power Amplifier Using a Switched-Quadrature Coupler", *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2019-2032, September 2012.

[21] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*, Artech House, Norwood, MA, 2003.

[22] A. M. Niknejad and H. Hashemi, *mm-Wave Silicon Technology 60 GHz and Beyond*, Springer Science+Business Media, New York, NY, 2008.

[23] A. Siligaris, O. Richard, B. Martineau, C. Mounet, F. Chaix, R. Ferragut, C. Dehos, J. Lanteri, L. Dussopt, S. D. Yamamoto, R. Pilard, P. Busson, A. Cathelin, D. Belot, and P. Vincent, "A 65-nm CMOS Fully Integrated Transceiver Module for 60-GHz Wireless HD Applications", *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 3005-3017, December 2011.

[24] J. P. Aikio and T. Rahkonen, "A Comprehensive Analysis of AM–AM and AM–PM Conversion in an LDMOS RF Power Amplifier", *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 2, pp. 262-270, February 2009.

[25] Y. Park, C.-H. Lee, J. D. Cressler, and J. Laskar, "The Analysis of UWB SiGe HBT LNA for Its Noise, Linearity, and Minimum Group Delay Variation", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 4, pp. 1687-1697, April 2006.

[26] J. B. Johnson, A. J. Joseph, D. C. Sheridan, R. M. Maladi, P.-O. Brandt, J. Persson, J. Andersson, A. Bjorneklett, U. Persson, F. Abasi, and L. Tilly, "Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications", *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1605-1614, October 2004.

[27] P. Ashburn, *SiGe Heterojunction Bipolar Transistors*, John Wiley & Sons Ltd, Chichester, West Sussex, 2003.

[28] K. Nellis and P. Zampardi, "A Comparison of Linear Handset Power Amplifiers in Different Bipolar Technologies", *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1746-1754, October 2004.

[29] G. Avenier, M. Diop, P. Chevalier, G. Troillard, N. Loubet, J. Bouvier, L. Depoyan, N. Derrier, M. Buczko, C. Leyris, S. Boret, S. Montusclat, A. Margain, S. Pruvost, S. T. Nicolson, K. H. K. Yau, N. Revil, D. Gloria, D. Dutartre, S.P. Voinigescu, and A. Chantre, "0.13 μm SiGe BiCMOS Technology Fully Dedicated to mm-Wave Applications", *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2312-2321, September 2009.

[30] D. L. Harame, D. C. Ahlgren, D. D. Coolbaugh, J. S. Dunn, G. G. Freeman, J. D. Gillis, R. A. Groves, G. N. Hendersen, R. A. Johnson, A. J. Joseph, S. Subbanna, A. M. Victor, K. M. Watson, C. S. Webster, and P. J. Zampardi, "Current Status and Future Trends of SiGe BiCMOS Technology", *IEEE Transaction on Electron Devices*, vol. 48, no. 11, pp. 2575-2594, November 2001.

[31] P. Sakalas, M. Ramonas, M. Schröter, C. Jungemann, A. Shimukovitch, and W. Kraus, "Impact Ionization Noise in SiGe HBTs: Comparison of Device and Compact Modeling with Experimental Results", *IEEE Transaction on Electron Devices*, vol. 56, no. 2, pp. 328-336, February 2009.

[32] H. Veenstra, G. A. M. Hurkx, D. van Goor, H. Brekelmans, and J. R. Long, "Analyses and Design of Bias Circuits Tolerating Output Voltages above BV_{CEO}", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 10, pp. 2008-2018, October 2005.

[33] A. Komijani and A. Hajimiri, "A Wideband 77-GHz, 17.5-dBm Fully Integrated Power Amplifier in Silicon", *IEEE Journal Solid-State Circuits*, vol. 41, no. 8, pp. 1749-1756, August 2006.

[34] Y. S. Noh, M. S. Uhm, and I. B. Yom, "A Compact Ku-Band SiGe Power Amplifier MMIC With On-Chip Active Biasing", *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 6, pp. 349-351, June 2010.

[35] U. R. Pfeiffer and A. Valdes-Garcia, "Millimeter-Wave Design Considerations for Power Amplifiers in an SiGe Process Technology", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 57-64, January 2006.

[36] A. Raghavan, N. Srirattana, and J. Laskar, *Modeling and Design Techniques for RF Power Amplifiers*, John Wiley & Sons, Hoboken, New Jersey, 2008.

[37] T. S. D. Cheung and J. R. Long, "Shielded Passive Devices for Silicon-Based Monolithic Microwave and Millimeter-Wave Integrated Circuits", *IEEE Journal Solid-State Circuits*, vol. 41, no. 5, pp. 1183-1200, May 2006.

[38] B. Gaucher, B. Floyd, S. Reynolds, U. Pfeiffer, J. Grzyb, A. Joseph, E. Mina, B. Orner, H. Ding, R. Wachnik, and K. Walter, "Silicon germanium based millimetre-wave ICs for Gbps wireless communications and radar systems", *Semiconductor Science and Technology*, vol. 22, no. 1, pp. 236-243, December 2006.

[39] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe Bipolar Transceiver Circuits Operating at 60 GHz", *IEEE Journal Solid-State Circuits*, vol. 40, no. 1, pp. 156-167, January 2005.

[40] U. R. Pfeiffer and D. Gordon, "A 23-dBm 60-GHz Distributed Active Transformer in a Silicon Process Technology", *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 5, pp. 857-865, May 2007.

[41] J. Vuolevi and T. Rahkonen, *Distortion in RF Power Amplifiers*, Artech House, Norwood, MA, 2003.

[42] S. Boumaiza and F. M. Ghannouchi, "Thermal Memory Effects Modeling and Compensation in RF Power Amplifiers and Predistortion Linearizers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 12, pp. 2427-2433, December 2003.

[43] P. B. Kenington, *High-linearity RF Amplifier Design*, Artech House, Norwood, MA 2000.

[44] H. Ishihara, M. Hosoya, S. Otaka, and O. Watanabe, "A 10-MHz Signal Bandwidth Cartesian Loop Transmitter Capable of Off-Chip PA Linearization", *IEEE Journal Solid-State Circuits*, vol. 45, no. 12, pp. 2785-2793, December 2010.

[45] H. H. Boo, S.W. Chung, and J. L. Dawson, "Digitally Assisted Feedforward Compensation of Cartesian-Feedback Power-Amplifier Systems", *IEEE Transactions on Circuits and Systems*, vol. 58, no. 8, pp. 457-461, August 2011.

[46] A. S. H. Ghadam, S. Burglechner, A. H. Gokceoglu, M. Valkama, and A. Springer, "Implementation and Performance of DSP-Oriented Feedforward Power Amplifier

Linearizer", *IEEE Transactions on Circuits and Systems*, vol. 59, no. 2, pp. 409-425, February 2012.

[47] M. Helaoui and F. M. Ghannouchi, "Linearization of Power Amplifiers Using the Reverse MM-LINC Technique", *IEEE Transactions on Circuits and Systems*, vol. 57, no. 1, pp. 6-10, January 2010.

[48] M. Vasić, O. Garcia, J. A. Oliver, P. Alou, D. Diaz, J. A. Cobos, A. Gimeno, J. M. Pardo, C. Benavente, and F. J. Ortega, "Efficient and Linear Power Amplifier Based on Envelope Elimination and Restoration", *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 5-9, January 2012.

[49] K. J. Muhonen, M. Kavehrad, and R. Krishnamoorthy, "Look-up table techniques for adaptive digital predistortion: a development and comparison", *IEEE Transactions on Vehicular Technology*, vol. 49, no. 5,pp. 1995-2002, September 2000.

[50] H.-C. Park, S.-C. Jung, K.-H. Lim, M.-S. Kim, H. Kim, C.-S. Park, and Y. Yang, "Analysis and Design of Compact Third-Order Intermodulation Generation Circuits", *Microwave and Optical Technology Letters*, vol. 51, no. 9, pp. 2137-2140, September 2009.

[51] Y.-S. Lee, M.-W. Lee, and Y.-H. Jeong, "A Wideband Analog Predistortion Power Amplifier With Multi-Branch Nonlinear Path for Memory-Effect Compensation", *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 7, pp. 476-478, July 2009.

[52] P. Jardin and G. Baudoin, "Filter Lookup Table Method for Power Amplifier Linearization", *IEEE Transactions on Vehicular Technology*, vol. 56, no. 3, pp. 1076-1087, May 2007.

[53] Y. Y. Woo, J. Kim, J. Yi, S. Hong, I. Kim, J. Moon, and B. Kim, "Adaptive Digital Feedback Predistortion Technique for Linearizing Power Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 5, pp. 932-940, May 2007.

[54] C. D. Presti, D. F. Kimball, and P. M. Asbeck, "Closed-Loop Digital Predistortion System With Fast Real-Time Adaptation Applied to a Handset WCDMA PA Module", *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 3, pp. 604-618, March 2012.

[55] IBM Microelectronics Division, "Electrical Parameters and Models", in *BiCMOS-8HP Design Manual Reference Guide*, 2007.

[56] M. P. van der Heijden, H. C. de Graaff, and L. C. N. de Vreede, "A Novel Frequency-Independent Third-Order Intermodulation Distortion Cancellation Technique for BJT Amplifiers", *IEEE Journal Solid-State Circuits*, vol. 37, no. 9, pp. 1176-1183, September 2002.

[57] K. L. Fong and R. G. Meyer, "High-Frequency Nonlinearity Analysis of Common-Emitter and Differential-Pair Transconductance Stages", *IEEE Journal Solid-State Circuits*, vol. 33, no. 4, pp. 548-555, April 1998.

[58] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*, Prentice Hall, Upper Saddle River, NJ, 1997.

[59] J. Jang, E. C. Kan, T. Arnborg, T. Johansson, and R. W. Dutton, "Characterization of RF Power BJT and Improvement of Thermal Stability with Nonlinear Base Ballasting", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 9, pp. 1428-1432, September 1998.

APPENDIX A: CIRCUIT LAYOUTS

The layout of each of the subsystems is illustrated in this appendix. The subsystems shown from Figures A1 to A7 include the:

- three-stage CE PA,
- power detector,
- ADC,
- control logic consisting of XOR gate and inverter, and
- DAC.

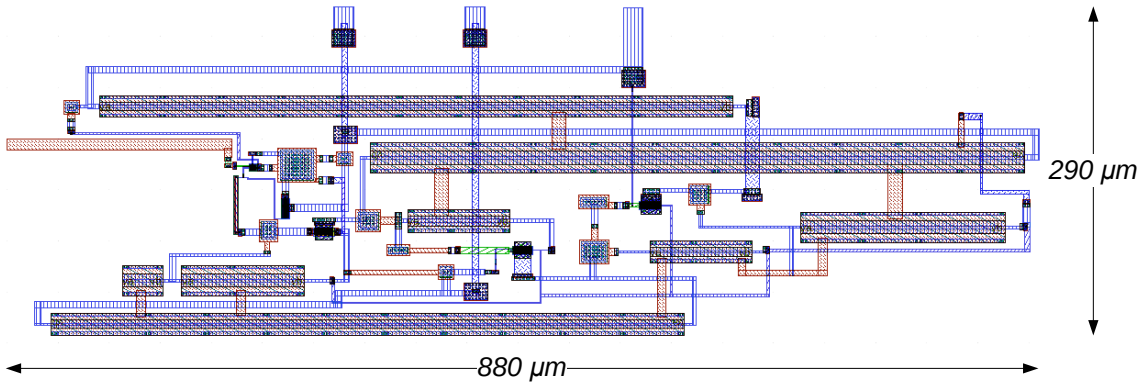


Figure A1. The three-stage PA including RFCs.

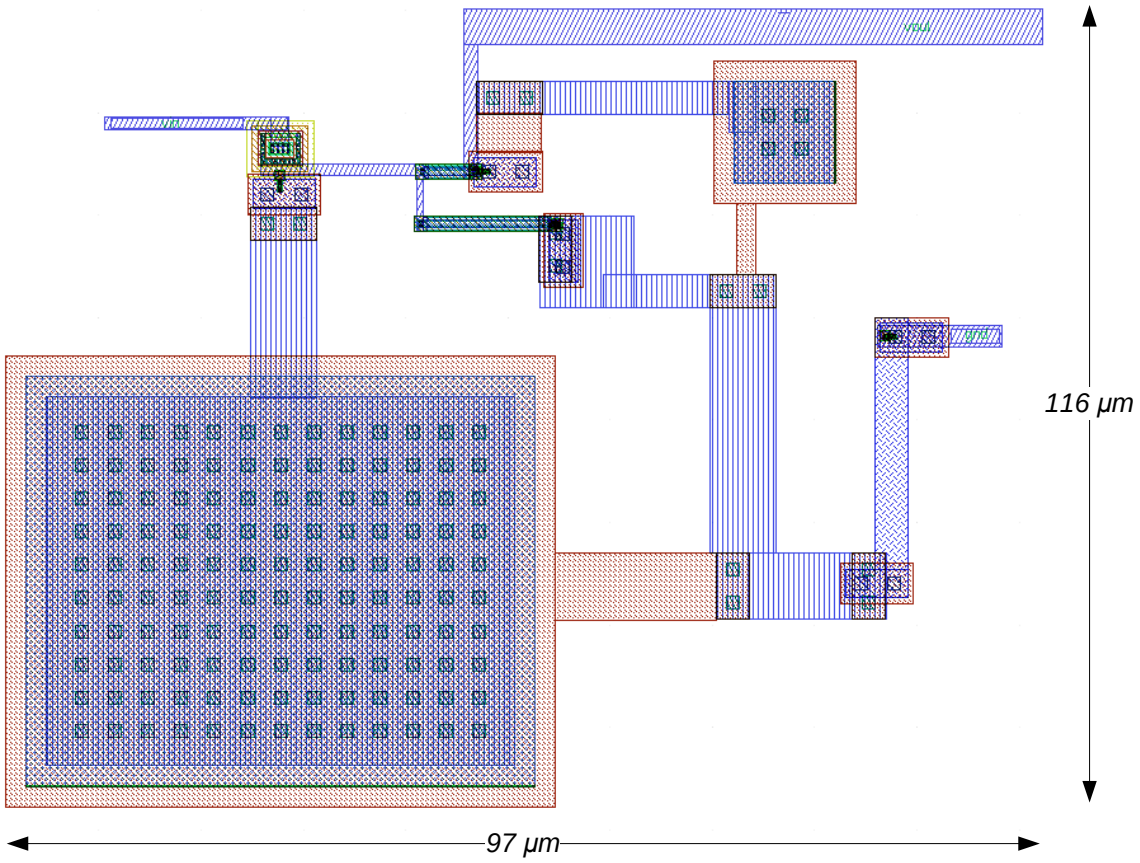


Figure A2. The power detector layout.

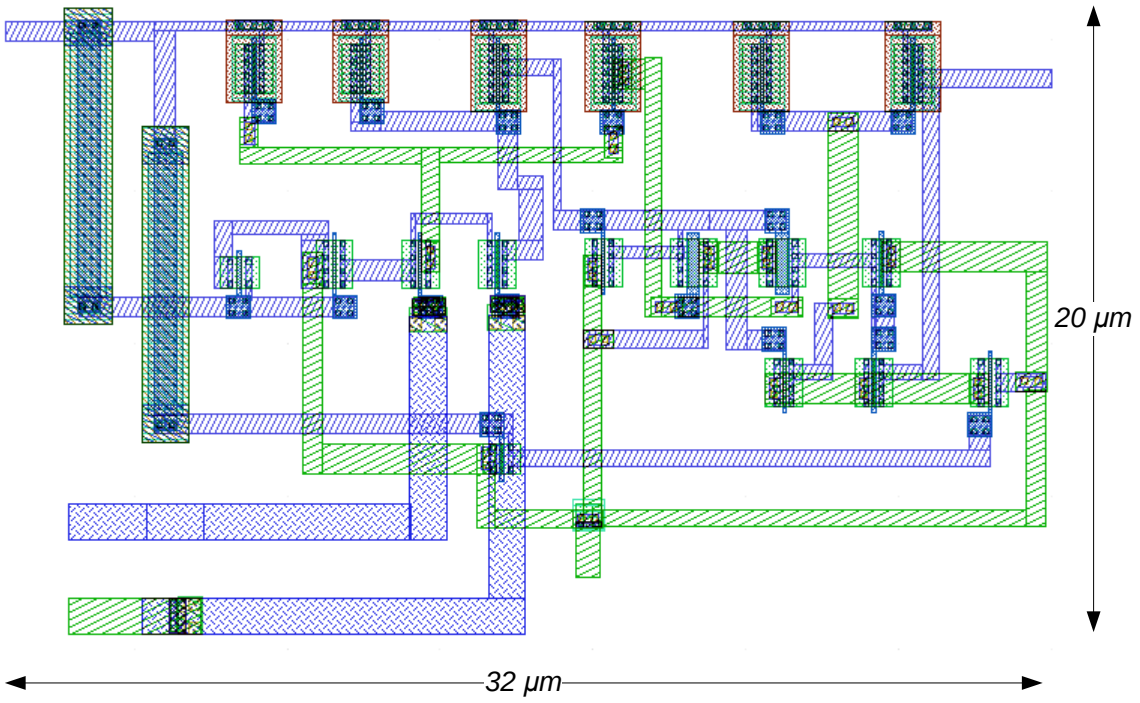


Figure A3. The comparator layout using NFETs and PFETs.

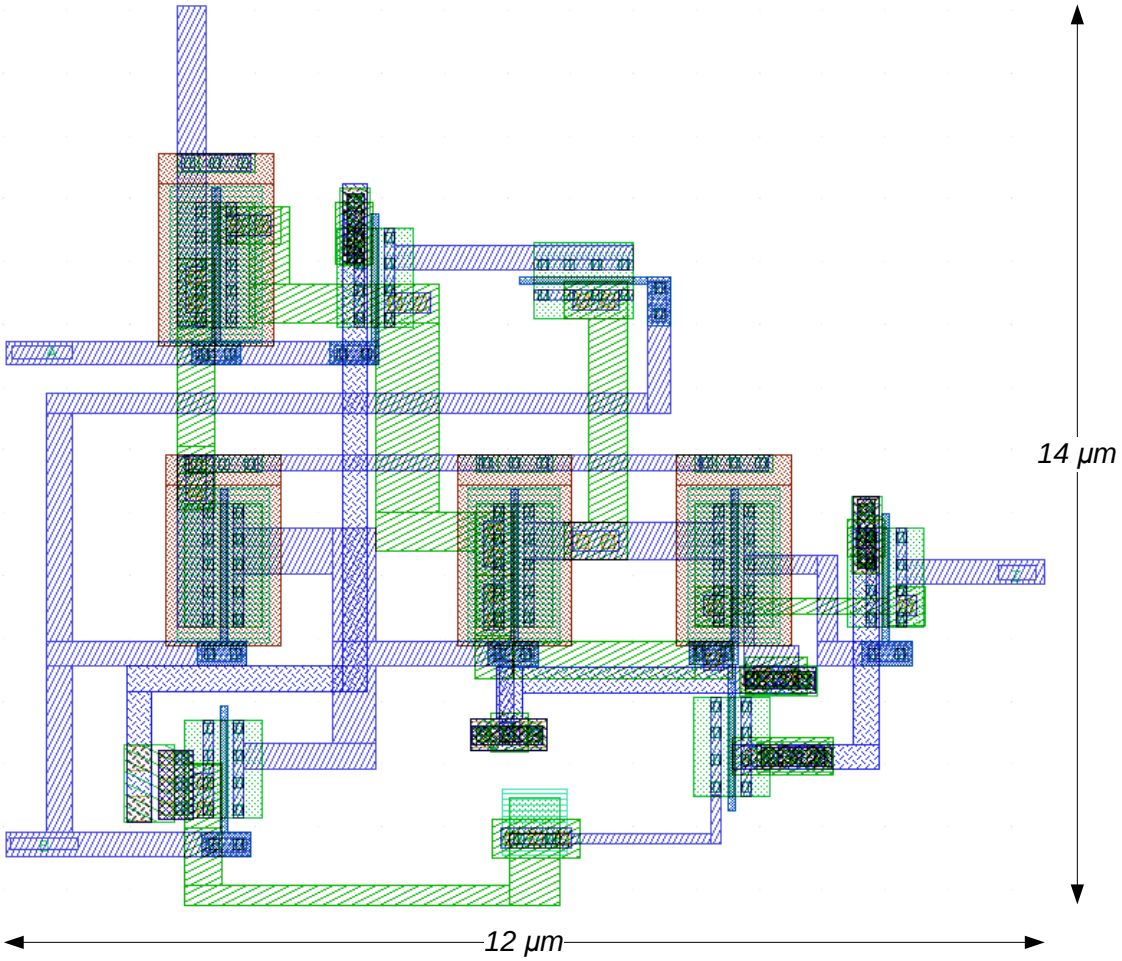


Figure A4. The XOR gate layout (part of the control logic circuit).

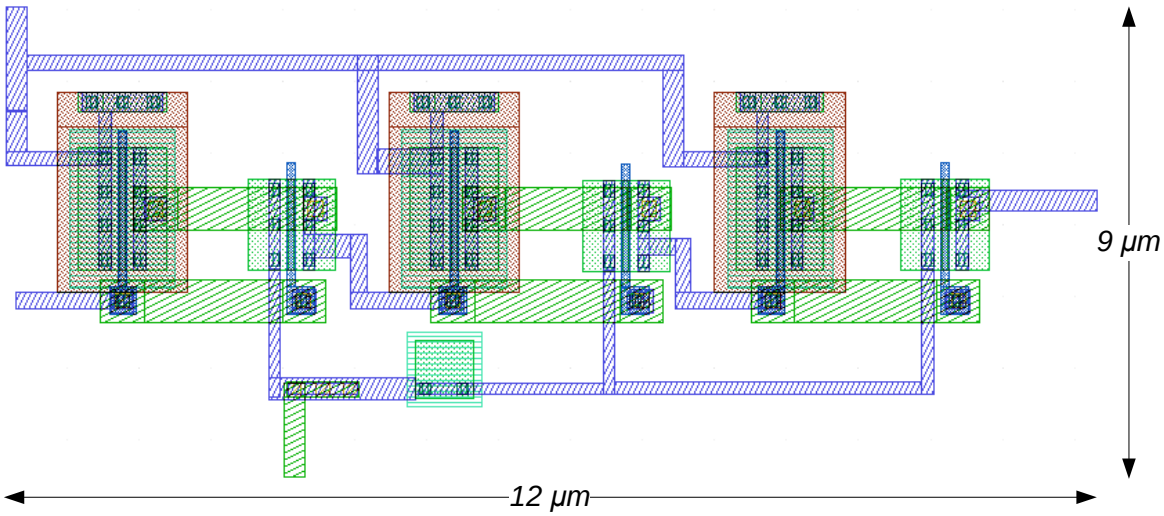


Figure A5. The inverter layout (final subsection of the control logic circuit).

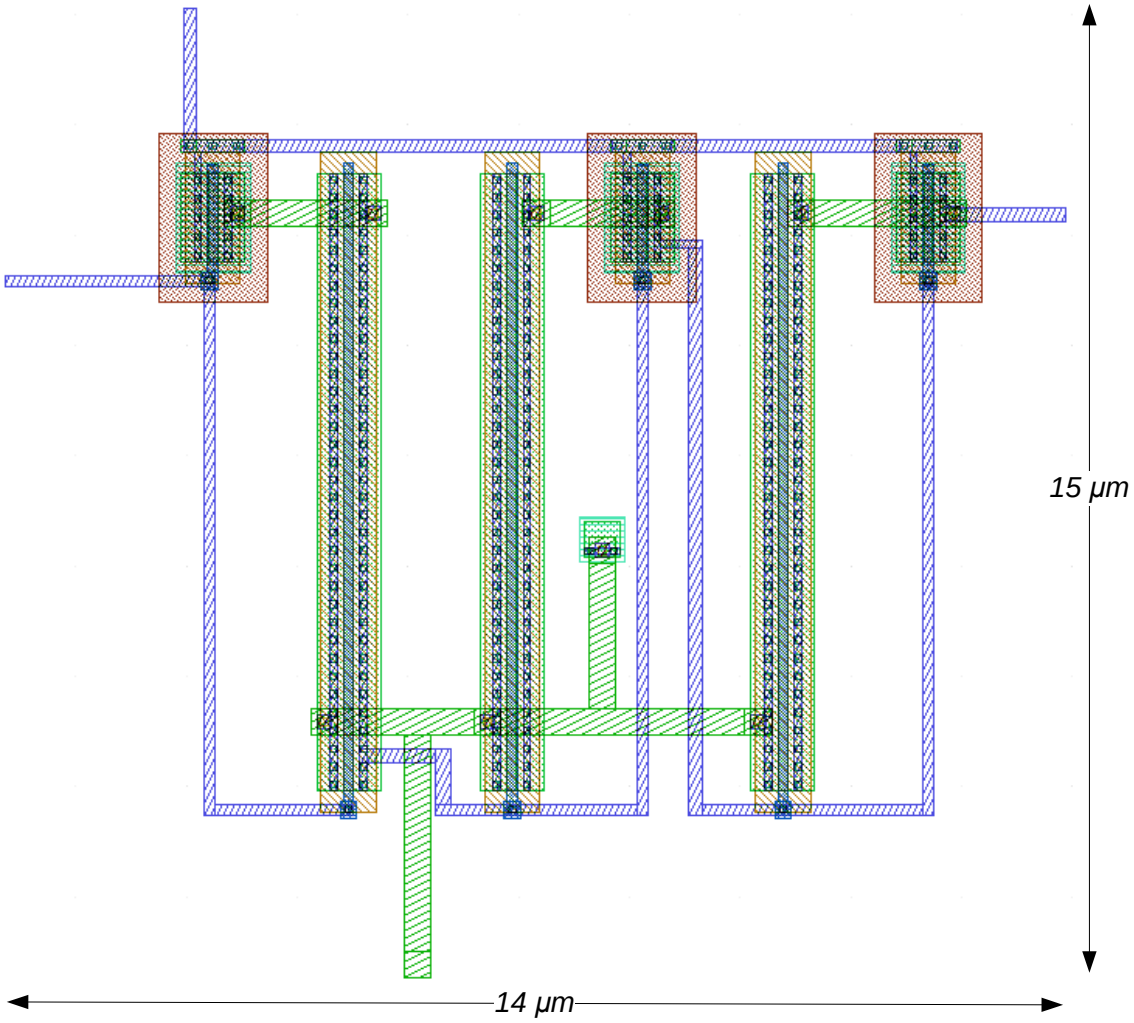


Figure A6. The inverter layout (input subsection of the DAC circuit).

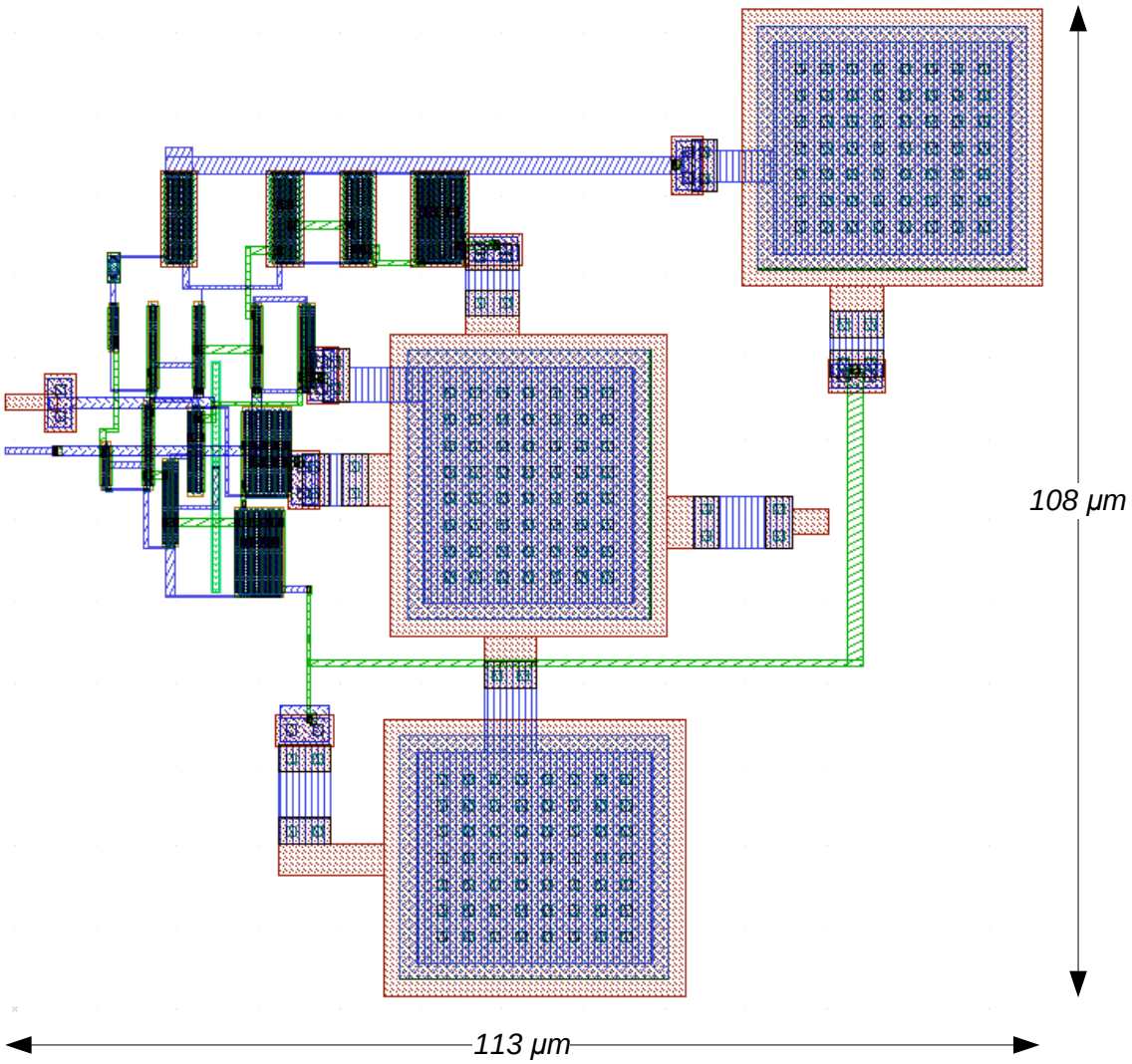


Figure A7. The DAC including the voltage buffer.