Nom du programme

Guide D'étude

(à lire avant de commencer le cours)

Techniques de conversions Numérique/Analogique et Analogique/Numérique

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Guide d'étude

Introduction

Ce module porte sur la chaîne d'acquisition et de restitution d'un signal analogique et mise en place d'une chaîne de mesure complète (carte CAN/CNA). Il couvre plus

spécifiquement les techniques des Conversions Numérique Analogique (CNA) et Analogique Numérique (CAN) On se concentre sur la nature des signaux électroniques Analogique et Numérique. On présente quelques principes de conversion numérique / analogique ainsi que les caractéristiques typiques liées à des réalisations pratiques. On passe en revue les principaux types de convertisseurs, en discutant leurs performances. Enfin annonce le théorème d'échantillonnage de Shannon. Ce dernier permet de cerner une limitation physique à la rapidité d'échantillonnage des signaux analogiques et le temps de conversions.

Le module s'adresse d'abord aux personnes souhaitent avoir des connaissances des bases sur les éléments d'une chaîne d'acquisition et de restitution des données… Il s'inscrit dans le programme du diplôme technicien supérieur en génie électrique, télécommunications et informatique (ISET) et du diplôme d'ingénieur en génie électrique, télécommunications et informatique L'étudiant ou l'étudiante devrait avoir une connaissance de base en électronique et circuits logiques. Il a comme préalable les module (s): Cours Electronique générale (théorèmes généraux, amplificateurs opérationnels) et Electronique numérique (Logique combinatoire et séquentielle).

Ce « Guide d'étude » a pour objectif de vous préparer à suivre le cours. Il définit en quelque sorte un mode d'emploi, non seulement pour le matériel didactique du cours, mais aussi pour le cheminement que vous devez adopter et les différentes exigences auxquelles vous devez répondre.

Bonne lecture et bon cours!

Pré-requis :

Cours Electronique générale (théorèmes généraux, amplificateurs opérationnels) et Electronique numérique (Logique combinatoire et séquentielle)

But et objectifs du cours

Le but de ce module est de se familiariser avec les éléments de bases d'unechaîne d'acquisition et de restitution des données et plus particulièrement les différents types

des CNA et CAN. Plus spécifiquement, au terme de ce module, l'étudiant ou l'étudiante sera en mesure :

- Acquérir les connaissances de bases pour la mise en œuvre d'une chaîne d'acquisition et restitution de données (aspects technologiques).
- Etudier les différents types des CNA et CAN
- Analyser le temps de la conversion analogique / numérique peut être plus ou moins important ; c'est donc un élément essentiel dans le choix du convertisseur
- De donner un avis professionnel sur le choix des convertisseurs
- Donner les outils mathématiques à

Contenu du cours

Tableau 1 : Le contenu du module se compose de 3 chapitres subdivisés en 13 leçons.

Chapitre	Leçon	Résumé
1	**1**	CHAÎNE D'ACQUISITION DE DONNEES
		CONVERTISSEUR NUMÉRIQUE/ANALOGIQUE. 1. Généralités sur le codage 2. Principe de fonctionnement.

2	**2**	3. Courbe de transfert d'un CNA 4. Définition des CNA unipolaire et bipolaire
2	**3**	CONVERTISSEUR NUMÉRIQUE/ANALOGIQUE. 5. Classification des CNA 6. CNA à réseau des résistances pondérées 7. CNAà courants pondérés
2	**4**	CONVERTISSEUR NUMÉRIQUE/ANALOGIQUE. 8. CNA à réseau R/2R. • Principe • Calcul de la tension de sortie Vs • Précision. • Exemple de réalisation • Avantages / inconvénients.
2	**5**	CONVERTISSEUR NUMÉRIQUE/ANALOGIQUE. 9. CNA à réseau R/2R à échelle inversée • Principe • Calcul de la tension de sortie Vs • Précision. • Exemple de réalisation 10. Montage pratique CNA unipolaire et CNA bipolaire

2	6	CONVERTISSEUR NUMÉRIQUE/ANALOGIQUE. 11. Les CNA indirects séquentiels • Convertisseur Numérique à rapport cyclique • Convertisseur à multiplication discre
2	7	CONVERTISSEUR NUMÉRIQUE/ANALOGIQUE. 12. Les paramètres des CNAs : • Paramètres de conversion • Paramètres dus aux erreurs introduites par les • Grandeurs d'influence
2	8	CONVERTISSEUR NUMÉRIQUE/ANALOGIQUE. 12. Utilisation des CNAs • Utilisation " classique " • Amplificateurs à gain programmable. • Multiplieur. • Générateur de fonctions analogiques

3	**9**	CONVERTISSEUR ANALOGIQUE/NUMÉRIQUE 1. Principe de fonctionnement. • Définitions. • Plage de conversion. • Résolution. • Dynamique. • Mise en relation. • Exemple : CAN 4 bits • Erreur de quantification. Amélioration.
3	**10**	CONVERTISSEUR ANALOGIQUE/NUMÉRIQUE 2. CAN parallèle • Principe. • Précision. • Utilisation
3	**11**	CONVERTISSEUR ANALOGIQUE/NUMÉRIQUE 3. CAN à comptage d'impulsions • Convertisseur simple rampe. • Convertisseur double rampe. • Résolution. Précision.

3	**12**	CONVERTISSEUR ANALOGIQUE/NUMÉRIQUE 4. CAN à approximation successives • Principe. • Exemple • Précision. • Utilisation 5. Simulation CAN à approximation successives
3	**13**	CONVERSION ANALOGIQUE/NUMÉRIQUE 6. Les paramètres des CNA • Paramètres de conversion • Paramètres dus aux erreurs introduites par les système • Grandeurs d'influence 7. Exemples d'utilisation des CNA • Utilisation " classique " • Filtres programmables

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Approche pédagogique

Ce cours… est conçu selon une approche pédagogique propre à la formation à distance. Le matériel didactique et la formule utilisée vous permettent d'adopter une démarche d'apprentissage autonome. Vous pouvez ainsi gérer votre temps d'étude et prendre en charge votre formation.

Toutefois, cette prise en charge est soutenue par la personne responsable de l'encadrement (le tuteur ou la tutrice), pendant toute le semestre. Sa tâche est de vous faciliter les conditions d'apprentissage et de vous aider dans votre démarche, de façon à ce que vous atteigniez les objectifs du cours. Il va de soi que le tuteur ou la tutrice ne donne pas les réponses des activités notées.Vous pouvez communiquer avec votre tuteur ou votre tutrice par le courrier électronique offert sur le site du cours ou en posant vos questions sur le forum. Votre tuteur ou votre tutrice y répondra à l'intérieur de 48 heures.

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Charge de travail et calendrier

Ce module est offert à distance sur un semestre de 13 semaines. Le volume de travail exigé pour l'étude du module et la réalisation des évaluations est de …[xx].. heures par semestre. En moyenne, la charge de travail hebdomadaire est donc d'environ 2 heures. Certains leçons [ou sections ou…] sont un peu plus longs à lire que d'autres, mais ils exigent moins de travail sous forme d'exercices. Un calendrier pédagogique détaillé est proposé au Tableau 3.

Tableau 3: Calendrier pédagogique

Semaine	Module	Tâche	Envoi de l'évaluation
1	1	· Lecture du guide pédagogique · Lecture de la leçon 1 · Auto-évaluation	
2	1	· Lecture de la leçon 2 · Auto-évaluation	
3	1	· Lecture de la leçon 3 · Auto-évaluation	
4	1	· Lecture de la leçon 4 · Auto-évaluation	Travail 1 : date
5	2	· Lecture de la leçon 5 · Auto-évaluation	

6	2	· Lecture de la leçon 6 · Auto-évaluation	
7	2	· Lecture de la leçon 7 · Auto-évaluation	
8	2	· Lecture de la leçon 8 · Auto-évaluation	Travail 2 : date
9	3	· Lecture de la leçon 9 · Auto-évaluation	
10	3	· Lecture de la leçon 10 · Auto-évaluation	
11	3	· Lecture de la leçon 11 · Auto-évaluation	
12	3	· Lecture de la leçon 12 · Auto-évaluation	

13	3	· Lecture de la leçon 13 · Auto-évaluation	
14	1-2-3	· Révision	
15		· Examen final sous surveillance	Date de l’examen

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Évaluation des apprentissages

L'auto-évaluation

Cette évaluation n'est pas notée. Elle est présentée sous forme d’activités d’intégration, de questions à répondre ou d'exercices à effectuer. Cette auto-évaluation met l'accent sur les points les plus importants de la matière. Le corrigé des exercices est disponible, mais nous vous suggérons de ne le consulter qu’après avoir complété les exercices. Ces derniers vous préparent aux évaluations notées.

Les travaux notés

Ces travaux visent à vérifier l'acquisition de vos connaissances et votre compétence à appliquer et à transférer les notions étudiées à des situations concrètes. Le français utilisé dans vos travaux d'évaluation doit être correct. Un travail illisible, jugé irrecevable par votre professeur, vous sera retourné pour être refait. Vous devez obligatoirement réaliser et retourner *aux dates prévues* (voir la fiche calendrier) les travaux notés et passer l'examen final sous surveillance.

Examen sous surveillance

L'examen final sous surveillance porte sur toute la matière du cours et sera constitué de [Expliquez ici le type d'examen : questions objectives, à développement, études de cas, problèmes, etc.]. L'utilisation des notes de cours et de la calculatrice sera autorisée [ou non, selon le cas].

L'ensemble des évaluations notées compte pour 100 % de la note du cours. En voici, à titre d'exemple, un partage :

Évaluation notée	Pondération	Seuil de passage
Travail 1	X_1 %	
Travail 2	X_2 %	
Examen final	40 %	50 %
Total	100 %	60 %

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OBJECTIF

Les Convertisseurs Numériques - Analogiques & Les Convertisseurs Analogiques - Numériques

OBJECTIF

Structure fonctionnelle d'une chaîne de mesure

1. Introduction

1.1 Introduction

Si nous souhaitons mesurer à l'aide d'un ordinateur la température d'un four entre T_{min} et T_{max}, on réalise le schéma d'acquisition des données figure1. Les capteurs fournissent à l'interface un signal électrique reproduisant la grandeur à mesurer. Ce signal est dit analogique, et est le plus souvent proportionnel à la mesure.

Un boîtier intermédiaire entre le capteur et l'interface est parfois nécessaire pour linéariser le signal, c'est à dire le rendre proportionnel à la grandeur mesurée, ou pour l'amplifier. Le signal analogique évolue de façon continue dans le temps.

L'interface mesure périodiquement le signal électrique analogique venant du capteur ou de son adaptateur et le traduit en une valeur numérique (à codage binaire) utilisable par l'unité centrale de l'ordinateur. Ces mesures constituent un échantillonnage du signal analogique.

L'ordinateur, correctement programmé par le logiciel approprié, traite les nombres fournis par l'interface pour en tirer des représentations graphiques ou des tableaux. Le logiciel peut aussi calculer certaines valeurs à partir de celles recueillies par le ou les capteurs.

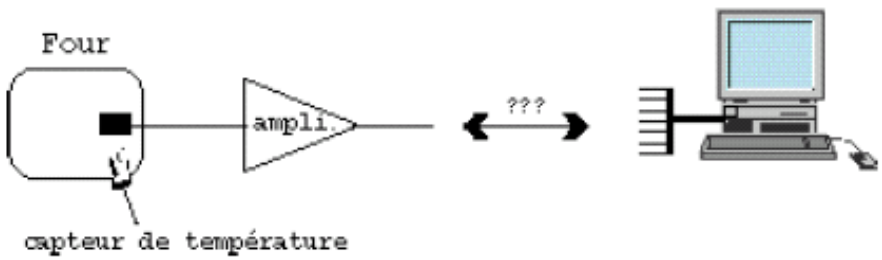

Figure1 : schéma d'une régulation numérique en boucle ouverte

Le capteur de température fournit une tension proportionnelle à température T variant de 0 à 10mV. On amplifie ce signal pour l'amener dans une plage de variation de tension facilement mesurable par exemple de 0 à 10V. Puis une opération de numérisation est nécessaire pour fournir à l'ordinateur des données proportionnelles à la tension analogique issues de capteurs température.

Dans cette boucle de régulation numérique, on rencontre deux types des signaux. Qui sont le signal analogique issue du capteur et les signaux numériques ou les signaux digitaux qui attaquent l'ordinateur. De façon générale les signaux analogiques et les signaux numériques sont caractérises par :

Un signal Analogique: la grandeur électrique ou le signal varie de façon **analogue** à la grandeur physique qu'elle décrit. Une caractéristique importante est la continuité temporelle du signal. Sur une intervalle de temps donnée (qui représente la duré de l'observation du signal durée de la mesure), le signal peut avoir une infinité de valeurs différentes. Par exemple tous les signaux issus des capteurs sont analogiques, et traduisent des phénomènes physiques qui varient continûment.

Un signal Numérique **:** où le signal prend uniquement deux états, un état haut et un état bas. La grandeur électrique est traduite en une suite de **nombres binaires**

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Un signal Numérique **:** où le signal prend uniquement deux états, un état haut et un état bas. La grandeur électrique est traduite en une suite de **nombres binaires**

Le passage d'un type de donnée à l'autre se fera par des convertisseurs, composants " mixtes " qui vont manipuler des tensions analogiques en entrée et des signaux logiques en sortie ou vice versa.

L'avantage de numérisation ; opération de transformation des signaux analogiques en signaux numériques (données) ; est la possibilité de stockage, de transformation et de restitution des données sans qu'elles ne soient altérées. Cette opération est maintenant prédominant grâce aux progrès faits par les microprocesseurs et les microordinateurs.

En générale le processus de numérisation des signaux se décompose en trois étapes :

- l'échantillonnage : passage d'un espace de temps continu à un espace de temps discret,
- la quantification : passage d'un espace de valeurs continu à un espace de valeurs discret,
- le codage : chaque niveau quantifié de valeurs est codé sur un nombre déterminé de bits.

1- Structure fonctionnelle d'une chaîne de mesure

2. Rôle des modules de la chaîne

1.2 Chaîne d'acquisition des données

Généralement, la chaîne permettant l'acquisition et les traitements des données est couramment appelée chaîne d'acquisition des données. Cette la chaîne d'acquisition (figure 2) est essentiellement bâtie autour de trois modules qui sont:

- Module d'acquisition des données (analogique)
- Module de conversion Analogique Numérique CAN.
- Module de traitement des données et de commandes : calculateur.

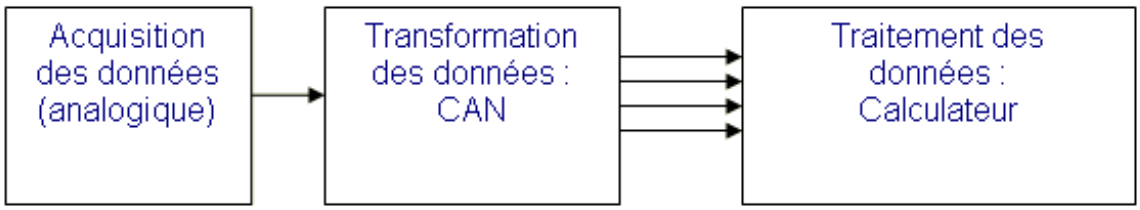


Figure 2: la chaîne d'acquisition des données

1-Le Module d'acquisition des données

Ce module est essentiellement composé de quatre composants qui sont : le capteur, le conditionneur et l'amplificateur, le filtre d'entrée et l' échantillonneur-bloqueur figure 4.

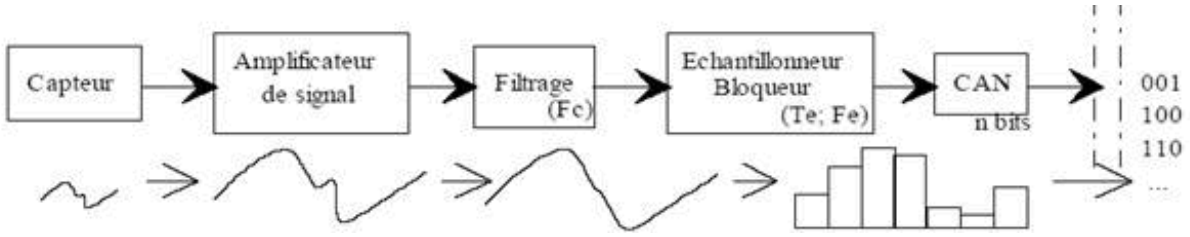


figure 4: Module d'acquisition des données

1-Le capteur:

Le capteur est le premier élément d'une chaîne de mesure ou chaîne d'acquisition de données. Il est l'interface entre le "monde physique" et le "monde électrique". En effet le capteur est un organe de prélèvement d'information qui élabore à partir d'une grandeur physique, une autre grandeur physique de nature différente (très souvent électrique). Cette grandeur représentative de la grandeur prélevée est utilisable à des fins de mesure ou de commande. Sur le tableau 1 nous illustrons la nature de la grandeur physique à mesurer l'effet utilisé ainsi que la nature de la grandeur de sortie.

Grandeur physique à mesurer	Effet utilisé	Grandeur de sortie
Température	Thermoélectricité	Tension
	Pyroélectricité	Charge
Flux de rayonnement optique	Photo-émission	Courant
	Effet photovoltaïque	Tension
	Effet photo-électrique	Tension
Force	Piézo-électricité	Charge
Pression		
Accélération	Induction électromagnétique	Tension
Vitesse		
Position (Aimant)	Effet Hall	Tension
Courant		

le tableau 1

2-Le conditionneur:

Le signal issu du capteur doit être conditionné avant sa conversion. En fait le signal analogique de sortie du capteur est très rarement dans la plage de tension d'entrée du convertisseur. Il faut donc mettre en forme le

signal de sortie du capteur à l'aide d'un conditionneur pour que la tension de sortie soit dans une gamme de tension compatible avec celle du convertisseur CAN standard (par exemple 0-5V) Le conditionnement peut être simplement une amplification à l'aide d'un amplificateur opérationnel, ou plus compliqué par exemple une amplification et un décalage, voire un changement de signe ou tout autre en fonction du signal de sortie du capteur. Le conditionneur doit avoir comme qualité essentielle de dégrader le moins possible le signal d'origine tout en lui faisant subir les opérations nécessaires au conditionnement .Les **conditionneur**, **amplificateur** adaptent et amplifient le signal pour l'amener dans une plage de variation de tension "confortable" par exemple de 0 à 5V.

3- Le filtre d'entrée:

Ce filtre est communément appelé **filtre anti-repliement**. Son rôle est de limiter le contenu spectral du signal aux fréquences qui nous intéressent. Ainsi il élimine les parasites. C'est un filtre passe bas que l'on caractérise par sa fréquence de coupure et son ordre.

4-L'**échantillonneur-bloqueur**

l'échantillonneur a pour rôle de "prélever" périodiquement un échantillon du signal électrique amplifié (période d'échantillonnage: T_e). L'ordre d'échantillonnage est fournis par le circuit de commande. On associe de manière quasi-systématique à l'**échantillonneur un bloqueur. Ce bloqueur** doit maintenir la tension échantillonnée constante durant le temps de conversion (T_{conv}). Souvent on parle d'**échantillonneur-bloqueur**

2- Le Module de conversion **Analogique Numérique** CAN

Les Convertisseurs Analogique Numérique (CAN, ADC en anglais, pour analog to digital converter), Le convertisseur transforme le signal analogique en signal numérique apte à être traité par microprocesseur

(numérisation des signaux).

On trouve dans le commerce plusieurs types de convertisseur (CAN) qui offrent différents atouts (temps de conversion rapide du type "flash" ou résolution pointue (10 bits, 12, ..., 20 bits ou plus) mais le prix de fabrication est en conséquence).

3-Module des commandes et de traitement des données

Le **circuit de commande** est le "chef d'orchestre" : il donne les ordres des commandes à l'échantilloneur-bloqueur et au convertisseur A/D puis il effectue l'acquisition et le traitement des données suivant l'algorithme:

- début d'échantillonnage à l'échantilloneur-bloqueur,
- début de conversion au convertisseur A/D dialogue avec l'ordinateur:
- conversion effectuée, lire la valeur convertie ==> ordinateur
- l'ordinateur répond, prêt pour la donnée suivante. ==> circuit de commande

1- Structure fonctionnelle d'une chaîne de mesure:

3.*Chaîne de restitution des données*

1.3 Chaîne de restitution des données

La chaîne de restitution des données est présentée à la figure 5. cette chaîne est essentiellement réalisée par un convertisseur numérique analogique (CNA), un filtre de sortie et un amplificateur de puissance

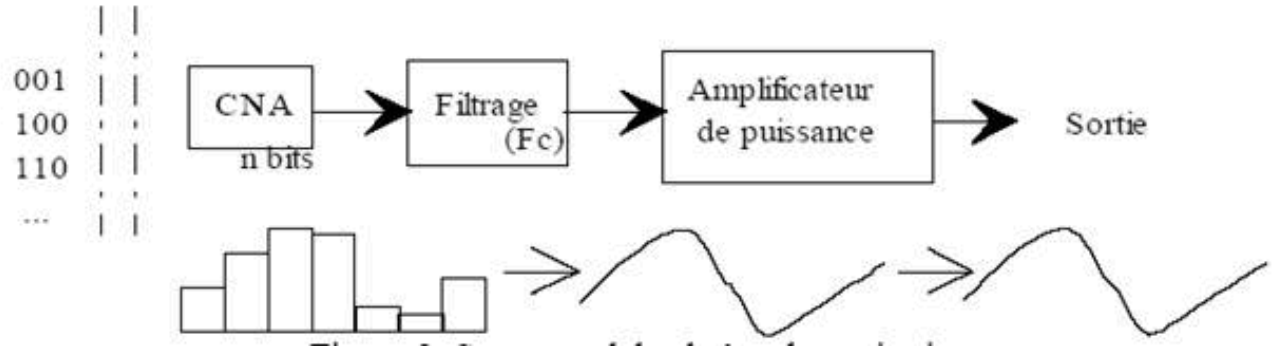


figure 5: La chaîne de restitution des données est présentée

Le convertisseur numérique analogique (CNA)

Il effectue l'opération inverse du CAN, il assure le passage du numérique vers l'analogique en restituant une tension proportionnelle au code numérique.

Le filtre de sortie

Son rôle est de « lisser » le signal de sortie pour ne restituer que le signal utile. Il a les mêmes caractéristiques que le filtre d’entrée.

Amplificateur de puissance

Il adapte la sortie du filtre à la charge.

1- Structure fonctionnelle d'une chaîne de mesure:

4. *Performances globale d'une chaîne de mesure*

1-4 Performances globale

Fréquence de fonctionnement

On peut définir la vitesse limite d'acquisition. Elle dépendre du temps pris pour effectuer les opérations d'échantillonnage ($\mathbf{T_{ech}}$), de conversion ($\mathbf{T_{conv}}$) et de stockage($\mathbf{T_{stock}}$)

Ainsi la somme de ces trois temps définit le temps minimum d'acquisition et donc la fréquence maximum de fonctionnement de la chaîne :

$$\mathbf{T_{acqmin} = T_{ech} + T_{conv} + T_{stock}}$$

Il existe deux catégories de convertisseurs :CNA et CAN

Les **Convertisseurs Numérique Analogique** (CNA, DAC en anglais, pour digital to analog converter) qui vont convertir les signaux logiques en tension analogique.

Les **Convertisseurs Analogique Numérique** (CAN, ADC en anglais, pour analog to digital converter), qui vont transformer les tensions analogiques en signaux logiques aptes à être traités par microprocesseur (numérisation des signaux).

Plusieurs types de convertisseurs sont disponibles dans chaque catégorie, qui se différencient par leur précision, leur vitesse de traitement de l'information, leur prix... Les principales caractéristique des CNA recherchés sont sa vitesse de conversion, résolution.

Nous abordons dans le chapitre 2 les techniques des convertisseurs numériques / analogique et nous présentons dans chapitre 3 les techniques des convertisseurs analogiques /numériques.

Remarque: nous présenterons les capteurs et l'amplificateur le filtre et l'échantillonneur /bloqueur dans un autre cours intitulé " Module d'acquisition des données".

Test d'auto-évaluation

Cours: *Conversions Numérique Analogique* **Question N°:**

15

Question suivante

Conversion Analogique-Numérique et Numérique-Analogique	Auteur
Conversion numérique-analogique et analogique-numérique	**Michel Hubin**
Convertisseurs Analogique / Numérique	**Ecole polytechnique fédérale de Lausanne**
Convertisseurs Numérique / Analogique	**Ecole polytechnique fédérale de Lausanne**
Convertisseurs N/A et A/N	**Dominique Chevalier**
Convertisseurs N/A et Convertisseurs A/N	**D. Piot**
Les Conversions D.A.C. et A.D.C.	**NeT_TroniquE**
Les technologies de CAN (simple & double rampes, à approx.) + TD	**CeLtiX**
Convertisseurs A/N et N/A " un bit " sigma delta	**Pierre-Louis Corrieu**
Conversion numérique analogique	**Patrick Dubief**

Liens

http://transdata.free.fr/cna.html	Ce site expose brièvement le principe de la Conversion Numérique Analogique et présente divers types de convertisseurs
http://www2.egr.uh.edu/~glover/	Il s'agit du site web d'un professeur à l'université de Houston, spécialisé entre autre, dans la conversion analogique-numérique. (Site en Anglais)
http://www.iut.u-bordeaux1.fr/geii/Cours/Ccouturie/cours3.pdf	Ce site présente en détail le principe de la conversion analogique numérique tant du point de vue éléctronique que du point de vue traitement du signal.
http://perso.wanadoo.fr/e-lektronik/LEKTRONIK/annexes/conversion.htm	Une page qui présente de façon assez complète la conversion analogique numérique.

http://www.jhu.edu/~signals/index.html

Divers applets Java ayant, plus ou moins, attrait à la conversion analogique numérique.

OBJECTIF

Cette page utilise des cadres. Pour pouvoir la consulter, votre navigateur doit supporter les cadres.

Les Convertisseurs Numériques - Analogiques & Les Convertisseurs Analogiques - Numériques

OBJECTIF

Les Convertisseurs Numériques /Analogiques*: CNA*

2.1 Généralités sur le codage

Dans un système de numération de base B, une quantité quelconque Q se représente à l'aide d'une suite de symboles a_{n-1} a_{n-2}.....a $_i$....a_2 a_1a_0. Chaque symbole a_i est caractérisé par sa position, ou rang, précisé par l'indice i qui définit automatiquement son poids B^i (B puissance i). Quant à la base B c'est le nombre de valeurs distinctes que peut prendre chaque symbole a_i. Dans ces conditions la valeur Q est égale à :

$$\mathbf{Q = a_{n-1}B^{n-1} + ...+a\ _iB^i+....+a_2B\ ^2+a_1B^1+a\ _0B^0}$$

Le nombre d'informations représenté par ces n symboles a_i est égale au nombre de combinaisons possibles soit B^n.

Exemples

1- si B =10 (base décimale) et Q =259, alors :

$259 = 2.10^2 +5.10^1 + 9.10^0 = 2.100 + 5.10 + 9.1$

2- si B=2 (base binaire) et Q = 100000011 alors en décimale la valeur de Q est:

$100000011 = 1.2^8+0.2^7 +0.2^6 +0.2^5+0.2^4+0.2\ ^3+0.2^2+1.2^1+1.2\ ^0 =256 +2 +1$

En pratique le système de numération à base 2, **le système binaire**, est imposé pour des raisons technologiques, les circuits électroniques à deux états connus depuis longtemps sont faciles à réaliser.

Les Convertisseurs Numériques/Analogiques:*CNA*

2.2 Principe de fonctionnement N/A

La Conversion Numérique Analogique, que nous désignerons dorénavant par CNA, consiste à transformer une information disponible sous forme binaire dans un code déterminé en une information analogique.

Soit l'information numérique N présentée dans le code binaire par:

$N = a_{n-1}\, a_{n-2}.....a_i.....a_2\, a_1 a_0$

avec :

n : nombre de bits du mot N

a_{n-1} : bit de poids fort MSB (Most Significant Bit)

a_0 : bit de poids faible LSB (Least Significant Bit)

Les Convertisseurs Numériques-Analogiques (CNA) ont pour but de convertir un mot numérique de N bits en une tension analogique. En effet un CNA va faire correspondre àl'information numérique N une tension Vs (ou courant Is) de sortie de la forme $Vs= F(N,V_{ref})$, avec V_{ref} est la tension de référence (figure 1).

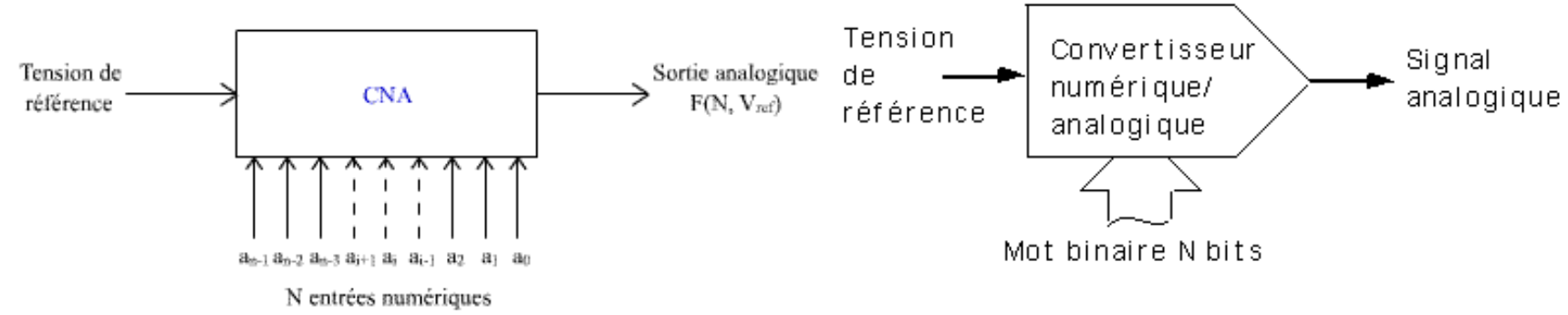


Figure 1 : Schéma simplifiée d'un CNA

Pour avoir une loi de variation linéaire, à chaque accroissement d'un bit de poids faible du mot N à convertir, on doit avoir un accroissement de la tension de sortie d'une quantité élémentaire appelée un quantum, noté q. La valeur du quantum est choisie par l'utilisateur, en fixant la tension de référence V_{ref} et le nombre de bits n du CNA ; en effet :

$$q = \frac{Vref}{2^n}$$

Exemple : Pour n = 8 et V_{ref} =10V alors q= 10/256 =39mv

Pour calculer Vs, nous devrons exprimer N sous sa forme décimale:

$N = a_{n-1}\,2^{n-1} + \ldots\ldots + a_i\,2^i + \ldots + a_2\,2^2 + a_1\,2^1 + a_0\,2^0$

On déduit la valeur de Vs

$$Vs = q.N = (V_{ref} /2^n) [a_{n-1} 2^{n-1} +.....+a_i 2^i +....+ a_2 2^2 + a_1 2^1 + a_0 2^0]$$

Remarques

1-: Quand l'information numérique est maximum?

l'information numérique est maximum lorsque tous les bits a_i sont égaux à 1,dans ce cas l'information analogique correspondant est maximum et sa valeur est égale à:

$$\mathbf{Vsmax = q.N = (V_{ref} 2^n) [2^{n-1} +.....+2^i +....+ 2^2 + 2^1 + 2^0] = q.(2^n -1)}$$

$$\mathbf{= (Vref/2^n) (2^n -1) = Vref - q}$$

On note que la tension de sortie maximum n'atteint pas la tension de référence mais elles se diffèrent de 1 quantum. La tension de référence est considérée comme étant la tension de la Pleine Échelle (PE), " Full Scale : FS"

2-: La valeur analogique minimum autre que zéro ne peut être que 1 quantum:

$$\mathbf{Vsmin =1. q = (Vref/2^n)}$$

3-: ***La résolution:*** Par définition, la résolution r d'un système est la plus petite valeur ou incrément minimum, que ce système peut reconnaître ou délivrer, ramenée à la valeur maximum. On déduit la valeur de r:

$$r = \frac{Vsmin}{Vsmax} = \frac{q}{q.(2^n-1)} = \frac{1}{(2^n-1)} \approx \frac{1}{2^n}$$

On peut définir la résolution comme étant la plus petite variation relative de tension (courant) de sortie par rapport à la pleine échelle.

Les Convertisseurs Numériques /Analogiques *: CNA*

2.3 Courbe de transfert d'un CNA

Utilisation du code binaire naturel

Formules

$$V_S = \frac{V_{ref}}{2^n}\left[a_{n-1}\,2^{n-1}+.....+a_i\,2^i+.....+a_2\,2^2+a_1\,2^1+a_0\,2^0\right]$$

ce qui s'écrit aussi :

$$V_S = V_{ref}\left[\frac{a_{n-1}}{2^1}+.....+\frac{a_i}{2^{n-i}}+.....+\frac{a_2}{2^{n-2}}+\frac{a_1}{2^{n-1}}+\frac{a_0}{2^n}\right]$$

V_{ref} : Tension de référence (tension de pleine échelle :PE)pour éxprimer Vs

$\frac{V_{ref}}{2^n}$: Valeur du quantum (q)

n : nombre de bits

an-1 : bit de poids fort (Most Sinificant Bit :**MSB**)

a_0 : bit de poids faible (Least Sinificant Bit :**LSB**)

Courbe de transfert (voir figure 2)

Entrées numériques	Sorties analogiques
N0 = 00...00	0
N1 = 00...01	q
N2 = 10...00	Vref/2
N3 = 11...11	Vref - q

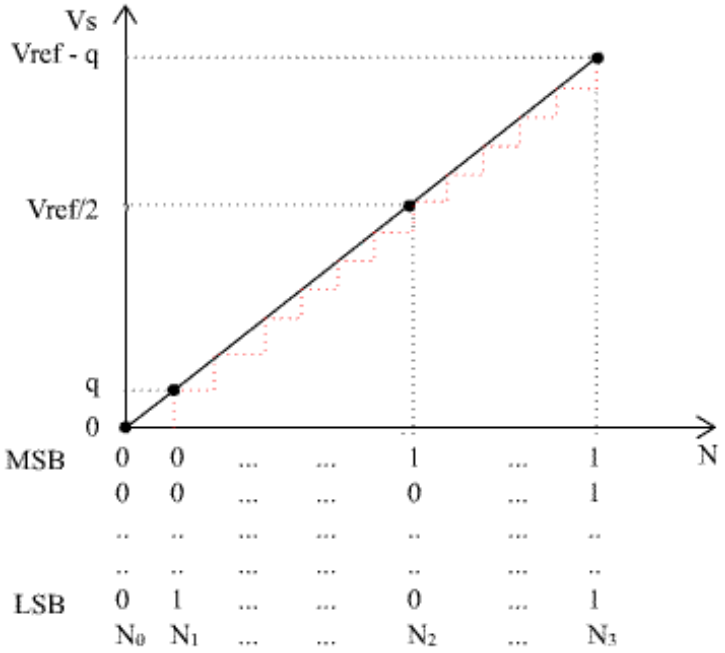


figure 2 : Courbe de transfert d'un CNA

Utilisation du code binaire codé décimal BCD

Définition du digit

Le **digit** est la représentation binaire des chiffres décimaux (0,1,...,9), donc on doit l'exprimer par 4 bits.

On définie:

-Le Digit de poids fort, " Digit le Plus Significatif " (Most Sinificant Digit: MSD)

-Le Digit de poids faible, " Digit le moins Significatif " (Least Sinificant Digit: LSD) :

Le tableau ci dessous illustre MSD et LSD d'un nombre de 4 digits.

a_{33} a_{32} a_{31} a_{30}	a_{23} a_{22} a_{21} a_{20}	a_{13} a_{12} a_{11} a_{10}	a_{03} a_{02} a_{01} a_{00}
MSD			**LSD**

Remarques

Très souvent l'information numérique N n'est pas un nombre entier de digits, mais un nombre fractionnaire, fréquemment on utilise le demi digit (1/2) et le trois quart digit (3/4).
Par exemple, on explique les significations d'un CNA à 3 Digits 1/2 et d'un CNA à 3 Digits 3/4 . En effet, les 3 digits les moins significatifs sont entiers, c'est à dire s'expriment par 4 bits, mais le quatrième digit qui est le plus significatif ne s'exprime pas par quatre bits. En règle générale les significations de demi digit 1/2 et de trois quart digit 3/4 sont :

- le 1/2 digit: veut dire que le digit le plus significatif est exprimé sur 1 bit, donc seul les valeurs 0 et 1 sont possibles.
La plage de conversion s'étend de 0000 à 1999, donc il y a 2000 point de conversion;on parle parfois de CNA à 2000 points de mesures; dans ce cas N peut prendre 2000 valeurs possibles, la tension (courant) de sortie du CNA peut avoir 2000 échelons de tension correspondant à ces 2000 valeurs.

- le 3/4 digit: veut dire que le digit le plus significatif est exprimé sur 2 bits, donc seul les valeurs 0, 1, 2 et 3 sont possibles. On note que N peut prendre 4000 valeurs possibles et la tension (courant) de sortie du CNA peut avoir 4000 échelons de tension.
Formule :

$$Vs = \frac{V_{ref}}{V.10^n}\left[\begin{array}{l}(a_{n1}\,2^1 + a_{n0}\,2^0)10^n + a_{n-1,3}2^3 + a_{n-1,2}2^2 + a_{n-1,1}2^1 + a_{n1,0}2^0)10^{n-1} + \\ \ldots\ldots\ldots\ldots\ldots\ldots + (a_{03}\,(a_{03}\,2^3 + a_{02}\,2^2 + a_{01}\,2^1 + a_{00}\,2^0)10^0\end{array}\right]$$

V_{ref} : Tension de référence pour éxprimer Vs
tension de pleine échelle :PE

$\frac{V_{ref}}{V.10^n}$: Valeur du quantum (q)

n : nombre de bits

V : Valeur maximum du digits fractionnaire + 1

Les techniques des conversions analogique-numérique:

Les Convertisseurs Numériques /Analogiques*: CNA*

4 Définition des CNA unipolaire et bipolaire

4.1 CNA unipolaire

Dans l'étude précédente des équations de transfert du CNA, nous avons considéré que la tension de sortie du CNA est toujours de même signe que celui de la tension de référence. Dans ce cas le convertisseur est dit **unipolaire**. L'allure de la courbe de transfert d'un CNA est présentée à la figure 3.

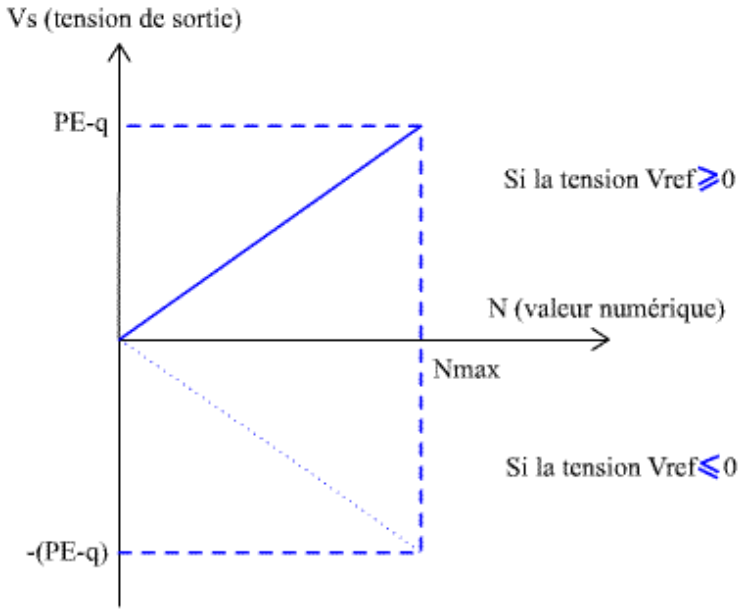


Figure 3: courbe de transfert d'un CNA unipolaire

On note que, Vs est positive si Vref est positive et elle est négative si Vref est négative.

Dans ce cas, les codes les plus utilisés sont le Code BInaire Naturel " BIN " et le code Binaire Codé Décimal "DCB"; mais il est possible d'utiliser d'autres codes dérivés de ces deux codes; par exemple le code binaire naturel complémenté et le code binaire codé décimal complémenté dont nous donnons leurs définition:

- Le code binaire naturel complémenté (Complementary Binary: CBIN): Ce code se déduit du code BIN en complémentant à un tous les bits; c'est à dire en inversant tous les bits (les 0 deviennent 1 et vice versa).

- Le code binaire codé décimal complémenté (Complementary Binary Coded Decimal: CBCD): Ce code se déduit du code BCD en complémentant tous les bits de chaque combinaison.

4.2 CNA bipolaire

Le CNA bipolaire est un convertisseur dont la tension de sortie change de signe en fonction de l'information numérique d'entrée. La courbe de transfert du CNA bipolaire est présenté à la figure 4. On constate que la courbe de transfert présente une translation de (Vref)/2 par rapport à la courbe de transfert d'un convertisseur unipolaire.

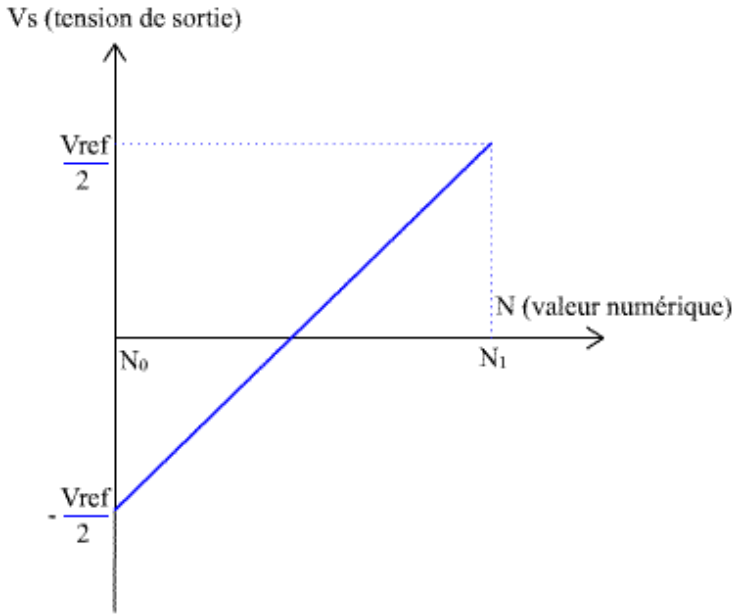


Figure 4 : Courbe de transfert d'un CNA bipolaire

D'après cette courbe, on constate que la tension de sortie peut être positive ou négative; ceci en fonction de la valeur numérique N. En effet pour la valeur numérique N_0, on fait correspondre la tension négative $-V_2$, et à la valeur N_1 correspond la tension positive V_1. On peut avoir également l'inverse.

Exercice 1 :

Compléter la suite logique de nombres croissants appartenant à différents systèmes de numération.

Binaire	octal	hexadécimal	binaire	Base 18	hexadécimal
011100	156	4CF9	111000	HC	9FFFC
011101					
011110					

Exercice 2

Effectuer les opérations d’arithmétiques binaires.

Les techniques des conversions analogique-numérique:

```
  0 1 0 0 0 0 1
+ 0 1 1 0 0 1 1
```

```
  0 1 1 1 1 1 1 0
+ 0 0 0 1 1 1 0 1
```

```
  0 1 1 0 0 0 1
- 0 1 0 1 0 1 1
```

```
  0 0 1 1 1 0 1 0
- 0 0 0 1 1 1 0 1
```

```
  0 1 0 0 0 0 1
- 0 1 1 0 0 1 1
```

```
  0 0 1 1 1 0 1 0
- 0 1 0 1 1 1 0 1
```

```
  1 1 1 1 1 0 0
+ 1 1 1 1 0 1 0
```

```
  1 1 1 0 0 1 0 1
+ 1 0 1 0 1 0 1 0
```

```
  1 1 1 1 1 0 0
- 1 1 1 1 1 1 0
```

```
  1 0 1 0 0 1 0 1
- 1 1 1 0 1 0 1 0
```

Exercice 3 :

Pour chaque opération de l’exercice 2, convertissez les nombres binaires en nombre décimal et effectuer les opérations décimales :

Conclusion :

Exercice 4 :

Effectuer les opérations d’arithmétiques hexadécimales.

```
    1   8          1  A  F  9          0  5  E  3
+   2   8      +   0  1  0  9      +   6  5  3  8

    2   8          1  A  F  9          6  5  3  8
-   1   8      -   0  1  0  9      -   0  5  E  3
```

1 8	1 A F 9	0 5 E 3
- 2 8	- 2 B 0 9	- 6 6 3 8

Exercice 5 :

Sous le même principe qu'une multiplication décimale, effectuez les multiplications binaires suivantes.

1 1 0 0	1 1 1 0 1
× 1 0	× 1 0 0

Remarque :

1 1 0 0	1 1 1 0 1
× 1 0 1 1	× 0 1 1 1 0

Test d'auto-évaluation

Cours: *Conversions Numérique Analogique* **Question N°:**

15

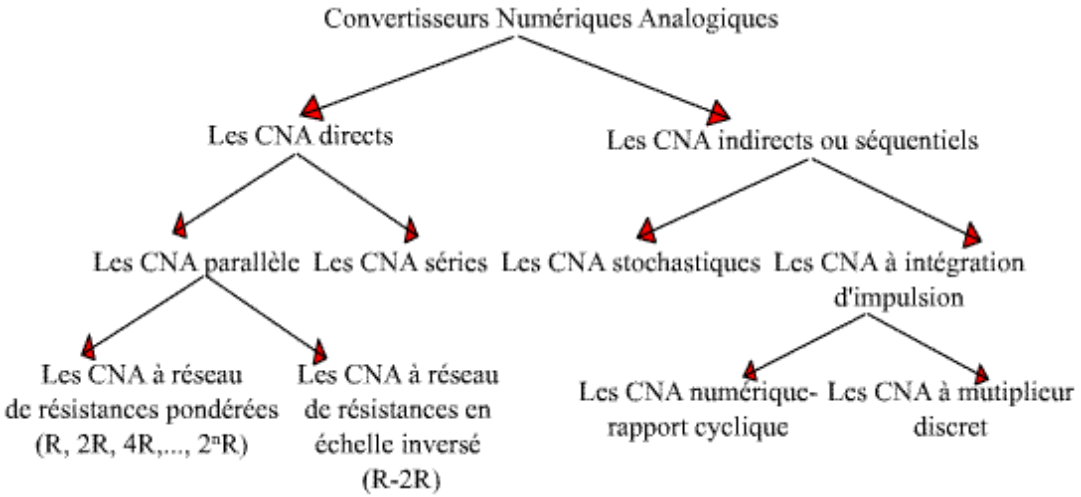
Question suivante

5.1.Introduction

Nous allons étudier les différentes techniques employées pour convertir une donnée binaire en une grandeur analogique. Nous distinguons deux techniques de conversions numériques analogiques qui sont les techniques de conversion N/A directs et les techniques de conversion N/A indirects.

Dans les techniques de conversion N/A direct le mot binaire est directement converti en signal analogique. Ces convertisseurs sont entièrement réalisés avec des composants analogiques (réseau de résistances, transistors, amplificateurs, etc...); le temps de conversion est relativement faible, mais ils sont assez coûteux.

Dans les techniques des convertisseurs indirects ou séquentiels le mot binaire subit une première conversion à un signal dont le rapport cyclique ou bien le nombre d'impulsions est proportionnel du mot binaire N. Une deuxième conversion (filtrage) pour transformer le signal variable en un signal continu. Ces convertisseurs sont réalisés en majorité avec des composants logiques (portes, bascules, registres, compteurs etc...); le temps de conversion est relativement élevé, mais ils sont peu coûteux. Le tableau ci dessous regroupe les différentes techniques des CNA que nous allons étudier en détail aux paragraphes suivants.



5.2Schéma de principe des convertisseurs N/A parallèles

A partir des équations de transfert démontrées précédemment, nous pouvons déduire le schéma de principe d'un CNA parallèle présenté à la figure 5.

$$Vs\ (ou\ Is) = \frac{V_{ref}}{2^n}\left[a_{n-1}\,2^{n-1} + \ldots\ldots + a_i\,2^i + \ldots\ldots + a_2 2^2 + a_1\,2^1 + a_0\,2^0\right]$$

ce qui s'écrit aussi :

$$Vs = V_{ref}\ (ou\ I_{ref})\left[\frac{a_{n-1}}{2^1} + \ldots\ldots + \frac{a_i}{2^{n-i}} + \ldots\ldots + \frac{a_2}{2^{n-2}} + \frac{a_1}{2^{n-1}} + \frac{a_0}{2^n}\right]$$

n : nombre de bits

Un convertisseur N/A comprendra donc :

- Une source de référence (soit en tension Vref ,soit Iref en courant); Cette source doit avoir une bonne précision.

- Un système de pondération pour retrouver les coefficients pondérés dans le code binaire naturel ou bien dans le cas de code BCD,

- Une commande numérique pour effectuer la multiplication par les coefficients a_{n-1},....., a_0, à l'aide d'interrupteurs électroniques.

- Un système de sommation pour calculer la somme suivante :

- un étage de sortie qui assure la conversion courant tension pour un CNA à sortie en tension.

Figure 5: Schéma de principe d'un convertisseur N/A parallèle

6 - CNA à réseau des résistances pondérées

Principe

Le schéma de principe d'un convertisseur à résistances pondérées (R, 2R, 4R...) utilisant le code binaire naturel est présenté à la figure 6.Ce convertisseur contient :

- Une tension de référence
- Une batterie de commutateurs commandés par le code numérique d'un registre binaire
- Une batterie de résistances pondérées de manière à ce que les courants générés soient dans une progression géométrique de raison 1/2

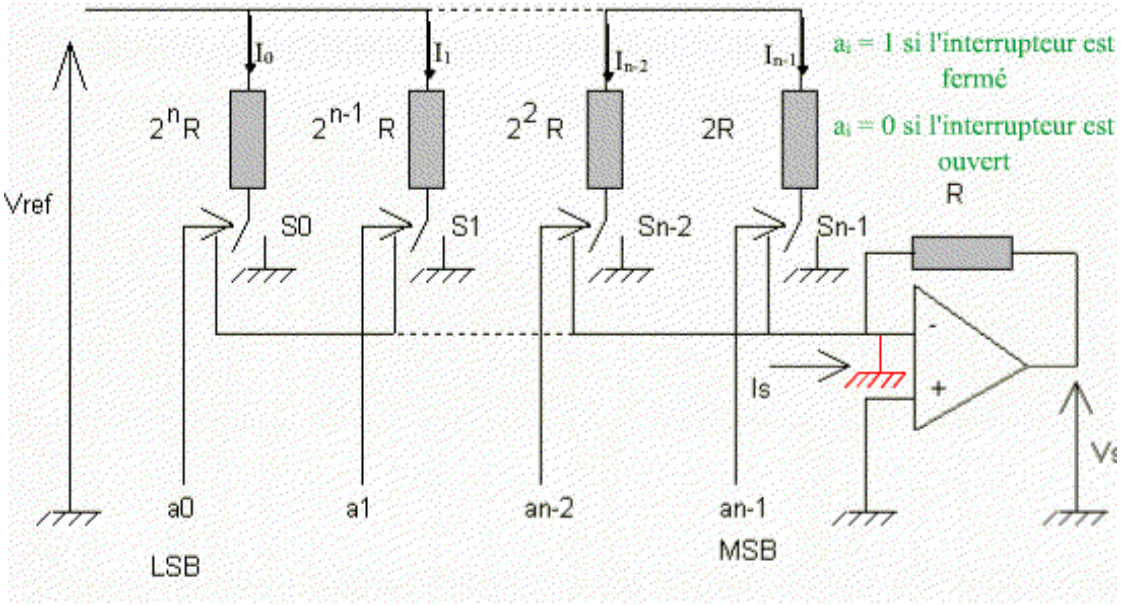


Figure 6: CNA à résistances pondérées

On se propose de calculer la tension de sortie pour différentes valeurs de N et de vérifier par la suite que ce montage rempli la fonction du convertisseur numérique analogique.

Calcul de la tension de sortie Vs

On remarque que le courant élémentaire I_i qui traverse la résistance pondérée 2^iR se dirige vers la masse réelle ou ou la masse virtuelle (entrée - de l'OP) en fonction de la position du commutateur S_i. En effet si a_i = 0 le commutateur se trouve à la position 2 par contre si a_i =1 le commutateur se trouve à la position 1. Le courant Is est la somme des courants élémentaires dont les commutateurs sont à la position 1.

$$Is= a_{n-1}I_{n-1}+ a_{n-2}I_{n-2}+.....+ a_2I_2+a_1I_1+a_0I_0$$

$$V_S = -R.I_S$$

$$I_S = I_{n-1} + I_{n-2} + \ldots\ldots + I_2 + I_1 + I_0$$

$$I_S = \frac{V_{ref}}{2.R} a_{n-1} + \frac{V_{ref}}{2^2.R} a_{n-2} + \ldots\ldots\ldots\ldots + \frac{V_{ref}}{2^{n-2}.R} a_2 + \frac{V_{ref}}{2^{n-1}.R} a_1 + \frac{V_{ref}}{2^n.R} a_0$$

Les S_i prennent les valeur 0 ou 1 en fonction de la valeur du bit correspondant a_i.

En multipliant l'expression par $\frac{2^n}{2^n}$ et en mettant en facteur $\frac{V_{ref}}{2^n.R}$ on obtient:

$$I_S = \frac{V_{ref}}{2^n.R} [a_{n-1}\, 2^{n-1} + \ldots\ldots + a_i\, 2^i + \ldots + a_2\, 2^2 + a_1\, 2^1 + a_0\, 2^0]$$

on déduit la fonction de transfert de ce convertisseur :

$$V_S = -\frac{V_{ref}}{2^n} [a_{n-1}\, 2^{n-1} + \ldots\ldots + a_i\, 2^i + \ldots + a_2\, 2^2 + a_1\, 2^1 + a_0\, 2^0]$$

Avantage et inconvénient

L'intérêt d'un tel convertisseur réside dans sa simplicité, mais il devient vite imprécis lorsque le nombre de bits augmente. En effet il nécessite des résistances de précision dans une grande gamme de valeurs (de R à 128 R pour un codage sur 8 bits, par exemple). C'est pourquoi on emploie rarement ce CNA au-delà de 4 bits. La principale source d'erreur provenant de la réalisation du réseau de résistances. La manière la plus simple de résoudre ce problème est d'utiliser plusieurs blocs identiques de quatre résistances, et de quatre interrupteurs appelés "quarts" et de faire une somme pondérée de ces courants fournis par les quarts. Cette solution est très employée pour réalisation de convertisseurs numériques analogiques utilisant le code binaire naturel (CBN) ou le code binaire codé décimal (BCD) en choisissant le diviseur de courant convenable, comme le montre les figure 7 et la figure 8.

Exemple de réalisation

Un exemple de réalisation industrielle d'un convertisseur N/A à 12 bits à réseau de résistances pondérés est

présenté à la figure 7. On note l'utilisation de 3 blocs identiques comprenant chacun quatre résistances et quatre interrupteurs.

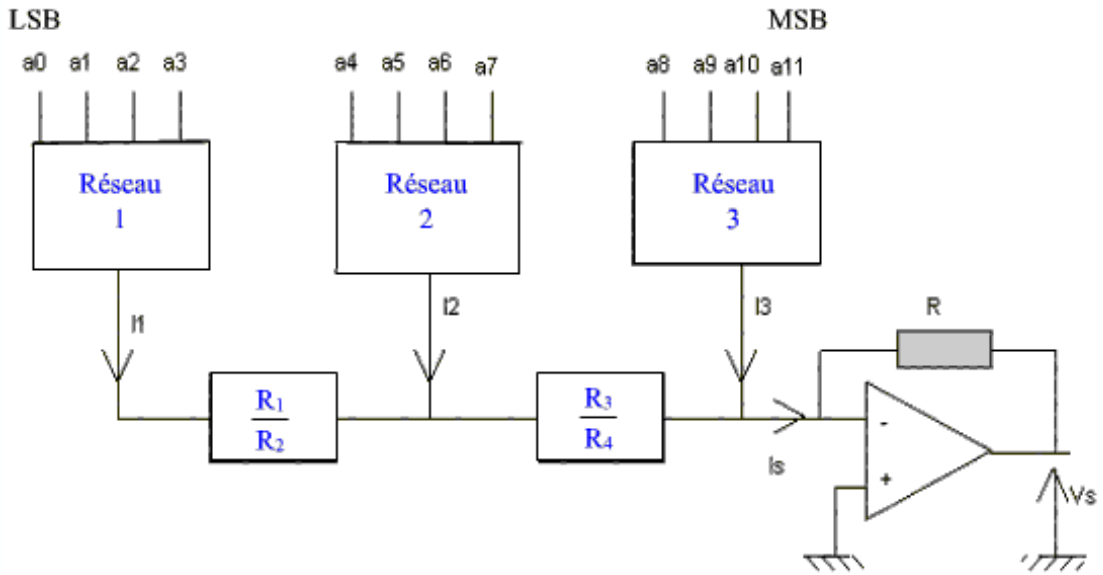


Figure 7 : CNA 12 bits utilisant le CBN

L'expression I_1est la même que celle de I_2 et I_3 seule les indices qui changent.

$$I_1 = \frac{Vref}{2^4.R}(a_3 2^3 + a_2 2^2 + a_1 2^1 + a_0 2^0)$$

$$I_2 = \frac{Vref}{2^4.R}(a_7 2^3 + a_6 2^2 + a_5 2^1 + a_4 2^0)$$

$$I_3 = \frac{Vref}{2^4.R}(a_{11} 2^3 + a_{10} 2^2 + a_9 2^1 + a_8 2^0)$$

Les résistances R1, R2, R3 et R4 sont choisies de telle sorte que l'on ait un pont diviseur par 16 pour avoir

l'expression habituelle du courant de sortie du convertisseur il faut que :

$$Is= I_3 + I_2/2^4 + I_1/2^8$$

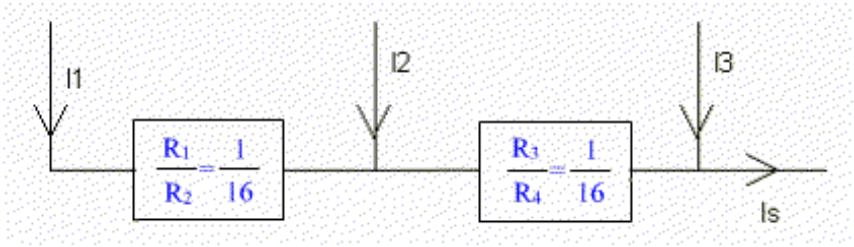


Figure 8 : choix du diviseur de tension pour le CBN

Le courant de sortie Is a pour expression:

$$I_s = \frac{I_1}{256} + \frac{I_2}{16} + I_3$$

7- CNA à courants pondérés

Le convertisseur R-2R présente certains inconvénients, notamment quand les courants qui circulent dans les résistances 2R changent de sens lors de la commutation. Ceci entraîne l'existence d'un régime transitoire et un retard de conversion.

En utilisant des courants constants qui sont toujours dirigés dans le même sens, L'inconvénient précédemment du CNA à réseau R - 2R est supprimé. Le principe du CNA à courants pondérés présenté dans la figure 12 consiste donc à générer des courants I, 2I, 4I, 8I, etc... et à additionner ces courants en fonction du code numérique. En associant par exemple trois décades constituées chacune de quatre sources de courant (I, 2I, 4I et 8I) et de trois résistances pondérées en série, on peut réaliser un CNA dont le code numérique se présente sous la norme BCD figure 6.

Figure 12 : Réseau à courants pondérés pour un CNA

L'avantage de ce type de convertisseur est la grande vitesse de conversion grâce à l'absence des régimes transitoires. Les CNA à courants pondérés sont en générales réalisées à l'aide des transistors bipolaires.

Remarque :

Le choix du courant I est très important

-Un courant trop faible est susceptible d'être gêné par des courants parasites.

-Un courant trop fort ne fait qu'augmenter la consommation.

On retiendra quand même que le principal avantage de ce type de CNA est sa grande vitesse de conversion, grâce à l'absence de régime transitoire.

- Evaluation
- QCM

Les techniques des conversions analogique-numérique:

Test d'auto-évaluation

Cours: *Conversions Numérique Analogique* **Question N°:**

15

Question suivante

8- CNA à réseau R/2R.

Principe

Ce réseau est constitué des résistances ayant pour valeurs R et 2R figure 9.

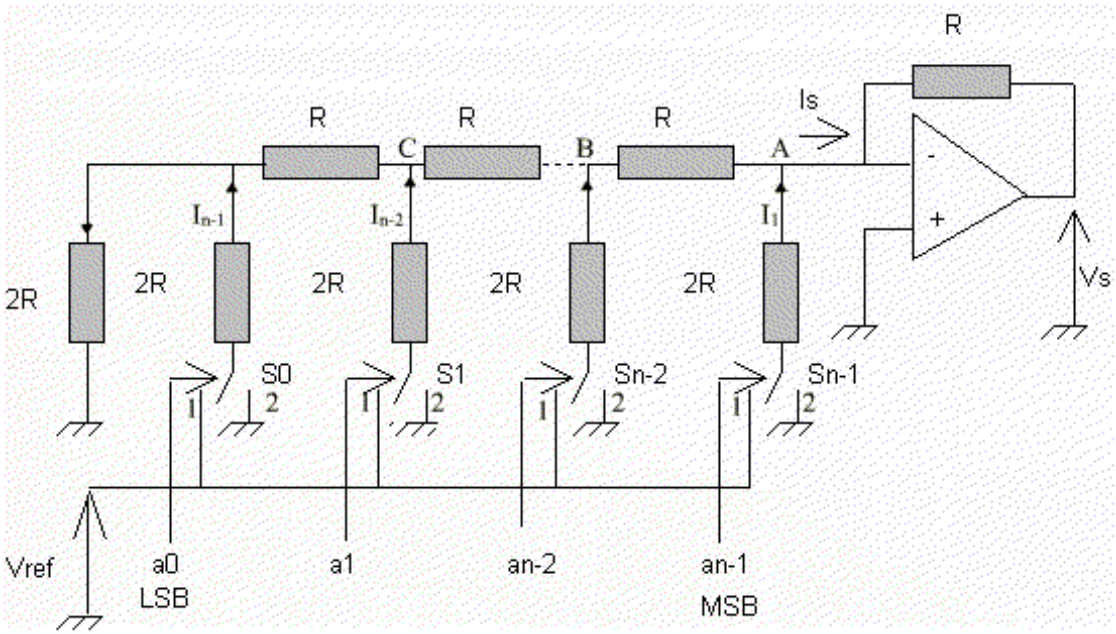


Figure 9: CNA à réseau R-2R

Si tous les a_i sont égaux à 0 ($a_i = 0$), les commutateurs se trouvent à la position 2 dans ce cas, tous les résistances 2R sont connectées à la masse (on suppose la résistance interne de la source de référence égale à 0) la résistance équivalente du réseau vue du point A est égale à R (2R en parallèle avec 2R est égale à R, R en série avec R donne 2R et ainsi de suite). Les commutateurs sont commandés par le code numérique. La valeur analogique est la somme de courants aboutissant à l'entrée "-" de l'amplificateur opérationnel, l'amplificateur opérationnel convertie le courant en tension.

- **Calcul des courants et de la tension de sortie**

1-Calculons le courant I_1 fourni à l'amplificateur par la seule fermeture de S_{n-1}.

Le mot binaire d'entrée est égale à 100..0 (seul le MSB =1).

En appliquant le théorème de Thevnin sur le schéma équivalent du CNA (R - 2R) de la figure 10, on déduit la valeur de ce courant :

$$I_s = I_1 = \frac{Vref}{R} \quad \text{donc} \quad V_s = -RI_s = \frac{-Vref}{2}$$

Figure 10: schéma équivalent du CNA par la seule fermeture de S_{n-1}

2- Calculons le courant I_2 fourni à l'amplificateur par la seule fermeture de S_{n-2} .

Le mot binaire d'entrée est égale à 010..0.

En appliquant le théorème de Thevnin sur le schéma équivalent du CNA R - 2R de la figure 11.

Schéma équivalent :

Figure 11 :schéma équivalent du CNA par la seule fermeture de S_{n-2}

On déduit la valeur de ce courant :

$$I_s = I_2 = \frac{Vref}{4R} \quad \text{donc} \quad V_s = -RI_s = \frac{-Vref}{4}$$

D'après le théorème de superposition, la fermeture de S_{n-1} et de S_{n-2} fournira à l'amplificateur la somme de courant $I_1 + I_2$ (le mot binaire est égale à1100..0) (figure 12), et la tension de sortie est la somme de deux tensions :

$$V_s = -\left(\frac{Vref}{2} + \frac{Vref}{4}\right)$$

Figure 12 : schéma équivalent du CNA par la seule fermeture de S_{n-1} et S_{n-2}

Grâce au théorème de superpositions, on calcule facilement la tension de sortie pour différentes combinaisons de l'information d'entrée d'où la formule générale:

$$Vs = \frac{V_{ref}}{2^n}\left[a_{n-1}\,2^{n-1}+.....+a_i\,2^i+.....+a_2 2^2+a_1\,2^1+a_0\,2^0\right]$$

- Avantages et inconvénients

Pour ce type de convertisseur, en plus de la tension de référence, les deux éléments qui fixent la précision sont le réseau de résistances qui devrait avoir un très faible coefficient de température et le réseau des interrupteurs qui devrait avoir une faible résistance équivalente.

- QCM
  - Test

3-

Convertisseur N/A R-2R

L'applet :

Mode manuel : Une série de cases à cocher permet de modifier la position des inverseurs. Des voltmètres idéaux affichent la valeur du potentiel pour chaque noeud. La valeur de la tension E de référence est égale à 2,56 V.

Mode automatique : Il est possible de choisir entre plusieurs formes d'onde et de modifier la résolution du convertisseur. Sur la courbe $V_S = F(t)$ qui s'affiche dans le bas de l'applet, bien noter l'aspect en échelons de la tension de sortie.

Un click sur le bouton droit de la souris permet de geler l'animation.

Les techniques des conversions analogique-numérique:

Test d'auto-évaluation

Cours: *Conversions Numérique Analogique* **Question N°:**

15

Question suivante

Les techniques des conversions analogique-numérique:

9 - CNA à réseau R/2R à échelle inversée

Actuelle, cette famille des convertisseur occupe une place importante dans le marché des convertisseurs; grâce à son prix accessible et ses performances supérieures à celles des montages précédents.

Le schéma de principe d'un CNAà réseau R-2R à échelle inversée est donné à la figure 14. Nous signalons que les bits de poids fort (MSB) et faible (LSB) sont inversés par rapport au montage R-2R classique, ce qui explique le nom de ce CNA. (figure 11). La structure de base reste un réseau R - 2R, mais les courants dans les résistances 2R circulent toujours dans le même sens; ils sont constamment orientés vers à la masse ou vers l'entrée de l'amplificateur (masse virtuelle), qui sont pratiquement au même potentiel électrique.

Figure 14 : CNA à réseau R - 2R à échelle inversée

1- Calculons le courant Ia fourni à l'amplificateur par la seule fermeture de S_{n-1} .

Le mot binaire d'entrée est égale à 100..0 (seul le MSB =1). Les schémas équivalents sont donnés à la figure 15.

(a)

(b)

figure 15 : CNA à réseau R - 2R à échelle inversée

(a) principe (b) code d'entrée N= 100...0

En appliquant le théorème de Thevnin sur le schéma équivalente du CNA R - 2R de la figure 15 (a) et figure 15 (b), on déduit la valeur de ce courant:

$$I_s = I_a = \frac{Vref}{2R} \quad \text{donc} \quad V_s = -RI_s = \frac{-Vref}{2}$$

2- Calculons le courant I_b fourni à l'amplificateur par la seule fermeture de S_{n-2} .

Le mot binaire d'entrée est égale à 010..0.

En appliquant le théorème de Thevnin sur le schéma équivalent du CNA R - 2R de la figure 16.

On déduit la valeur de ce courant :

$$I_s = I_b = \frac{Vref}{4R} \quad donc \quad V_s = -RI_s = \frac{-Vref}{4}$$

Figure 16 : schéma du CNA pour le code d'entrée N=010..0

D'après le théorème de superposition, la fermeture de S_{n-1} et de S_{n-2} fournira à l'amplificateur la somme de courant I_a+I_b (le mot binaire est égale à 1100..0 , et la tension de sortie est la somme de deux tensions) :

$$V_s = -\left(\frac{Vref}{2} + \frac{Vref}{4}\right)$$

Grâce au théorème de superpositions, on calcule facilement la tension de sortie pour différentes combinaisons de l'information d'entrée; d'où la formule générale:

$$Vs = -\frac{V_{ref}}{2^n}\left[a_{n-1}\,2^{n-1} + \ldots\ldots + a_i\,2^i + \ldots\ldots + a_2 2^2 + a_1\,2^1 + a_0\,2^0\right]$$

On peut utiliser des résistances de fortes valeurs sans compromettre la vitesse de conversion, ceci permet de diminuer les erreurs dues aux résistances de fuite (quelques centaines d'ohms) des commutateurs analogiques. Ce courant étant assez faible, les imperfections de l'amplificateur opérationnel (courant de polarisation, tension de décalage etc..) sont des éléments à ne pas négliger dans le calcul de précision du système. La place importante de ce CNA sur le marché actuel nécessite naturellement une étude approfondie de cette famille. Cette étude sera menée avec un exemple concret pour mieux comprendre les divers problèmes technologiques et les solutions apportées par l'électronique moderne. La description se rapporte au modèle AD 7533 de Analog Devices 

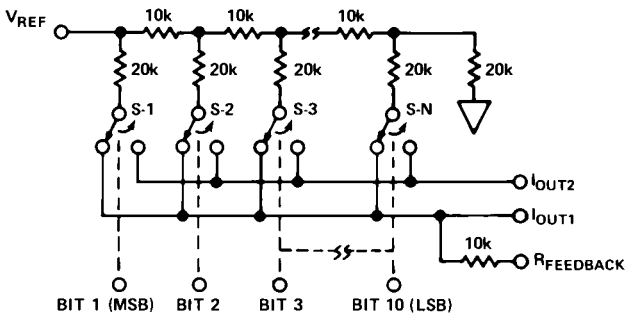
CMOS Low Cost 10-Bit Multiplying DAC

AD7533

FEATURES
Lowest Cost 10-Bit DAC
Low Cost AD7520 Replacement
Linearity: 1/2, 1 or 2LSB
Low Power Dissipation
Full Four-Quadrant Multiplying DAC
CMOS/TTL Direct Interface
Latch Free (Protection Schottky not Required)
End-Point Linearity

APPLICATIONS
Digitally Controlled Attenuators
Programmable Gain Amplifiers
Function Generation
Linear Automatic Gain Control

Functional Block Diagram



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Nonlinearity (% FSR max)	Package Option[3]
AD7533JN	−40°C to +85°C	±0.2	N-16
AD7533KN	−40°C to +85°C	±0.1	N-16
AD7533LN	−40°C to +85°C	±0.05	N-16
AD7533JP	−40°C to +85°C	±0.2	P-20A
AD7533KP	−40°C to +85°C	±0.1	P-20A
AD7533LP	−40°C to +85°C	±0.05	P-20A
AD7533JR	−40°C to +85°C	±0.2	R-16
AD7533KR	−40°C to +85°C	±0.1	R-16
AD7533LR	−40°C to +85°C	±0.05	R-16
AD7533AQ	−40°C to +85°C	±0.2	Q-16
AD7533BQ	−40°C to +85°C	±0.1	Q-16
AD7533CQ	−40°C to +85°C	±0.05	Q-16
AD7533SQ	−55°C to +125°C	±0.2	Q-16
AD7533TQ	−55°C to +125°C	±0.1	Q-16
AD7533UQ	−55°C to +125°C	±0.05	Q-16
AD7533SE	−55°C to +125°C	±0.2	E-20A
AD7533TE	−55°C to +125°C	±0.1	E-20A
AD7533UE	−55°C to +125°C	±0.05	E-20A

NOTES
[1]Analog Devices reserves the right to ship ceramic (package outline D-16) packages in lieu of cerdip (package outline Q-16) packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

REV. A

One Technology Way; P. O. Box 9106; Norwood, MA 02062-9106 U.S.A.
Tel: 617/329-4700 **Twx: 710/394-6577**
Telex: 174059 **Cables: ANALOG NORWOODMASS**

AD7533—SPECIFICATIONS (V_{DD} = +15V, V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy[1]			
AD7533JN, AD, SD, AQ, SQ	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD, BQ, TQ	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD, CQ, UQ	±0.05% FSR max	±0.05% FSR max	
Gain Error[2,3]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[4]			
$\Delta Gain/\Delta V_{DD}$	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1}	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2}	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[4]	800ns[5]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[5]	±0.1% FSR max[5]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sine wave.
REFERENCE INPUT			
Input Resistance (Pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[6]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1}	100pF max[5]	100pF max[5]	Digital Inputs = V_{INH}
C_{OUT2}	35pF max[5]	35pF max[5]	
C_{OUT1}	35pF max[5]	35pF max[5]	Digital Inputs = V_{INL}
C_{OUT2}	100pF max[5]	100pF max[5]	
DIGITAL INPUTS			
Input High Voltage			
V_{INH}	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	8pF max[5]	8pF max[5]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[5]	+5V to +16V	+5V to +16V	Functionality with Degraded Performance
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}

NOTES
[1]"FSR" is Full-Scale Range.
[2]Full Scale (FS) = (V_{REF})
[3]Max gain change from T_A = +25°C to T_{min} or T_{max} is ±0.1% FSR.
[4]AC parameter, sample tested to ensure specification compliance.
[5]Guaranteed, not tested.
[6]Absolute temperature coefficient is approximately −300ppm/°C.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
R_{FB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage Range	−0.3V to V_{DD} +0.3V
OUT 1, OUT 2 to GND	−0.3V to V_{DD}
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Plastic (JN, KN, LN versions)	0 to +70°C
Hermetic (AD, BD, CD, AQ, BQ, CQ versions)	−25°C to +85°C
Hermetic (SD, TD, UD, SQ, TQ, UQ versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % of full-scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution fo $[2^{-(n-1)}]$ $(V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

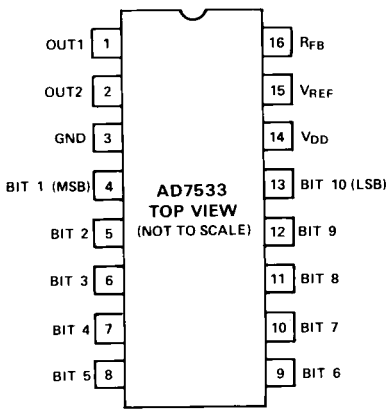
GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustble to zero with an external potentiometer.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

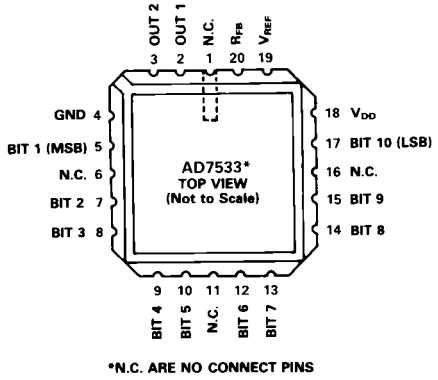
OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

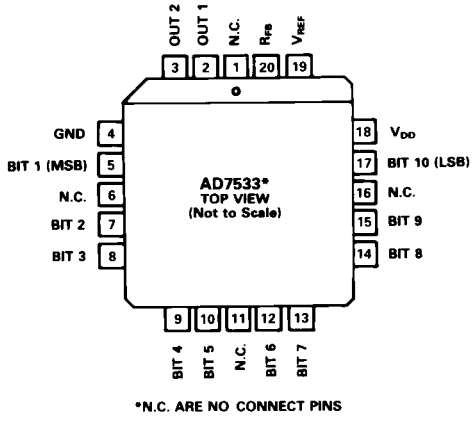
PIN CONFIGURATIONS



DIP



LCCC



PLCC

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

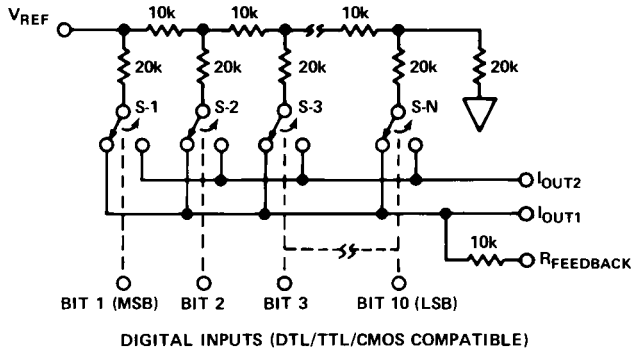


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20Ω, switch 2 for 40Ω, and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

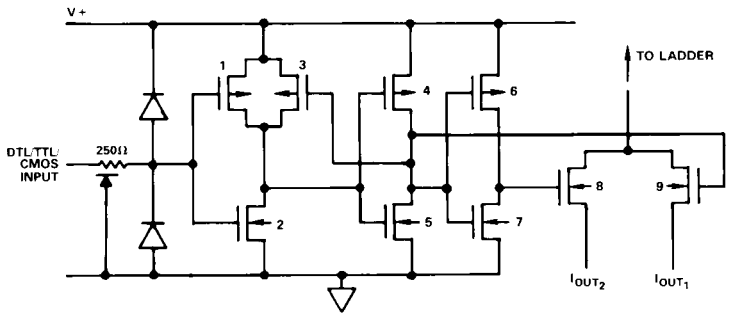


Figure 2. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 100pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 35pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

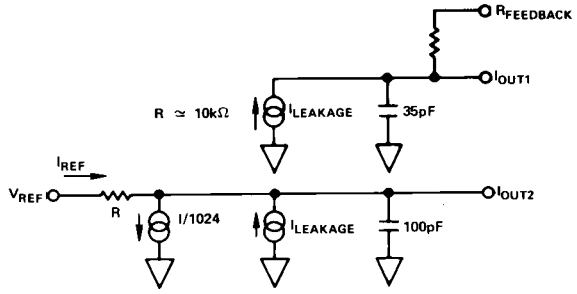


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

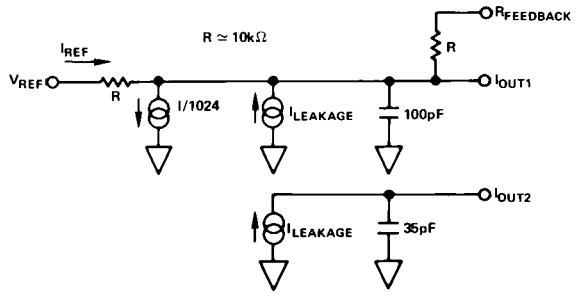


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right)=\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right)=0$

NOTE:
1. Nominal LSB magnitude for the circuit of Figure 5 is given by $LSB = V_{REF}\left(\frac{1}{1024}\right)$

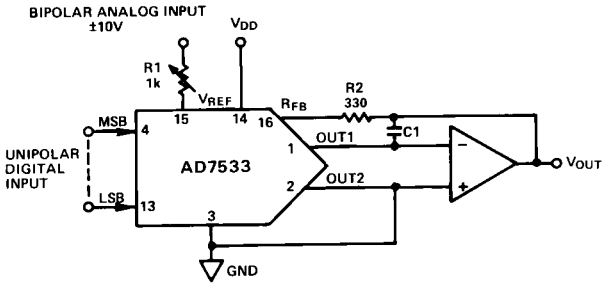
Table I. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{511}{512}\right)$
1 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{512}\right)$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{512}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{511}{512}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{512}\right)$

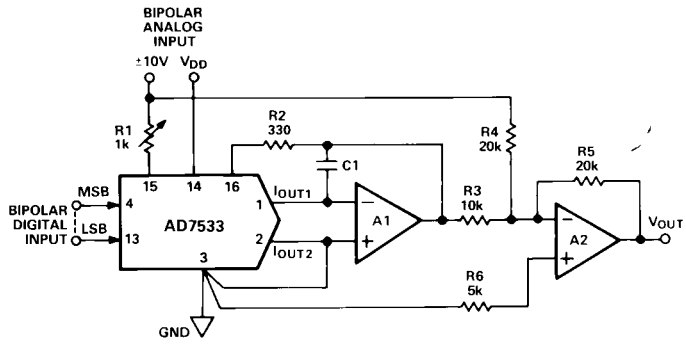
NOTE
1. Nominal LSB magnitude for the circuit of Figure 6 is given by $LSB = V_{REF}\left(\frac{1}{512}\right)$

Table II. Bipolar (Offset Binary) Code Table



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

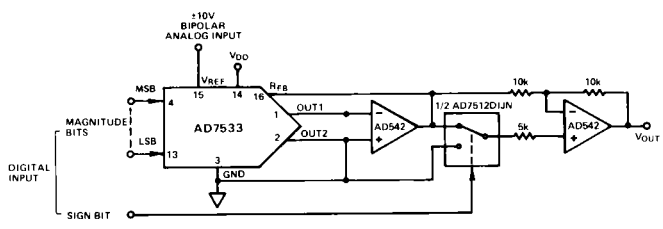


NOTES
1. R3, R4 AND R5 SELECTED FOR MATCHING AND TRACKING.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. C1 PHASE COMPENSATION (5-15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.

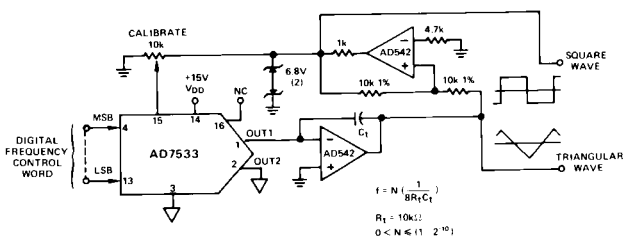
Figure 6. Bipolar Operation (4-Quadrant Multiplication)

APPLICATIONS

10-BIT AND SIGN MULTIPLYING DAC

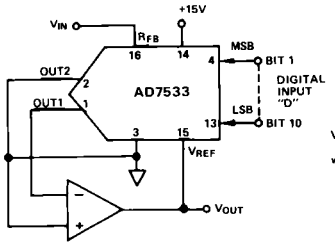


PROGRAMMABLE FUNCTION GENERATOR



APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



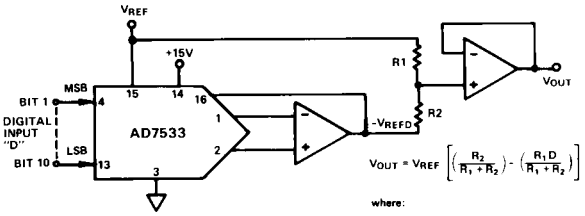
$$V_{OUT} = \frac{-V_{IN}}{D}$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$0 < D \leq \frac{1023}{1024}$$

MODIFIED SCALE FACTOR AND OFFSET



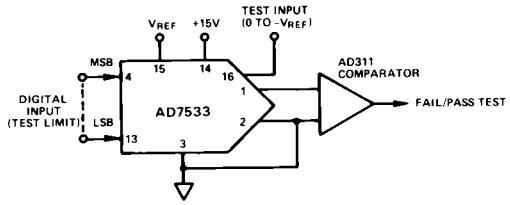
$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1+R_2}\right) - \left(\frac{R_1 D}{R_1+R_2}\right)\right]$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$\left(0 \leq D \leq \frac{1023}{1024}\right)$$

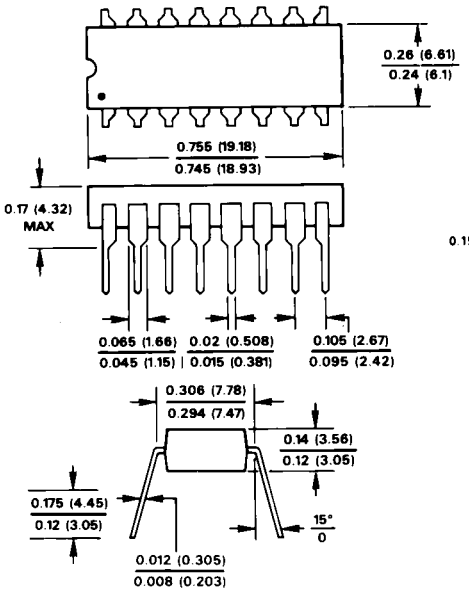
DIGITALLY PROGRAMMABLE LIMIT DETECTOR



OUTLINE DIMENSIONS

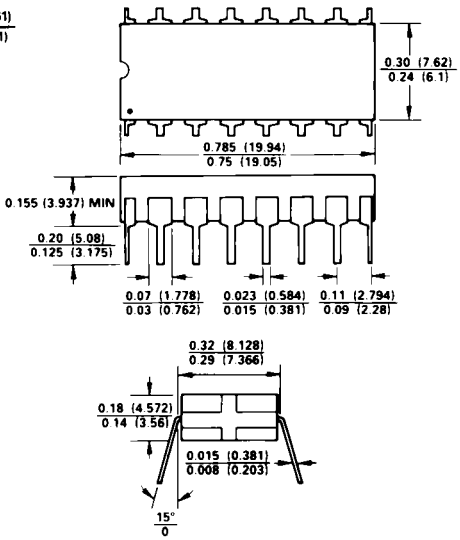
Dimensions shown in inches and (mm).

16-PIN PLASTIC DIP (SUFFIX N)



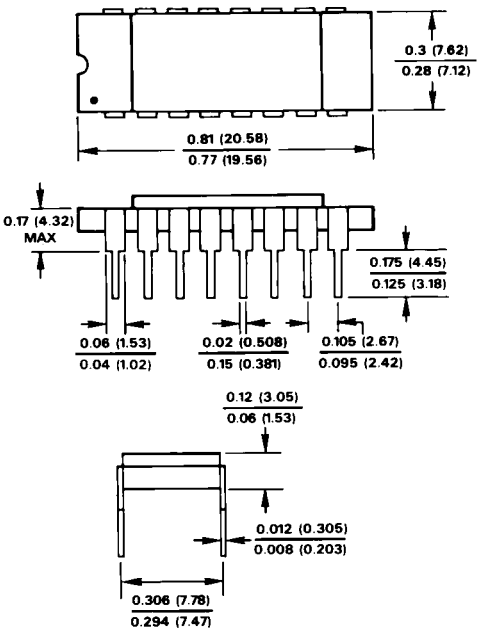
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16-PIN CERDIP (SUFFIX Q)



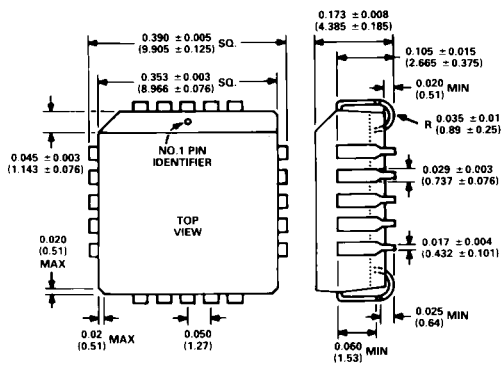
NOTES
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16-PIN CERAMIC DIP (SUFFIX D)

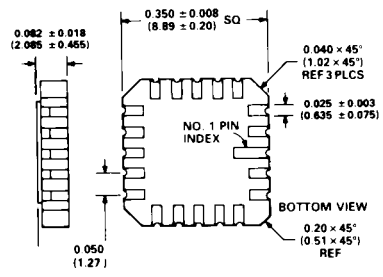


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED
IN ACCORDANCE WITH MIL-M38510 REQUIREMENTS

20-TERMINAL PLASTIC LEADED CHIP CARRIER (SUFFIX P)



20-TERMINAL LEADLESS CHIP CARRIER (SUFFIX E)



10-Montage pratique CNA unipolaire et CNA bipolaire

☐ présentation du CNA AD 7533

La place importante de ce CNA sur le marché actuel nécessite naturellement une étude approfondie de cette famille. Cette étude sera menée avec un exemple concret pour mieux comprendre les divers problèmes technologiques et les solutions apportées par l'électronique moderne. La description se rapporte au modèle AD 7533 de Analog Devices.

Description du CNA 7533 de Analog Devices à 10 bits (voir figure 17).

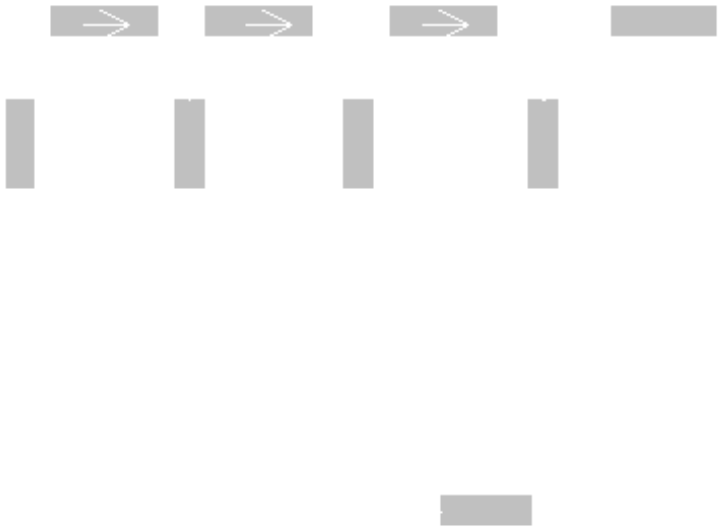


Figure 17 : Schéma du CNA AD 7533

Le CNA AD 7533 est un convertisseur unipolaire ou bipolaire fonctionnant à 10 bits. Les courants fonctions des poids binaires traversent en permanence les résistances 2R du réseau, indépendamment de la position des commutateurs.

Les sorties I_{out1} et I_{out2} sont maintenues aux potentiels des masses virtuelle ou réelle. Les commutateurs aiguillent les courants aux sorties appropriées en fonction des niveaux logiques appliqués. Si la tension de référence est égale 10V, le niveau logique "1" sur le MSB fournit une tension égale à (-0.5 mA).(10 kΩ) = -5 V à la sortie de l'amplificateur. Quand toutes les entrées sont à "1", la tension de sortie sera égale à -9.99 V. Quand toutes les entrées logiques sont à "0", la tension de sortie sera égale à 0 V. Les variations de R_{on} en fonction de la température peuvent transformer le réseau R - 2R en un réseau R - nR avec n suffisamment diffèrent de 2 pour changer le caractère binaire du réseau et rendre le convertisseur non monotone. La technologie CMOS utilisée dans la réalisation des commutateurs de cette famille de CNA permet de contrôler la valeur de la résistance R_{on}. Ainsi, le commutateur correspondant au premier bit est conçu pour réaliser R_{on} = 20 Ω, pour le second bit R_{on} = 40 Ω etc..., et cela jusqu'au $6^{ème}$ bit ou Ron = 640Ω. Ainsi, les tensions aux bornes des ces résistances R_{on}, des dix premiers bits les plus significatifs sont toutes égales à 10 mV. Cette tension en série avec la tension de référence, elle n'affecte pas la linéarité du convertisseur.

1- Conversion unipolaire

Comme la tension de sortie du convertisseur est de même signe que celle de la tension de référence alors il s'agit d'un convertisseur unipolaire et la tension de sortie est égale à:

Vout = - N. Eref, N étant la valeur binaire du code numérique d'entrée.

Les valeurs des a_i sont déterminées par l'état respectif des bits du code numérique N

2- Conversion bipolaire

Le CNA fonctionne en multiplieur à quatre quadrants car les deux entrées analogiques (Eref) et numérique (N) peuvent être simultanément bipolaires figure 19. On remarque que le courant $Iout_2$ est le complément de $Iout_1$. La tension de sortie analogique V0 est donnée par V0 = -R.(Iout1-Iout2).

Calcul de Vo :

$$I_a = I_{out1} + I_{out2} + I_0 \qquad \text{avec} \qquad I_0 = \frac{Eref}{R} \cdot \frac{1}{1024}$$

$$I_{out1} = \frac{Eref}{2^n R} .N$$

En négligeant le terme $\frac{Eref}{R} \cdot \frac{1}{1024}$, qui correspond au LSB, on a alors :

$$I_{out1} + I_{out2} = \frac{Eref}{R}$$

$$I_{out2} = \frac{Eref}{R} - I_{out1}$$

$$I_{out1} - I_{out2} = 2\,I_{out1} - \frac{Eref}{R} = 2\,\frac{Eref\,.N}{2^n R} - \frac{Eref}{R} = \frac{Eref}{2^n R}.(2N - 2^n)$$

$$V_0 = -RI_0 = -\frac{Eref}{2^n}.(2N - 2^n)$$

Le tableau ci-dessous donne les valeurs de tension de sortie du CNA dans le cas unipolaire et bipolaire.

Conversionunipolaire		**Conversionbipolaire**	
Entrées numériques	***Sorties analogiques***	***Entrées numériques***	***Sorties analogiques***
MSB LSB		MSB LSB	
1111111111	-Eref (1023/1024)	1111111111	-Eref (511/512)
1000000001	-Eref (513/1024)	1000000001	-Eref (1/512)
1000000000	-Eref (512/1024)	1000000000	0

0111111111	-Eref (511/1024)	0111111111	Eref (1/512)
0000000001	-Eref (1/1024)	0000000001	Eref (511/512)
0000000000	-Eref (0/1024)	0000000000	Eref (512/512)

La conversion bipolaire fournit une échelle analogique doublée mais la résolution est réduite de moitié. Pour obtenir $V_0 = 0$, avec le code numérique d'entrée égale à 1000000 (code binaire décalé), on

ajoute une résistance de 10.24MΩ pour compenser le décalage de (1/1024) entre $Iout_1$ et $Iout_2$ inhérent à cette technique.

Figure 19 : Montage pratique pour la conversion bipolaire

Comparaison des différentes technologies

(CNA)			
Type	**Vitesse**	**Erreur**	**Résolution**
Résistances Pondérées	Elevée (1µs à 10µs) (Sortie en tension 1µs à 10µs) (Sortie en courant 50 ns à 1µs)	Elevée	Faible (quelques bits)
R-2R		Faible	Elevée

Exemple de Convertisseur Numérique/Analogique

Convertisseur Numérique / Analogique

Référence	*Nombre de bits*	*Tc(µs)*	*linéarité*	*Sortie*	*constructeur*	*prix HT*
AD7523	8	0,15	+/- 0,5 q	Courant	Intersil	35
DAC08CN	8	0,15	+/- 0,5 q	Courant	Analog Devices	28
AD557	8	1,5	+/- 0,5 q	Tension	National Semiconducteur	67

AD7533	10	0,6	+/- 2 q	Courant	Analog Devices	48
AD7390	10	75	+/- 1,6 q	Tension	Analog Devices	72
AD668	12	0,05	+/- 0.5 q	Courant	Analog Devices	499

ADDAC80	12	5	+/- 0,5 q	Tension	Analog Devices	140
DAC8043	12	1	+/- 1 q	Courant	Burr Brown	125
AD7840	14	2	+/- 2 q	Tension	Analog Devices	167

DAC712	16	6	+/- 4 q	Tension	Burr Brown	171

Simulation

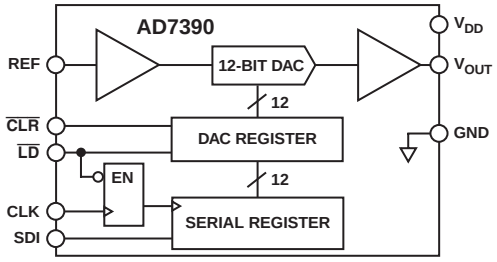
3 V Serial-Input Micropower 10-Bit and 12-Bit DACs

AD7390/AD7391

FEATURES
Micropower—100 μA
Single-Supply—2.7 V to 5.5 V Operation
Compact 1.75 mm Height SO-8 Package and 1.1 mm Height TSSOP-8 Package
AD7390—12-Bit Resolution
AD7391—10-Bit Resolution
SPI and QSPI Serial Interface Compatible with Schmitt Trigger Inputs

APPLICATIONS
Automotive 0.5 V to 4.5 V Output Span Voltage
Portable Communications
Digitally Controlled Calibration

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7390/AD7391 family of 10-bit and 12-bit voltage-output digital-to-analog converters is designed to operate from a single 3 V supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease-of-use in single-supply 3 V systems. Operation is guaranteed over the supply voltage range of 2.7 V to 5.5 V consuming less than 100 μA making this device ideal for battery operated applications.

The full-scale voltage output is determined by the external reference input voltage applied. The rail-to-rail REF_{IN} to DAC_{OUT} allows for a full-scale voltage set equal to the positive supply V_{DD} or any value in between.

A doubled-buffered serial-data interface offers high-speed, 3-wire, SPI and microcontroller compatible inputs using data in (SDI), clock (CLK) and load strobe ($\overline{LD}$) pins. Additionally, a $\overline{CLR}$ input sets the output to zero scale at power on or upon user demand.

Both parts are offered in the same pinout to allow users to select the amount of resolution appropriate for their application without circuit card redesign.

The AD7390/AD7391 are specified over the extended industrial (−40°C to +85°C) temperature range. The AD7391AR is specified for the −40°C to +125°C automotive temperature range. The AD7390/AD7391s are available in plastic DIP, and low profile 1.75 mm height SO-8 surface mount packages. The AD7391ARU is available for ultracompact applications in a thin 1.1 mm TSSOP-8 package.

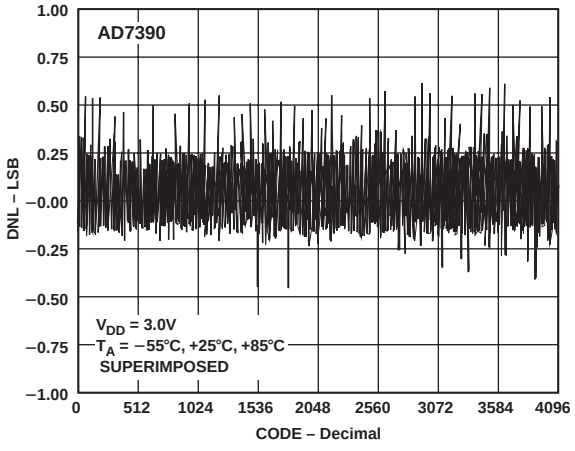


Figure 1. Differential Nonlinearity Error vs. Code

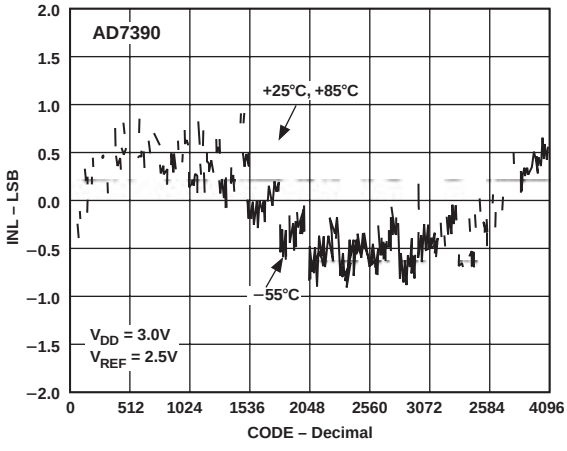


Figure 2. INL Error vs. Code and Temperature

REV. A

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Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD7390/AD7391–SPECIFICATIONS

AD7390 ELECTRICAL CHARACTERISTICS (@ $V_{REF\ IN}$ = 2.5 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL	T_A = 25°C	±1.6	±1.6	LSB max
	INL	T_A = −40°C, +85°C	±2.0	±2	LSB max
Differential Nonlinearity[2]	DNL	T_A = 25°C, Monotonic	±0.9	±0.9	LSB max
	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	4.0	4.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = 25°C, 85°C, Data = FFF_H	±8	±8	mV max
	V_{FSE}	T_A = −40°C, Data = FFF_H	±20	±20	mV max
Full-Scale Tempco[3]	TCV_{FS}		16	16	ppm/°C typ
REFERENCE INPUT					
$V_{REF\ IN}$ Range	V_{REF}		$0/V_{DD}$	$0/V_{DD}$	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} − 0.6	V_{DD} − 0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Clock Width High	t_{CH}		50	30	ns min
Clock Width Low	t_{CL}		50	30	ns min
Load Pulsewidth	t_{LDW}		30	20	ns min
Data Setup	t_{DS}		10	10	ns min
Data Hold	t_{DH}		30	15	ns min
Clear Pulsewidth	t_{CLRW}		15	15	ns min
Load Setup	t_{LD1}		30	15	ns min
Load Hold	t_{LD2}		40	20	ns min
AC CHARACTERISTICS[6]					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	0.05	0.05	V/µs typ
Settling Time	t_S	To ±0.1% of Full Scale	70	60	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nVs typ
Digital Feedthrough	Q		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} + 1 V p-p, Data = 000_H, f = 100 kHz	−63	−63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load, T_A = 25°C	55	55	µA typ
	I_{DD}	V_{IL} = 0 V, No Load	100	100	µA max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	300	500	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES

[1]One LSB = V_{REF}/4096 V for the 12-bit AD7390.

[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]Typicals represent average readings measured at 25°C.

[5]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

AD7391 ELECTRICAL CHARACTERISTICS (@ $V_{REF\ IN}$ = 2.5 V, −40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL	T_A = 25°C	±1.75	±1.75	LSB max
	INL	T_A = −40°C, +85°C, +125°C	±2.0	±2.0	LSB max
	INL	T_A = −55°C, S Grade		±3	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±0.9	±0.9	LSB max
	DNL	T_A = −55°C, S Grade		±2	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	9.0	9.0	mV max
	V_{ZSE}	T_A = −55°C, S Grade		20	mV max
Full-Scale Error	V_{FSE}	T_A = 25°C, 85°C, 125°C, Data = $3FF_H$	±32	±32	mV max
	V_{FSE}	T_A = −55°C, S Grade		±55	mV max
Full-Scale Tempco[3]	TCV_{FS}		16	16	ppm/°C typ
	TCV_{FS}	T_A = −55°C, S Grade		32	ppm/°C typ
REFERENCE INPUT					
$V_{REF\ IN}$ Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} − 0.6	V_{DD} − 0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Clock Width High	t_{CH}		50	30	ns
Clock Width Low	t_{CL}		50	30	ns
Load Pulsewidth	t_{LDW}		30	20	ns
Data Setup	t_{DS}		10	10	ns
Data Hold	t_{DH}		30	15	ns
Clear Pulsewidth	t_{CLRW}		15	15	ns
Load Setup	t_{LD1}		30	15	ns
Load Hold	t_{LD2}		40	20	ns
AC CHARACTERISTICS[6]					
Output Slew Rate	SR	Data = 000_H to $3FF_H$ to 000_H	0.05	0.05	V/µs typ
Settling Time	t_S	To ±0.1% of Full Scale	70	60	µs typ
	t_S	T_A = –55°C, S Grade		100	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nVs typ
Digital Feedthrough	Q		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} +1 V p-p, Data = 000_H, f = 100 kHz	−63	−63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load, T_A = 25°C	55	55	µA typ
	I_{DD}	V_{IL} = 0 V, No Load	100	100	µA max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	300	500	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES
[1]One LSB = V_{REF}/1024 V for the 10-bit AD7391.
[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
[3]These parameters are guaranteed by design and not subject to production testing.
[4]Typicals represent average readings measured at 25°C.
[5]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.6 V.
[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND ..... −0.3 V, +8 V
V_{REF} to GND ..... +0.3 V, V_{DD} + 0.3 V
Logic Inputs to GND ..... −0.3 V, +8 V
V_{OUT} to GND ..... −0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND ..... 50 mA
Package Power Dissipation ..... $(T_{J\,MAX} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
8-Lead Plastic DIP Package (N-8) ..... 103°C/W
8-Lead SOIC Package (SO-8) ..... 158°C/W
TSSOP-8 Package (RU-8) ..... 240°C/W
Maximum Junction Temperature ($T_{J\,MAX}$) ..... 150°C
Operating Temperature Range ..... −40°C to +85°C
AD7391AR ..... −40°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.

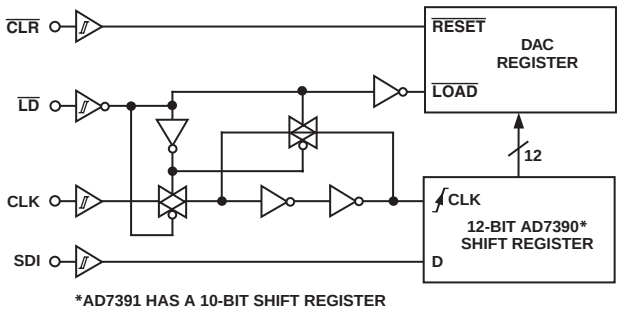
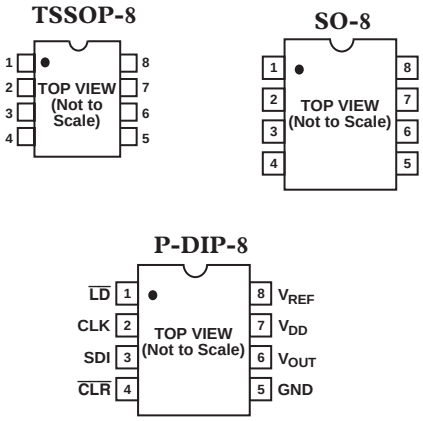


Figure 3. Digital Control Logic

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin No.	Name	Function
1	$\overline{LD}$	Load Strobe. Transfers shift register data to DAC register while active low. See truth table for operation.
2	CLK	Clock Input. Positive edge clocks data into shift register.
3	SDI	Serial Data Input. Data loads directly into the shift register.
4	$\overline{CLR}$	Resets DAC register to zero condition. Active low input.
5	GND	Analog and Digital Ground.
6	V_{OUT}	DAC Voltage Output. Full-scale output 1 LSB less than reference input voltage REF.
7	V_{DD}	Positive Power Supply Input. Specified range of operation 2.7 V to 5.5 V.
8	V_{REF}	DAC Reference Input Pin. Establishes DAC full-scale voltage.

ORDERING GUIDE[1]

Model	Resolution	Temperature Range	Package Description	Package Option	Top Mark[2]	Number of Devices Per Container
AD7390AN	12	−40°C to +85°C	8-Lead P-DIP	N-8	AD7390[2]	50
AD7390AR	12	−40°C to +85°C	8-Lead SOIC	SO-8	AD7390[3]	196
AD7390AR-REEL7	12	−40°C to +85°C	8-Lead SOIC	SO-8	AD7390[3]	1000
AD7391AN	10	−40°C to +85°C	8-Lead P-DIP	N-8	AD7391[2]	50
AD7391AR	10	−40°C to +125°C	8-Lead SOIC	SO-8	AD7391[3]	196
AD7391SR	10	−55°C to +125°C	8-Lead SOIC	SO-8	AD7391[3]	39
AD7391ARU-REEL	10	−40°C to +85°C	TSSOP-8	RU-8	AD7391A[4]	2500

NOTES
[1]The AD7390 contains 588 transistors. The die size measures 70 mm × 68 mm.
[2]Line 1 contains ADI logo symbol and part number. Line 2 contains grade and date code YWW. Line 3 contains the letter G plus the 4-digit lot number.
[3]Line 1 contains part number. Line 2 contains grade and date code YWW. Line 3 contains the letter G plus the 4-digit lot number and the ADI logo symbol.
[4]Line 1 contains the date code YWW. Line 2 contains the 4-digit part number plus grade.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7390/AD7391 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

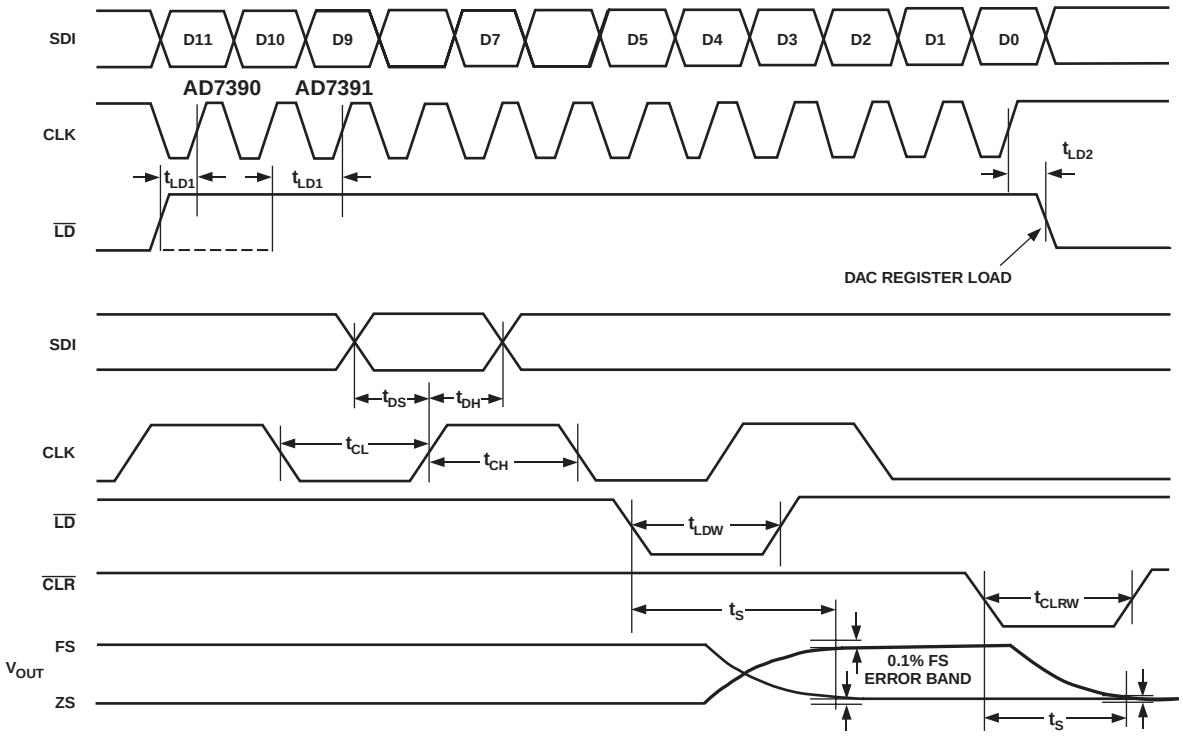


Figure 4. Timing Diagram

Table I. Control-Logic Truth Table

CLK	$\overline{CLR}$	$\overline{LD}$	Serial Shift Register Function	DAC Register Function
↑	H	H	Shift-Register-Data Advanced One-Bit	Latched
X	H	L	Disables	Updated with Current Shift Register Contents
X	L	X	No Effect	Loaded with all Zeros
X	↑	H	No Effect	Latched with all Zeros
X	↑	L	Disabled	Previous SR Contents Loaded (Avoid usage of $\overline{CLR}$ when $\overline{LD}$ is logic low, since SR data could be corrupted if a clock edge takes place, while $\overline{CLR}$ returns high.)

↑ = Positive logic transition.
X = Don't care.

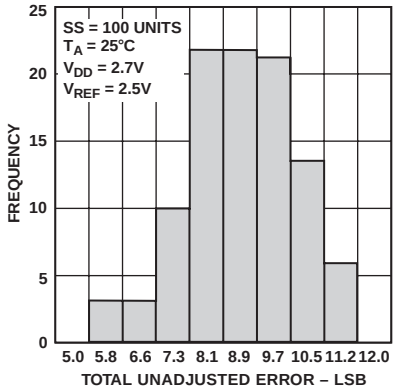
Table II. AD7390 Serial Input Register Data Format, Data is Loaded in the MSB-First Format

	MSB											LSB
	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
AD7390	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

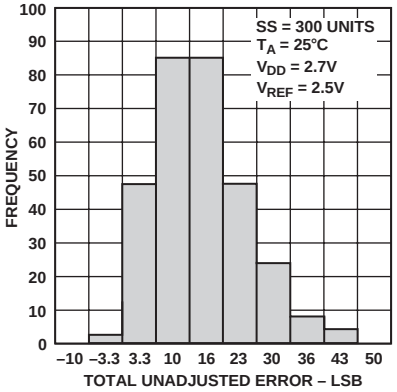
Table III. AD7391 Serial Input Register Data Format, Data is Loaded in the MSB-First Format

	MSB									LSB
	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
AD7391	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

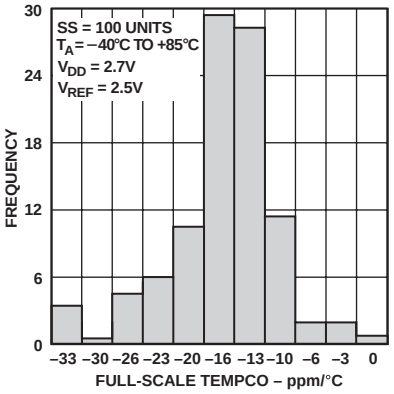
AD7390/AD7391–Typical Performance Characteristics



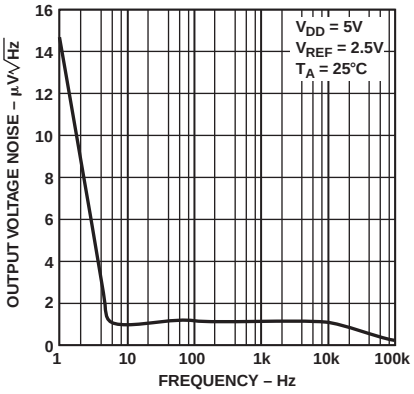
TPC 1. AD7390 Total Unadjusted Error Histogram



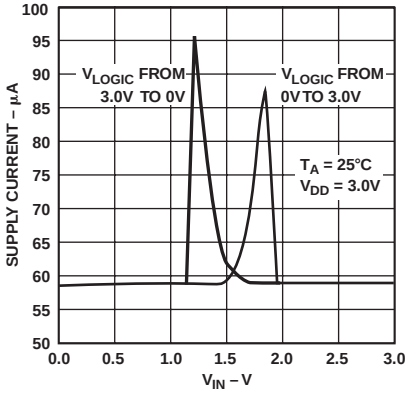
TPC 2. AD7391 Total Unadjusted Error Histogram



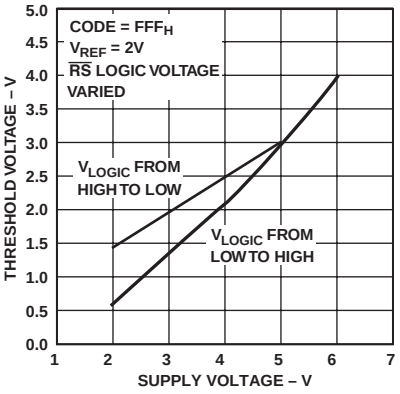
TPC 3. AD7391 Full-Scale Output Tempco Histogram



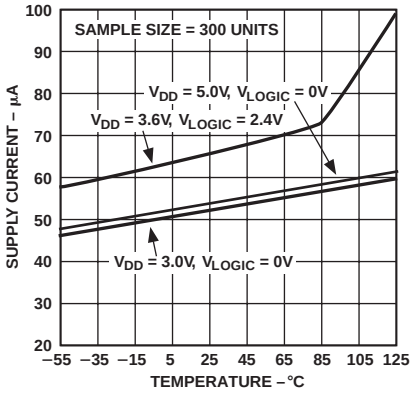
TPC 4. AD7390 Voltage Noise Density vs. Frequency



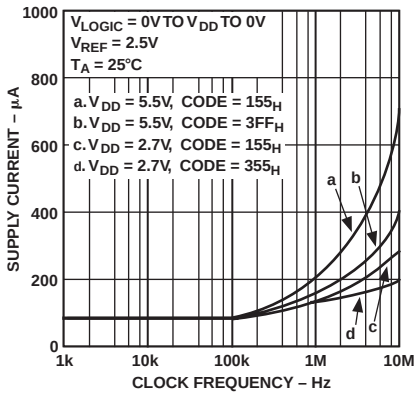
TPC 5. AD7390 Supply Current vs. Logic Input Voltage



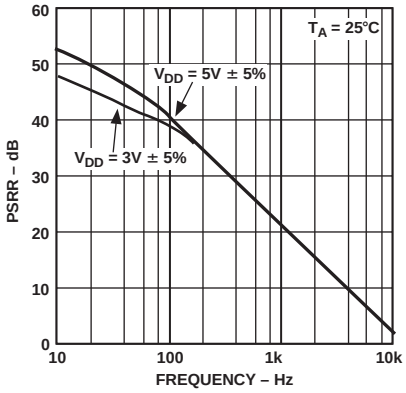
TPC 6. AD7390 Logic Threshold vs. Supply Voltage



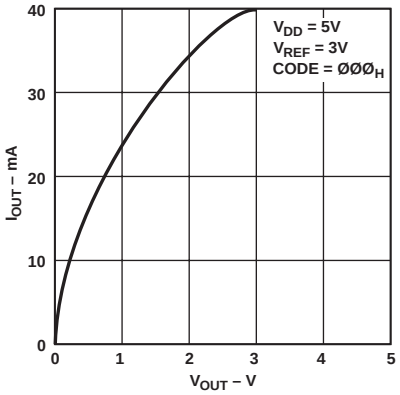
TPC 7. AD7390 Supply Current vs. Temperature



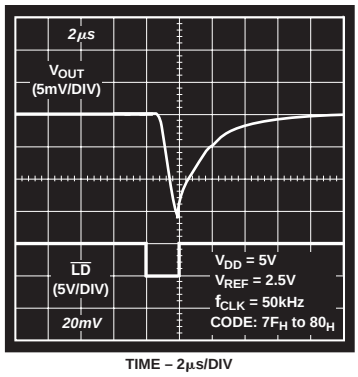
TPC 8. AD7391 Supply Current vs. Clock Frequency



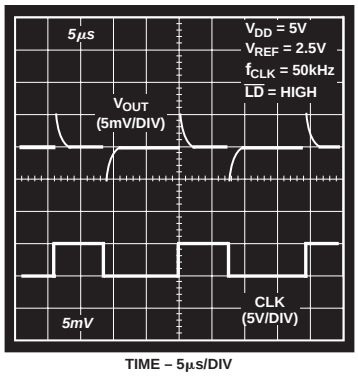
TPC 9. Power Supply Rejection vs. Frequency



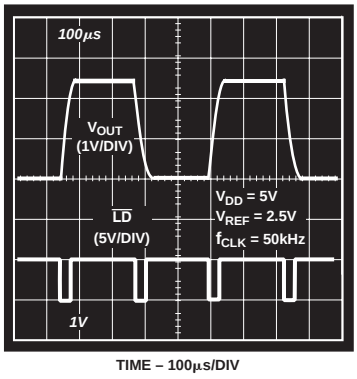
TPC 10. I_{OUT} at Zero Scale vs. V_{OUT}



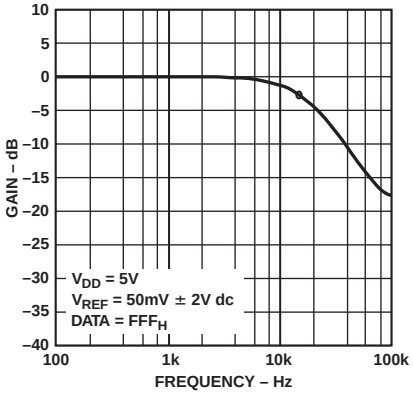
TPC 11. AD7390 Midscale Transition Performance



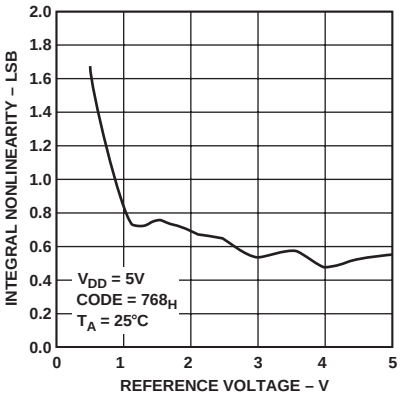
TPC 12. Digital Feedthrough



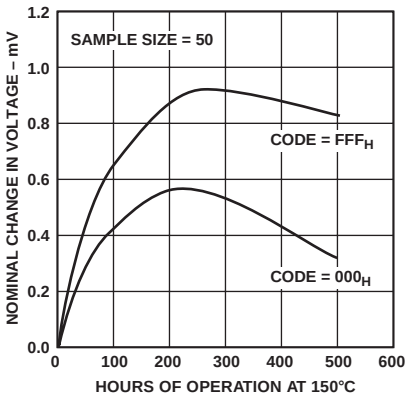
TPC 13. AD7390 Large Signal Settling Time



TPC 14. AD7390 Gain vs. Frequency



TPC 15. AD7390 INL Error vs. Reference Voltage



TPC 16. AD7390 Long-Term Drift Accelerated by Burn-In

OPERATION

The AD7390 and AD7391 are a set of pin compatible, 12-bit/10-bit digital-to-analog converters. These single-supply operation devices consume less than 100 microamps of current while operating from power supplies in the 2.7 V to 5.5 V range making them ideal for battery operated applications. They contain a voltage-switched, 12-bit/10-bit, laser-trimmed digital-to-analog converter, rail-to-rail output op amps, serial-input register, and a DAC register. The external reference input has constant input resistance independent of the digital code setting of the DAC. In addition, the reference input can be tied to the same supply voltage as V_{DD} resulting in a maximum output voltage span of 0 to V_{DD}. The SPI compatible, serial-data interface consists of a serial data input (SDI), clock (CLK), and load ($\overline{LD}$) pins. A $\overline{CLR}$ pin is available to reset the DAC register to zero-scale. This function is useful for power-on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The voltage switched R-2R DAC generates an output voltage dependent on the external reference voltage connected to the V_{REF} pin according to the following equation:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \quad (1)$$

where D is the decimal data word loaded into the DAC register, and N is the number of bits of DAC resolution. In the case of the 10-bit AD7391 using a 2.5 V reference, Equation 1 simplifies to:

$$V_{OUT} = 2.5 \times \frac{D}{1024} \quad (2)$$

Using Equation 2 the nominal midscale voltage at V_{OUT} is 1.25 V for D = 512; full-scale voltage is 2.497 V. The LSB step size is = 2.5 × 1/1024 = 0.0024 V.

For the 12-bit AD7390 operating from a 5.0 V reference Equation 1 becomes:

$$V_{OUT} = 5.0 \times \frac{D}{4096} \quad (3)$$

Using Equation 3 the AD7390 provides a nominal midscale voltage of 2.5 V for D = 2048, and a full-scale output of 4.998 V. The LSB step size is = 5.0 × 1/4096 = 0.0012 V.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. The op amp has a 60 µs typical settling time to 0.1% of full scale. There are slight differences in settling time for negative slewing signals versus positive. Also, negative transition settling time to within the last 6 LSBs of zero volts has an extended settling time. The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 5 shows an equivalent output schematic of the rail-to-rail amplifier with its N-channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P-channel pull-up device that can source current to GND terminated loads.

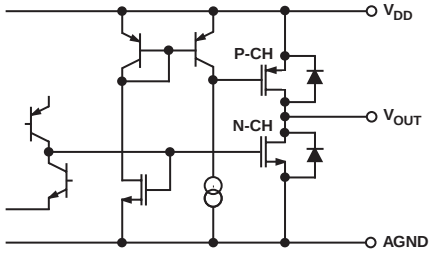


Figure 5. Equivalent Analog Output Circuit

The rail-to-rail output stage provides ±1 mA of output current. The N-channel output pull-down MOSFET shown in Figure 5 has a 35 Ω ON resistance, which sets the sink current capability near ground. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 100 pF capacitive load driving capability.

REFERENCE INPUT

The reference input terminal has a constant input-resistance independent of digital code which results in reduced glitches on the external reference voltage source. The high 2 MΩ input-resistance minimizes power dissipation within the AD7390/AD7391 D/A converters. The V_{REF} input accepts input voltages ranging from ground to the positive-supply voltage V_{DD}. One of the simplest applications which saves an external reference voltage source is connection of the V_{REF} terminal to the positive V_{DD} supply. This connection results in a rail-to-rail voltage output span maximizing the programmed range. The reference input will accept ac signals as long as they are kept within the supply voltage range, $0 < V_{REF\,IN} < V_{DD}$. The reference bandwidth and integral nonlinearity error performance are plotted in the typical performance section (see TPCs 14 and 15). The ratiometric reference feature makes the AD7390/AD7391 an ideal companion to ratiometric analog-to-digital converters such as the AD7896.

POWER SUPPLY

The very low power consumption of the AD7390/AD7391 is a direct result of a circuit design optimizing the use of a CBCMOS process. By using the low power characteristics of CMOS for the logic, and the low noise, tight-matching of the complementary bipolar transistors, excellent analog accuracy is achieved. One advantage of the rail-to-rail output amplifiers used in the AD7390/AD7391 is the wide range of usable supply voltage. The part is fully specified and tested for operation from 2.7 V to 5.5 V.

POWER SUPPLY BYPASSING AND GROUNDING

Precision analog products, such as the AD7390/AD7391, require a well filtered power source. Since the AD7390/AD7391 operates from a single 3 V to 5 V supply, it seems convenient to simply tap into the digital logic power supply. Unfortunately, the logic supply is often a switch-mode design, which generates noise in the 20 kHz to 1 MHz range. In addition, fast logic gates can generate glitches hundred of millivolts in amplitude due to wiring resistance and inductance. The power supply noise generated thereby means that special care must be taken to assure that the inherent precision of the DAC is maintained. Good engineering judgment should be exercised when addressing the power supply grounding and bypassing of the AD7390.

The AD7390 should be powered directly from the system power supply. This arrangement, shown in Figure 6, employs an LC filter and separate power and ground connections to isolate the analog section from the logic switching transients.

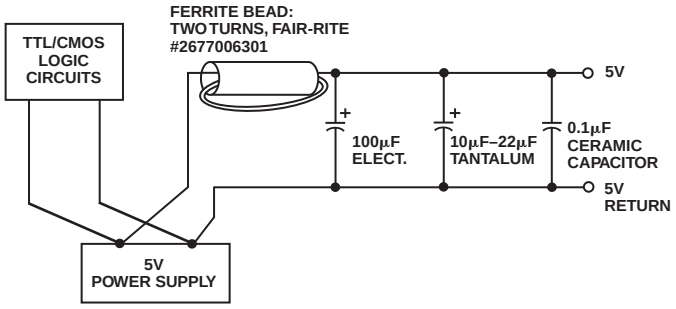


Figure 6. Use Separate Traces to Reduce Power Supply Noise

Whether or not a separate power supply trace is available, however, generous supply bypassing will reduce supply-line induced errors. Local supply bypassing consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic capacitor is recommended in all applications (Figure 7).

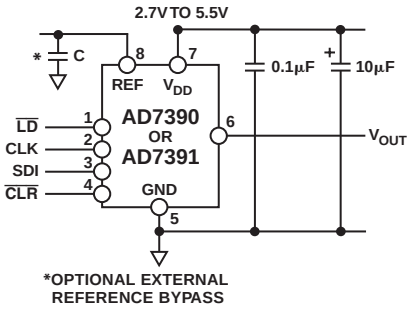


Figure 7. Recommended Supply Bypassing

INPUT LOGIC LEVELS

All digital inputs are protected with a Zener-type ESD protection structure (Figure 8) that allows logic input voltages to exceed the V_{DD} supply voltage. This feature can be useful if the user is driving one or more of the digital inputs with a 5 V CMOS logic input-voltage level while operating the AD7390/AD7391 on a 3 V power supply. If this mode of interface is used, make sure that the V_{OL} of the 5 V CMOS meets the V_{IL} input requirement of the AD7390/AD7391 operating at 3 V. See TPC 6 for a graph for digital logic input threshold versus operating V_{DD} supply voltage.

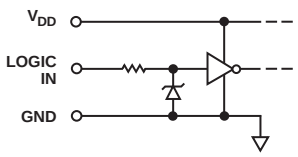


Figure 8. Equivalent Digital Input ESD Protection

In order to minimize power dissipation from input-logic levels that are near the V_{IH} and V_{IL} logic input voltage specifications, a Schmitt trigger design was used that minimizes the input-buffer current consumption compared to traditional CMOS input stages. TPC 5 shows a plot of incremental input voltage versus supply current showing that negligible current consumption takes place when logic levels are in their quiescent state. The normal crossover current still occurs during logic transitions. A secondary advantage of this Schmitt trigger is the prevention of false triggers that would occur with slow moving logic transitions when a standard CMOS logic interface or opto isolators are used. The logic inputs SDI, CLK, $\overline{LD}$, $\overline{CLR}$ all contain the Schmitt trigger circuits.

DIGITAL INTERFACE

The AD7390/AD7391 have a double-buffered serial data input. The serial-input register is separate from the DAC register, which allows preloading of a new data value into the serial register without disturbing the present DAC values. A functional block diagram of the digital section is shown in Figure 4, while Table I contains the truth table for the control logic inputs. Three pins control the serial data input. Data at the Serial Data Input (SDI) is clocked into the shift register on the rising edge of CLK. Data is entered in MSB-first format. Twelve clock pulses are required to load the 12-bit AD7390 DAC value. If additional bits are clocked into the shift register, for example when a microcontroller sends two 8-bit bytes, the MSBs are ignored (Figure 9). The CLK pin is only enabled when Load ($\overline{LD}$) is high. The lower resolution 10-bit AD7391 contains a 10-bit shift register. The AD7391 is also loaded MSB first with 10 bits of data. Again if additional bits are clocked into the shift register, only the last 10 bits clocked in are used.

The Load pin ($\overline{LD}$) controls the flow of data from the shift register to the DAC register. After a new value is clocked into the serial-input register, it will be transferred to the DAC register by the negative transition of the Load pin ($\overline{LD}$).

BYTE 1								BYTE 0							
MSB							LSB	MSB							LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D11–D0: 12-BIT AD7390 DAC VALUE; D9–D0: 10-BIT AD7391 DAC VALUE
X = DON'T CARE
THE MSB OF BYTE 1 IS THE FIRST BIT THAT IS LOADED INTO THE DAC

Figure 9. Typical AD7390-Microprocessor Serial Data Input Forms

RESET ($\overline{CLR}$) PIN

Forcing the $\overline{CLR}$ pin low will set the DAC register to all zeros and the DAC output voltage will be zero volts. The reset function is useful for setting the DAC outputs to zero at power-up or after a power supply interruption. Test systems and motor controllers are two of many applications which benefit from powering up to a known state. The external reset pulse can be generated by the microprocessor's power-on RESET signal, by an output from the microprocessor, or by an external resistor and capacitor. $\overline{CLR}$ has a Schmitt trigger input which results in a clean reset function when using external resistor/capacitor generated pulses. The $\overline{CLR}$ input overrides other logic inputs, specifically $\overline{LD}$. However, $\overline{LD}$ should be set high before $\overline{CLR}$ goes high. If $\overline{CLR}$ is kept low, then the contents of the shift register will be transferred to the DAC register as soon as $\overline{CLR}$ returns high. See the Control-Logic Truth Table I.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7390. As shown in Figure 10, the AD7390 has been designed to drive loads as low as 5 kΩ in parallel with 100 pF. The code table for this operation is shown in Table IV.

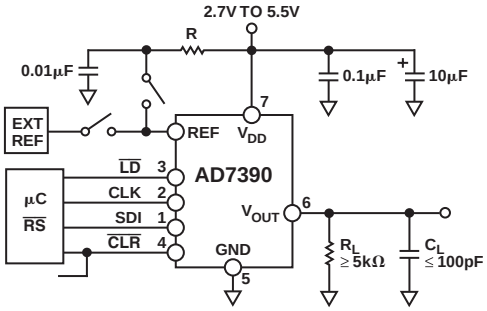


Figure 10. AD7390 Unipolar Output Operation

Table IV. AD7390 Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Output Voltage (V) V_{REF} = 2.5 V
FFF	4095	2.4994
801	2049	1.2506
800	2048	1.2500
7FF	2047	1.2494
000	0	0

The circuit can be configured with an external reference plus power supply, or powered from a single dedicated regulator or reference, depending on the application performance requirements.

BIPOLAR OUTPUT OPERATION

Although the AD7391 has been designed for single-supply operation, the output can be easily configured for bipolar operation. A typical circuit is shown in Figure 11. This circuit uses a clean regulated 5 V supply for power, which also provides the circuit's reference voltage. Since the AD7391 output span swings from ground to very near 5 V, it is necessary to choose an external amplifier with a common-mode input voltage range that extends to its positive supply rail. The micropower consumption OP196 has been designed just for this purpose and results in only 50 microamps of maximum current consumption. Connection of the equally valued 470 kΩ resistors results in a differential amplifier mode of operation with a voltage gain of two, which results in a circuit output span of ten volts, that is, 25 V to 15 V. As the DAC is programmed with zero-code 000_H to midscale 200_H to full-scale $3FF_H$, the circuit output voltage V_O is set at 25 V, 0 V and 15 V (minus 1 LSB). The output voltage V_O is coded in offset binary according to Equation 4.

$$V_O = \left[\left(\frac{D}{512}\right) - 1\right] \times 5 \qquad (4)$$

where *D* is the decimal code loaded in the AD7391 DAC register. Note that the LSB step size is 10/1024 = 10 mV. This circuit has been optimized for micropower consumption including the 470 kΩ gain setting resistors, which should have low temperature coefficients to maintain accuracy and matching (preferably the same material, such as metal film). If better stability is required, the power supply could be substituted with a precision reference voltage such as the low dropout REF195, which can easily supply the circuit's 162 µA of current, and still provide additional power for the load connected to V_O. The micropower REF195 is guaranteed to source 10 mA output drive current, but only consumes 50 µA internally. If higher resolution is required, the AD7390 can be used with the addition of two more bits of data inserted into the software coding, which would result in a 2.5 mV LSB step size. Table V shows examples of nominal output voltages V_O provided by the Bipolar Operation circuit application.

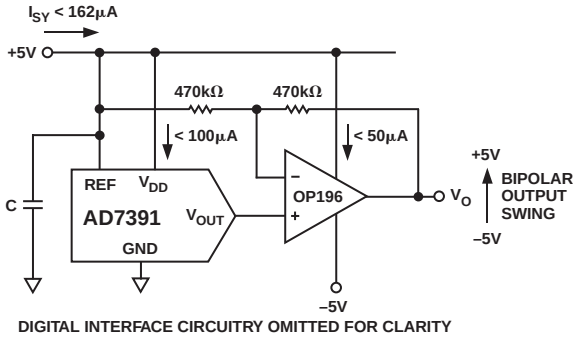


Figure 11. Bipolar Output Operation

Table V. Bipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
3FF	1023	4.9902
201	513	0.0097
200	512	0.0000
1FF	511	–0.0097
000	0	–5.0000

MICROCOMPUTER INTERFACES

The AD7390 serial data input provides an easy interface to a variety of single-chip microcomputers (µCs). Many µCs have a built-in serial data capability which can be used for communicating with the DAC. In cases where no serial port is provided, or it is being used for some other purpose (such as an RS-232 communications interface), the AD7390/AD7391 can easily be addressed in software.

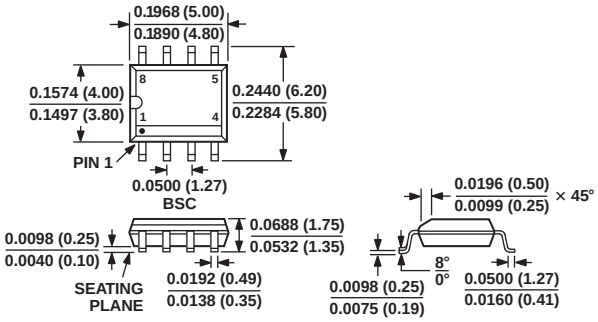
Twelve data bits are required to load a value into the AD7390. If more than 12 bits are transmitted before the load $\overline{LD}$ input goes high, the extra (i.e., the most-significant) bits are ignored. This feature is valuable because most µCs only transmit data in 8-bit increments. Thus, the µC sends 16 bits to the DAC instead of 12 bits. The AD7390 will only respond to the last 12 bits clocked into the SDI input, however, so the serial-data interface is not affected.

Ten data bits are required to load a value into the AD7391. If more than 10 bits are transmitted before load $\overline{LD}$ returns high, the extra bits are ignored.

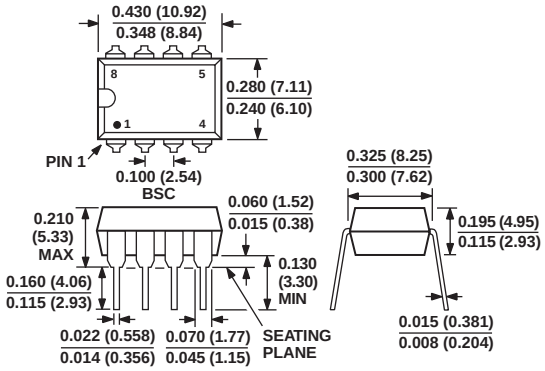
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

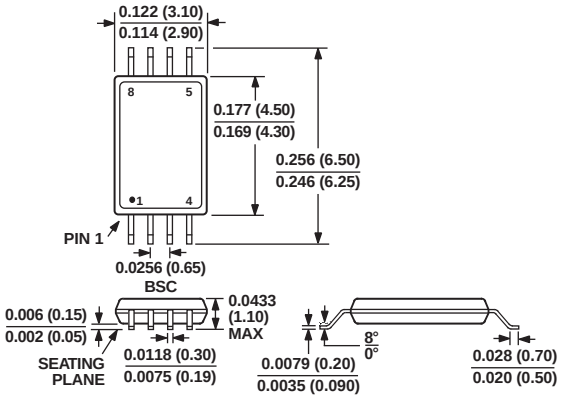
8-Lead SOIC
(R-8)



8-Lead Plastic DIP
(N-8)



8-Lead TSSOP
(RU-8)



Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Edits to SPECIFICATIONS	2
Edits to ABSOLUTE MAXIMUM RATINGS	3
Edits to ORDERING GUIDE	3
Edit to Figure 4	4
Edit to TPC 14	7

C01120–0–2/02(A)

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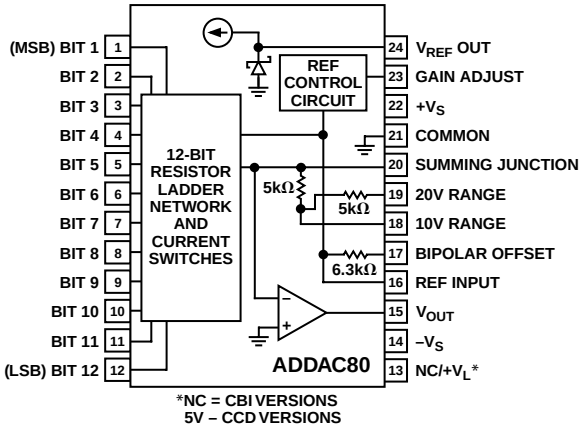
Complete Low Cost 12-Bit D/A Converters

ADDAC80/ADDAC85/ADDAC87

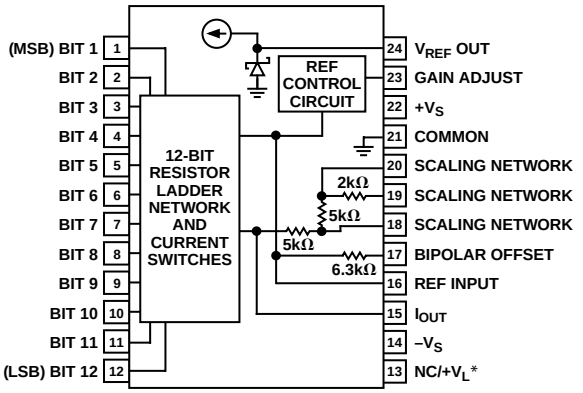
FEATURES

Single Chip Construction
On-Board Output Amplifier
Low Power Dissipation: 300 mW
Monotonicity Guaranteed over Temperature
Guaranteed for Operation with 12 V Supplies
Improved Replacement for Standard DAC80, DAC800 HI-5680
High Stability, High Current Output Buried Zener Reference
Laser Trimmed to High Accuracy 1/2 LSB Max Nonlinearity
Low Cost Plastic Packaging

FUNCTIONAL BLOCK DIAGRAM



*NC = CBI VERSIONS
5V – CCD VERSIONS



*NC = CBI VERSIONS
5V – CCD VERSIONS

PRODUCT DESCRIPTION

The ADDAC80 Series is a family of low cost 12-bit digital-to-analog converters with both a high stability voltage reference and output amplifier combined on a single monolithic chip. The ADDAC80 Series is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional DAC80 devices. Innovative circuit design reduces the total power consumption to 300 mW, which not only improves reliability, but also improves long term stability.

The ADDAC80 incorporates a fully differential, nonsaturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface Zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete Zener references.

The ADDAC80 Series is available in three performance grades and three package types. The ADDAC80 is specified for use over the 0°C to 70°C temperature range and is available in both plastic and ceramic DIP packages. The ADDAC85 and ADDAC87 are available in hermetically sealed ceramic packages and are specified for the –25°C to +85°C and –55°C to +125°C temperature ranges.

PRODUCT HIGHLIGHTS

1. The ADDAC80 series of D/A converters directly replaces all other devices of this type with significant increases in performance.
2. Single chip construction and low power consumption provides the optimum choice for applications where low cost and high reliability are major considerations.
3. The high speed output amplifier has been designed to settle within 1/2 LSB for a 10 V full scale transition in 2.0 µs, when properly compensated.
4. The precision buried Zener reference can supply up to 2.5 mA for use elsewhere in the application.
5. The low TC binary ladder guarantees that all units are monotonic over the specified temperature range.
6. System performance upgrading is possible without redesign.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

ADDAC80/ADDAC85/ADDAC87–SPECIFICATIONS (T_A = 25°C, rated power supplies unless otherwise noted.)

Model	ADDAC80 Min	ADDAC80 Typ	ADDAC80 Max	ADDAC85 Min	ADDAC85 Typ	ADDAC85 Max	ADDAC87 Min	ADDAC87 Typ	ADDAC87 Max	Unit
TECHNOLOGY		Monolithic			Monolithic			Monolithic		
DIGITAL INPUT										
Binary–CBI			12			12			12	Bits
BCD–CCD										Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	**2.0**		**5.5**	**2.0**		**5.5**	**2.0**		**5.5**	V
V_{IL} (Logic "0")	**0**		**0.8**	**0**		**0.8**	**0**		**0.8**	V
I_{IH} (V_{IH} = 5.5 V)			**250**			**250**			**250**	µA
I_{IL} (V_{IL} = 0.8 V)			**100**			**100**			**100**	µA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ 25°C										
CBI			±1/2			±1/2			±1/2	LSB[1]
CCD										LSB
T_A @ T_{MIN} to T_{MAX}		±1/4	**±1/2**		±1/4	**±1/2**		±1/2	**±3/4**	LSB
Differential Linearity Error @ 25°C										
CBI			**±3/4**			**±3/4**			**±3/4**	LSB
CCD										LSB
T_A @ T_{MIN} to T_{MAX}			±3/4			±1			±1	LSB
Gain Error[2]		±0.1	**±0.3**		±0.1	**±0.2**		±0.1	±0.2	%FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05	**±0.1**		±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	–25		+85	–55		+125	°C
DRIFT (T_{MIN} to T_{MAX})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20			±20			±30	ppm of FSR/°C
Total Error (T_{MIN} to T_{MAX})[4]										
Unipolar		±0.08	±0.15		±0.12	±0.2		±0.18	±0.3	% of FSR
Bipolar		±0.06	±0.10		±0.08	±0.12		±0.14	±0.24	% of FSR
Gain Including Internal Reference		±15	**±30**			**±20**			**±20**	ppm of FSR/°C
Gain Excluding Internal Reference		±4	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3			±3			**±3**	ppm of FSR/°C
Bipolar Offset		±5	±10			±10			**±10**	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR Change (2 kΩ‖500 pF load)										
with 10 kΩ Feedback		3	4		3	4		3	4	µs
with 5 kΩ Feedback		2	3		2	3		2	3	µs
For LSB Change		1			1			1		µs
Slew Rate	10			10			10			V/µs
ANALOG OUTPUT										
Voltage Models										
Ranges–CBI		±2.5, ±5, ±10, +5, 10			±2.5, ±5, ±10, +5, 10			±2.5, ±5, ±10, +5, 10		V V V
–CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
Internal Reference Voltage (V_R)	**6.23**	6.3	**6.37**	**6.23**	6.3	**6.37**	**6.23**	6.3	**6.37**	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			**2.5**			**2.5**			**2.5**	mA
Tempco of Drift		±10	±20		±10	±20			±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15 V ± 10%, 5 V supply when applicable			**±0.002**			**±0.002**			**±0.002**	% of FSR/%V_S
±12 V ± 5%			**±0.002**			**±0.002**			**±0.002**	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15			±15			±15		V
Range										
Analog Supplies	±11.4[7]		±16.5	±11.4[7]		±16.5	±11.4[7]		±16.5	V
Logic Supplies										V
Supply Drain										
+12 V, +15 V		5	**10**		5	**10**		5	**10**	mA
–12 V, –15 V		14	**20**		14	**20**		14	**20**	mA

Model	ADDAC80 Min	ADDAC80 Typ	ADDAC80 Max	ADDAC85 Min	ADDAC85 Typ	ADDAC85 Max	ADDAC87 Min	ADDAC87 Typ	ADDAC87 Max	Unit
TEMPERATURE RANGE										
Specifications	0		+70	–25		+85	–55		+125	°C
Operating	–25		+85	–55		+125	–55		+125	°C
Storage	–25		+125	–65		+150	–65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20 V for the ±10 V range and 10 V for the ±5 V range.
[4]Gain and offset errors adjusted to zero at 25°C.
[5]C_F = 0, see Figure 3a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]A minimum of ±12.3 V is required for a ±10 V full scale output and ±11.4 V is required for all other voltage ranges.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

Model	ADDAC80 Min	ADDAC80 Typ	ADDAC80 Max	ADDAC85 Min	ADDAC85 Typ	ADDAC85 Max	ADDAC87 Min	ADDAC87 Typ	ADDAC87 Max	Unit
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary–CBI			12			12			12	Bits
BCD–CCD			3			3			3	Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	2.0		5.5	2.0		5.5	2.0		5.5	V
V_{IL} (Logic "0")	0		0.8	0		0.8	0		0.8	V
I_{IH} (V_{IH} = 5.5 V)		250			250			250		µA
I_{IL} (V_{IL} = 0.8 V)		–100			–100			–100		µA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ 25°C										
CBI		±1/4	±1/2			±1/2			±1/2	LSB[1]
CCD		±1/8	±1/4			±1/4			±1/4	LSB
T_A @ T_{MIN} to T_{MAX}		±1/4	±1/2		±1/4	±1/2		±1/2	±1/2	LSB
Differential Linearity Error @ 25°C										
CBI		±1/2	±3/4		±1/2			±1/2		LSB
CCD		±1/4	±1/2		±1/2			±1/2		LSB
T_A @ T_{MIN} to T_{MAX}			±1			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1			±0.1		%FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05			±0.05		%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	0		+70	–25		+85	°C
DRIFT (T_{MIN} to T_{MAX})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20							ppm of FSR/°C
Total Error (T_{MIN} to T_{MAX})[4]										
Unipolar		±0.08	±0.15							% of FSR
Bipolar		±0.06	±0.10							% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±5	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3		±1			±1		ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR Change (2 kΩ‖500 pF load)										
with 10 kΩ Feedback		5			5			5		µs
with 5 kΩ Feedback		3			3			3		µs
For LSB Change		1.5			1.5			1.5		µs
Slew Rate	10	15			20			20		V/µs
Current Model (I)										
Settling time to ±0.01% of FSR for FSR Change										
10 Ω to 100 Ω Load		300			300			300		ns
for 1 kΩ		1			1			1		µs

ADDAC80/ADDAC85/ADDAC87–SPECIFICATIONS (continued)

Model	ADDAC80 Min	ADDAC80 Typ	ADDAC80 Max	ADDAC85 Min	ADDAC85 Typ	ADDAC85 Max	ADDAC87 Min	ADDAC87 Typ	ADDAC87 Max	Unit
ANALOG OUTPUT										
Voltage Models										
Ranges–CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Ranges–CCD		±10			+10			+10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration	Indefinite to Common			Indefinite to Common			Indefinite to Common			
Current Models										
Ranges–Unipolar		–2.0			–2.0			–2.0		mA
Ranges–Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance										
Bipolar		3.2			3.2			3.2		kΩ
Unipolar		6.6			6.6			6.6		kΩ
Compliance		–1.5, +10			–2.5, +10			–2.5, +10		V
Internal Reference Voltage (V_R)	6.17	6.3	6.43	6.17	6.3	6.43	6.17	6.3	6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			2.5			2.5			2.5	mA
Tempco of Drift		±10	±20		±10	±20		±10	±20	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15 V ± 10%, 5 V Supply When Applicable		±0.002			±0.002			±0.002		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, +5			±15, +5			±15, +5		V
Range										
Analog Supplies	±14		±16	±14.5		±15.5	±14.5		±15.5	V
Logic Supplies	4.5		16	4.5		15.5	4.5		15.5	V
Supply Drain[7]										
+15 V		10	20		15	20		15	20	mA
–15 V		20	35		25	30		25	30	mA
+5 V[8]		8	20		15	20		15	20	mA
TEMPERATURE RANGE										
Specifications	0		+70	0		+70	–25		+85	°C
Operating	–25		+85	–25		+85	–55		+125	°C
Storage	–55		+130	–65		+150	–65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20 V for the ±10 V range and 10 V for the ±5 V range.
[4]Gain and offset errors adjusted to zero at 25°C.
[5]C_F = 0, see Figure 3a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5 mA load.
[8]5 V supply required only for CCD versions.

Specifications subject to change without notice.

Model	ADDAC85LD Min	Typ	Max	ADDAC85MIL Min	Typ	Max	ADDAC87 Min	Typ	Max	Unit
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary–CBI			12			12			12	Bits
BCD–CCD										Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	2.0		5.5	2.0		5.5	2.0		5.5	V
V_{IL} (Logic "0")	0		0.8	0		0.8	0		0.8	V
I_{IH} (V_{IH} = 5.5 V)		250			250			250		µA
I_{IL} (V_{IL} = 0.8 V)		–100			–100			–100		µA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ 25°C										
CBI			±1/2			±1/2		±1/4	±1/2	LSB[1]
CCD										LSB
T_A @ T_{MIN} to T_{MAX}			±1/2			±3/4			±3/4	LSB
Differential Linearity Error @ 25°C										
CBI		±1/2			±1/2			±1/2		LSB
CCD										LSB
T_A @ T_{MIN} to T_{MAX}			±1			±1			±1	LSB
Gain Error[2]		±0.1			±0.1			±0.1	±0.2	%FSR[3]
Offset Error[2]		±0.05			±0.05			±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	–25		+85	–55		+125	–55		+125	°C
DRIFT (T_{MIN} to T_{MAX})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)								±15	±30	ppm of FSR/°C
Total Error (T_{MIN} to T_{MAX})[4]										
Unipolar								±0.13	±0.30	% of FSR
Bipolar								±0.12	±0.24	% of FSR
Gain										
Including Internal Reference			±10			±20		±10	±25	ppm of FSR/°C
Excluding Internal Reference								±5	±10	ppm of FSR/°C
Unipolar Offset		±1			±2			±1	±3	ppm of FSR/°C
Bipolar Offset			±5			±10		±5	±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2 kΩ‖500 pF load)										
with 10 kΩ Feedback		5			5			5		µs
with 5 kΩ Feedback		3			3			3		µs
For LSB Change		1.5			1.5			1.5		µs
Slew Rate		20			20			20		V/µs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change										
10 Ω to 100 Ω Load		300			300			300		ns
for 1 kΩ		1			1			1		µs
ANALOG OUTPUT										
Voltage Models										
Ranges–CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
–CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration	Indefinite to Common			Indefinite to Common			Indefinite to Common			
Current Models										
Ranges–Unipolar		–2.0			–2.0			–2.0		mA
–Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance										
Bipolar		3.2			3.2		2.5	3.2	4.1	kΩ
Unipolar		6.6			6.6		5.0	6.6	8.2	kΩ
Compliance		–2.5, +10			–2.5, +10			–1.5, +10		V
Internal Reference Voltage (V_R)	6.17	6.3	6.43	6.17	6.3	6.43	6.17	6.3	6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			2.5			2.5			2.5	mA
Tempco of Drift		±10	±20		±10	±20		±5	±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15 V ± 10%, 5 V supply when applicable		±0.002			±0.002			±0.002	±0.003	% of FSR/%V_S

ADDAC80/ADDAC85/ADDAC87–SPECIFICATIONS (continued)

Model	ADDAC85LD Min	ADDAC85LD Typ	ADDAC85LD Max	ADDAC85MIL Min	ADDAC85MIL Typ	ADDAC85MIL Max	ADDAC87 Min	ADDAC87 Typ	ADDAC87 Max	Unit
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14.5		±15.5	±14.5		±15.5	±13.5		±16.5	V
Logic Supplies	+4.5		±15.5	+4.5		+15.5	+4.5		±16.5	V
Supply Drain[7]										
+15 V		15	20		15	20		10	20	mA
–15 V		25	30		25	30		20	35	mA
+5 V[8]		15	20		15	20		10	20	mA
TEMPERATURE RANGE										
Specification	–25		+85	–55		+125	–55		+125	°C
Operating	–55		+125	–55		+125	–55		+125	°C
Storage	–55		+125	–55		+125	–65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full-Scale Range" and is 20 V for the ±10 V range and 10 V for the ±5 V range.
[4]Gain and offset errors adjusted to zero at 25°C.
[5]C_F = 0, see Figure 3a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5 mA load.
[8]5 V supply required only for CCD versions.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to Power Ground . . . . . 0 V to +18 V
$-V_S$ to Power Ground . . . . . 0 V to –18 V
Digital Inputs (Pins 1 to 12) to Power Ground . . . . . .
. . . . . –1.0 V to +7 V
Ref In to Reference Ground . . . . . ±12 V
Bipolar Offset to Reference Ground . . . . . ±12 V
10 V Span R to Reference Ground . . . . . ±12 V
20 V Span R to Reference Ground . . . . . ±24 V
Ref Out . . . . . Indefinite Short to Power Ground or $+V_S$

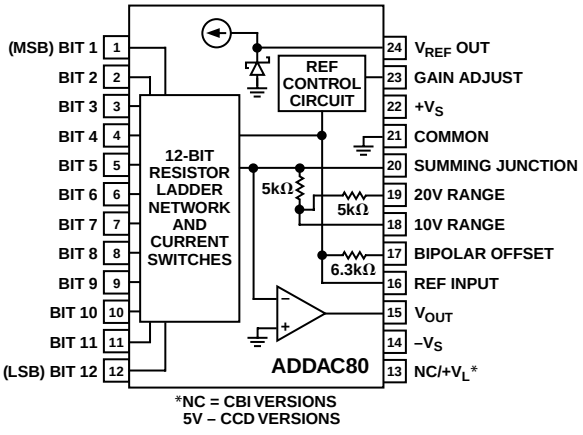


Figure 1. Voltage Model Function Diagram and Pin Configuration

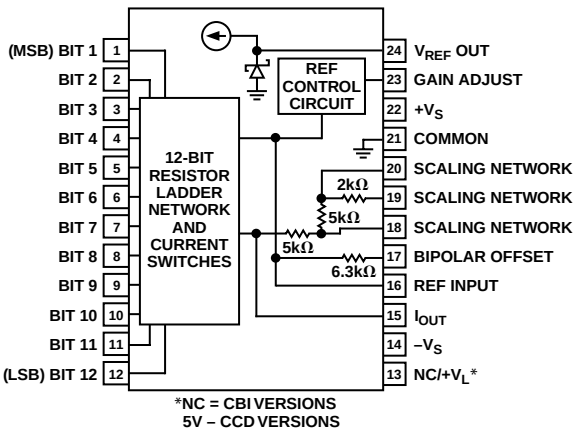


Figure 2. Current Model Functional Diagram and Pin Configuration

ORDERING GUIDE

Model	Input Code	Output Mode	Technology	Temperature Range	Linearity Error	Package Option[1]
ADDAC80N-CBI-V	Binary	Voltage	Monolithic	0°C to 70°C	±1/2 LSB	N-24A
ADDAC80D-CBI-V	Binary	Voltage	Monolithic	0°C to 70°C	±1/2 LSB	D-24
ADDAC85D-CBI-V	Binary	Voltage	Monolithic	–25°C to +85°C	±1/2 LSB	D-24
ADDAC87D-CBI-V	Binary	Voltage	Monolithic	–55°Cto +125°C	±1/2 LSB	D-24
ADDAC80-CBI-V	Binary	Voltage	Hybrid	0°C to 70°C	±1/2 LSB	DH-24A
ADDAC80-CBI-I	Binary	Current	Hybrid	0°C to 70°C	±1/2 LSB	DH-24A
ADDAC80-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0°C to 70°C	±1/4 LSB	DH-24A
ADDAC80-CCD-I	Binary Coded Decimal	Current	Hybrid	0°C to 70°C	±1/4 LSB	DH-24A
ADDAC80Z-CBI-V[2]	Binary	Voltage	Hybrid	0°C to 70°C	±1/2 LSB	DH-24A
ADDAC80Z-CBI-I[2]	Binary	Current	Hybrid	0°C to 70°C	±1/2 LSB	DH-24A
ADDAC80Z-CCD-V[2]	Binary Coded Decimal	Voltage	Hybrid	0°C to 70°C	±1/4 LSB	DH-24A
ADDAC80Z-CCD-I[2]	Binary Coded Decimal	Current	Hybrid	0°C to 70°C	±1/4 LSB	DH-24A
ADDAC85C-CBI-V[3]	Binary	Voltage	Hybrid	0°C to 70°C	±1/2 LSB	DH-24A
ADDAC85C-CBI-I	Binary	Current	Hybrid	0°C to 70°C	±1/2 LSB	DH-24A
ADDAC85-CBI-V[3]	Binary	Voltage	Hybrid	–25°C to +85°C	±1/2 LSB	DH-24A
ADDAC85-CBI-I[3]	Binary	Current	Hybrid	–25°C to +85°C	±1/2 LSB	DH-24A
ADDAC85LD-CBI-V[3]	Binary	Voltage	Hybrid	–25°C to +85°C	±1/2 LSB	DH-24A
ADDAC85LD-CBI-I[3]	Binary	Current	Hybrid	–25°C to +85°C	±1/2 LSB	DH-24A
ADDAC85MIL-CBI-V[3]	Binary	Voltage	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC85MIL-CBI-I[3]	Binary	Current	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC85C-CCD-V[3]	Binary Coded Decimal	Voltage	Hybrid	0°C to 70°C	±1/4 LSB	DH-24A
ADDAC85C-CCD-I[3]	Binary Coded Decimal	Current	Hybrid	0°C to 70°C	±1/4 LSB	DH-24A
ADDAC85-CCD-V[3]	Binary Coded Decimal	Voltage	Hybrid	–25°C to +85°C	±1/4 LSB	DH-24A
ADDAC85-CCD-I[3]	Binary Coded Decimal	Current	Hybrid	–25°C to +85°C	±1/4 LSB	DH-24A
ADDAC85MILCBII8	Binary	Current	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC85MILCBIV8	Binary	Voltage	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC87-CBI-V[3]	Binary	Voltage	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC87-CBI-I[3]	Binary	Current	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC87-CBII883	Binary	Current	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC87-CBIV883	Binary	Voltage	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A

NOTES
[1]For outline information see Package Information section.
[2]Z-Suffix devices guarantee performance of 0 V to +5 V and ±5 V spans with minimum supply voltages of ±11.4 V.
[3]These models have been discontinued. This is for historical information only.

PRODUCT OFFERING

Analog Devices has developed a number of technologies to support products within the data acquisition market. In serving the market new products are implemented with the technology best suited to the application. The DAC80 series of products was first implemented in hybrid form and now it is available in a single monolithic chip. We will provide both the hybrid and monolithic versions of the family so that in existing designs changes to documentation or product qualification will not have to be done. Specifications and ordering information for both versions are delineated in this data sheet.

DIGITAL INPUT CODES

The ADDAC80 Series accepts complementary digital input code in binary (CBI) format. The CBI model may be connected by the user for anyone of three complementary codes: CSB, COB or CTC.

Table I. Digital Input Codes

Digital Input	Analog Input		
MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full-Scale	+Full-Scale	–1 LSB
011111111111	+1/2 Full-Scale	Zero	–Full-Scale
100000000000	Midscale	–1 LSB	+Full-Scale
111111111111	Zero	–Full-Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected. Linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than its maximum specification, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 1 1/2 LSB when the input changes from one adjacent input state to the next.

DRIFT

Gain Drift

A measure of the change in the full scale range output over temperature expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain drift is established by: 1) testing the end point differences for each ADDAC80 model at the lowest operating temperature, 25°C and the highest operating temperature; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change.

Offset Drift

A measure of the actual change in output with all "1"s on the input over the specified temperature range. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output Models

Three settling times are specified to 0.01% of full scale range (FSR); two for maximum full scale range changes of 20 V, 10 V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0 1 1 1 . . . 1 1 to 1 0 0 0 . . . 0 0), the point at which the worst case settling time occurs. The settling time characteristic depends on the compensation capacitor selected, the optimum value is 25 pF as shown in Figure 3a.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 Ω to 100 Ω and 1000 Ω to 1875 Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000 Ω to 1800 Ω for output voltage ranges of ±1 V and 0 V to –2 V.

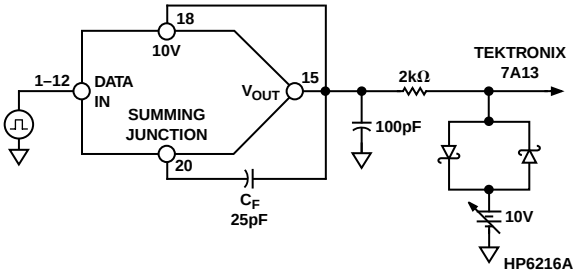


Figure 3a. Voltage Model Settling Time Circuit

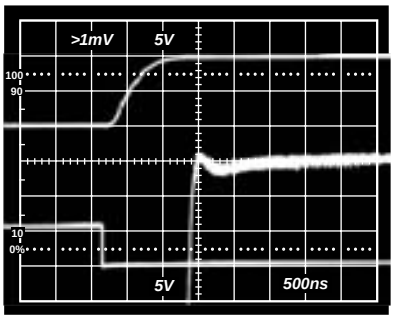


Figure 3b. Voltage Model Settling Time C_F = 25 pF

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All models are supplied with an internal 6.3 V reference voltage supply. This voltage (Pin 24) is accurate to ±1% and must be connected to the Reference Input (Pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5 mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations. All gain adjustments should be made under constant load conditions.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 4. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input codes, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients that contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

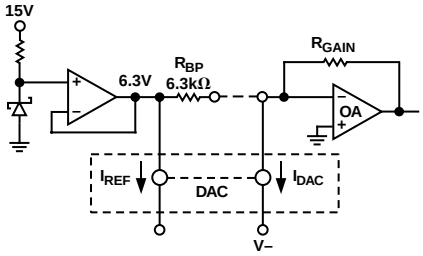


Figure 4. Bipolar Configuration

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input that calls for zero output to a point that is defined as full-scale. A specification for total error over temperature assumes that both the zero and full-scale points have been trimmed for zero error at 25°C. Total error is normally expressed as a percentage of the full-scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried Zener diode reference element results in superior wide temperature range performance. The gain setting resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

MONOTONICITY AND LINEARITY

The initial linearity error of ±1/2 LSB max and the differential linearity error of ±3/4 LSB max guarantee monotonic performance over the specified range. It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 5. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see Figure 4) to generate a current that exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 5. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts previously discussed will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the ADDAC80 this error is held to 10 ppm/°C max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full-scale drift, but again is held to 10 ppm/°C max.

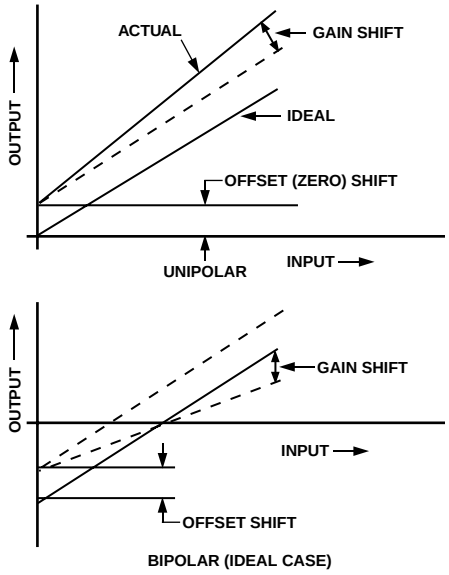


Figure 5. Unipolar and Bipolar Drifts

USING THE ADDAC80 SERIES
POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams. These capacitors (1 µF electrolytic recommended) should be located close to the ADDAC80. Electrolytic capacitors, if used, should be paralleled with 0.01 µF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100 ppm/°C or less. The 3.9 MΩ and 10 MΩ resistors (20% carbon or better) should be located close to the ADDAC80 to prevent noise pickup. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 8 may be substituted in each case. The gain adjust (Pin 23) is a high impedance point and a 0.01 µF ceramic capacitor should be connected from this pin to common to prevent noise pickup.

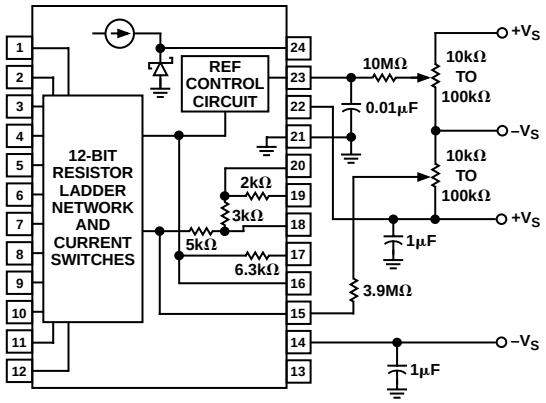


Figure 6. External Adjustment and Voltage Supply Connection Diagram, Current Model

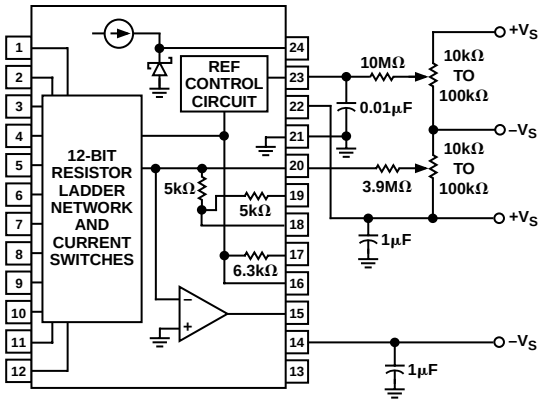


Figure 7. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 V, the maximum negative output voltage is –10 V. See Table II for corresponding codes.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages.

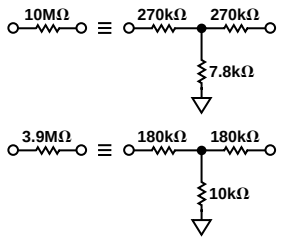


Figure 8. Equivalent Resistances

Table II. Digital Input Analog Output

Digital Input	Analog Output			
12-Bit Resolution	Voltage*		Current	
MSB LSB	0 to +10 V	±10 V	0 to –2 mA	±1 mA
0 0 0 0 0 0 0 0 0 0 0 0	+9.9976 V	+9.9951 V	–1.9995 mA	–0.9995 mA
0 1 1 1 1 1 1 1 1 1 1 1	+5.0000 V	0.0000 V	–1.0000 mA	0.0000 mA
1 0 0 0 0 0 0 0 0 0 0 0	+4.9976 V	4.88 mV	–0.9995 mA	+0.0005 mA
1 1 1 1 1 1 1 1 1 1 1 1	0.0000 V	–10.0000 V	0.0000 mA	–1.00 mA
l LSB	2.44 mV	–0.0049 V	0.488 μA	0.488 μA

*To obtain values for other binary ranges 0 to 5 V range: divide 0 to 10 values by 2; ±5 V range: divide ±10 V range values by 2; ±2.5 V range: divide ±10 V range values by 4.

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the ADDAC80 may be connected to produce bipolar output voltage ranges of ±10 V, ±5 V or ±2.5 V or unipolar output voltage ranges of 0 V to +5 V or 0 V to +10 V (see Figure 9).

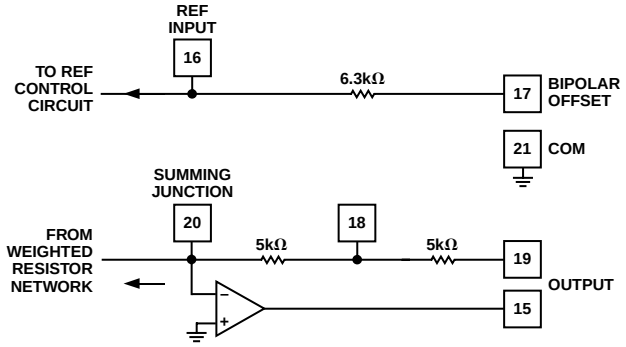


Figure 9. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the ADDAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full-scale range change: 4 μs for a 10 kΩ feedback resistor; 3 μs for a 5 kΩ feedback resistor when using the compensation capacitor shown in Figure 3a.

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 10 and 11. External R_{LS} resistors are required to produce exactly 0 V to –2 V or ±1 V output. TCR of these resistors should be ±100 ppm/°C or less to maintain the ADDAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

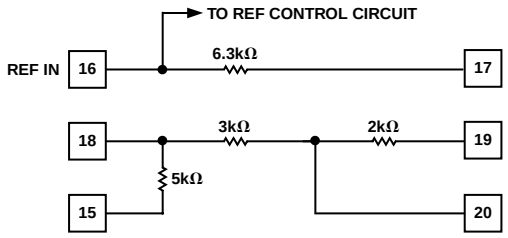


Figure 10. Internal Scaling Resistors

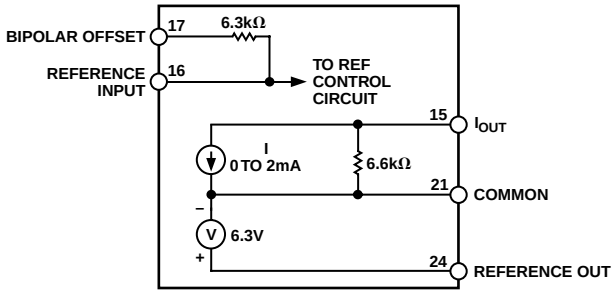


Figure 11. ADDAC80 Current Model Equivalent Output Circuit

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1 V or 0 V to –2 V. These resistors (R_{LI} TCR = 20 ppm/°C) are an integral part of the ADDAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25 ppm/°C or less to minimize drift. This will typically add ±50 ppm/°C + the TCR of R_L (or R_F) to the total drift.

Table III. Output Voltage Range Connections, Voltage Model ADDAC80

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10 V	COB or CTC	19	20	15	24
±5 V	COB or CTC	18	20	NC	24
±2.5 V	COB or CTC	18	20	20	24
0 V to 10 V	CSB	18	21	NC	24
0 V to 5 V	CSB	18	21	20	24
0 V to 10 V	CCD	19	NC	15	24

NC = No Connect

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 12 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2\ mA\left(\frac{6.6\ k\Omega \times R_L}{6.6\ k\Omega + R_L}\right) \quad (1)$$

where R_L max = 1.54 kΩ and V_{OUT} max = –2.5 V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 V to –2 V. With R_{LS} = 0 V, V_{OUT} = –1.69 V.

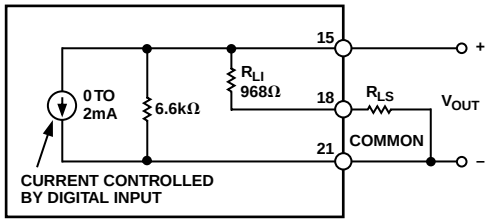


Figure 12. Equivalent Circuit ADDAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 13, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1\,mA\left(\frac{R_L \times 3.22\,k\Omega}{R_L + 3.22\,k\Omega}\right) \quad (2)$$

where R_L max = 11.18 kΩ and V_{OUT} max = ±2.5 V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1 V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874 V.

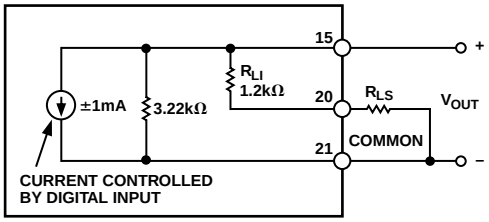


Figure 13. ADDAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

DRIVING AN EXTERNAL OP AMP

The current model ADDAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 14,

$$V_{OUT} = I_{OUT} \times R_F \quad (3)$$

where I_{OUT} is the ADDAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model ADDAC80 provides output voltage ranges the same as the voltage model ADDAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 14.

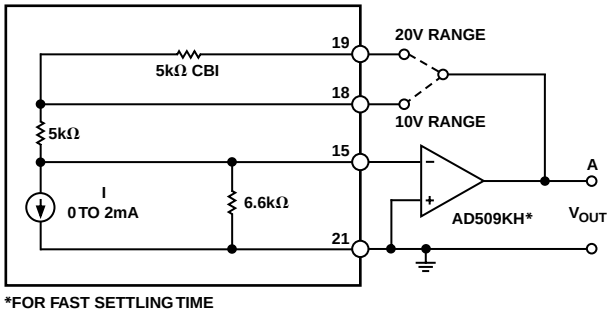


Figure 14. External Op Amp Using Internal Feedback Resistors

OUTPUT LARGER THAN 20 V RANGE

For output voltage ranges larger than ±10 V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1 mA for bipolar voltage ranges and –2 mA for unipolar voltage ranges (see Figure 15). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

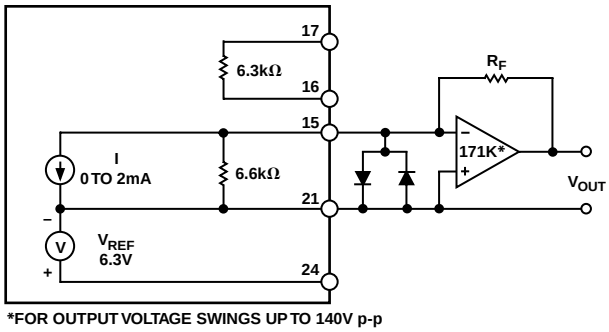


Figure 15. External Op Amp Using External Feedback Resistors

Table IV. Current Model/Resistive Load Connections

Digital Input Codes	Output Range	Internal Resistance R_{LI} (kΩ)	1% Metal Film External Resistance R_{LS}	R_{LI} Connections			Reference	Bipolar Offset	
				Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R_{LS}
CSB	0 to –2 V	0.968	210 Ω	20	19 and R_{LS}	15	24	Com (21)	Between Pin 18 and Com (21)
COB or CTC	±1 V	1.2	249 Ω	18	19	R_{LS}	24	15	Between Pin 20 and Com (21)
CCD	0 to ±2 V	3	N/A	NC	21	NC	24	NC	N/A

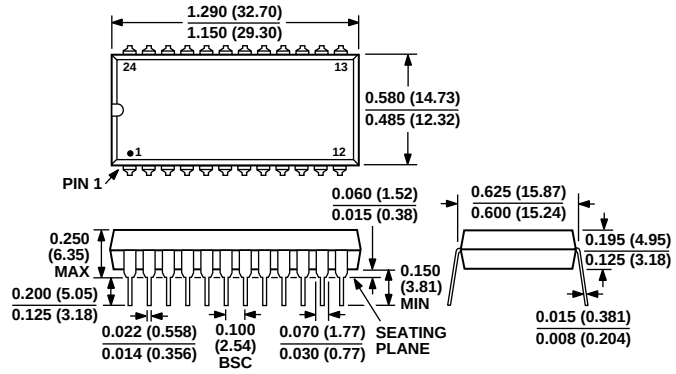
Table V. External Op Amp Voltage Mode Connections

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10 V	COB or CTC	19	15	A	24
±5 V	COB or CTC	18	15	NC	24
±2.5 V	COB or CTC	18	15	15	24
0 V to 10 V	CSB	18	21	NC	24
0 V to 5 V	CSB	18	21	15	24

OUTLINE DIMENSIONS

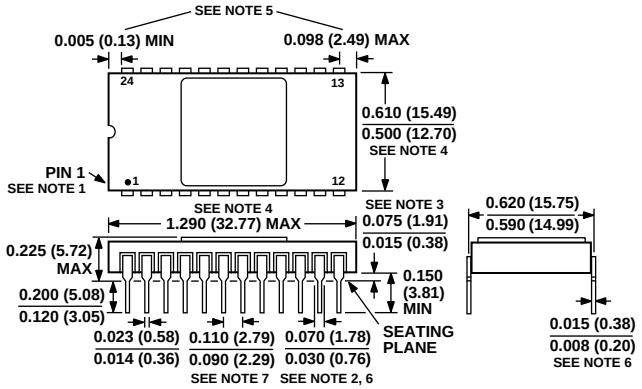
Dimensions shown in inches and (mm).

24-Lead Plastic DIP (N-24A)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS: INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

24-Lead Ceramic DIP (D-24)

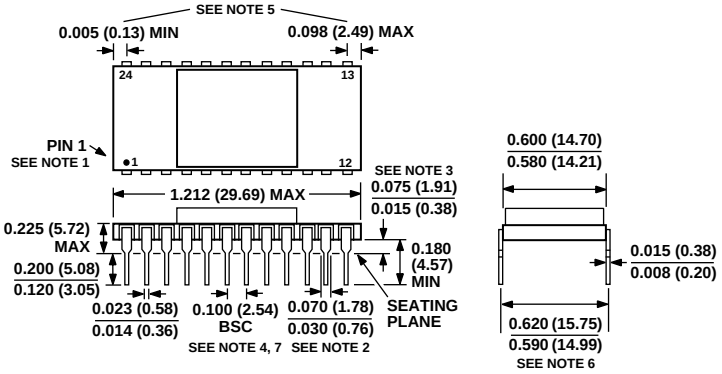


NOTES
1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.
2. THE MINIMUM LIMIT FOR DIMENSION MAY BE 0.023" (0.58 mm) FOR ALL FOUR CORNER LEADS ONLY.
3. DIMENSION SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. APPLIES TO ALL FOUR CORNERS.
6. ALL LEADS — INCREASE MAXIMUM LIMIT BY 0.003" (0.08 mm) MEASURED AT THE CENTER OF THE FLAT, WHEN HOT SOLDER DIP LEAD FINISH IS APPLIED.
7. TWENTY TWO SPACES.
8. CONTROLLING DIMENSIONS ARE IN MILLIMETERS. INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Side Brazed Ceramic DIP for Hybrid (DH-24A)



NOTES
1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.
2. THE MINIMUM LIMIT FOR DIMENSION MAY BE 0.023" (0.58 mm) FOR ALL FOUR CORNER LEADS ONLY.
3. DIMENSION SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THE BASIC PIN SPACING IS 0.100" (2.54 mm) BETWEEN CENTERLINES.
5. APPLIES TO ALL FOUR CORNERS.
6. SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
7. TWENTY TWO SPACES.
8. CONTROLLING DIMENSIONS ARE IN MILLIMETERS: INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Revision History

Location	Page
Data Sheet changed from REV. A to REV. B.	
Update OUTLINE DIMENSION drawings	1

C00381–0–1/02(B)

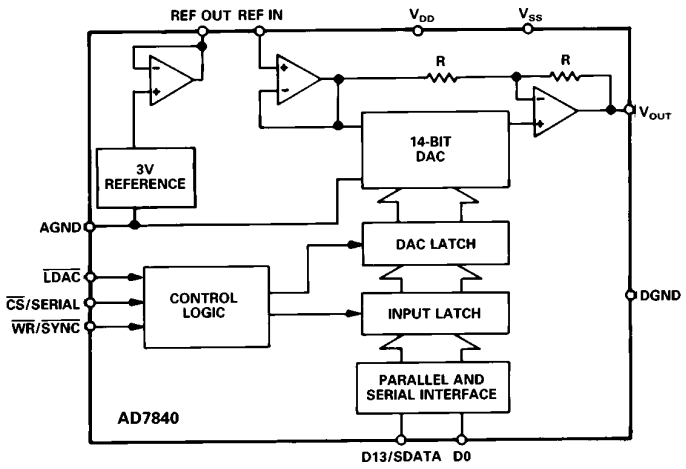
PRINTED IN U.S.A.

LC²MOS Complete 14-Bit DAC

AD7840

FEATURES
Complete 14-Bit Voltage Output DAC
Parallel and Serial Interface Capability
80 dB Signal-to-Noise Ratio
Interfaces to High Speed DSP Processors
e.g., ADSP-2100, TMS32010, TMS32020
45 ns min $\overline{WR}$ Pulse Width
Low Power – 70 mW typ.
Operates from ±5 V Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7840 is a fast, complete 14-bit voltage output D/A converter. It consists of a 14-bit DAC, 3 V buried Zener reference, DAC output amplifier and high speed control logic.

The part features double-buffered interface logic with a 14-bit input latch and 14-bit DAC latch. Data is loaded to the input latch in either of two modes, parallel or serial. This data is then transferred to the DAC latch under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 21 ns allows direct parallel interfacing to digital signal processors and high speed 16-bit microprocessors. In the serial mode, the maximum serial data clock rate can be as high as 6 MHz.

The analog output from the AD7840 provides a bipolar output range of ±3 V. The AD7840 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion as well as for traditional dc specifications. Full power output signals up to 20 kHz can be created.

The AD7840 is fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin plastic and hermetic dual-in-line package (DIP) and is also packaged in a 28-terminal plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete 14-Bit D/A Function
   The AD7840 provides the complete function for creating ac signals and dc voltages to 14-bit accuracy. The part features an on-chip reference, an output buffer amplifier and 14-bit D/A converter.
2. Dynamic Specifications for DSP Users
   In addition to traditional dc specifications, the AD7840 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Fast, Versatile Microprocessor Interface
   The AD7840 is capable of 14-bit parallel and serial interfacing. In the parallel mode, data setup times of 21 ns and write pulse widths of 45 ns make the AD7840 compatible with modern 16-bit microprocessors and digital signal processors. In the serial mode, the part features a high data transfer rate of 6 MHz.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD7840–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, REF IN = +3 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless othewise noted.)

Parameter	J, A[1]	K, B[1]	S[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR)	76	78	76	dB min	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically 82 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Total Harmonic Distortion (THD)	–78	–80	–78	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically –84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Peak Harmonic or Spurious Noise	–78	–80	–78	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically –84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
DC ACCURACY					
Resolution	14	14	14	Bits	
Integral Nonlinearity	±2	±1	±2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	±10	LSB max	
Positive Full Scale Error[5]	±10	±10	±10	LSB max	
Negative Full Scale Error[5]	±10	±10	±10	LSB max	
REFERENCE OUTPUT[6]					
REF OUT @ +25°C	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	V max	
REF OUT TC	±60	±60	±60	ppm/°C max	
Reference Load Change (ΔREF OUT vs. ΔI)	–1	–1	–1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT					
Reference Input Range	2.85	2.85	2.85	V min	3 V ± 5%
	3.15	3.15	3.15	V max	
Input Current	50	50	50	μA max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Current ($\overline{CS}$ Input Only)	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	pF max	
ANALOG OUTPUT					
Output Voltage Range	±3	±3	±3	V nom	
DC Output Impedance	0.1	0.1	0.1	Ω typ	
Short-Circuit Current	20	20	20	mA typ	
AC CHARACTERISTICS[7]					
Voltage Output Settling Time					Settling Time to within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	4	μs max	Typically 2 μs
Negative Full-Scale Change	4	4	4	μs max	Typically 2.5 μs
Digital-to-Analog Glitch Impulse	10	10	10	nV secs typ	
Digital Feedthrough	2	2	2	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	14	14	15	mA max	Output Unloaded, SCLK = +5 V. Typically 10 mA
I_{SS}	6	6	7	mA max	Output Unloaded, SCLK = +5 V. Typically 4 mA
Power Dissipation	100	100	110	mW max	Typically 70 mW

NOTES
[1]Temperature ranges are as follows: J, K Versions, 0°C to +70°C; A, B Versions, –25°C to +85°C; S Version, –55°C to +125°C.
[2]V_{OUT} (pk-pk) = ±3 V
[3]SNR calculation includes distortion and noise components.
[4]Using external sample-and-hold (see Testing the AD7840).
[5]Measured with respect to REF IN and includes bipolar offset error.
[6]For capacitive loads greater than 50 pF, a series resistor is required (see Internal Reference section).
[7]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V.)

Parameter	Limit at T_{MIN}, T_{MAX} (J, K, A, B Versions)	Limit at T_{MIN}, T_{MAX} (S Version)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	**45**	**50**	ns min	$\overline{WR}$ Pulse Width
t_4	**21**	**28**	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	**10**	**15**	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6	40	40	ns min	$\overline{LDAC}$ Pulse Width
t_7	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge
t_8[3]	150	200	ns min	SCLK Cycle Time
t_9	30	40	ns min	Data Valid to SCLK Setup Time
t_{10}	75	100	ns min	Data Valid to SCLK Hold Time
t_{11}	75	100	ns min	$\overline{SYNC}$ to SCLK Hold Time

NOTES
[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 6 and 8.
[3]SCLK mark/space ratio is 40/60 to 60/40.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . –0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to –7 V
AGND to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND . . . . . V_{SS} to V_{DD}
REF OUT to AGND . . . . . 0 V to V_{DD}
REF IN to AGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (J, K Versions) . . . . . 0°C to +70°C
  Industrial (A, B Versions) . . . . . –25°C to +85°C
  Extended (S Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

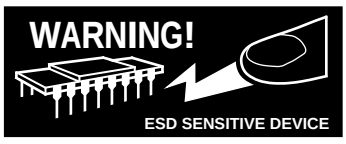
ORDERING GUIDE

Model[1]	Temperature Range	SNR (dB)	Integral Nonlinearity (LSB)	Package Option[2]
AD7840JN	0°C to +70°C	78 min	±2 max	N-24
AD7840KN	0°C to +70°C	80 min	±1 max	N-24
AD7840JP	0°C to +70°C	78 min	±2 max	P-28A
AD7840KP	0°C to +70°C	80 min	±1 max	P-28A
AD7840AQ	–25°C to +85°C	78 min	±2 max	Q-24
AD7840ARS	–25°C to +85°C	78 min	±2 max	RS-24
AD7840BQ	–25°C to +85°C	80 min	±1 max	Q-24
AD7840SQ[3]	–55°C to +125°C	78 min	±2 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip.
[3]This grade will be available to /883B processing only.

CAUTION

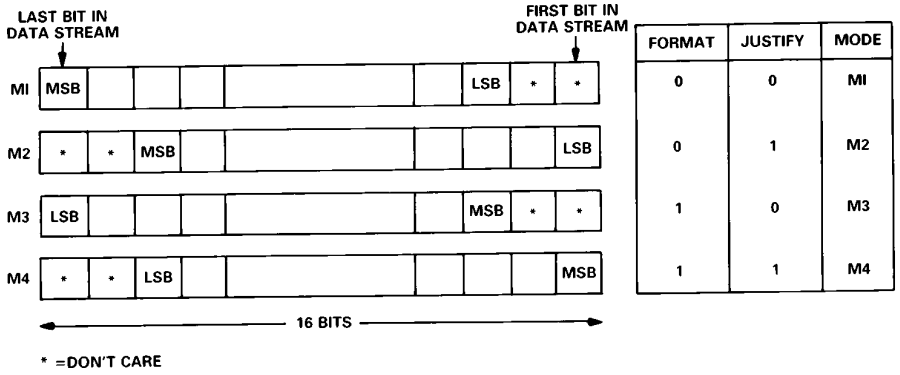
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7840 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTION

DIP Pin No.	Pin Mnemonic	Function
1	$\overline{CS}$/SERIAL	Chip Select/Serial Input. When driven with normal logic levels, it is an active low logic input which is used in conjunction with $\overline{WR}$ to load parallel data to the input latch. For applications where $\overline{CS}$ is permanently low, an R, C is required for correct power-up (see $\overline{LDAC}$ input). If this input is tied to V_{SS}, it defines the AD7840 for serial mode operation.
2	$\overline{WR}$/$\overline{SYNC}$	Write/Frame Synchronization Input. In the parallel data mode, it is used in conjunction with $\overline{CS}$ to load parallel data. In the serial mode of operation, this pin functions as a Frame Synchronization pulse with serial data expected after the falling edge of this signal.
3	D13/SDATA	Data Bit 13(MSB)/Serial Data. When parallel data is selected, this pin is the D13 input. In serial mode, SDATA is the serial data input which is used in conjunction with $\overline{SYNC}$ and SCLK to transfer serial data to the AD7840 input latch.
4	D12/SCLK	Data Bit 12/Serial Clock. When parallel data is selected, this pin is the D12 input. In the serial mode, it is the serial clock input. Serial data bits are latched on the falling edge of SCLK when $\overline{SYNC}$ is low.
5	D11/FORMAT	Data Bit 11/Data Format. When parallel data is selected, this pin is the D11 input. In serial mode, a Logic 1 on this input indicates that the MSB is the first valid bit in the serial data stream. A Logic 0 indicates that the LSB is the first valid bit (see Table I).
6	D10/JUSTIFY	Data Bit 10/Data Justification. When parallel data is selected, this pin is the D10 input. In serial mode, this input controls the serial data justification (see Table I).
7–11	D9–D5	Data Bit 9 to Data Bit 5. Parallel data inputs.
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	D4–D1	Data Bit 4 to Data Bit 1. Parallel data inputs.
17	D0	Data Bit 0 (LSB). Parallel data input.
18	V_{DD}	Positive Supply, +5 V ± 5%.
19	AGND	Analog Ground. Ground reference for DAC, reference and output buffer amplifier.
20	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Bipolar output range (±3 V with REF IN = +3 V).
21	V_{SS}	Negative Supply Voltage, –5 V ± 5%.
22	REF OUT	Voltage Reference Output. The internal 3 V analog reference is provided at this pin. To operate the AD7840 with internal reference, REF OUT should be connected to REF IN. The external load capability of the reference is 500 μA.
23	REF IN	Voltage Reference Input. The reference voltage for the DAC is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7840 is 3 V.
24	$\overline{LDAC}$	Load DAC. Logic Input. A new word is loaded into the DAC latch from the input latch on the falling edge of this signal (see Interface Logic Information section). The AD7840 should be powered-up with $\overline{LDAC}$ high. For applications where $\overline{LDAC}$ is permanently low, an R, C is required for correct power-up (see Figure 19).

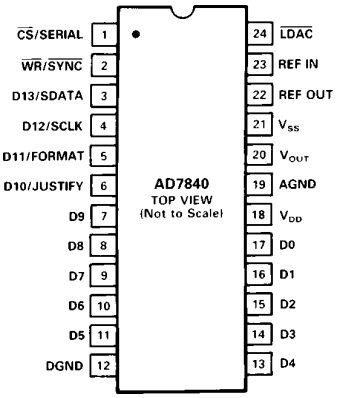
Table I. Serial Data Modes



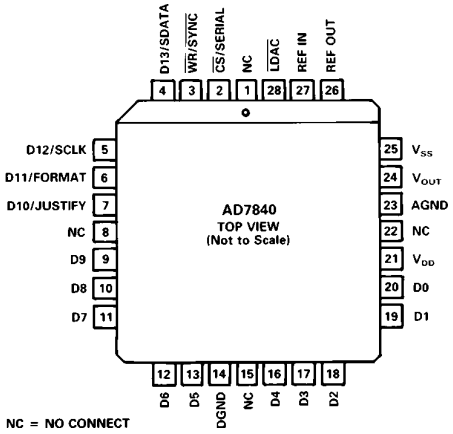
FORMAT	JUSTIFY	MODE
0	0	MI
0	1	M2
1	0	M3
1	1	M4

PIN CONFIGURATIONS

DIP/SSOP



PLCC



D/A SECTION

The AD7840 contains a 14-bit voltage mode D/A converter consisting of highly stable thin film resistors and high speed NMOS single-pole, double-throw switches. The simplified circuit diagram for the DAC section is shown in Figure 1. The three MSBs of the data word are decoded to drive the seven switches A–G. The 11 LSBs switch an 11-bit R-2R ladder structure. The output voltage from this converter has the same polarity as the reference voltage, REF IN.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter and the bipolar bias circuitry. The D/A converter is configured and sealed for a 3 V reference and the device is tested with 3 V applied to REF IN. Operating the AD7840 at reference voltages outside the ±5% tolerance range may result in degraded performance from the part.

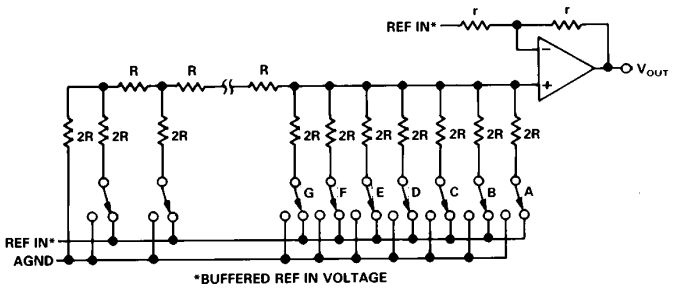


Figure 1. DAC Ladder Structure

INTERNAL REFERENCE

The AD7840 has an on-chip temperature compensated buried Zener reference (see Figure 2) which is factory trimmed to 3 V ±10 mV. The reference voltage is provided at the REF OUT pin. This reference can be used to provide both the reference voltage for the D/A converter and the bipolar bias circuitry. This is achieved by connecting the REF OUT pin to the REF IN pin of the device.

The reference voltage can also be used as a reference for other components and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should he decoupled to AGND with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

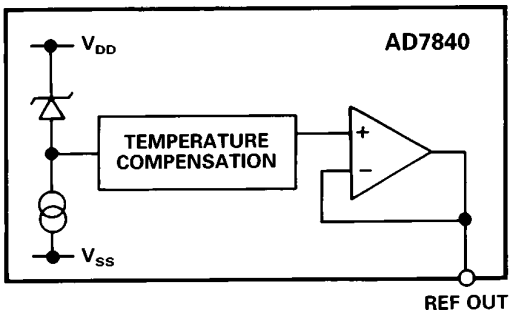


Figure 2. Internal Reference

EXTERNAL REFERENCE

In some applications, the user may require a system reference or some other external reference to drive the AD7840 reference input. Figure 3 shows how the AD586 5 V reference can be conditioned to provide the 3 V reference required by the AD7840 REF IN. An alternate source of reference voltage for the AD7840 in systems which use both a DAC and an ADC is to use the REF OUT voltage of ADCs such as the AD7870 and AD7871. A circuit showing this arrangement is shown in Figure 20.

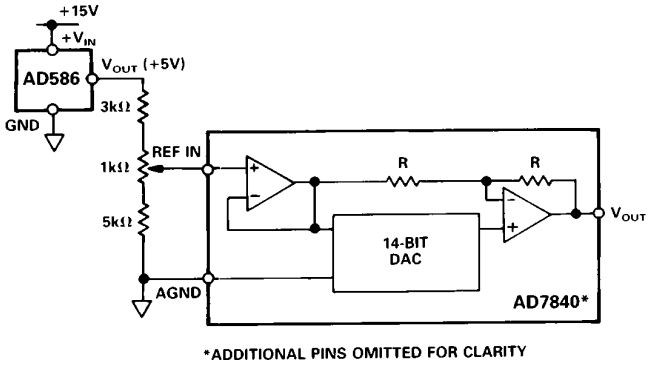


Figure 3. AD586 Driving AD7840 REF IN

OP AMP SECTION

The output from the voltage mode DAC is buffered by a noninverting amplifier. Internal scaling resistors on the AD7840 configure an output voltage range of ±3 V for an input reference voltage of +3 V. The arrangement of these resistors around the output op amp is as shown in Figure 1. The buffer amplifier is capable of developing ±3 V across a 2 kΩ and 100 pF load to ground and can produce 6 V peak-to-peak sine wave signals to a frequency of 20 kHz. The output is updated on the falling edge of the $\overline{\text{LDAC}}$ input. The amplifier settles to within 1/2 LSB of its final value in typically less than 2.5 μs.

The small signal (200 mV p-p) bandwidth of the output buffer amplifier is typically 1 MHz. The output noise from the amplifier is low with a figure of 30 nV/√Hz at a frequency of 1 kHz. The broadband noise from the amplifier exhibits a typical peak-to-peak figure of 150 μV for a 1 MHz output bandwidth. Figure 4 shows a typical plot of noise spectral density versus frequency for the output buffer amplifier and for the on-chip reference.

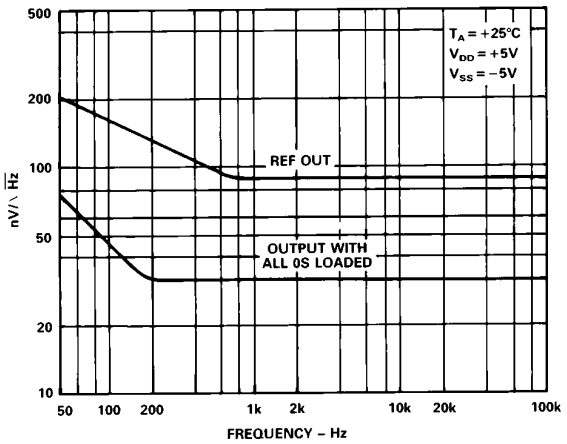


Figure 4. Noise Spectral Density vs. Frequency

TRANSFER FUNCTION

The basic circuit configuration for the AD7840 is shown in Figure 5. Table II shows the ideal input code to output voltage relationship for this configuration. Input coding to the DAC is 2s complement with 1 LSB = FS/16,384 = 6 V/16,384 = 366 μV.

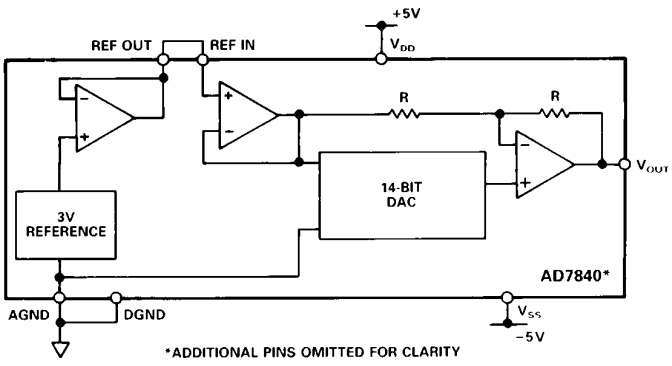


Figure 5. AD7840 Basic Connection Diagram

Table II. Ideal Input/Output Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
0 1 1 1 1 1 1 1 1 1 1 1 1 1	+2.999634 V
0 1 1 1 1 1 1 1 1 1 1 1 1 0	+2.999268 V
0 0 0 0 0 0 0 0 0 0 0 0 0 1	+0.000366 V
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 V
1 1 1 1 1 1 1 1 1 1 1 1 1 1	–0.000366 V
1 0 0 0 0 0 0 0 0 0 0 0 0 1	–2.999634 V
1 0 0 0 0 0 0 0 0 0 0 0 0 0	–3 V

*Assuming REF IN = +3 V.

The output voltage can be expressed in terms of the input code, N, using the following expression:

$$V_{OUT} = \frac{2 \times N \times REFIN}{16384} - 8192 \le N \le +8191$$

INTERFACE LOGIC INFORMATION

The AD7840 contains two 14-bit latches, an input latch and a DAC latch. Data can be loaded to the input latch in one of two basic interface formats. The first is a parallel 14-bit wide data word; the second is a serial interface where 16 bits of data are serially clocked into the input latch. In the parallel mode, $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the loading of data. When the serial data format is selected, data is loaded using the SCLK, $\overline{\text{SYNC}}$ and SDATA serial inputs. Data is transferred from the input latch to the DAC latch under control of the $\overline{\text{LDAC}}$ signal. Only the data in the DAC latch determines the analog output of the AD7840.

Parallel Data Format

Table III shows the truth table for AD7840 parallel mode operation. The AD7840 normally operates with a parallel input data format. In this case, all 14 bits of data (appearing on data inputs D13 (MSB) through D0 (LSB)) are loaded to the AD7840 input latch at the same time. $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the loading of this data. These control signals are level-triggered; therefore, the input latch can be made transparent by holding both signals at a logic low level. Input data is latched into the input latch on the rising edge of $\overline{\text{CS}}$ or $\overline{\text{WR}}$.

The DAC latch is also level triggered. The DAC output is normally updated on the falling edge of the $\overline{\text{LDAC}}$ signal. However, both latches cannot become transparent at the same time. Therefore, if $\overline{\text{LDAC}}$ is hardwired low, the part operates as follows; with $\overline{\text{LDAC}}$ low and $\overline{\text{CS}}$ and $\overline{\text{WR}}$ high, the DAC latch is transparent. When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ go low (with $\overline{\text{LDAC}}$ still low), the input latch becomes transparent but the DAC latch is disabled. When $\overline{\text{CS}}$ or $\overline{\text{WR}}$ return high, the input latch is locked out and the DAC latch becomes transparent again and the DAC output is updated. The write cycle timing diagram for parallel data is shown in Figure 6. Figure 7 shows the simplified parallel input control logic for the AD7840.

Table III. Parallel Mode Truth Table

$\overline{CS}$	$\overline{WR}$	$\overline{LDAC}$	Function
H	X	H	} Both Latches Latched
X	H	H	
L	L	H	Input Latch Transparent
H	H	L	} Input Latch Latched
H	X	L	} DAC Latch Transparent
X	H	L	} Analog Output Updated
↓	↓	L	Input Latch Transparent DAC Latch Data Transfer Inhibited
L	↑	L	} Input Latch Is Latched
↑	L		} DAC Latch Data Transfer Occurs

X = Don't Care

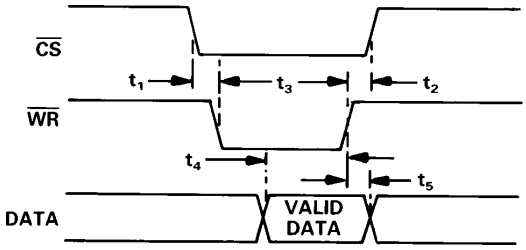


Figure 6. Parallel Mode Timing Diagram

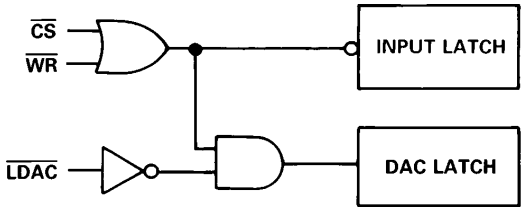


Figure 7. AD7840 Simplified Parallel Input Control Logic

Serial Data Format

The serial data format is selected for the AD7840 by connecting the $\overline{CS}$/SERIAL line to –5 V. In this case, the $\overline{WR}$/$\overline{SYNC}$, D13/SDATA, D12/SCLK, D11/FORMAT and D10/JUSTIFY pins all assume their serial functions. The unused parallel inputs should not be left unconnected to avoid noise pickup. Serial data is loaded to the input latch under control of SCLK, $\overline{SYNC}$ and SDATA. The AD7840 expects a 16-bit stream of serial data on its SDATA input. Serial data must be valid on the falling edge of SCLK. The $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7840 that valid serial data will be available for the next 16 falling edges of SCLK. Figure 8 shows the timing diagram for serial data format.

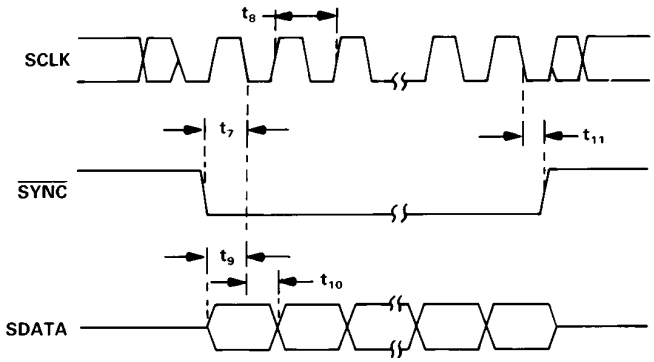


Figure 8. Serial Mode Timing Diagram

Although 16 bits of data are clocked into the AD7840, only 14 bits go into the input latch. Therefore, two bits in the stream are don't cares since their value does not affect the input latch data. The order and position in which the AD7840 accepts the 14 bits of input data depends upon the FORMAT and JUSTIFY inputs. There are four different input data modes which can be chosen (see Table I in the Pin Function Description section).

The first mode (M1) assumes that the first two bits of the input data stream are don't cares, the third bit is the LSB and the last (or 16th bit) is the MSB. This mode is chosen by tying both the FORMAT and JUSTIFY pins to a logic 0. The second mode (M2; FORMAT = 0, JUSTIFY = 1) assumes that the first bit in the data stream is the LSB, the fourteenth bit is the MSB and the last two bits are don't cares. The third mode (M3; FORMAT= 1, JUSTIFY 0) assumes that the first two bits in the stream are again don't cares, the third bit is now the MSB and the sixteenth bit is the LSB. The final mode (M4; FORMAT = 1, JUSTIFY= 1) assumes that the first bit is the MSB, the fourteenth bit is the LSB and the last two bits of the stream are don't cares.

As in the parallel mode, the $\overline{\text{LDAC}}$ signal controls the loading of data to the DAC latch. Normally, data is loaded to the DAC latch on the falling edge of $\overline{\text{LDAC}}$. However, if $\overline{\text{LDAC}}$ is held low, then serial data is loaded to the DAC latch on the sixteenth falling edge of SCLK. If $\overline{\text{LDAC}}$ goes low during the transfer of serial data to the input latch, no DAC latch update takes place on the falling edge of $\overline{\text{LDAC}}$. If $\overline{\text{LDAC}}$ stays low until the serial transfer is completed, then the update takes place on the sixteenth falling edge of SCLK. If $\overline{\text{LDAC}}$ returns high before the serial data transfer is completed, no DAC latch update takes place. Figure 9 shows the simplified serial input control logic for the AD7840.

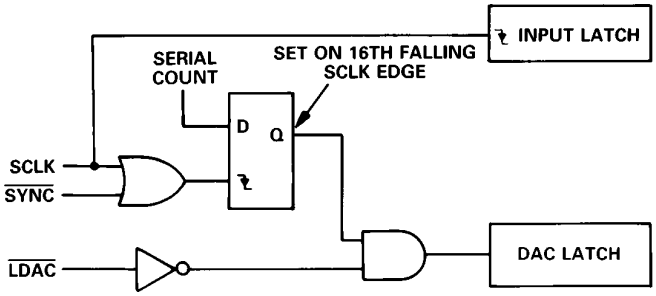


Figure 9. AD7840 Simplified Serial Input Control Logic

AD7840 DYNAMIC SPECIFICATIONS

The AD7840 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for the signal processing applications such as speech synthesis, servo control and high speed modems. These applications require information on the DAC's effect on the spectral content of the signal it is creating. Hence, the parameters for which the AD7840 is specified include signal-to-noise ratio, harmonic distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave output is given by

$$SNR = (6.02N + 1.76)\ dB \qquad (1)$$

where N is the number of bits. Thus for an ideal 14-bit converter, SNR = 86 dB.

Figure 10 shows a typical 2048 point Fast Fourier Transform (FFT) plot of the AD7840KN with an output frequency of 1 kHz and an update rate of 100 kHz. The SNR obtained from this graph is 81.8 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

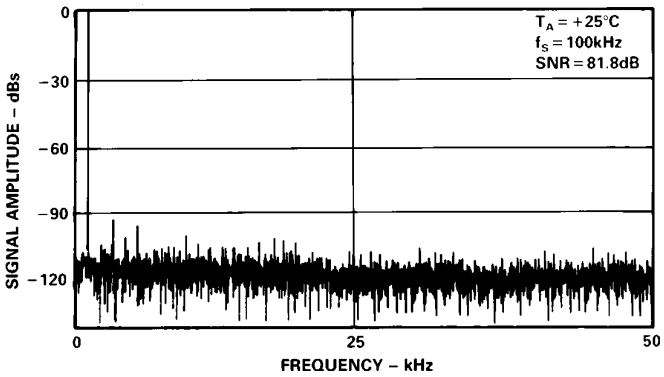


Figure 10. AD7840 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2) it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \qquad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7840, total harmonic distortion (THD) is defined as

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the 2048-point FFT plot.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the DAC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

Testing the AD7840

A simplified diagram of the method used to test the dynamic performance specifications is outlined in Figure 11. Data is loaded to the AD7840 under control of the microcontroller and associated logic at a 100 kHz update rate. The output of the AD7840 is applied to a ninth order, 50 kHz, low-pass filter. The output of the filter is in turn applied to a 16-bit accurate digitizer. This digitizes the signal and the microcontroller generates an FFT plot from which the dynamic performance of the AD7840 can be evaluated.

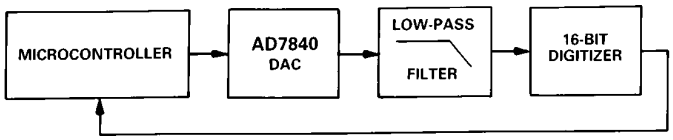


Figure 11. AD7840 Dynamic Performance Test Circuit

The digitizer sampling is synchronized with the AD7840 update rate to ease FFT calculations. The digitizer samples the AD7840 after the output has settled to its new value. Therefore, if the digitizer was to sample the output directly it would effectively be sampling a dc value each time. As a result, the dynamic performance of the AD7840 would not be measured correctly. Using the digitizer directly on the AD7840 output would give better results than the actual performance of the AD7840. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7840 is measured.

Some applications will require improved performance versus frequency from the AD7840. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 12 will extend the very good performance of the AD7840 to 20 kHz.

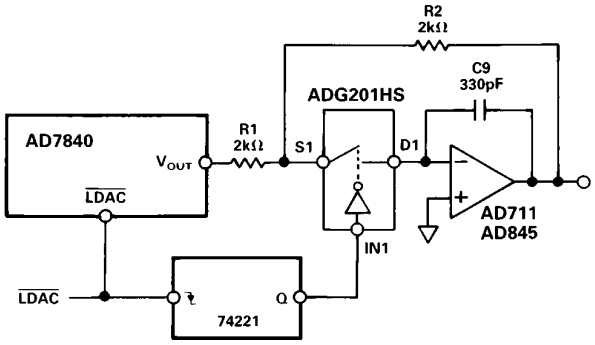


Figure 12. Sample-and-Hold Circuit

Other applications will already have an inherent sample-and-hold function following the AD7840. An example of this type of application is driving a switched-capacitor filter where the updating of the DAC is synchronized with the switched-capacitor filter. This inherent sample-and-hold function also extends the frequency range performance of the AD7840.

Performance versus Frequency

The typical performance plots of Figures 13 and 14 show the AD7840's performance over a wide range of input frequencies at an update rate of 100 kHz. The plot of Figure 13 is without a sample-and-hold on the AD7840 output while the plot of Figure 14 is generated with the sample-and-hold circuit of Figure 12 on the output.

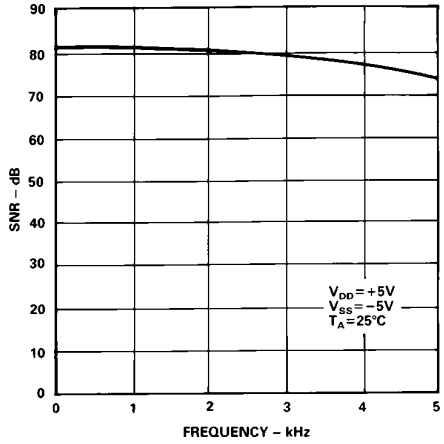


Figure 13. Performance vs. Frequency (No Sample-and-Hold)

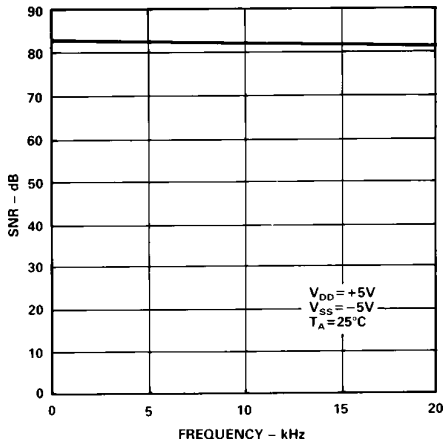


Figure 14. Performance vs. Frequency (with Sample-and-Hold)

MICROPROCESSOR INTERFACING

The AD7840 logic architecture allows two interfacing options for interfacing the part to microprocessor systems. It offers a 14-bit wide parallel format and a serial format. Fast pulse widths and data setup times allow the AD7840 to interface directly to most microprocessors including the DSP processors. Suitable interfaces to various microprocessors are shown in Figures 15 to 23.

Parallel Interfacing

Figures 15 to 17 show interfaces to the DSP processors, the ADSP-2100, the TMS32010 and TMS32020. An external timer controls the updating of the AD7840. Data is loaded to the AD7840 input latch using the following instructions:

ADSP-2100: DM(DAC) = MR0
TMS32010: OUT DAC,D
TMS32020: OUT DAC,D
MR0 = ADSP-2100 MR0 Register
D = Data Memory Address
DAC = AD7840 Address

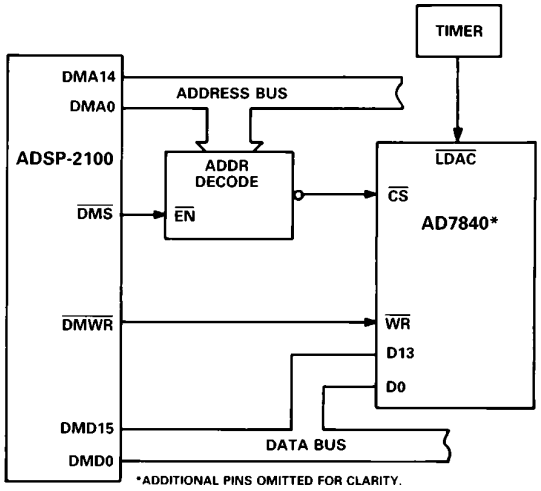


Figure 15. AD7840–ADSP-2100 Parallel Interface

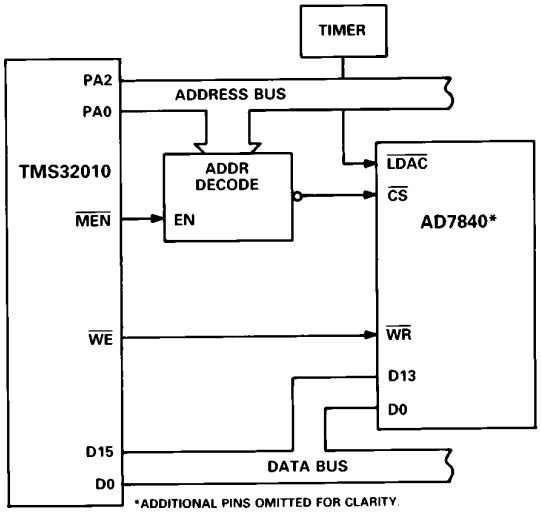


Figure 16. AD7840–TMS32010 Parallel Interface

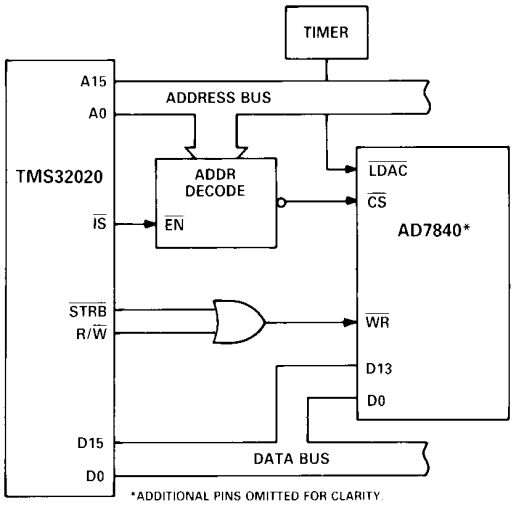


Figure 17. AD7840–TMS32020 Parallel Interface

Some applications may require that the updating of the AD7840 DAC latch be controlled by the microprocessor rather than the external timer. One option (for double-buffered interfacing) is to decode the AD7840 $\overline{LDAC}$ from the address bus so that a write operation to the DAC latch (at a separate address than the input latch) updates the output. An example of this is shown in the 8086 interface of Figure 18. Note that connecting the $\overline{LDAC}$ input to the $\overline{CS}$ input will not load the DAC latch correctly since both latches cannot he transparent at the same time.

AD7840–8086 Interface

Figure 18 shows an interface between the AD7840 and the 8086 microprocessor. For this interface, the $\overline{LDAC}$ input is derived from a decoded address. If the least significant address line, A0, is decoded then the input latch and the DAC latch can reside at consecutive addresses. A move instruction loads the input latch while a second move instruction updates the DAC latch and the AD7840 output. The move instruction to load a data word WXYZ to the input latch is as follows:

MOV DAC,#YZWX
DAC = AD7840 Address

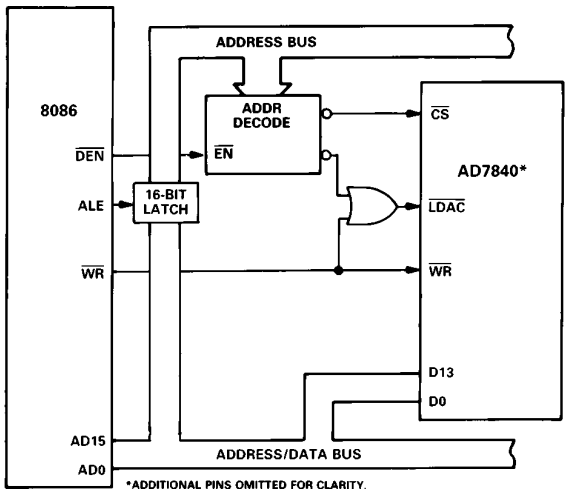


Figure 18. AD7840–8086 Parallel Interface

AD7840–68000 Interface
An interface between the AD7840 and the 68000 microprocessor is shown in Figure 19. In this interface example, the $\overline{LDAC}$ input is hardwired low. As a result the DAC latch and analog output are updated on the rising edge of $\overline{WR}$. A single move instruction, therefore, loads the input latch and updates the output.

MOVE.W D0,$DAC
D0 = 68000 D0 Register
DAC = AD7840 Address

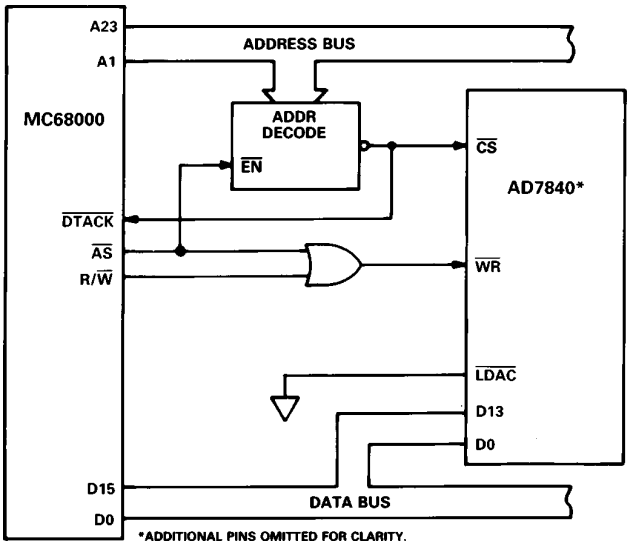


Figure 19. AD7840–MC68000 Parallel Interface

Serial Interfacing
Figures 20 to 23 show the AD7840 configured for serial interfacing with the $\overline{CS}$ input hardwired to –5 V. The parallel bus is not activated during serial communication with the AD7840.

AD7840–ADSP-2101/ADSP-2102 Serial Interface
Figure 20 shows a serial interface between the AD7840 and the ADSP-2101/ADSP-2102 DSP processor. Also included in the interface is the AD7870, a 12-bit A/D converter. An interface such as this is suitable for modem and other applications which have a DAC and an ADC in serial communication with a microprocessor.

The interface uses just one of the two serial ports of the ADSP-2101/ADSP-2102. Conversion is initiated on the AD7870 at a fixed sample rate (e.g., 9.6 kHz) which is provided by a timer or clock recovery circuitry. While communication takes place between the ADC and the ADSP-2101/ ADSP-2102, the AD7870 $\overline{SSTRB}$ line is low. This $\overline{SSTRB}$ line is used to provide a frame synchronization pulse for the AD7840 $\overline{SYNC}$ and ADSP-2101/ADSP-2102 TFS lines. This means that communication between the processor and the AD7840 can only take place while the AD7870 is communicating with the processor. This arrangement is desirable in systems such as modems where the DAC and ADC communication should be synchronous.

The use of the AD7870 SCLK for the AD7840 SCLK and ADSP-2101/ADSP-2102 SCLK means that only one serial port of the processor is used. The serial clock for the AD7870 must be set for continuous clock for correct operation of this interface.

Data from the ADSP-2101/ADSP-2102 is valid on the falling edge of SCLK. The $\overline{LDAC}$ input of the AD7840 is permanently low so the update of the DAC latch and analog output takes place on the sixteenth falling edge of SCLK (with $\overline{SYNC}$ low). The FORMAT pin of the AD7840 must be tied to +5 V and the JUSTIFY pin tied to DGND for this interface to operate correctly.

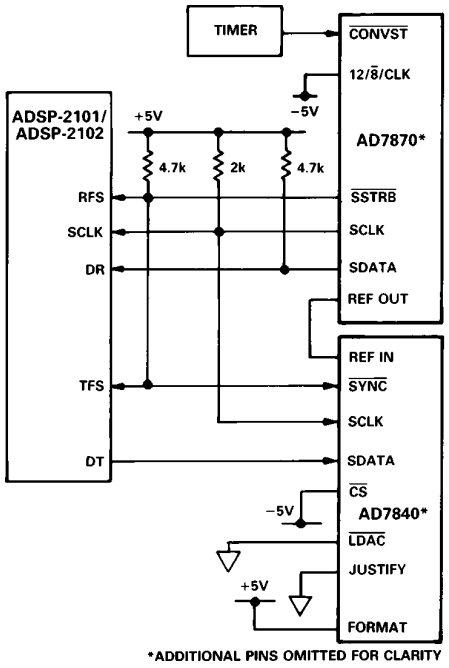


Figure 20. Complete DAC/ADC Serial Interface

AD7840–DSP56000 Serial Interface
A serial interface between the AD7840 and the DSP56000 is shown in Figure 21. The DSP56000 is configured for normal mode synchronous operation with gated clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a 0. SCK is internally generated on the DSP56000 and applied to the AD7840 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{SYNC}$ input of the AD7840.

The $\overline{LDAC}$ input of the AD7840 is connected to DGND so the update of the DAC latch takes place on the sixteenth falling edge of SCLK. As with the previous interface, the FORMAT pin of the AD7840 must be tied to +5 V and the JUSTIFY pin tied to DGND.

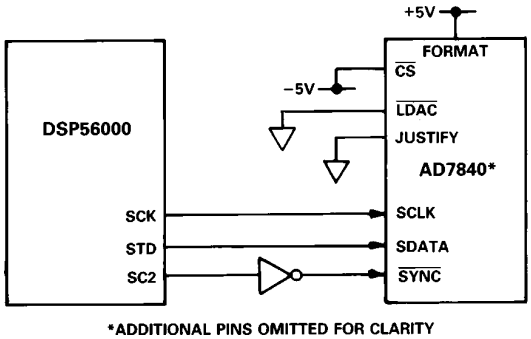


Figure 21. AD7840–DSP56000 Serial Interface

AD7840–TMS32020 Serial Interface

Figure 22 shows a serial interface between the AD7840 and the TMS32020 DSP processor. In this interface, the CLKX and FSX pin of the TMS32020 are generated from the clock/timer circuitry. The same clock/timer circuitry generates the $\overline{\text{LDAC}}$ signal of the AD7840 to synchronize the update of the output with the serial transmission. The FSX pin of the TMS32020 must be configured as an input.

Data from the TMS32020 is valid on the falling edge of CLKX. Once again, the FORMAT pin of the AD7840 must be tied to +5 V while the JUSTIFY pin must be tied to DGND.

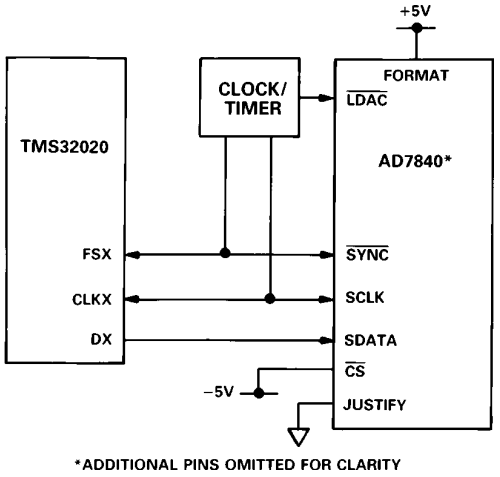


Figure 22. AD7840–TMS32020 Serial Interface

AD7840–NEC7720 Serial Interface

A serial interface between the AD7840 and the NEC7720 is shown in Figure 23. The serial clock must be inverted before being applied to the AD7840 SCLK input because data from the processor is valid on the rising edge of SCK.

The NEC7720 is programmed for the LSB to be the first bit in the serial data stream. Therefore, the AD7840 is set up with the FORMAT pin tied to DGND and the JUSTIFY pin tied to +5 V.

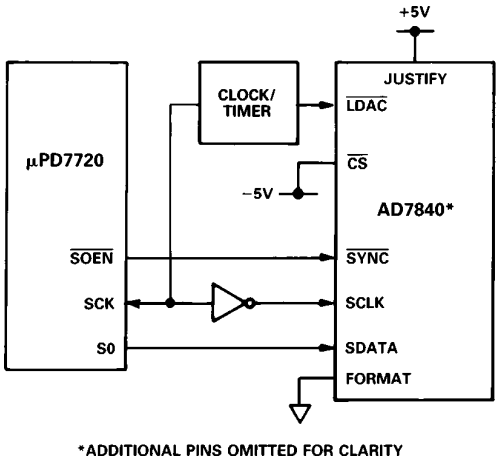


Figure 23. AD7840–NEC7720 Serial Interface

APPLYING THE AD7840

Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7840 works on an LSB size of 366 μV. Therefore, the designer must be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as the switching spikes can feed through to the on-chip amplifier. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any high performance converter, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this star ground as close as possible to the AD7840 as shown in Figure 24. Connect all analog grounds to this star ground and also connect the AD7840 DGND pin to this ground. Do not connect any other digital grounds to this analog ground point.

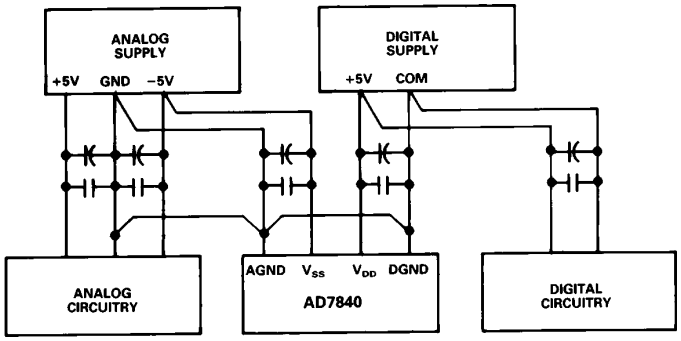


Figure 24. Power Supply Grounding Practice

Low impedance analog and digital power supply common returns are essential to low noise operation of high performance converters. Therefore, the foil width for these tracks should be kept as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layouts of Figures 27 and 28 have both analog and digital ground planes which are kept separated and only joined at the star ground close to the AD7840.

NOISE

Keep the signal leads on the V_{OUT} signal and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible, use a shielded cable between the DAC output and its destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

DATA ACQUISITION BOARD

Figure 25 shows the AD7840 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 26 to 28. The board layout has three interface ports: one serial and two parallel. One of the parallel ports is directly compatible with the ADSP-2100 evaluation board expansion connector.

Some systems will require the addition of a re-construction filter on the output of the AD7840 to complete the data acquisition system. There is a component grid provided near the analog output on the PCB which may be used for such a filter or any other output conditioning circuitry. To facilitate this option, there is a shorting plug (labeled LK1 on the PCB) on the analog output track. If this shorting plug is used, the analog output connects to the output of the AD7840; otherwise this shorting plug can be omitted and a wire link used to connect the analog output to the PCB component grid.

The board also contains a simple sample-and-hold circuit which can be used on the output of the AD7840 to extend the very good performance of the AD7840 over a wider frequency range. A second wire link (labelled LK2 on the PCB) connects V_{OUT} (SKT1) to either the output of this sample-and-hold circuit or directly to the output of the AD7840.

INTERFACE CONNECTIONS

There are two parallel connectors, labeled SKT4 and SKT6, and one serial connector, labeled SKT5. A shorting plug option (LK8 in Figure 25) on the AD7840 $\overline{CS}$/SERIAL input configures the DAC for the appropriate interface (see Pin Function Description).

SKT6 is a 96-contact (3-row) Eurocard connector which is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded chip enable outputs labeled $\overline{ECE1}$ to $\overline{ECE8}$. $\overline{ECE6}$ is used to drive the AD7840 $\overline{CS}$ input on the data acquisition board. To avoid selecting on-board sockets at the same time, LK6 on the ADSP-2100 board must be removed. The AD7840 and ADSP-2100 data lines are aligned for left justified data transfer.

SKT4 is a 26-way (2-row) IDC connector. This connector contains the same signal contacts as SKT6 and in addition contains decoded R/$\overline{W}$ and $\overline{STRB}$ inputs which are necessary for TMS32020 interfacing. This decoded $\overline{WR}$ can be selected via LK4. The pinout for this connector is shown in Figure 29.

SKT5 is a nine-way D-type connector which is meant for serial interfacing only. The evaluation board has the facility to invert $\overline{SYNC}$ line via LK7. This is necessary for serial interfacing between the AD7840 and DSP processors such as the DSP56000. The SKT5 pinout is shown in Figure 30.

SKT1, SKT2 and SKT3 are three BNC connectors which provide connections for the analog output, the $\overline{LDAC}$ input and an external reference input. The use of an external reference is optional; the shorting plug (LK3) connects the REF IN pin to either this external reference or to the AD7840's own internal reference.

Wire links LK5 and LK6 connect the D11 and D10 inputs to the data lines for parallel operation. In the serial mode, these links allow the user to select the required format and justification for serial data (see Table I).

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5 V digital supply. Connections to the analog supplies are made directly to the PCB as shown on the silkscreen in Figure 26. The connections are labelled V+ and V– and the range for both of these supplies is 12 V to 15 V. Connection to the 5 V digital supply is made through any of the connectors (SKT4 to SKT6). The –5 V analog supply required by the AD7840 is generated from a voltage regulator on the V– power supply input (IC5 in Figure 25).

SHORTING PLUG OPTIONS

There are eight shorting plug options which must be set before using the board. These are outlined below:

LK1	Connects the analog output to SKT1. The analog output may also be connected to a component grid for signal conditioning.
LK2	Selects either the AD7840 V_{OUT} or the sample-and-hold output.
LK3	Selects either the internal or external reference.
LK4	Selects the decoded R/$\overline{W}$ and $\overline{STRB}$ inputs for TMS32020 interfacing.
LK5	Configures the D11/FORMAT input.
LK6	Configures the D10/JUSTIFY input.
LK7	Selects either the inverted or noninverted $\overline{SYNC}$.
LK8	Selects either parallel or serial interfacing.

COMPONENT LIST

IC1	AD7840 Digital-to-Analog Converter
IC2	AD711 Op Amp
IC3	ADG201HS High Speed Switch
IC4	74HC221 Monostable
IC5	79L05 Voltage Regulator
IC6	74HC02
C1, C3, C5, C7, C11, C13, C15, C17	10 µF Capacitors
C2, C4, C6, C8, C12, C14, C16, C18	0.1 µF Capacitors
C9	330 pF Capacitor
C10	68 pF Capacitor
R1, R2	2.2 kΩ Resistors
R3	15 kΩ Resistor
RP1, RP2	100 kΩ Resistor Packs
LK1, LK2, LK3, LK4, LK5, LK6, LK7, LK8	Shorting Plugs
SKT1, SKT2, SKT3	BNC Sockets
SKT4	26-Contact (2-Row) IDC Connector
SKT5	9-Contact D-Type Connector
SKT6	96-Contact (3-Row) Eurocard Connector

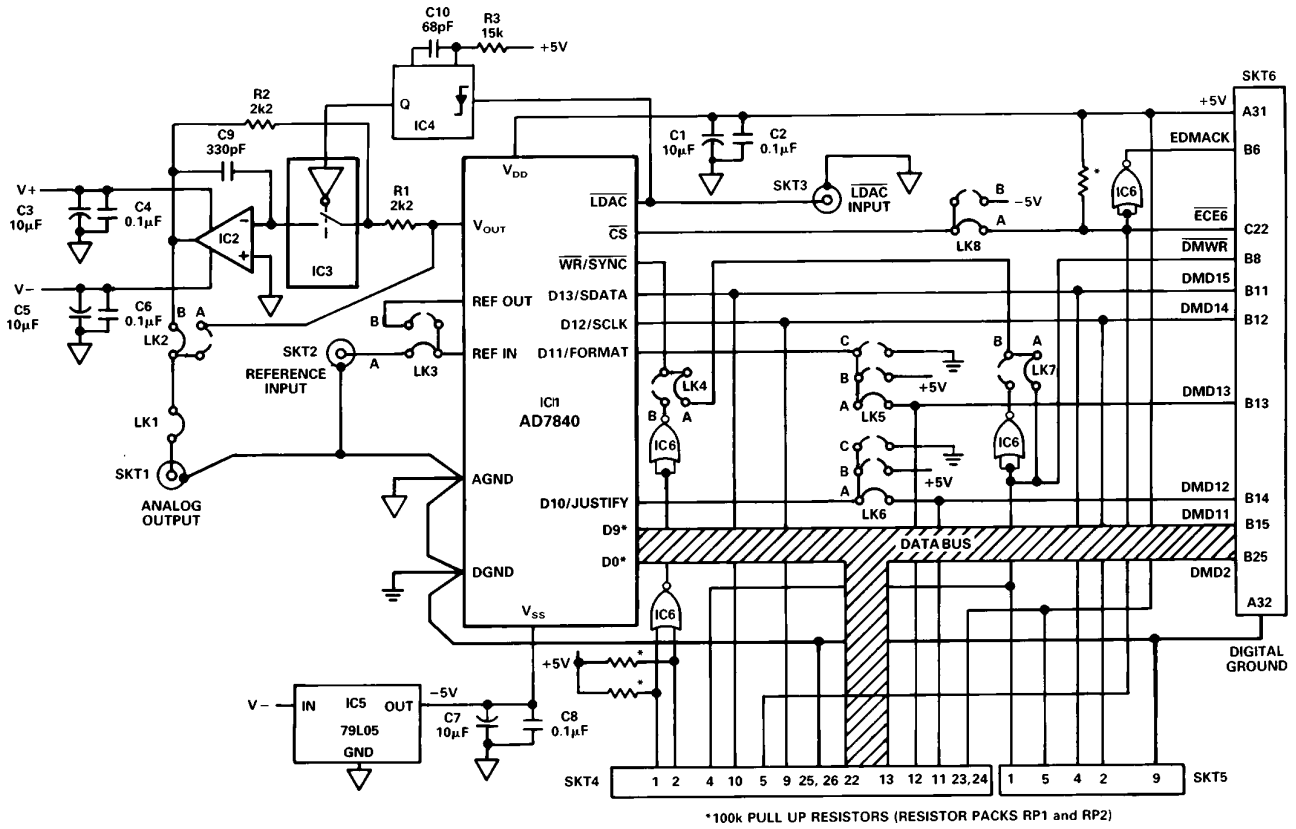


Figure 25. Data Acquisition Circuit Using the AD7840

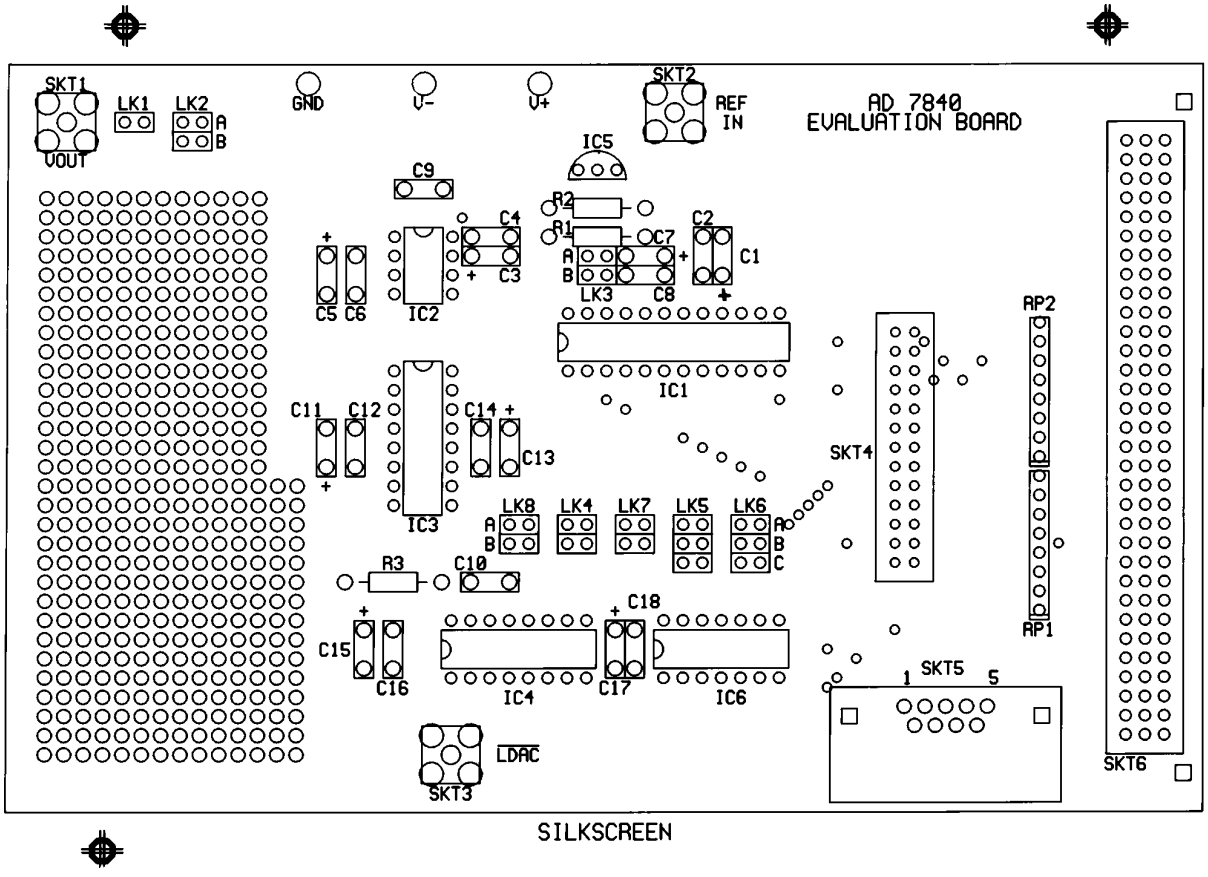


Figure 26. PCB Silkscreen for Figure 25

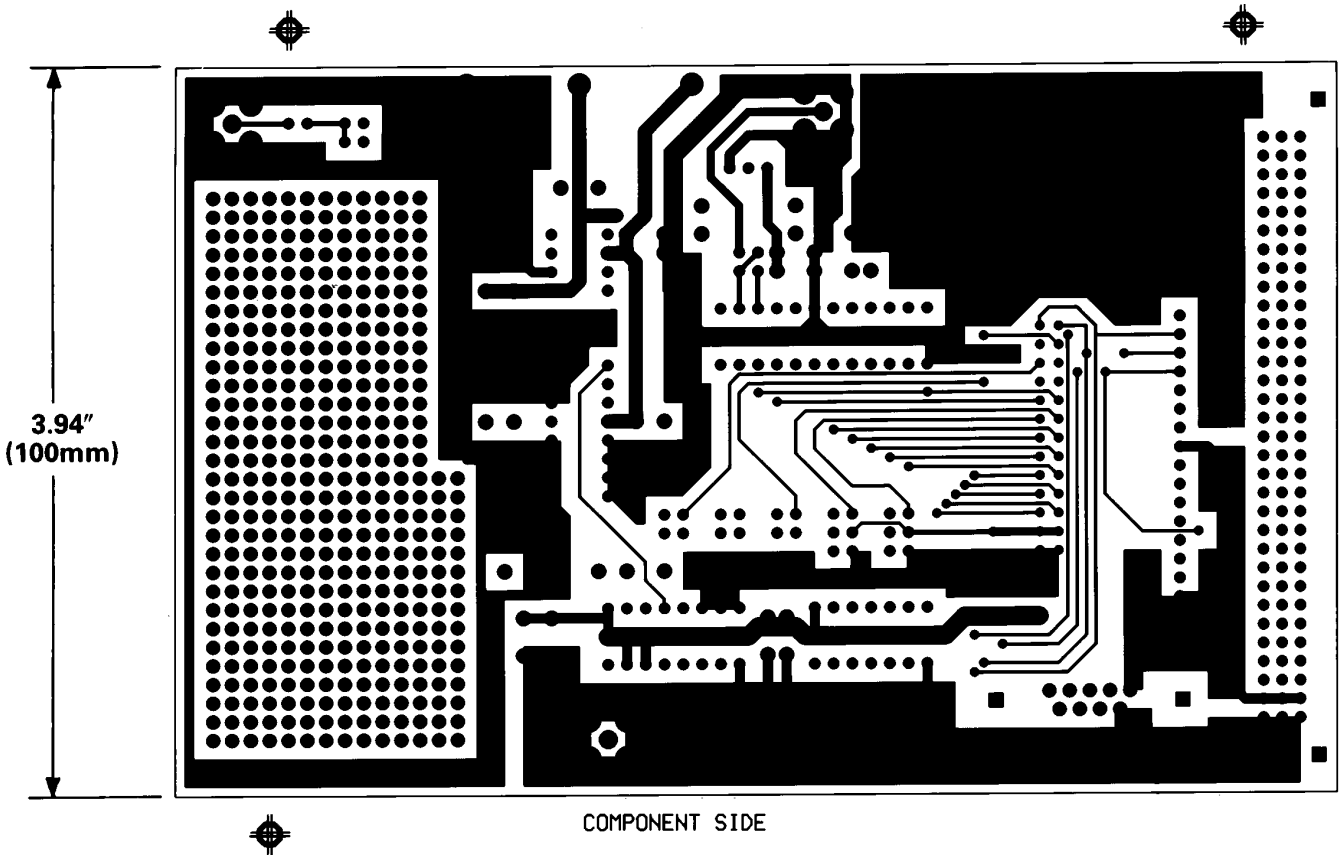


Figure 27. PCB Component Side Layout for Figure 25

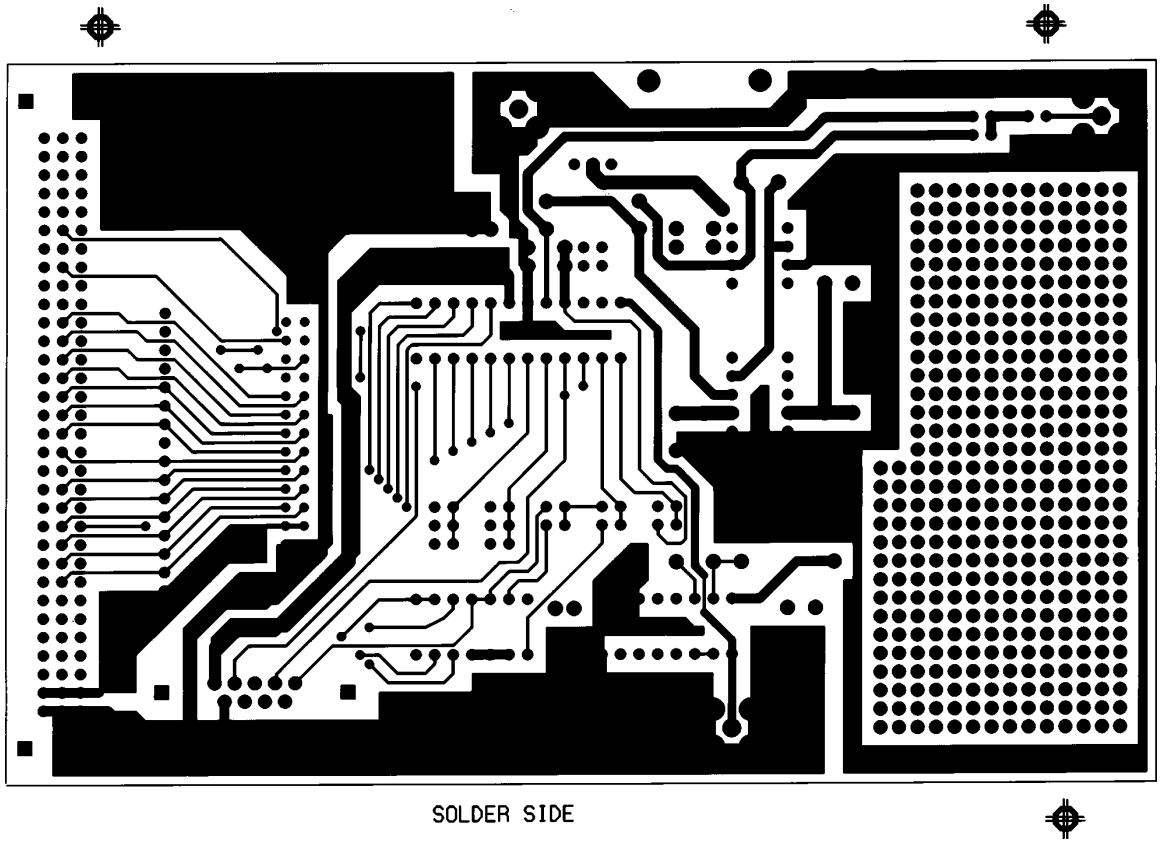


Figure 28. PCB Solder Side Layout for Figure 25

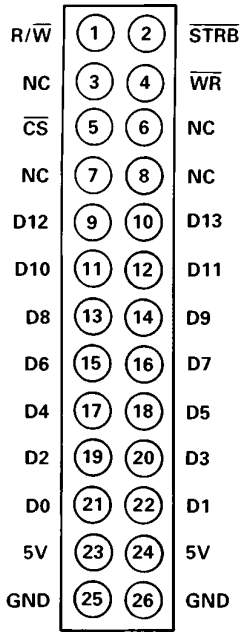


Figure 29. SKT4, IDC Connector Pinout

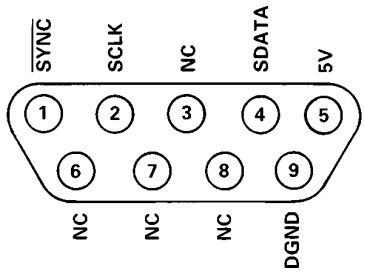
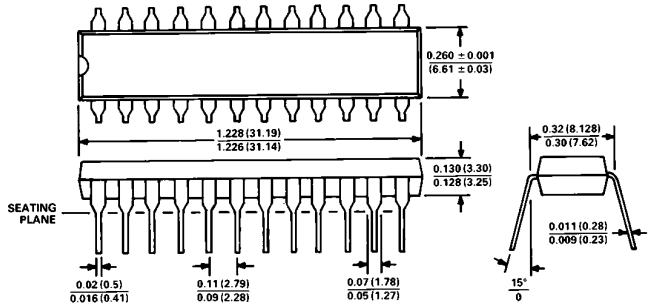


Figure 30. SKT5, D-Type Connector Pinout

OUTLINE DIMENSIONS

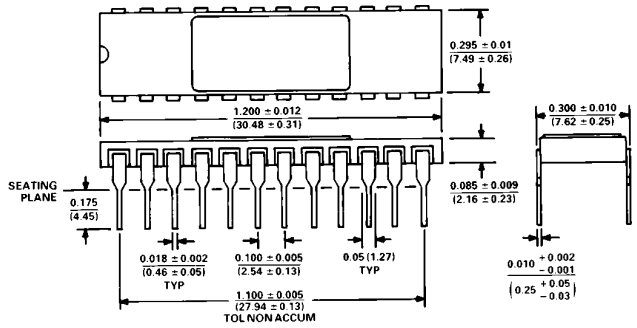
Dimensions shown in inches and (mm).

Plastic DIP (N-24)



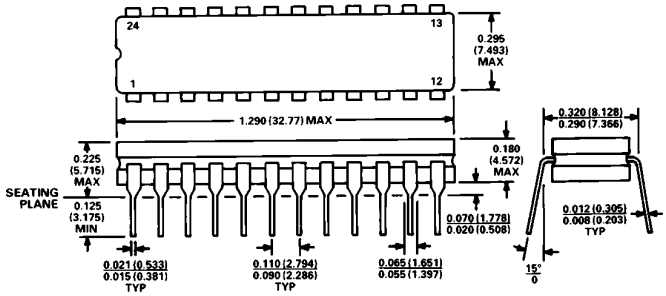
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

Ceramic DIP (D-24A)



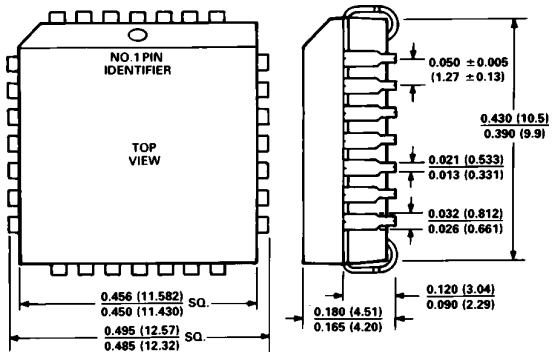
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-385 TO REQUIREMENTS.
3. METAL LID IS CONNECTED TO DGND.

Cerdip (Q-24)



1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

PLCC (P-28A)



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11- Les CNA indirects séquentiels

Les convertisseurs numériques analogiques directs sont essentiellement constitués de circuits analogiques. Leurs performances en termes du temps de conversion et précision sont excellentes, mais leur réalisation pratique est très coûteuse. Dans certaines applications, il n'est pas nécessaire de travailler avec un nombre de bits élevé et d'effectuer la conversion rapidement. Pour ces applications, il sera intéressant d'utiliser des méthodes séquentielles pour effectuer la conversion, qui conduisent à des configurations où les circuits logiques occupent une grande place.

11.1 Les CNA indirects à intégration d'impulsion

Convertisseur Numérique rapport cyclique

Principe

Le principe de ce convertisseur est de généré un signal périodique à rapport cyclique égal à τ/T figure 21. En effet, durant un intervalle de temps T, on génère une impulsion rectangulaire de largeur τ proportionnelle à la valeur numérique d'entrée N. L'intégration de ces impulsions donnera une valeur moyenne de la tension de sortie proportionnelle à N, cette opération d'intégration est assure par un filtre passe bas.

Ce type de convertisseur comporte deux parties:

- Une partie digitale: pour générer l'impulsion de durée proportionnelle au mot d'entrée N durant l'intervalle de temps T.

- Une partie analogique: pour le filtrage du signal (un filtre passe bas).

La conversion d'un nombre N à tension n'est pas directe, mais elle doit passer par ces deux modules c'est pour cette raison que nous l'avons appel convertisseur indirect.

Étude du fonctionnement

Le convertisseur est essentiellement composé d'un compteur à n bits pour fixer la période du signal, d'un registre tampon pour fixer la valeur de N constamment disponible, un décompteur de n bits, d'une porte analogique (interrupteur) délivrant une tension E et un étage de sortie avec un filtre passe bas (figure 20).

Figure 20 : convertisseur numérique rapport - cyclique

L'horloge de fréquence F_0 ($F_0 = 1/T_0$) pilote le compteur; lorsque sa valeur est maximum, il délivre une impulsion de chargement de l'information

d'entrée N dans le décompteur. Si cette valeur est différente de 0, l'horloge du décompteur est autorisée et il y a fermeture de l'interrupteur (porte). Le décompteur décompte à partir de la valeur N, et lorsqu'il atteint la valeur 0, son horloge est bloquée et l'interrupteur s'ouvre. Lorsque le compteur atteint à nouveau la valeur maximum les cycles de chargement et du comptage recommencent de nouveau. On présente à la figure 21 le diagramme des temps d'un convertisseur numérique rapport - cyclique à 3 bits avec une application pour N = 5 et une autre pour N = 2.

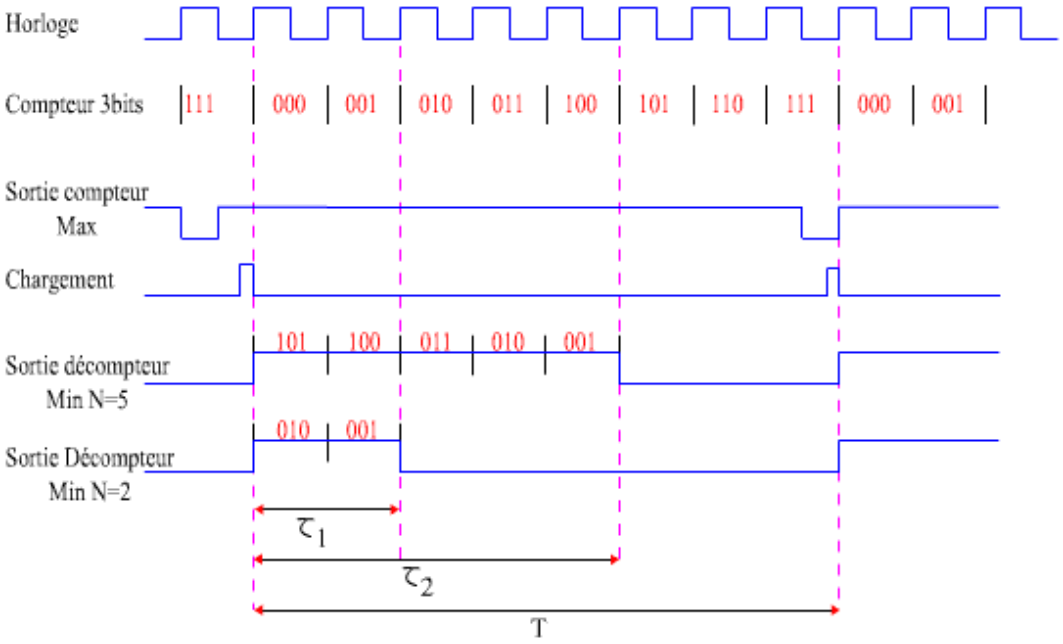


Figure 21: diagramme des signaux

Calcul de la tension de sortie

Soient :

T : période de conversion

τ : largeur de l'impulsion de commande de l'interuupteur

N : Valeur numérique d'entrée

La composante continue du signal de sortie a pour expression :

$$Vs = Eref \frac{\tau}{T}$$

$$\tau = N.T_0 \text{ et } T_0 = \frac{1}{F_0}$$

$$T = 2^n.T_0$$

$$Vs = Eref \frac{N.T_0}{2^n.T_0} = \frac{Eref}{2^n} N$$

$$Vs = \frac{Eref}{2^n} N$$

Evaluation

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

12- Les paramètres des CNAs :

Paramètres dus aux erreurs introduites par le système

Ces sont les erreurs introduites par les différents éléments du convertisseur (réseau de résistances, interrupteurs, amplificateur de sortie ..).

Erreur de décalage (Offest error)

Elle caractérise l'écart entre la tension nulle correspondant du code 0..0 et la tension de sortie réelle. Cette erreur est due aux parties analogiques du convertisseur; par exemple le courant de fuite dans les interrupteurs. Généralement, elle peut être corrigée en ajustant la valeur d'un potentiomètre externe (optional zero offset trim). L'erreur de décalage s'exprime en pourcentage de la pleine échelle ou en fraction de quantum ou •V (• A) (figure 29).

Figure 29 : Erreur de décalage

Erreur de gain (ou d'échelle) (Gain error , Gain Variation, Scale Factor error)

Cette erreur se traduit par une pente de la courbe réelle de transfert différente de la pente théorique. Cette erreur est fonction de la précision avec laquelle peuvent être réalisés tous les éléments. Cette erreur s'exprime en pourcentage de la pleine échelle (figure 30).

Figure 30 : Erreur de gain

Erreur de linéarité (Non linearity)

La non linéarité est l'écart maximum ε_i observé entre la caractéristique de transfert du convertisseur et la ligne droite joignant les deux points extrêmes, d'après la figure 31. Elle s'exprime en pourcentage de la pleine échelle ou en fraction de quantum.

Figure 31 : Erreur de non linéarité

Erreur de Linéarité différentielle (differentiel linearity error)

La transition d'un code à un code adjacent pour un CNA idéal entraîne une variation de 1 quantum de la tension. Pour un CNA réel cette variation peut être différente et vaut ΔV; l'erreur de non linéarité différentielle égale à:$|\ \Delta V - q\ |$.

Monotonicité(Monotonicity)

Un convertisseur N/A est dit monotone lorsque la sortie suit rigoureusement le sens de variation du signal d'entrée. C'est à dire, si N augmente donc Vs (Is) doit augmenter; de même si N diminue Vs (Is) doit diminuer. Si ce n'est pas le cas, c'est à dire pour une augmentation de la valeur binaire de 1 LSB, donne une diminution du signal de sortie par rapport à la valeur numérique précédente, on dit qu'il y a non monotonicité comme le montre la figure 32. La non monotonicité est dûe à une non linéarité différentielle dépassant ±q.

Figure 32: Non monotonicité

Précision (Accurancy)

Elle tient compte de toutes les erreurs citées, donc c'est une fonction de plusieurs paramètres. Elle caractérise l'écart entre la valeur effectivement obtenue en sortie (lue) et la valeur théorique, rapportée à la pleine échelle. Elle s'exprime en pourcentage de la pleine échelle ou en fraction de LSB.

Exemple: ±0.2 % P.E ou ± 1/2 LSB.

Etats transitoires (Glitches, Spikes)

Lors de la modification de l'information numérique d'entrée, des états transitoires peuvent apparaître durant quelques instants. Le signal de sortie présentera alors des pointes de tension (courant) correspondant à ces états transitoires. Par exemple le passage de l'information numérique d'entrée de la valeur 3 à 4 (011 → 100); si le MSB change avant les derniers bits, il apparaîtra l'état transitoire 111, d'où en sortie une pointe de tension (courant) comme le montre la figue 33.

Figure 33 : Etat transitoire

La valeur de l'amplitude maximum du transitoire ainsi que la durée (Skew time) sont données dans les caractéristiques du convertisseur. Pour certaines applications, il est nécessaire d'éliminer ces états transitoires. Une solution simple consiste à utiliser un circuit échantillonneur bloqueur qui a la propriété de mémoriser la valeur instantanée d'un signal analogique, sous contrôle d'une commande, comme le montre la figue 34.

Figure 34 : Association d'un CNA et E/B pour élimination des Glitches

Grandeurs d'influence

1 - Influence de la température: souvent, les spécifications sont affectées d'un coefficient de température exprimé en ppm/°c (part par million soit 10^{-6}/ C°).

2 - Influence de la dérive à long terme (long term drift): cette dérive est dûe au vieillissement des composants; la caractéristique la plus affectées est généralement l'erreur de gain.

3 - Influence aux variations de la tension d'alimentation: Le coefficient de tension exprime la variation que subit la tension de sortie pour une

variation des alimentations du convertisseur N/A Pour chaque variation d'alimentation il y a donc une variation maximum garantie de la tension de sortie, exprimé en ppm de la pleine échelle et en pourcentage de la variation de la tension d'alimentation exemple (± 1 ppm de PE %)

.

Remarques sur Les CNA de haute résolution

Pour bénéficier des grandes performances des convertisseurs N/A de haute résolution, l'utilisateur doit apporter au montage pratique un soin particulier à savoir:

- il doit distinguer la masse analogique de sortie et la masse d'alimentation analogique;

- il doit raccourcir la connexion entre la broche Iout et l'amplificateur pour minimiser les effets capacitifs, s'il recherche une grande vitesse d'établissement;

- il doit découpler, au plus prés du CNA, les deux alimentations;

- il doit bien choisir l'amplificateur opérationnel pour conserver la vitesse et la précision du dispositif.

Nous classerons ces paramètres en deux familles; à savoir les paramètres de conversions (résolution, variation du signal de sortie, temps de conversion, temps de réponse) et les paramètres dus aux erreurs introduites par le système (erreurs de gain, de décalage, de linéarité, de linéarité différentielle, monotonie, précision etc..). Nous donnons les définitions des principaux paramètres des CNA afin que vous prouviez choisir au mieux le CNA convenable à votre application et interpréter facilement les résultats des conversions obtenus.

Paramètres de conversion

Résolution

Elle peut être définie par $(1 / 2^n)n$, n étant le nombre de bits du convertisseur; Elle est donc liée au quantum: (q) (Eref / 2^n), et elle peut être définie en pourcentage de la pleine échelle (F.S.R : Full Scale Range).

Variation du signal de sortie (output voltage range or current range)

C'est la plage de variation de la tension de sortie (ou du courant) pour le convertisseur. Elle est donnée pour les deux modes de fonctionnement (unipolaire et bipolaire).

Temps de conversion (d'établissement) (Setting time)

C'est le temps nécessaire, après application de l'information numérique, pour que le signal de sortie atteigne sa valeur finale en régime établi avec une précision donnée (± ε %). En général, la variation du code d'entrée correspond à une variation à la sortie du convertisseur de 0 à la tension de pleine échelle (figure 27).

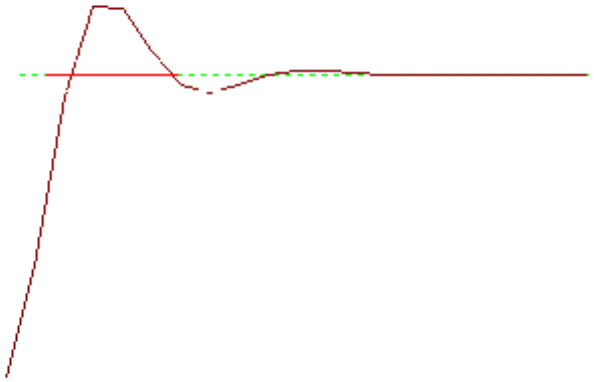


Figure 27 : Définition du temps d'établissement

Cadence de conversion

C'est le nombre maximal de conversions par seconde pour lequel les spécifications sont respectées.

Vitesse de réponse (slew rate)

C'est la vitesse de variation maximum ($\Delta V / \Delta t$) du signal de sortie lorsque celui-ci varie de la valeur minimum à la valeur maximum (figure 28).

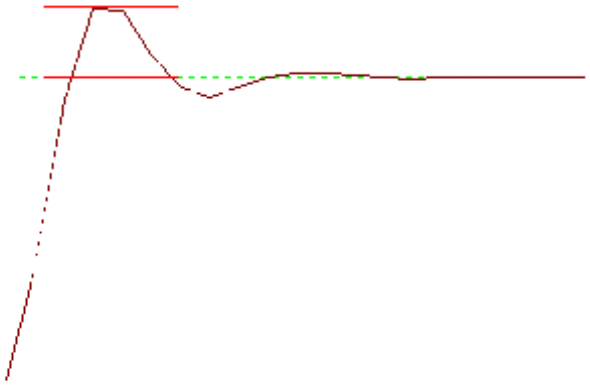


Figure 28 : Vitesse de réponse

Evaluation

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

13 - Exemples d'utilisation des CNA

Additionneur "hybride"

Deux convertisseurs numériques analogiques à sortie en courant permettent d'effectuer l'addition de deux valeurs numériques N_1 et N_2, le résultat étant exprimé en analogique. Le schéma de principe de l'additionneur est donné à la figure 35, la charge Rc doit être faible devant l'impédance de sortie des convertisseurs. Cette charge peut être remplacée par l'impédance d'entrée.

Figure 35 : Additionneur hybride

$$I_S = I_1 + I_2$$
$$I_1 = K_1 .Vref. N_1$$
$$I_2 = K_2 .Vref. N_2$$
$$K_1 = k_2 = \frac{1}{2^n}$$
$$I_S = K.Vref.(N_1 + N_2)$$
$$V_S = K.Vref.R_C .(N_1 + N_2)$$

Réalisation d'une source de tension programmable

Un Convertisseur numérique analogique associé à un amplificateur de puissance réalise une source de tension programmable comme le montre la figure 36.

Figure 36 : Source de tension programmable

Visualisation de caractères sur tube cathodique

La visualisation de caractères sur écran cathodique se fait par matrices de 35 points (5x7) ou plus. Le schéma de principe est présenté sur la figure 37. Pour expliquer le fonctionnement de ce système, nous allons analyser la séquence d'inscription de la lettre R (figure 38).

Figure 37: Schéma de principe de visualisation point par point sur CRT

Les deux convertisseurs numériques - analogiques déterminent la position en X et Y de chaque point de la matrice 35 points. L'éclairement ou extinction de chaque point de la matrice sera commandé par la tension de wehnelt du tube cathodique et programmé dans une mémoire morte ROM (Read Only Memory) appelée générateur de caractères.

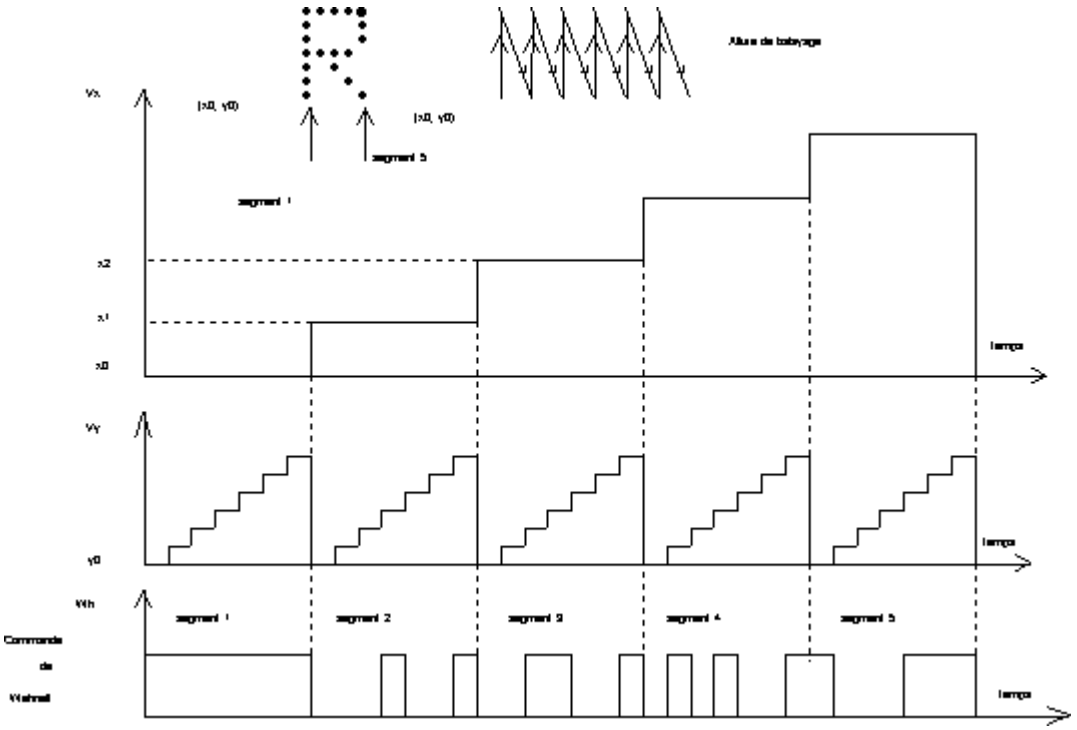


Figure 38: Séquence de la visualisation de la lettre "R" sur TRC

Amplificateur à gain variable sous commande numérique

La réalisation d'un amplificateur à gain commandé numériquement découle immédiatement des propriétés des convertisseurs N/A comme le montre la figure 39.

Figure 39 : Amplificateur à gain variable numériquement

D'après la fonction de transfert du convertisseur on peut déduire l'expression de Vs:

$$V_S = K.Vref.N$$

Si on considère que la tension de référence comme tension d'entrée, on déduit le gain de l'amplificateur:

$$G = \frac{Vs}{Vref} = K.N \quad \text{(atténuateur contrôlé par N)}$$

Si on change la valeur de N, le gain change (atténuateur contrôlé par N).

Multiplieur "hybride"

Deux convertisseurs montés en cascade permettent d'effectuer la multiplication de deux valeurs numériques et d'obtenir le résultat en analogique

figure 40

Figure 40 : Multiplieur " hybride "

$$V'_s = K_1 . Vref. N_1$$
$$Vs = K_2 V's. N_2$$
$$Vs = K_1.K_2.V'ref.N_1. N_2 \text{ avec } K_1 = k_2 = \frac{1}{2^n}$$

Réalisation d'un déphaseur à commande numérique

Le schéma de principe d'un déphaseur à commande numérique est présenté à la figure 41, les CNA1 et CNA2 sont des convertisseurs à sortie en courant.

Figure 41 : Déphaseur numérique

$I_1 = K_1 .Esin(\omega t). N_1$

$I_2 = K_2 .Ecos(\omega t). N_2$

Si : $N_1 = \cos(d)$ et $N_2 = \sin(d)$

On calcule le courant Is

$Is = I_1 + I_2 = K_1 .Esin(\omega t).\cos(d) + K_2 .Ecos(\omega t).\sin(d)$

Si : $K_1 = K_2 = K$ (même nombre de bits)

Donc :

Is = K .Esin(ωt + d) et **Vs = - R.K.Esin(ωt + d)**

Evaluation

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

Générateur de fonction analogique

Générateur de dents de scie

Le schéma de principe d'un générateur de fonction est présenté à la figure 42.

Figure 42 : Principe d'un générateur de fonction

Les valeurs numériques appliquées au convertisseur augmentent de la valeur 00..0 à la valeur 11...1. On obtient ainsi en sortie Vs, une rampe croissante en marche d'escaliers. Lorsque le compteur atteint sa valeur maximum : 11...1, il recommence à compter à partir de la valeur 00...0 et il y a génération de la rampe suivante, etc... Ce signal est ensuite filtré pour obtenir un signal en dents de scie présentant une grande

stabilité en amplitude figure 43 .

Figure 43 : Générateur de dents de scie

Générateur sinusoïdal

L'utilisation d'une mémoire ROM et un CNA permet d'obtenir la génération d'une fonction sinusoïdale figure 44.

Figure 44: Générateur sinusoïdal

Un oscillateur à quartz de fréquence F_0 commande un compteur/décompteur. Le convertisseur N/A reconstitue la sinusoïde à l'aide des 2^n échantillons numériques de la mémoire R.O.M.

Le principe de fonctionnement

Durant le premier quart de période le compteur évolue depuis la valeur 00...0 à la valeur 11...1. Ces 2^n échantillons numériques sont les adresses de la mémoire ROM. Celle-ci fournit en sortie les valeurs numériques de sinus des 2^n angles entre 0 et 90 degrés.

Lorsque le compteur prend la valeur maximum (11...1), cet état est détecté par la logique de contrôle qui programme le compteur / décompteur en décompteur. Ainsi à partir de la prochaine impulsion d'horloge, la mémoire ROM sera lue en sens inverse pour reconstituer le deuxième quart de période du signal.

Lorsque le compteur prend la valeur minimum (00...00), cet état est détecté par la logique de contrôle qui programme le compteur / décompteur en compteur, et inverse le bit de signe du convertisseur, donc il y a inversion de polarité. Ainsi à partir de la prochaine impulsion d'horloge, on décrit le troisième quart de période, et le quatrième quart de la même manière que précédemment comme le montre la figure 45.

Figure 45: Génération du signal sinusoïdal

On constate que le quart de période est constitué de 2^n-1 intervalles de temps élémentaire, donc on déduit la période T du signal sinusoïdale ($T = 4.(2^n-1).T_0$, avec T_0 période de l'horloge).

La programmation de la ROM se fait de la manière suivante:

On cherche l'incrément angulaire u ($u = (90° / 2^X-1)$), on dresse la table donnant les valeurs sin (0), sin (u), sin (2u), etc.... jusqu'à sin (90°). Ces valeurs théoriques des sin(u) sont ensuite approximées et converties en binaire à l'aide d'un nombre à m bits suffisant pour ne pas apporter une erreur supplémentaire appréciable. Une fois le résultat obtenu, la mémoire ROM peut être ainsi programmée.

Adresse	angle	sin (θ)	63.sin (θ)	Valeur	Valeur

mémoire(2^n-1)	θ degré	approché	(2^m-1).sin (θ)	choisie	binaire 6bits
0000	0	0	0	0	000000
0001	6	0.104	6.66	7	000111
0010	12	0.208	13.1	13	001101
0011	18	0.609	19.47	19	010011
0100	24	0.406	25.58	26	011010
0101	30	0.500	31.5	32	100000
0110	36	0.588	36.6	37	100101
0111	42	0.669	42.2	42	101010
1000	48	0.743	46.8	47	101111
1001	54	0.809	51	51	110011
1010	60	0.866	54.6	55	110111
1011	66	0.913	57.6	58	111010
1100	72	0.951	60	60	111100
1101	78	0.978	61	61	111101
1110	84	0.994	62.6	63	111111
1111	90	1.000	63	63	111111

Table de conversion sur 6 bits d'une valeur sin(θ) pour 16 valeur d'angle

Réalisation d'un filtre programmable

On désire réaliser un filtre passe-bande dont la fréquence centrale F_0 est programmable entre 10 Hz et 10 KHz par pas de 10 Hz. La commande de F_0 sera effectuée par un code numérique de 10 bits. Le coefficient de surtension du filtre est constant et égal à Q = 5. Le filtre à réaliser peut avoir la structure de la figure 46, où K est une variable réalisée par un CNA fonctionnant en multiplieur à 2 cadrans, conformément à la figure 47.

Figure 46: montage d'un filtre programmable

Figure 47 : Fonctionnement en multiplieur à 2 cadrans du AD 7533

La fonction de transfert s'écrit:

$$F(p) = \frac{S(p)}{E(p)} = \frac{K.R_2.p_2.C_2.p}{R_1\ p_1\ p_2\ C_1\ C_2\ p^2 - R_2\ p_2\ K\ C_2\ p + K_2\ R_2}$$

$$Q = \sqrt{\frac{R_1\ p_1\ C_1}{R_2\ p_2\ C_2}}$$

$$W_0 = K.\sqrt{\frac{R_2}{R_1\ p_1\ p_2\ C_1\ C_2}}$$

Pour K = 1, on a à peu près $F_0 = 10^4 Hz$

On prend : $R_1 = R_2 = 10\ K\Omega$ et $C_1 = C_2 = 1\ nF$ on a donc

$p_1 = 80\ K\Omega$ et $p_2 = 3\ K\Omega$

Les performances du filtre sont limitées essentiellement par une tension de décalage à la sortie, variable avec le code numérique de commande et pouvant atteindre des valeurs considérables. En effet on signale que, vu

de la borne de sortie Iout , le réseau R - 2R se comporte comme une source de tension en série avec une résistance interne variant en fonction de l'écart des commutateurs.

Traceur des caractéristiques des transistors

On utilise l'oscilloscope pour visualiser le réseau des courbes d'un transistor $I_c = f(V_{ce})$ à $I_b =$ constant, . Les différentes valeurs de I_b sont engendrées par une rampe de N marches d'escaliers qui sont appliquées à la base du transistor. La variation de la tension de polarisation est assurée par des rampes de tension synchrones avec les marches précédentes, appliquées entre les points C et E du montage de la figure 49.

Les marches d'escaliers et les rampes de tension sont générées à partir du microprocesseur et de deux CNAs, conformément au schéma de principe d la figure 48.

Figure 48 : Générateur des marches d'escaliers et des rampes de tension

Il faut bien remarquer que la tension Rc.Ic qui représente la variation de Ic doit être appliquée à l'oscilloscope

à travers un amplificateur différentiel pour des raisons de masse.

Figure 49 : L'interface entre l'oscilloscope et le système électronique

OBJECTIF

Les Convertisseurs Numériques - Analogiques & Les Convertisseurs Analogiques - Numériques

OBJECTIF

Les Convertisseurs Analogiques/Numériques *: CAN*

1.1Introduction

Effectuer une conversion analogique numérique c'est rechercher une expression numérique dans un code déterminé, pour représenter une information analogique avec une précision et une résolution donnée. Ces modules font correspondre à un code numérique une tension ou un courant analogique. La possibilité d'intégration des commandes analogiques a permis le développement rapide des CNA et CAN.

Dans la chaîne d'acquisition et de traitement de données, les CNA peut constituer l'interface de sortie de l'ordinateur pour, en restituer, en analogique, une grandeur préalablement numérisée et mémorisée afin de commander un processeur, une visualisation, des tables traçantes, etc...

2.1 Principe

Pour convertir une grandeur analogique en une grandeur numérique, il faut comparer cette grandeur analogique à une grandeur de référence Vref. En présence d'une valeur analogique Va le CAN calcule la valeur du rapport $\frac{Va}{Vref}$. Vref étant la valeur étalon de référence très souvent interne au convertisseur. Ce rapport de deux valeurs analogiques doit être exprimé en valeur numérique N et la relation $\frac{Va}{Vref} \Rightarrow N$ est obtenue avec un degré de résolution et de précision qui dépend du convertisseur choisi. On pourra écrire en général:

$$Va = N.Vref + \varepsilon_d + \varepsilon_a$$

N: est exprimé à l'aide de n bits, donc une seule valeur parmi les 2^n combinaisons possibles.

V_a: est la valeur analogique qui est distante de $N.V_{ref}$ de $\varepsilon_d + \varepsilon_a$

ε_d : est le terme d'erreur dûe à la quantification qui est toujours présent même si les parties analogiques du convertisseur sont rigoureusement parfaites

ε_a : est le terme d'erreur analogique introduite par la partie analogique du convertisseur (résistances, intégrateurs, etc..).

Comme on le présente sur la courbe de transfert de la figure 1.1 l'erreur de quantification est une erreur inhérente au procédé de conversion, elle est au maximums 1 LSB; mais très souvent le système de conversion étant centré, cette erreur est de $\pm\frac{1}{2}$ LSB.

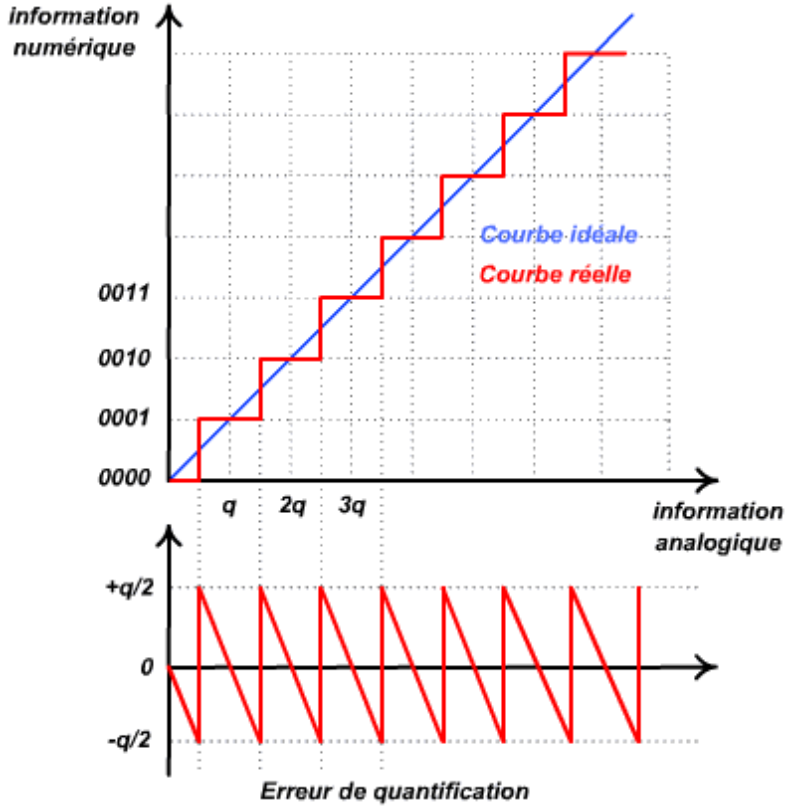


Figure 1.1: Quantification d'un signal analogique

Un convertisseur AN reçoit une tension d'entrée analogique qu'il convertit, après un certain temps, en un code de sortie numérique correspondant à l'entrée. La conversion AN est généralement plus complexe et plus longue que la conversion NA. Différentes méthodes de conversion AN ont été mises au point et sont utilisées. Nous allons consacrer le reste de cette section à l'étude détaillée de quelques méthodes, bien qu'il y ait fort à parier que vous n'aurez jamais à concevoir ou à construire de convertisseurs AN (qui sont vendus complètement montés dans des boîtiers). Toutefois, la connaissance des techniques utilisées vous fera prendre conscience des facteurs qui déterminent le rendement d'un convertisseur AN.

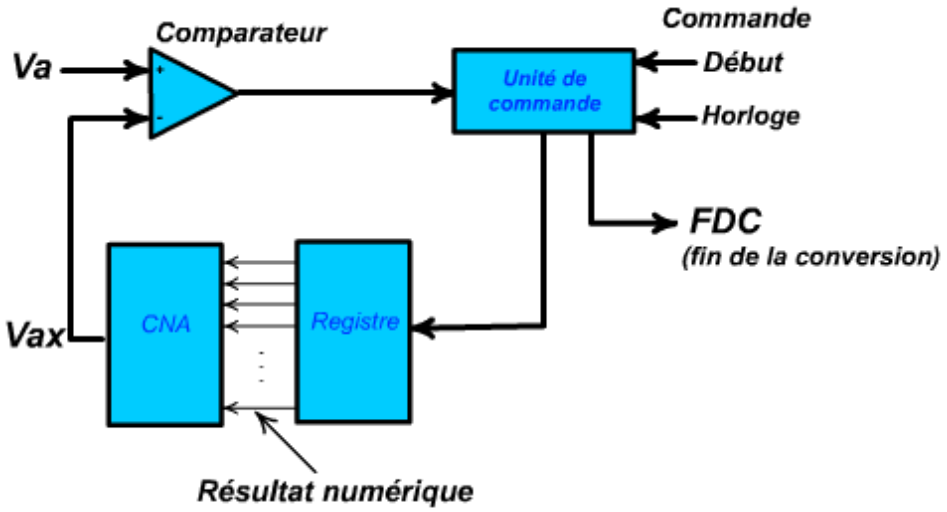


Figure 1.2: Schéma général d'une catégorie de convertisseurs AN.

Simulation

On retrouve dans les circuits de plusieurs types de CAN un convertisseur NA. La figure 1.2 nous montre le schéma fonctionnel général de cette catégorie de CAN. La synchronisation de la conversion est assurée par un signal d'horloge d'entrée. L'unité de commande renferme les circuits logiques qui génèrent la séquence appropriée d'opérations après l'arrivée de la COMMANDE DÉBUT qui initie le processus de conversion. Le comparateur (un amplificateur opérationnel) a deux entrées *analogiques* et une sortie *numérique* qui prend un état ou l'autre, selon l'entrée analogique qui est la plus grande.

Voici le fonctionnement de base des convertisseurs AN de cette catégorie:

1- La COMMANDE DÉBUT lance la conversion.

2- À une cadence déterminée par le signal d'horloge, l'unité de commande modifie sans arrêt le nombre binaire mémorisé dans le registre.

3- Le nombre binaire du registre est converti en une tension analogique V_{ax} par le convertisseur NA.

4- Le comparateur compare V_{ax} avec l'entrée analogique Va. Tant que $V_{ax} < V_a$, la sortie du comparateur demeure au niveau HAUT. Quand V_{ax} dépasse V_a d'une valeur au moins égale à V_T (tension seuil), la sortie du comparateur passe au niveau BAS et met fin au processus de progression du nombre dans le registre. À ce point, Vax est une très bonne approximation de Va et le nombre numérique qui se trouve dans le registre, qui est l'équivalent numérique de V_{ax}, est également l'équivalent numérique de Va, à l'intérieur des limites de résolution et de précision propres à ce système.

5- La logique de commande valide le signal FDC, fin de conversion, quand la conversion est achevée.

Les diverses variantes de cette solution de conversion NA se distinguent surtout par la façon dont la section de commande modifie sans cesse les nombres dans les registres. À part cela, le principe de base est le même, et la sortie numérique recherchée est mémorisée dans le registre quand la conversion est achevée

.

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

Les Convertisseurs Analogiques/Numériques *: CAN*

2- CAN parallèle

Principe:

Il s'agit du CAN le plus rapide, et également du circuit qui contient le plus grand nombre de comparateurs. Par exemple, un CAN parallèle de 6 bits exige 63 (2^6-1)comparateurs analogiques, une CAN de 8 bits en exige 255 (2^8-1) comparateurs analogiques et un convertisseur de 10 bits en exige 1023(2^{10}-1)comparateurs analogiques. Dans la pratique, le grand nombre de comparateurs nécessaires limite la réalisation des convertisseurs parallèles *discret*s. Par contre, les convertisseurs parallèles intégrés atteignent couramment 8 bits, et plusieurs fabricants annoncent pour prochainement des unités de 9 et de 10 bits.
Par la suite, nous décrivons le principe de fonctionnement d'un convertisseur parallèle à 3 bits seulement afin de ne pas trop compliquer les schémas de fonctionnement. Lorsque vous comprendrez le fonctionnement de ce convertisseur, vous pourrez sans difficulté appliquer son principe à des convertisseurs ayant un grand nombre de bits.
Le convertisseur parallèle de la figure 4.1 a une résolution de 3 bits et un pas de progression de 1 V. Le diviseur de tension établit des niveaux de référence pour chaque comparateur de sorte qu'on retrouve sept niveaux dont les valeurs sont 1 V (poids le plus faible), 2 V, 3 V, ..., et 7 V (pleine échelle). L'entrée analogique Va est appliquée à l'autre entrée de chaque comparateur.
Si Va < 1 V, toutes les sorties des comparateurs C1 à C7 sont au niveau HAUT. Si Va > 1 V, une au moins des sorties des comparateurs est au niveau BAS. Les sorties des comparateurs sont délivrées à un codeur de priorité vrai au niveau BAS qui produit une sortie binaire égale à la sortie du comparateur qui se trouve au niveau BAS dont le nombre est le plus élevé. Par exemple, quand Va se trouve entre 3 et 4 V, les sorties C1, C2 et C3 sont au niveau BAS et toutes les autres sont au niveau HAUT. Le codeur de priorité ne réagit qu'à la valeur basse de C3 et donne une sortie binaire CBA = 011, qui représente l'équivalent numérique de Va avec une résolution de 1 V. Quand Va est supérieure à 7 V, C1 à C7 sont tous BAS, et la sortie du codeur sera CBA = 111, ce qui est l'équivalent numérique de Va. Le tableau de la figure 4.2 nous fait voir les réponses pour toutes les valeurs possibles du signal analogique.
Le CAN de la figure 4.1 a comme résolution 1 V, puisque l'entrée analogique doit changer de 1 V pour amener la sortie numérique au pas suivant. Pour obtenir des résolutions plus fines, il faut accroître les niveaux de la tension d'entrée (c'est-à-dire utiliser un plus grand nombre de résistances dans le diviseur de tension) et le nombre de comparateurs. Par exemple, pour réaliser un convertisseur parallèle de 8 bits, le nombre de niveaux de tension doit être 2^8 = 256, en comptant le niveau 0. Et pour obtenir cela, il faut 256 résistances et 255 comparateurs (il n'y a pas de comparateur pour le niveau 0 V). Les 255 sorties de comparateur sont délivrées à un circuit codeur de priorité qui fournit en sortie un code de 8 bits correspondant à la sortie du comparateur de rang le plus élevé dont la sortie est BASSE. De façon générale, un convertisseur parallèle de N

bits a besoin de 2^N - 1 comparateurs, de 2^N résistances et des circuits de la logique de codage.

Durée de conversion Il n'y a pas de signal d'horloge dans un convertisseur parallèle et c'est pourquoi il n'y a pas de synchronisation ou de séquencement à considérer. La conversion se produit continuellement. Quand la valeur de l'entrée analogique change, les sorties du comparateur suivent, ce qui entraîne la modification des sorties du codeur. La durée de conversion est le temps qui s'écoule entre un changement de Va et l'apparition d'une nouvelle sortie numérique; cette durée est fonction seulement des retards de propagation des comparateurs et des circuits logiques de codage. C'est donc dire que la durée de conversion dans un convertisseur parallèle est extrêmement courte. Par exemple, le AD9002 de Analog Devices est un CAN parallèle de 8 bits dont la durée de conversion nominale est de 10 ns.

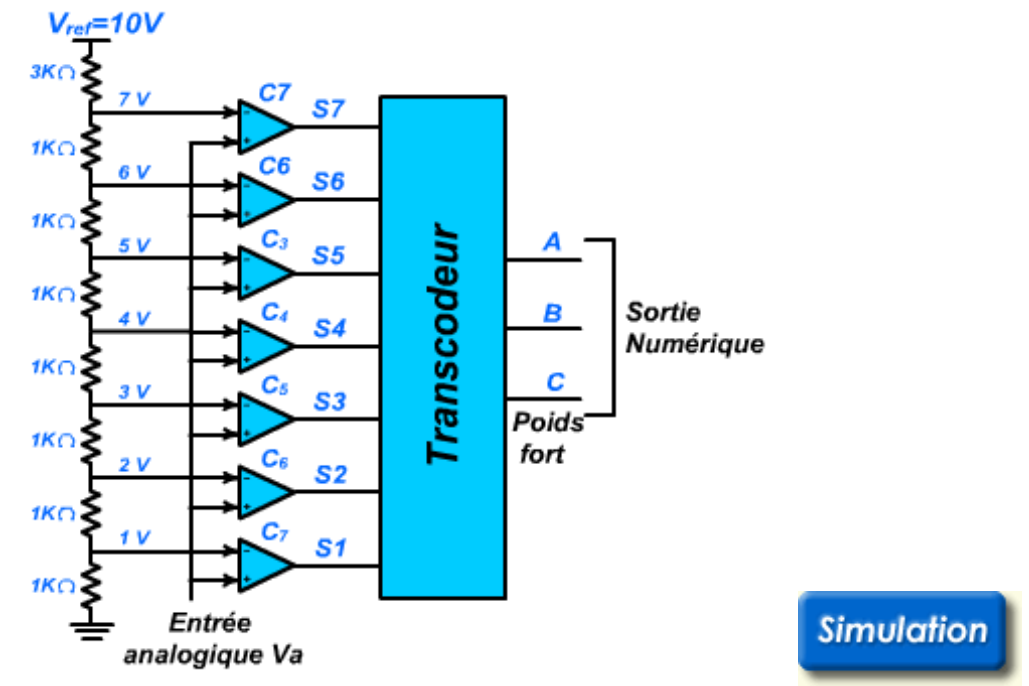


figure 4.1: Convertisseur AN 3 bits à fonctionnement parallèle

Entrée analogique	Sorties du comparateur							Sortie numérique		
V_a	S_1	S_2	S_3	S_4	S_5	S_6	S_7	C	B	A
V_a<1 V	0	0	0	0	0	0	0	0	0	0
1 V<V_a<2 V	1	0	0	0	0	0	0	0	0	1
2 V<V_a<3 V	1	1	0	0	0	0	0	0	1	0
3 V<V_a<4 V	1	1	1	0	0	0	0	0	1	1
4 V<V_a<5 V	1	1	1	1	0	0	0	1	0	0
5 V<V_a<6 V	1	1	1	1	1	0	0	1	0	1
6 V<V_a<7 V	1	1	1	1	1	1	0	1	1	0
7 V<V_a	1	1	1	1	1	1	1	1	1	1

Figure 4.2: Table de vérité

D'après la table de vérité on déduit les équations logiques de $_{A\ B\ C}$ et le logigramme du transcodeur (figure 4.3).

$$C=S4$$
$$B=S6+S2.\overline{S4}$$
$$A=S7+S5.\overline{S6}+S3.\overline{S4}+S1.\overline{S2}$$

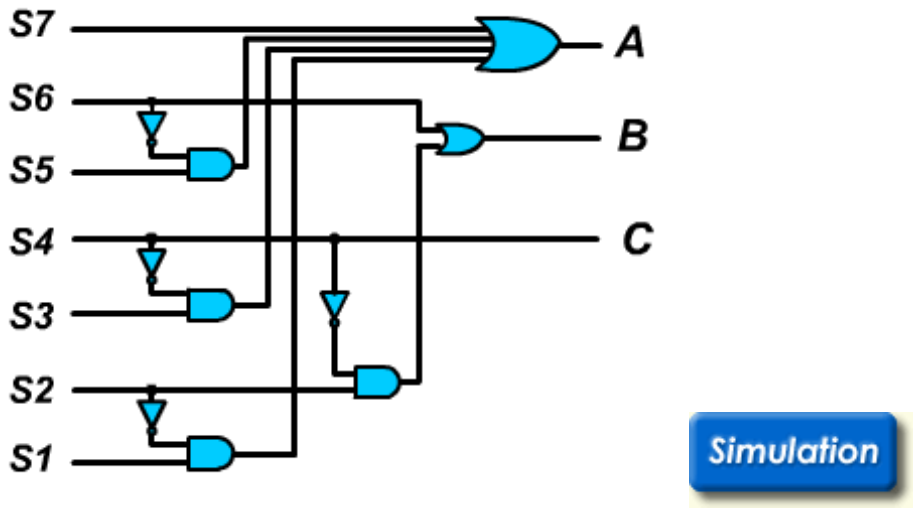


Figure 4.3: Logigramme du transcodeur

Le CAN parallèle exige un nombre de comparateurs égale à 2^n-1 pour un CAN à n bits. Ce nombre de comparateurs élevé restreint naturellement les applications. Lorsque la vitesse de conversion n'est pas un critère crucial, il est possible de réduire le nombre de comparateurs au bénéfice

d'une amélioration de la résolution à l'aide de l'artifice du montage (figure 4.4)

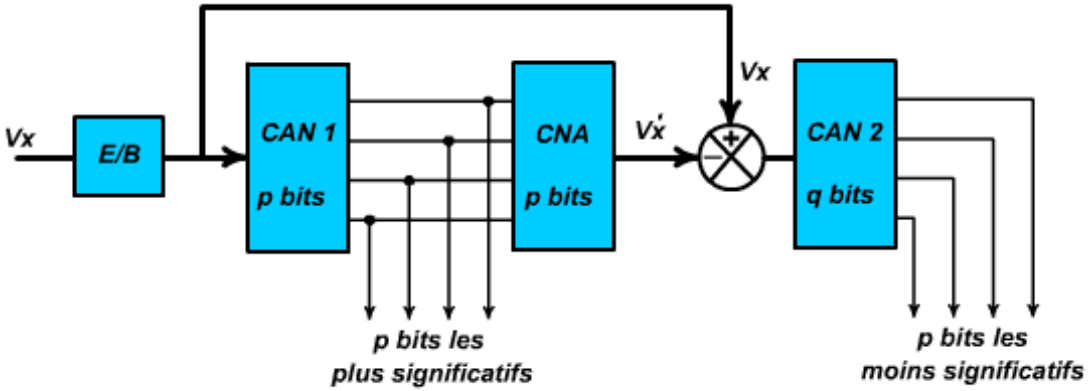


Figure 4.4: Amélioration de la résolution d'un CAN parallèle

Evaluation

1- Donnez la valeur de la tension à convertire puis appuyer sur valide

2 - Observer la sortie du convertisseur (nombre N en binaire)

3- pour voir le schéma interne du transcodeur appuyer sur "marche"

Les techniques des conversions analogique-numérique:

Les techniques des conversions analogique-numérique:

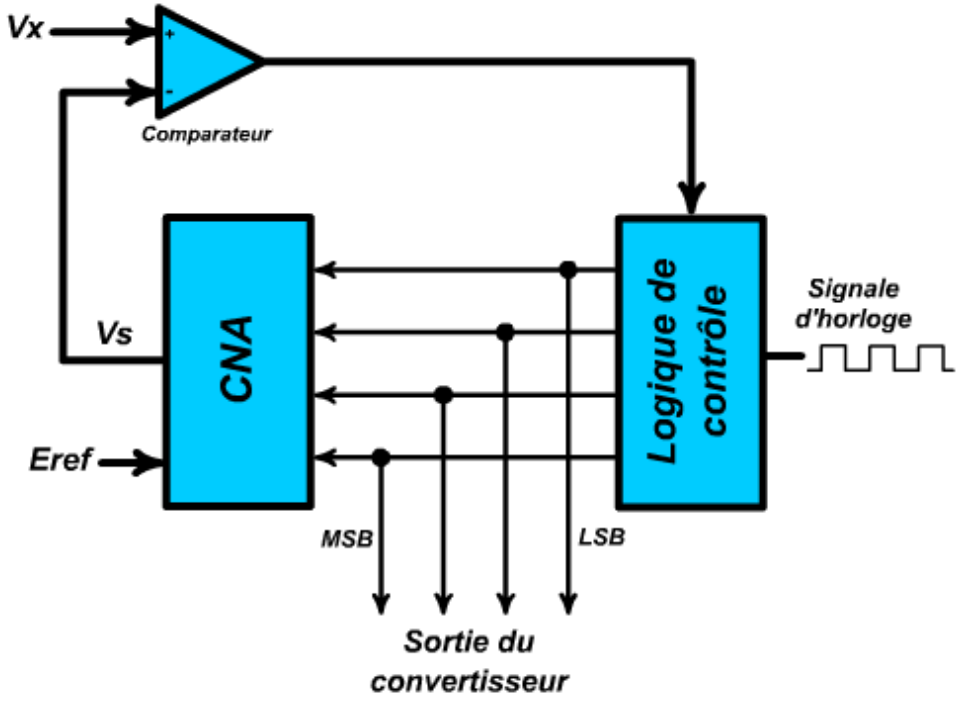
Les techniques des conversions analogique-numérique:

Les Convertisseurs Analogiques /Numériques *: CAN*

3- CAN à approximation successives

Principe de fonctionnement:

Le fonctionnement est décrit par le schéma synoptique simplifié de la figure 3.1; on note une grande similitude qui existe entre ce principe et le principe de pesées successives: le fluos de la balance et l'opérateur jouent le rôle du comparateur C, l'opérateur est représenté par le registre qui décide des bits à décaler de façon à arriver à l'équilibre.
Le comparateur C compare la tension analogique à convertir Vx à la tension Vs issue d'un convertisseur N/A et élabore suivant un processus que l'on va décrire. La sortie du comparateur est liée à la différence V_x - Vs appliquée sur son entrée différentielle.



Simulation

Figure 3.1: Convertisseur AN par approximations successives.

Lorsque l'ordre de départ " début de conversion" est donné, le système est mis à l'état initial. Après un certain délai, la logique de commande donne au convertisseur l'information (10..00), c'est à dire MSB seul à un et les autres bits sont égaux à zéro. Deux cas se présentent selon la comparaison .

1)-La tension inconnue V_x est supérieure à la tension V_s que le CNA fait correspondre à l'information 10..0,

2)-Ou bien, la tension inconnue V_x est inférieure à V_s .

Si la tension Vx est supérieure à Vs pour N = 100..0, la réponse du comparateur est 1 , et la logique de commande ajoute à cette information binaire le bit de rang immédiatement inférieur. La comparaison suivante se fait donc entre Vx et Vs pour N=1100..0.

Si la tension Vx est inférieure à Vs pour N = 100..0, la réponse du comparateur est 0, et la logique de commande remplace l'information 10...00 par l'information de valeur moitié 0100...0. La comparaison n° 2 se fait de la même manière que la première etc...

En définitive suivant la valeur de Vx, le processus de recherche va se faire selon l'un de 2^n chemins qui sont possibles. Dans le cas de la figure 3.2 il y a 16 chemins possibles puisque n = 4. Chacun de ces 2^n chemins aboutit à l'une des 2^n expressions binaires possibles pour N, que l'on trouve dans l'état final du CNA de n bits. A ce moment là, Vx = Vs et N est bien l'expression binaire de Vx. Parmi les 2^n chemins sont possibles un seul est pris et dans chaque cas, n comparaisons sont nécessaires.

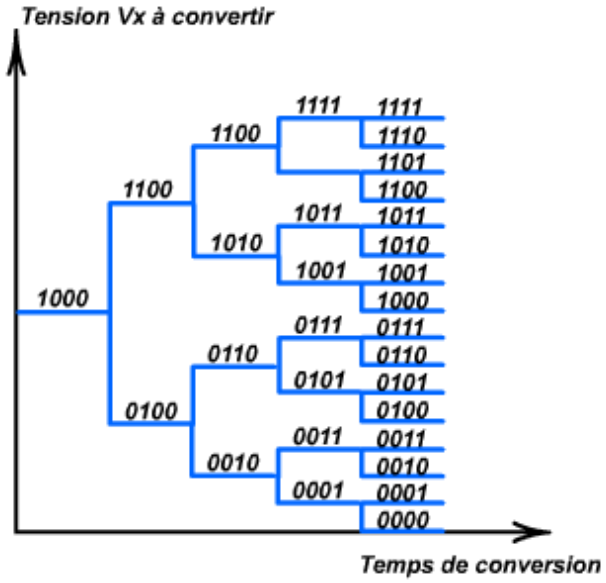


Figure 3.2: Les chemins possibles pour N=4.

La durée de conversion dépend du nombre de bits du registre et du CNA, et de la fréquence d'horloge. Elle atteint actuellement la microseconde.

Simulation

La tension Vx à convertir peut s'écrire sous la forme:

$$Vx=\frac{Eref}{2^n}\left[S_1.2^{n-1}+.....+S_{n-i}.2^i+.....+S_{n-2}.2^2+S_{n-1}.2^1+S_n.2^0\right]$$

Les valeurs des bits S_{n-1} .....S_i ....S_2, S_1 ,S_0 sont pris égaux à "0" ou à "1" selon le résultat de la comparaison.

L'exemple suivant illustre le fonctionnement (figure 3.3). Pour simplifier l'explication de ce convertisseur, on suppose que n est égale à 3.

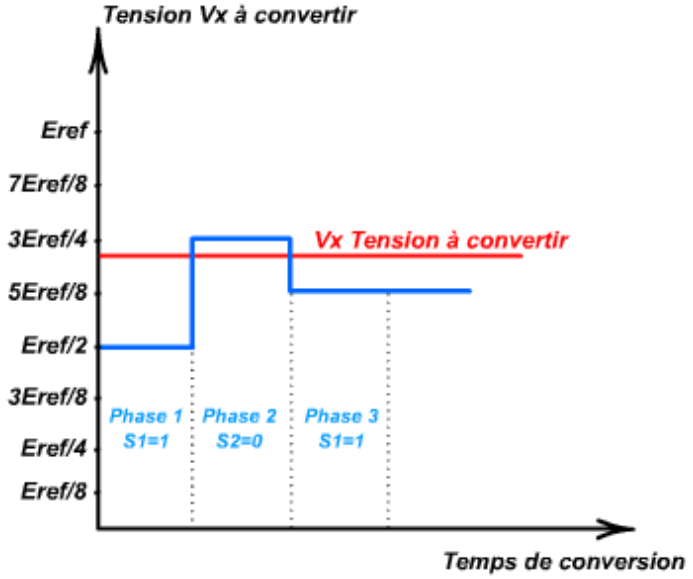


Figure 3.3: Diagramme de fonctionnement d'un CAN à approximation

successives à 3 bits

Phase 1 Vx est comparée à $\frac{Eref}{2}$

$Vx > \frac{Eref}{2} \Rightarrow S_1 = 1\ (MSB)$

Phase 1 Vx est comparée à $\frac{Eref}{2} + \frac{Eref}{4} = \frac{3Eref}{4}$

$Vx > \frac{3Eref}{4} \Rightarrow S_2 = 1$

Phase 1 Vx est comparée à $\frac{Eref}{2} + \frac{Eref}{4} + \frac{Eref}{8} = \frac{7Eref}{8}$

$Vx > \frac{7Eref}{8} \Rightarrow S_3 = 1\ (LSB)$

Comme nous sommes limités à 3 bits, le résultat est alors:

$$Vx = \frac{Eref}{2^3}\left[S_1 \cdot 2^2 + S_2 \cdot 2^1 + S_3 \cdot 2^0\right] = \frac{5Eref}{8}$$

Nous notons que la différence entre la tension Vx et la tension Vs de comparaison n'est pas nulle. Mais cette différence est simplement minimisée pour être inférieure à quantum q ($\frac{Eref}{2^n}$). Pour obtenir une erreur nulle, nous devrons avoir n infini.

convertisseur A/N et la figure 3.5 donne le diagramme des temps pour les différents signaux
générés par la logique de commande.

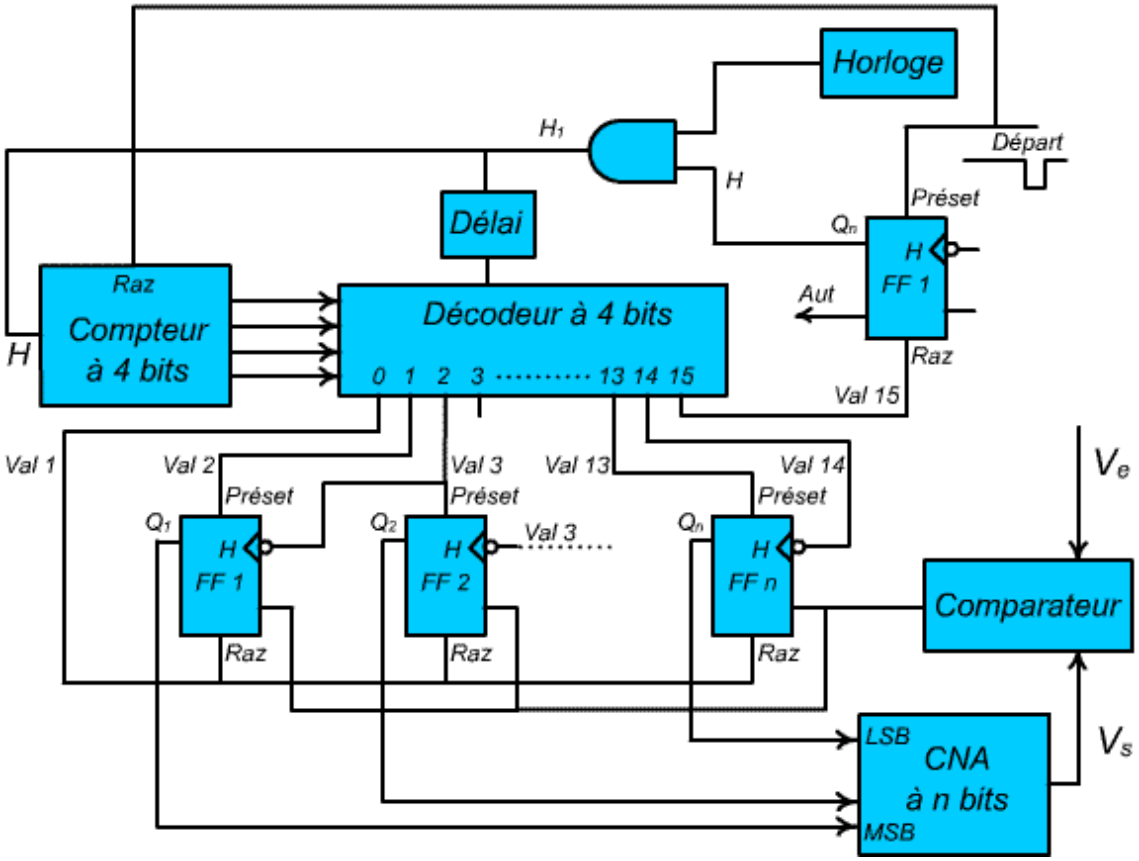


Figure 3.4: Convertisseur AN par approximations successives

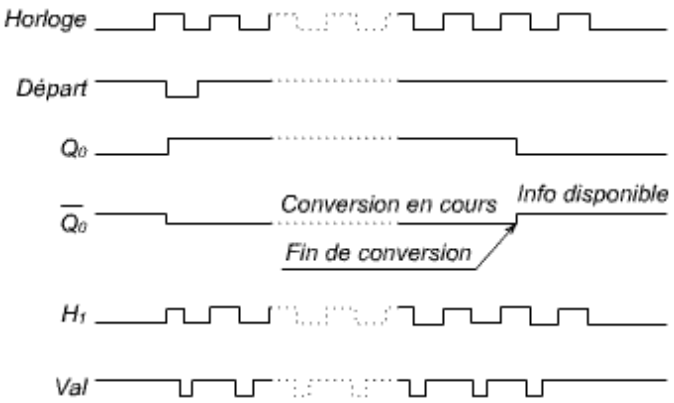


Figure 3.5: Diagramme des temps (CAN)

Pour le compromis rapidité-prix, cette famille se trouve couramment utilisée dans les systèmes d'acquisition rapide; dans ces applications, il est souvent indispensable d'associer au CAN un échantillonneur-bloqueur. L'utilisation fréquente de ces deux dispositifs implique la nécessité de décrire un exemple de mise en ouvre pratique. Ainsi, la figure 3.6 représente un montage associant les deux modules suivants:

Le CAN AD7570 (Analog Devices)

L'échantillonneur-bloqueur AD 582 du même fabricant.

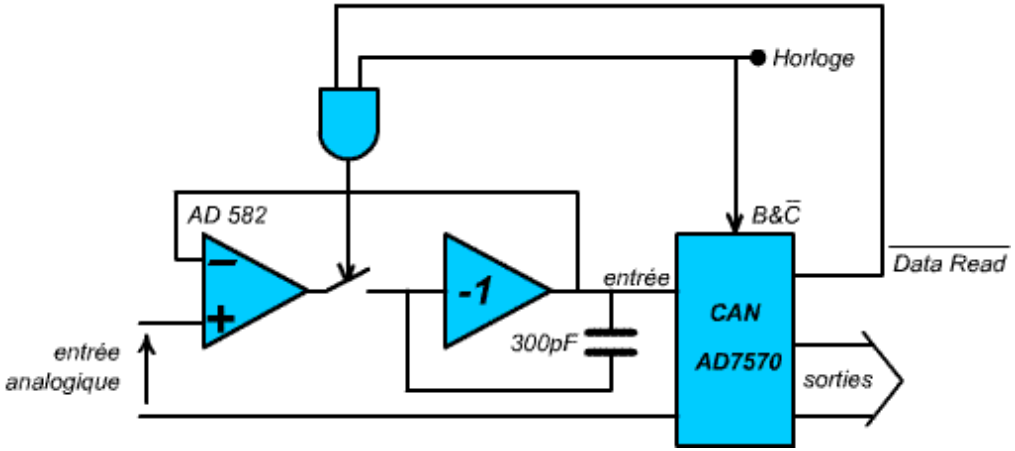


Figure 3.6: Association du CAN 7570 et de l'échantionneur-bloqueur AD582

La figure 3.7 représente les séquences de fonctionnement du CAN:

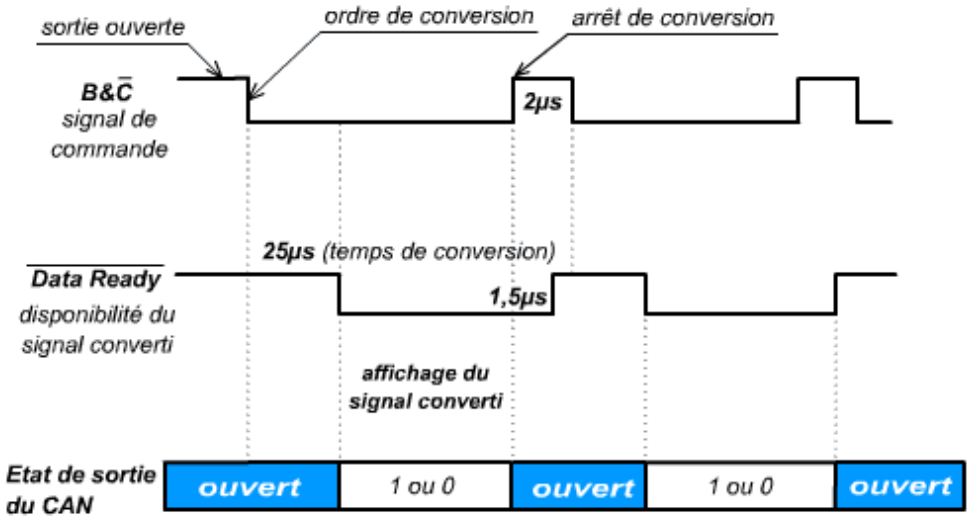


Figure 3.7: Diagramme temporel de fonctionnement du CAN 7570

1- L'ordre de conversion est donné par le front descendant du signal de commande appliqué en $B\&\overline{C}$ (Blank and $\overline{convert}$)

2- La durée de conversion est de l'ordre de 25µs. A la fin de conversion, un signal informant de la disponibilité du résultat est fourni par $\overline{DR}$ $(\overline{DataRead})$

3- Le retour du signal $B\&\overline{C}$ au niveau "1" ramène également l'état de $\overline{C}$ à "1"; la sortie se trouve alors "ouverte" (état haute impédance).

4- La largeur minimale du signal de commande entre l'arrêt de conversion et le nouveau début de conversion est de l'ordre de 2µs.

5- L'échantillonneur-bloqueur AD482 associé au CAN AD7570, conformément au schéma de la figure 3.7 permet d'acquérir un signal de 10 V en moins de 10µs avec une dérive inférieure à 100µV/ms.

6- L'ordre de blocage est donné par le front descendant du signal de commande $B\&\overline{C}$;le blocage est maintenu pendant toute la durée de la conversion par le niveau "1" du signal $\overline{DR}$ appliqué sur l'autre entrée de la porte de commande de l'échantillonneur-bloqueur.

7- A la fin de chaque conversion, le signal $\overline{DR}$, en basculant au niveau "0", donne l'ordre d'échantillonnage

Simulation

Amélioration de la résolution d'un CAN à approximation successive:

Pour améliorer la résolution d'un CAN à approximation successive, il est nécessaire d'ajuster les résistances des réseaux R - 2R du CNA. Cette correction, bien qu'elle soit effectuée par la technique très précise du laser, n'apporte pas forcement d'amélioration en ce qui concerne les erreurs de superposition dûes à l'interaction entre les courants dans le réseau et les non linéarités des résistances de contre-réaction.
On a donc imaginé de corriger ces erreurs à l'aide de mémoire PROM intégrée dans le dispositif. Cette mémoire permet la correction des erreurs du réseau après encapsulation. En effet, après encapsulation, on envoie à l'entrée une tension de valeur connue correspondant à un bit, on lit le mot de la sortie puis on programme la mémoire PROM de telle sorte que la somme "mot de sortie" + "mot PROM" corresponde à la valeur du bit testé.
Cette technique est utilisée par la société Intersil pour son CAN ICL 7115 de 14 bits, de 40µs de temps de conversion et présentant ses sorties à 3 états en octets a fin de pouvoir se connecter sur les bus des microprocesseurs.

Simulation CAN à approximation successives

Evaluation

1- Donnez la valeur de la tension à convertire puis appuyer sur valide

2- choisir le mode de simulation continue ou le mode pas à pas, par la suit appuyer sur début de conversion

3 - Observer la sortie du convertisseur (nombre N en binaire)

1- Donnez la valeur de la tension à convertire puis appuyer sur valide

2- choisir le mode de simulation continue ou le mode pas à pas, par la suit appuyer sur début de conversion

3 - Observer la sortie du convertisseur (nombre N en binaire)

Les Convertisseurs Analogiques /Numériques *: CAN*

4- CAN à comptage d'impulsions

Cette procédure de conversion très simple nécessite peu de composants mais offre une très bonne précision. Cependant, le temps de conversion est considérablement plus long que les procédés précédents; il se trouve généralement entre 0.1 et 100 ms. Comme la plus part des grandeurs physiques usuelles évoluent lentement, ces CAN trouvent un domaine d'application très large.

1.1 Convertisseur à simple rampe ou modulation de largeur d'impulsion

Cette technique repose sur la transformation qui fait correspondre à une amplitude de tension continue une impulsion rectangulaire de largeur (t_1- t_0) proportionnelle. Cette transformation est réalisée par un intégrateur et un comparateur. Le nombre d'impulsions élémentaires délivrées par une horloge , comptées pendant cet intervalle de temps (t_1- t_0), fournira la valeur de la tension Vx à convertir. L'organisation du CAN à rampe (analogique) est donnée au schéma de la figure 5.1.

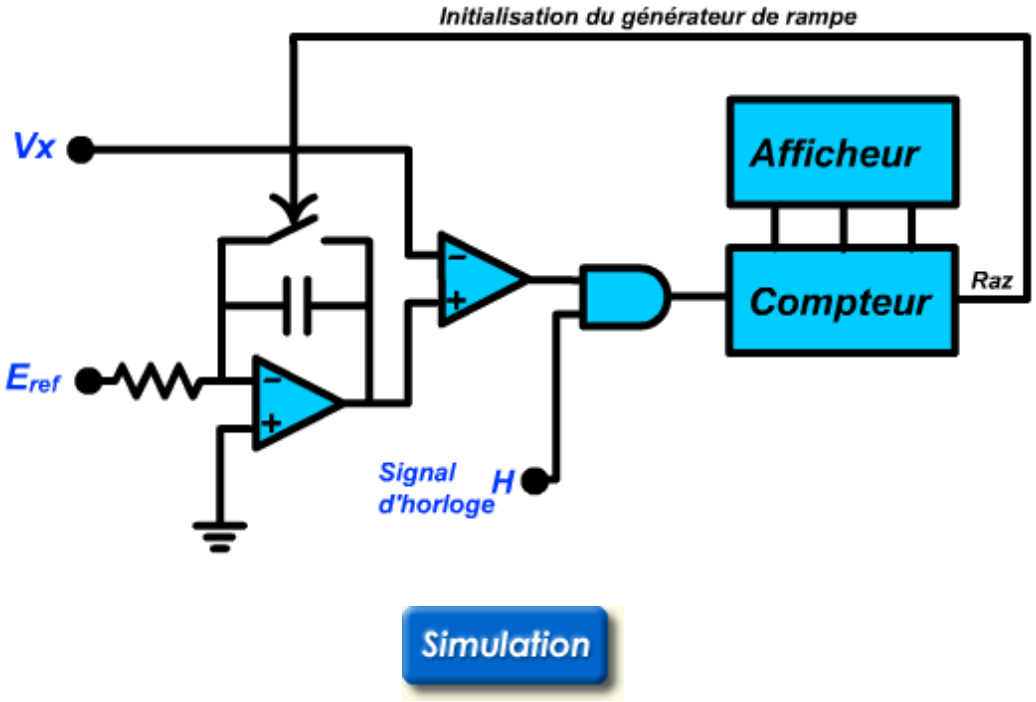


Figure 5.1: Convertisseur simple rampe

Cas simple d'une tension unipolaire (Vx > 0)

Pour mieux comprendre le principe de fonctionnement, supposons qu'on ait à convertir une tension Vx supérieure à zéro figure 5.2.

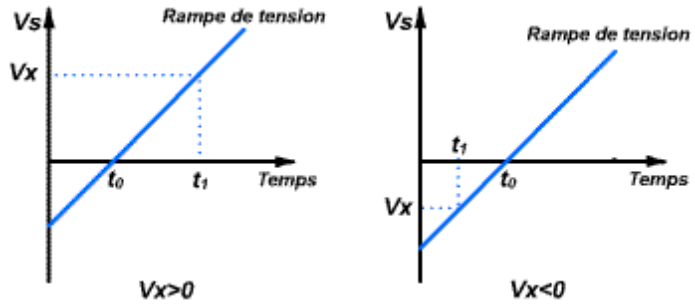


Figure 5.2: Comparaison entre la rampe de tension et la tension à convertir

La rampe de tension fournie par un intégrateur est comparée directement à Vx. Cette rampe est générée au moment du déclenchement de la mesure, à l'instant t_0; en même temps, la porte est ouverte pour laisser passer les impulsions d'horloge au compteur. A l'égalité des deux tensions (Vs = Vx), le comparateur bascule est ferme la porte. Le nombre d'impulsion N de période T compté pendant l'intervalle de temps t_1- t_0 est directement proportionnel à Vx:

$$V_x = \frac{E_{ref}}{R.C}(t_1 - t_0) \quad \text{ou encore} \quad V_x = \frac{E_{ref}}{R.C} T_0.N$$

Cas d'une tension Vx de polarité quelconque figure 5.3

Le convertisseur comporte deux comparateurs et la rampe débutera à une tension négative -V. Si Vx < 0, la conversion débutera à l'instant t_2 où $V_s = V_{x2}$, ce qui fait basculer le comparateur A et valide le comptage qui s'arrête à l'instant t_0 ou $V_s = 0$, avec comme conséquence le basculement du comparateur B.

L'affichage de la polarité ainsi que l'ordre de compter peuvent être réalisées à l'aide d'un système logique. En effet, supposons que les comparateurs donnent une sortie nulle quand le potentiel de l'entrée **+** est inférieur à celui de l'entrée **-** et que A et B soient les variables logiques des sorties des comparateurs; on peut établir les tables vérités dans les deux cas Vx >0 et Vx < 0.

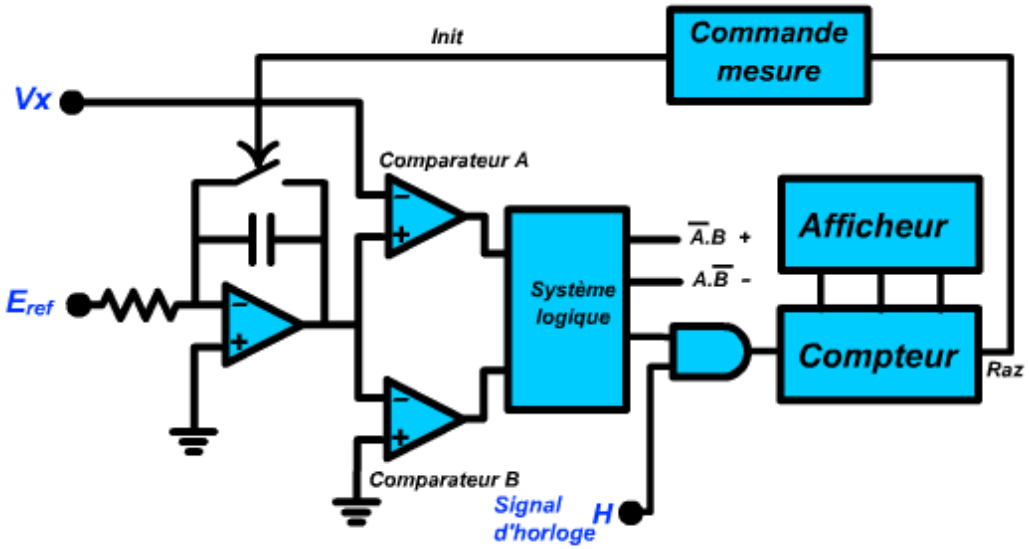


Figure 5.3: Convertisseur à simple rampe à double polarité

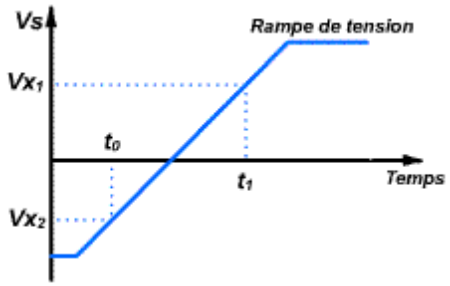


Figure 5.4: Tension de polarité quelconque

Cas: Vx > 0

	$t<t_0$	$t_2<t<t_0$	$t>t_1$
A	***0***	***0***	***1***
B	***0***	***1***	***1***
Conversion	***0***	***1***	***0***

$$\text{Conversion} = \overline{A}\,B$$

Cas: Vx < 0

	$t<t_2$	$t_2<t<t_0$	$t>t_0$
A	***0***	***1***	***1***
B	***0***	***0***	***1***
Conversion	***0***	***1***	***0***

$$\text{Conversion} = A\,\overline{B}$$

Dans le cas où Vx > 0, le comptage doit s'effectuer entre t_0 et t_1 donc lorsque $\overline{A}B = 1$, tandis que dans le cas où Vx < 0 le comptage doit s'effectuer entre t_2 et t_0, donc lorsque $A\overline{B} = 1$; comme le montre le schéma de principe de la figure 5.4.

Remarques

1- La précision de ce convertisseur est mauvaise car elle dépend de la précision et de la stabilité de la tension de référence Eref, du générateur de rampe (R, C) et de la période d'horloge (T) .

2- Un CAN de n bits peut nécessiter (2^n-1) incrémentations pour convertir la tension Vx , donc un temps de conversion égal à : t = (2^n-1). T, (dans le cas où la tension analogique Vx a la valeur maximum).

3- On remarque de plus que dans cette technique un parasite superposé à la tension Vx pourra perturber le résultat, en avançant ou en reculant l'instant ou le signal comparateur arrête le comptage. On pourrait utiliser un filtre d'entrée pour éliminer ces bruits mais il réduirait inévitablement le temps de réponse de l'appareil. On obtient l'élimination de certains bruits périodiques superposés au signal utile en appliquant ce dernier à l'entrée d'un intégrateur; c'est l'intérêt du convertisseur tension fréquence.

1.2 Convertisseur à double rampe:

Principe:

La technique de conversion à double rampe permet de rendre le système de conversion moins sensible aux parasites d'entrée superposés à la tension à convertir, moyennant une légère augmentation de la complexité comme le montre la figure 5.6.

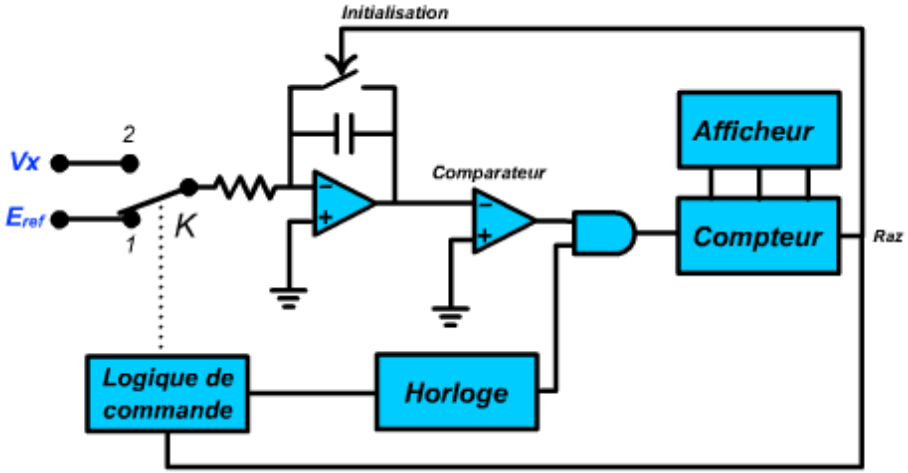


Figure 5.6: Convertisseur AN à double rampe

La conversion s'effectue en deux phases figure 5.7

- **Première phase:**

Dans La première phase (l'interrupteur K est sur la position 2), le signal d'entrée V_x plus les parasites qui lui sont superposés sont intégrés durant un temps constant t_1 égal à N_1 périodes T d'horloge. En pratique jusqu'à ce que le contenu du compteur n bits soit maximum, (N_1 a en général une valeur de 2^n-1 pour un convertisseur à n bits). Les signaux parasites sont considérés comme un bruit aléatoire de fréquences assez grandes par rapport au temps d'intégration ce qui donne lieu à une moyenne pratiquement nulle. On peut écrire :

$$\frac{1}{R.C}\int_0^{t_1} V_x dt = \frac{V_x}{R.C}.t_1 = \frac{V_x}{R.C}.N_1.T$$

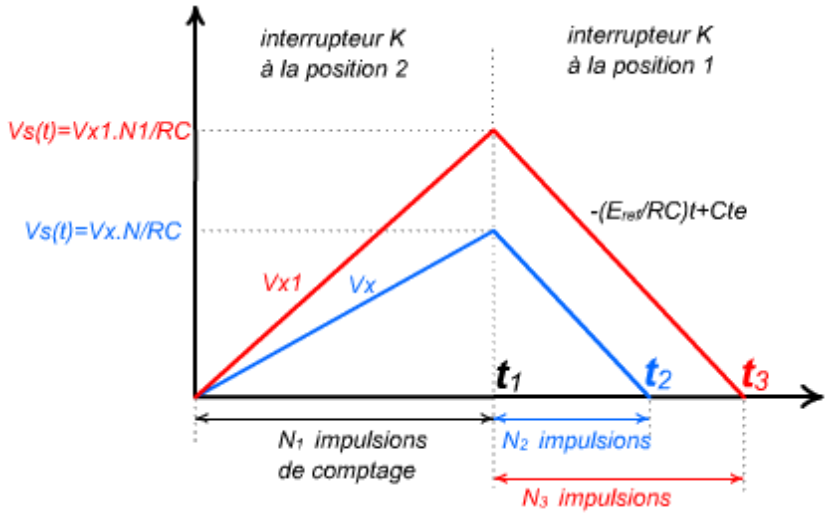


Figure 5.7: Phase de conversion

- **Deuxième phase:**

Dans la deuxième phase, le compteur ayant été remis à zéro par l'impulsion d'horloge suivant l'instant t_1 et commute l'entrée de l'intégrateur sur une tension référence E_{ref} de polarité opposée à V_x .

L'intégration s'effectue jusqu'à ce que la tension de sortie s'annule. Le comparateur doit détecter le passage par zéro de Vs pour arrêter le comptage à l'instant t_2. Soit N le nombre de périodes d'horloge, comptées pendant cette deuxième phase; on peut écrire:

$$t_2 - t_1 = N.T$$

$$\frac{V_x}{R.C}.N_1.T=\frac{E_{ref}}{R.C}.N.T$$

$$\Rightarrow V_x=\frac{N}{N_1}.E_{ref}$$

La valeur de V_x est directement proportionnelle à N et cette valeur est indépendante de R, C et de T, seule les variations de E_{ref} qui peuvent affecter la conversion.

On constate que le temps de conversion peut atteindre la valeur de $t = 2.(2^n-1).T$ si la tension à convertir est égale à la valeur maximum. Malgré que le temps de conversion soit assez long (égale à t_2), cette méthode donne, dans la plupart des applications industrielles, des performances satisfaisantes. On atteint des précisions meilleures que 10^{-4}, une résolution de 1µv, une linéarité de 0.005 % de la pleine échelle, une stabilité d'étalonnage de quelques ppm /°C, une impédance d'entrée de l'ordre de GΩ une réjection de mode commun de 150 dB en continu et de 100 dB en alternatif...

Sources d'erreurs:

- Stabilité de la tensions de références
- Imperfections des commutateurs
- Imperfections de l'intégrateur
-Imperfections du comparateur

1.3Convertisseur à triple rampe:

Dans le convertisseur triple rampe, la première étape du convertisseur double rampe est conservée comme le montre la figure 5.8. C'est à dire que la tension V_x est appliquée à l'entrée d'un intégrateur pendant un intervalle de temps t_1 égale N_1 périodes d'horloge, donc on à:

$$V=\frac{V_x}{R.C}.N_1.T$$

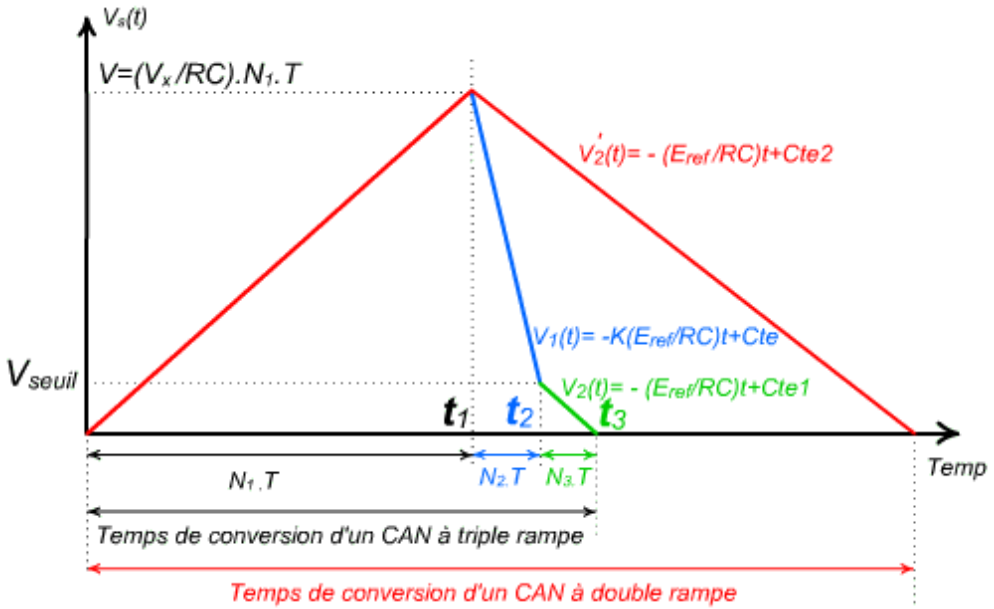


Figure 5.8: Principe d'un CAN à triple rampe

L'étape suivante comporte deux phases:

- **Première phase:**

On a la décharge très rapide à partir de t_1 jusqu'à une tension de seuil **Vseuil** faible (100 mv par exemple). Cette décharge rapide sera obtenue en remplacement R par une résistance R' plus faible. Par exemple, si R est remplacée par R/100, la décharge est alors 100 fois plus rapide. Soit N_2 le nombre de périodes d'horloge comptées pendant cette décharge; on a :

$$V - V_{seuil} = \frac{E_{ref}}{R.C}.100.N_2.T$$

- **Deuxième phase:**

Un détecteur de V_{seuil} placé à la sortie de l'intégrateur remplacera R' par R lorsque V_s atteint V_{seuil}. Cette phase est courte car V_{seuil} est très faible. Soit N_3 le nombre de périodes d'horloge comptées durant cette phase qui s'arrête évidement lorsque Vs = 0; on a:

$$V_{seuil}=\frac{E_{ref}}{R.C}.N_3.T$$

Le bilan de la première étape et des deux phases de la deuxième étape donne:

$$\frac{V_x}{R.C}.N_1.T=\frac{E_{ref}}{R.C}.100.N_2.T+\frac{E_{ref}}{R.C}.N_3.T$$

d'ou

$$V_x=\frac{E_{ref}}{N_1}(100.N_2+N_3)$$

Dans la deuxième phase, la décharge est ralentie pour permettre un comptage précis des dernières impulsions. Le temps de conversion peut être plus court que dans la méthode précédente, tout en conservant la même résolution.
Une autre variante de ce type de convertisseur consiste à fixer la tension de V_{seuil} au top d'horloge suivant immédiatement après le passage de V_s par zéro (figure 5.9). Le nombre d'impulsions N_2 donne une valeur par excès de Vx. Le compteur affiche en fait $100N_2$ comme l'opération faite lors de la première phase de la variation précédente. On commute alors l'entrée de l'intégrateur sur la tension $-E_{ref}$ avec de nouveau la résistance R à l'entrée de l'intégrateur et on décompte jusqu'au passage par 0 à partir de $100N_2$.

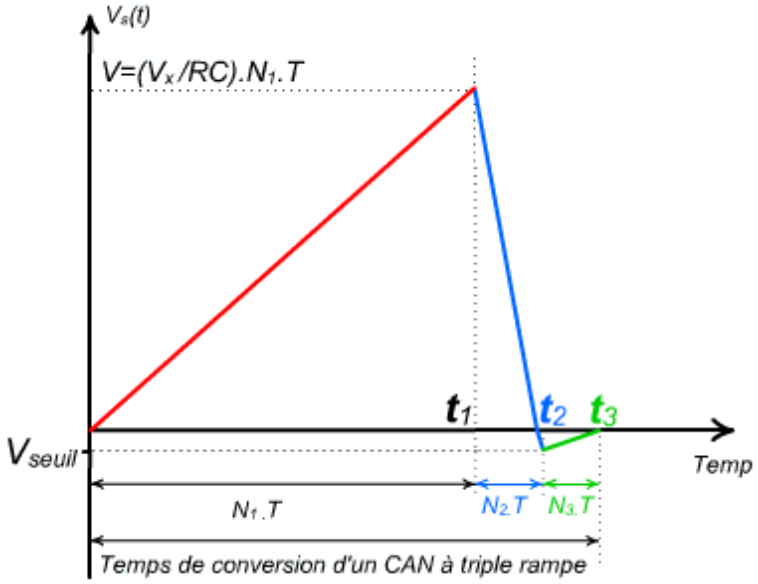


Figure 5.9: Deuxième variante de la conversion à triple rampe

Evaluation

1- Donnez la valeur de la tension à convertir appuyer sur valide puis sur début de conversion

2 - Observer la sortie du convertisseur (nombre N en binaire)

Les Convertisseurs Analogiques /Numériques *: CAN*

5- Convertisseurs tension /fréquence

Il s'agit de convertir la tension V_x en un signal périodique de fréquence F proportionnelle à V_x puis de mesurer F en comptant le nombre de période dans un intervalle de temps. Dans le cas de la figure 5.5, la tension analogique V_x est intégrée, ce qui donne à la sortie de l'intégrateur une tension en dent de scie $V_s(t)$ de pente proportionnelle à l'amplitude de V_x. Cette tension $V_s(t)$ est comparée par le comparateur C à un niveau de référence E_{ref}. Dés que $V_s(t) = E_{ref}$ est détectée, il y a simultanément l'émission d'une impulsion calibrée et la remise à zéro (raz) de l'intégrateur. Ce qui se traduit essentiellement par une décharge très rapide de la capacité C puis l'intégration reprend. Dans ces conditions la fréquence d'émission est proportionnelle à l'amplitude de V_x.

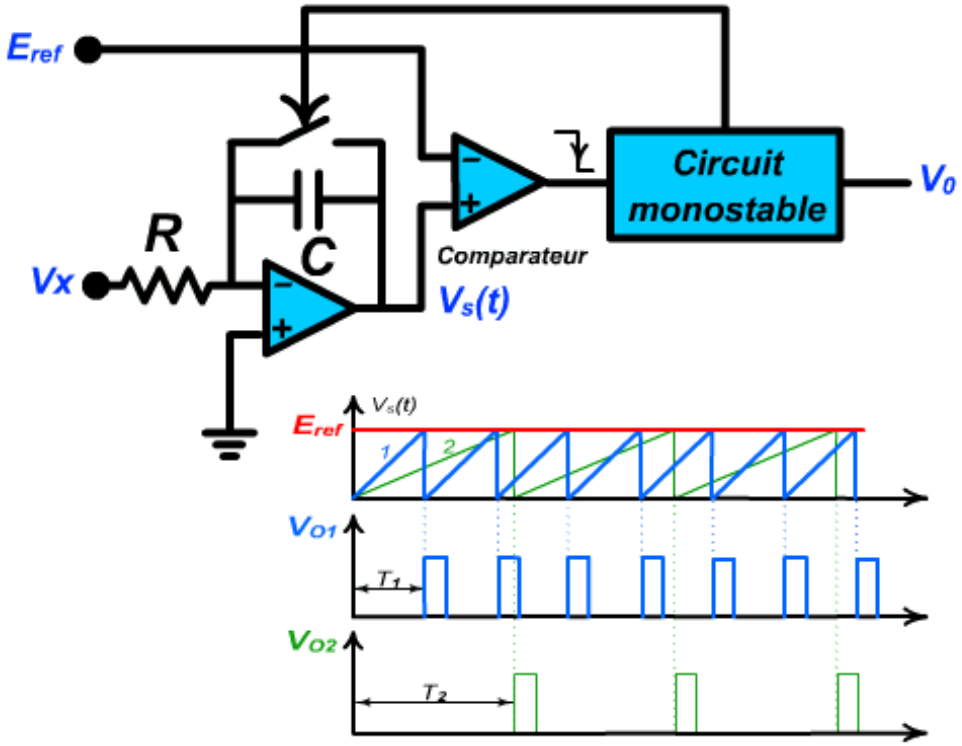


Figure 5.5: Convertisseur tension fréquence

Si T est la période du signal (Vo) obtenu, on a:

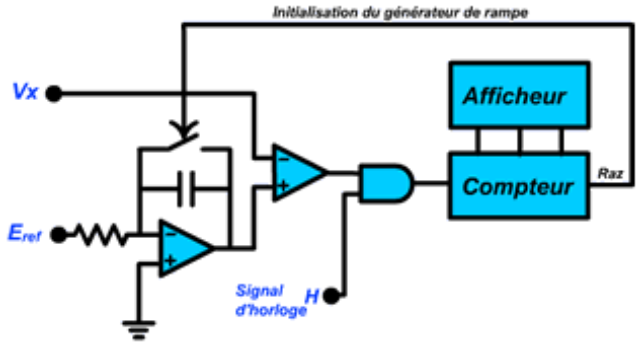
$$E_{ref}=\frac{1}{R.C}.V_x.T$$

$$V_x=R.C.E_{ref}.F_0$$

On mesure F_0 en comptant

- le nombre de périodes par seconde
- le nombre de périodes N dans un intervalle de temps θ puisque:

avec $F=\frac{N}{\theta}$ on peut écrire:



Un des avantages de cette technique est l'élimination des signaux alternatifs parasites superposés au signal à mesurer si le temps d'intégration est convenablement choisi. Comme ces signaux parasites proviennent notamment du réseau 50 Hz, si la durée d'intégration est de 20 ms ou un multiple, les signaux parasites sont intégrés et n'interviennent que par leur valeur moyenne, qui est nulle. On dit alors qu'il y a réjection du bruit.

La précision de ce convertisseur reste liée, comme pour le convertisseur à simple rampe, à la précision et à la stabilité de l'intégrateur, de la tension de référence et à la période d'horloge. Il est difficile de réaliser une horloge stable et précise pendant une durée de plusieurs mois; par contre, sur une période assez courte, de quelques centaines de ms à quelques secondes, on peut admettre que la dérive de la fréquence de l'horloge est nulle.

La conversion à double rampe permettra de s'affranchir de l'instabilité à long terme de l'horloge.

Comparaison des différentes technologies

(CAN)			
Type	**Vitesse**	**Erreur**	**Résolution**
Simple Rampe	Faible (ms)	Elevée	Moyenne à élevée (7 à 14 bits)
Double Rampe	Faible (ms)	Faible	Elevée (10 à 18 bits)
Approximations Successives	Moyenne (quelque 10 µS)	Moyenne 0,5 à 1 LSB	Moyenne à élevée (8 à 16 bits)
Flash	Elevée (ns , µs)	Moyenne 0,5 à 1 LSB	Faible à élevée (4 à 10 bits)

Exemple des quelques convertisseur Analogique / Numérique

Référence	***Nombre de bits***	***Tc(µs)***	***linéarité (+/-LSB)***	***constructeur***	***prix HT***
ADC0804	8	73	1	Philips	56,7
ADC0808	8	100	0,5	Philips	58
AD673JN	8	30	0,5	Analog Devices	172
AD573JD	10	30	1	Analog Devices	570
AD773JD	10	0,055	1	Analog Devices	683,55
LTC1285CS8	12	100	2	Linear technologie	91
MAX186BCPP	12	10	1	Maxim	251

LTC1410CS	12	0,75	1	Linear technologie	290
AD679JN	14	7,8	2	Analog Devices	389,5
AD7885AQ	16	5,3	2	Analog Devices	536

http://www.analog.com/en/index.html

ADC0802, ADC0803 ADC0804

8-Bit, Microprocessor-Compatible, A/D Converters

August 1997

Features

- **80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required**
- **Conversion Time < 100μs**
- **Easy Interface to Most Microprocessors**
- **Will Operate in a "Stand Alone" Mode**
- **Differential Analog Voltage Inputs**
- **Works with Bandgap Voltage References**
- **TTL Compatible Inputs and Outputs**
- **On-Chip Clock Generator**
- **0V to 5V Analog Voltage Input Range (Single + 5V Supply)**
- **No Zero-Adjust Required**

Description

The ADC0802 family are CMOS 8-Bit, successive-approximation A/D converters which use a modified potentiometric ladder and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

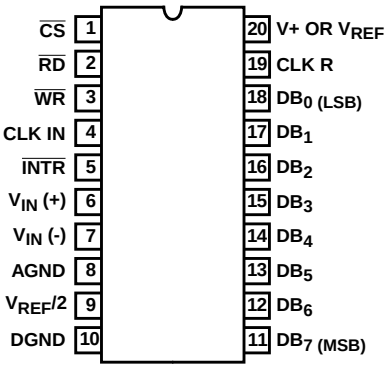
The differential analog voltage input has good common-mode-rejection and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Ordering Information

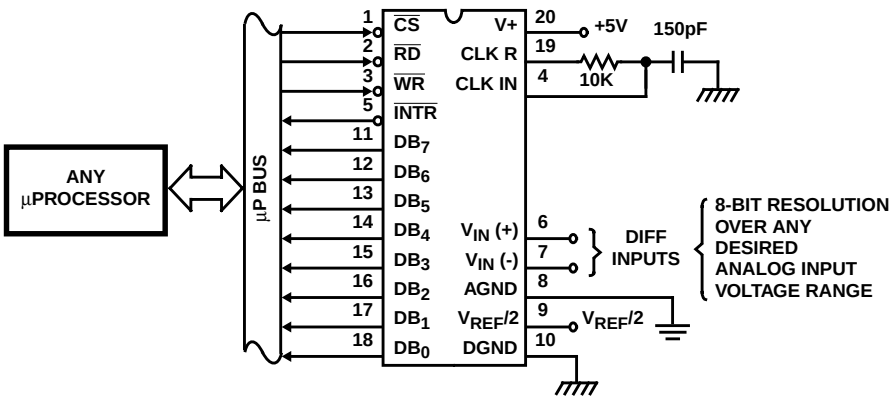
PART NUMBER	ERROR	EXTERNAL CONDITIONS	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO
ADC0802LCN	$\pm^{1}/_{2}$ LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3
ADC0802LCD	$\pm^{3}/_{4}$ LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0802LD	±1 LSB		-55 to 125	20 Ld CERDIP	F20.3
ADC0803LCN	$\pm^{1}/_{2}$ LSB	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	0 to 70	20 Ld PDIP	E20.3
ADC0803LCD	$\pm^{3}/_{4}$ LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0803LCWM	±1 LSB		-40 to 85	20 Ld SOIC	M20.3
ADC0803LD	±1 LSB		-55 to 125	20 Ld CERDIP	F20.3
ADC0804LCN	±1 LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3
ADC0804LCD	±1 LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0804LCWM	±1 LSB		-40 to 85	20 Ld SOIC	M20.3

Pinout

ADC0802, ADC0803, ADC0804
(PDIP, CERDIP)
TOP VIEW



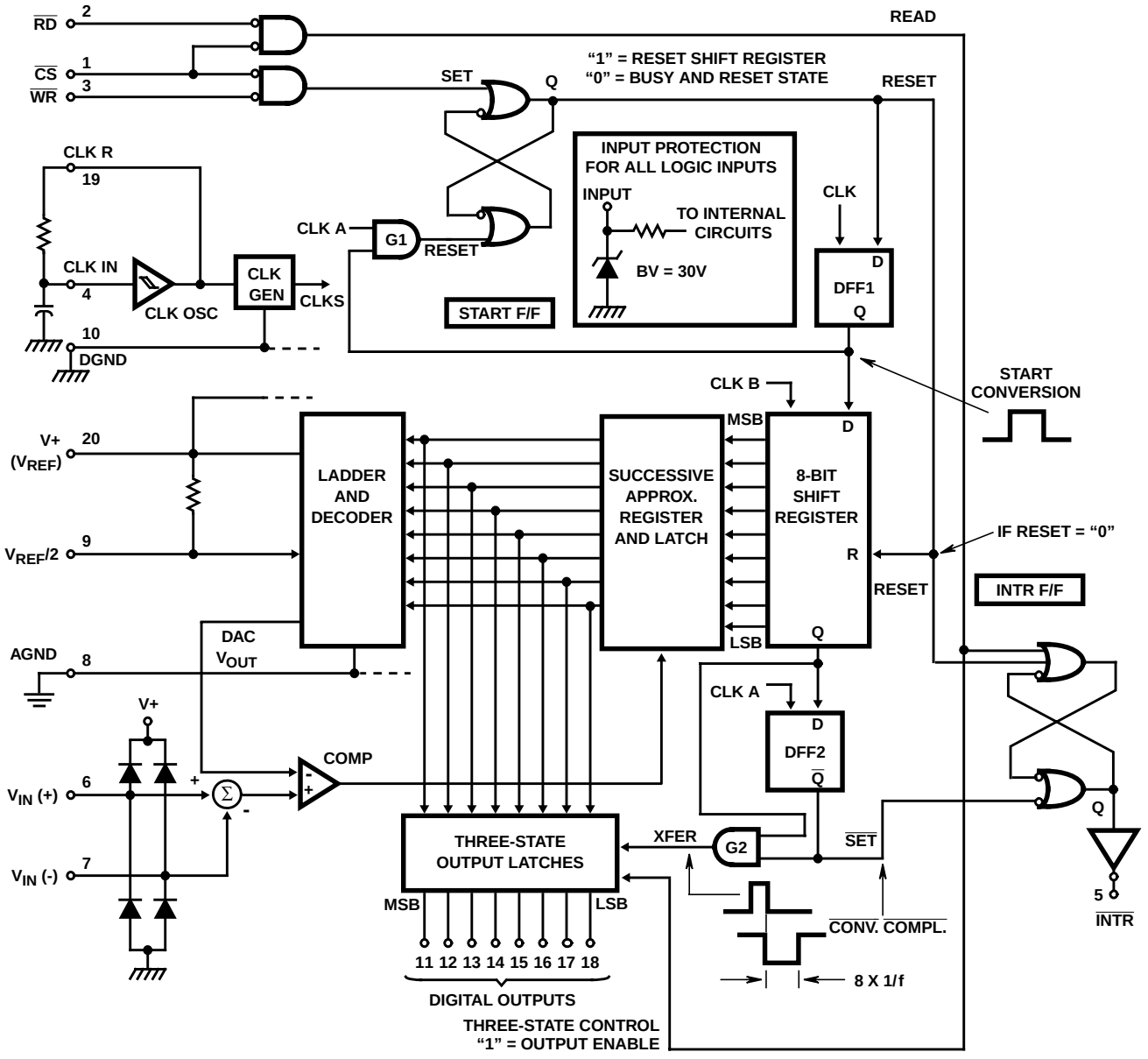
Typical Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **3094.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage 6.5V
Voltage at Any Input . . . . . -0.3V to (V^+ +0.3V)

Operating Conditions

Temperature Range
- ADC0802/03LD . . . . . -55^oC to 125^oC
- ADC0802/03/04LCD . . . . . -40^oC to 85^oC
- ADC0802/03/04LCN . . . . . 0^oC to 70^oC
- ADC0803/04LCWM . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	125	N/A
CERDIP Package	80	20
SOIC Package	120	N/A

Maximum Junction Temperature
- Hermetic Package . . . . . 175^oC
- Plastic Package . . . . . 150^oC

Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications (Notes 1, 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS	V+ = 5V, $T_A = 25^oC$ and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm 1/2$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	$\pm 1/2$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
CONVERTER SPECIFICATIONS	V+ = 5V, 0^oC to 70^oC and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm 1/2$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	$\pm 1/2$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
CONVERTER SPECIFICATIONS	V+ = 5V, -25^oC to 85^oC and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm 3/4$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	$\pm 3/4$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB

Electrical Specifications (Notes 1, 7) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS V+ = 5V, -55°C to 125°C and f_{CLK} = 640kHz, Unless Otherwise Specified					
Total Unadjusted Error ADC0802	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
AC TIMING SPECIFICATIONS V+ = 5V, and T_A = 25°C, Unless Otherwise Specified					
Clock Frequency, f_{CLK}	V+ = 6V (Note 3)	100	640	1280	kHz
	V+ = 5V	100	640	800	kHz
Clock Periods per Conversion (Note 4), t_{CONV}		62	-	73	Clocks/Conv
Conversion Rate In Free-Running Mode, CR	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0V, f_{CLK} = 640kHz	-	-	8888	Conv/s
Width of $\overline{WR}$ Input (Start Pulse Width), $t_{W(WR)I}$	$\overline{CS}$ = 0V (Note 5)	100	-	-	ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid), t_{ACC}	C_L = 100pF (Use Bus Driver IC for Larger C_L)	-	135	200	ns
Three-State Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State), t_{1H}, t_{0H}	C_L = 10pF, R_L= 10K (See Three-State Test Circuits)	-	125	250	ns
Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$, t_{WI}, t_{RI}		-	300	450	ns
Input Capacitance of Logic Control Inputs, C_{IN}		-	5	-	pF
Three-State Output Capacitance (Data Buffers), C_{OUT}		-	5	-	pF
DC DIGITAL LEVELS AND DC SPECIFICATIONS V+ = 5V, and T_{MIN} to T_{MAX}, Unless Otherwise Specified					
CONTROL INPUTS (Note 6)					
Logic "1" Input Voltage (Except Pin 4 CLK IN), V_{INH}	V+ = 5.25V	2.0	-	V+	V
Logic "0" Input Voltage (Except Pin 4 CLK IN), V_{INL}	V+ = 4.75V	-	-	0.8	V
CLK IN (Pin 4) Positive Going Threshold Voltage, $V+_{CLK}$		2.7	3.1	3.5	V
CLK IN (Pin 4) Negative Going Threshold Voltage, $V-_{CLK}$		1.5	1.8	2.1	V
CLK IN (Pin 4) Hysteresis, V_H		0.6	1.3	2.0	V
Logic "1" Input Current (All Inputs), I_{INHI}	V_{IN} = 5V	-	0.005	1	µA
Logic "0" Input Current (All Inputs), I_{INLO}	V_{IN} = 0V	-1	-0.005	-	µA
Supply Current (Includes Ladder Current), I+	f_{CLK} = 640kHz, T_A = 25°C and $\overline{CS}$ = HI	-	1.3	2.5	mA
DATA OUTPUTS AND $\overline{INTR}$					
Logic "0" Output Voltage, V_{OL}	I_O = 1.6mA, V+ = 4.75V	-	-	0.4	V

Electrical Specifications (Notes 1, 7) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Output Voltage, V_{OH}	I_O = -360µA, V+ = 4.75V	2.4	-	-	V
Three-State Disabled Output Leakage (All Data Buffers), I_{LO}	V_{OUT} = 0V	-3	-	-	µA
	V_{OUT} = 5V	-	-	3	µA
Output Short Circuit Current, I_{SOURCE}	V_{OUT} Short to Gnd $T_A = 25^oC$	4.5	6	-	mA
Output Short Circuit Current, I_{SINK}	V_{OUT} Short to V+ $T_A = 25^oC$	9.0	16	-	mA

NOTES:

1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.
2. For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V+ supply. Be careful, during testing at low V+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct - especially at elevated temperatures, and cause errors for analog inputs near full scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.
3. With V+ = 6V, the digital logic interfaces are no longer TTL compatible.
4. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.
5. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).
6. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.
7. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0V, or if a narrow full scale span exists (for example: 0.5V to 4V full scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See the Zero Error description in this data sheet.

Timing Waveforms

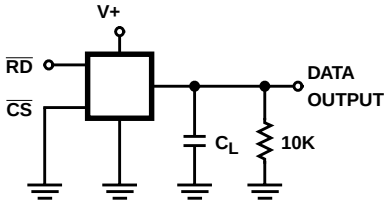


FIGURE 1A. t_{1H}

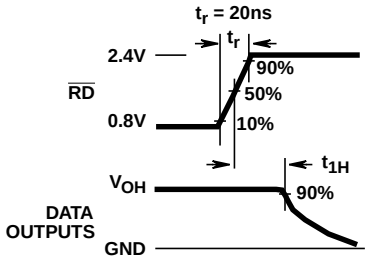


FIGURE 1B. t_{1H}, C_L = 10pF

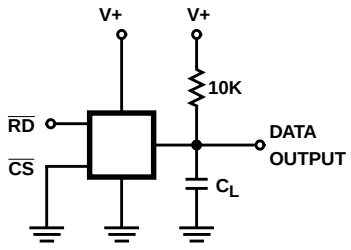


FIGURE 1C. t_{0H}

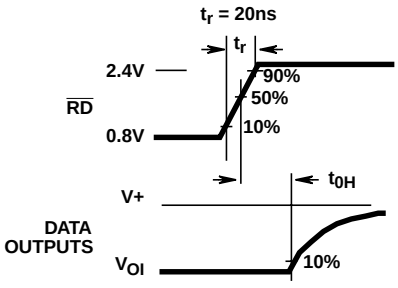


FIGURE 1D. t_{0H}, C_L = 10pF

FIGURE 1. THREE-STATE CIRCUITS AND WAVEFORMS

Typical Performance Curves

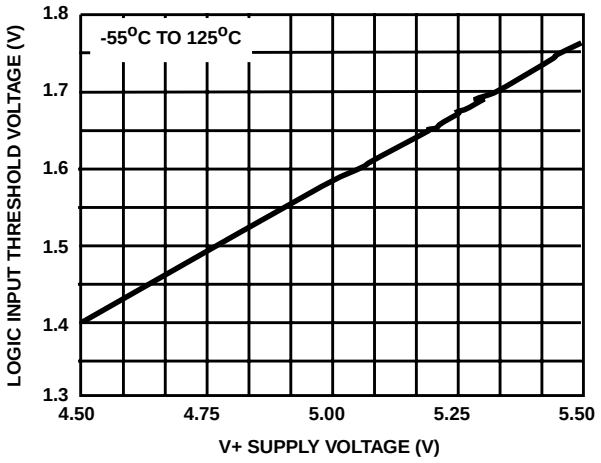


FIGURE 2. LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

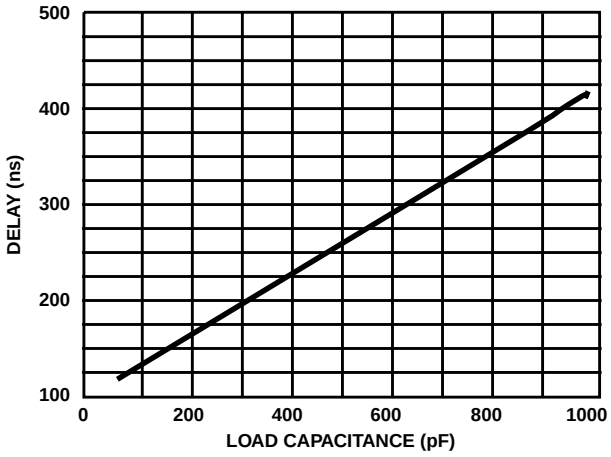


FIGURE 3. DELAY FROM FALLING EDGE OF $\overline{RD}$ TO OUTPUT DATA VALID vs LOAD CAPACITANCE

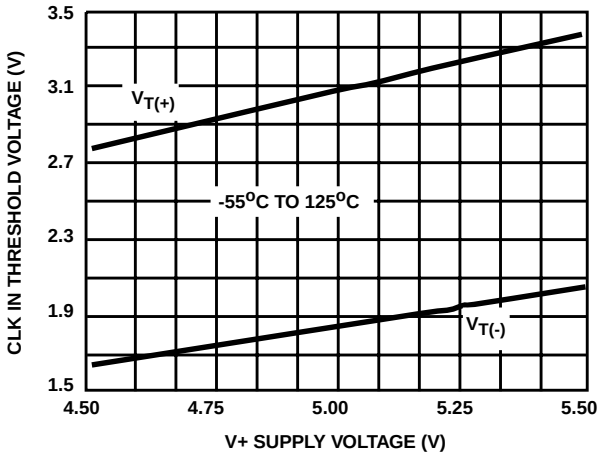


FIGURE 4. CLK IN SCHMITT TRIP LEVELS vs SUPPLY VOLTAGE

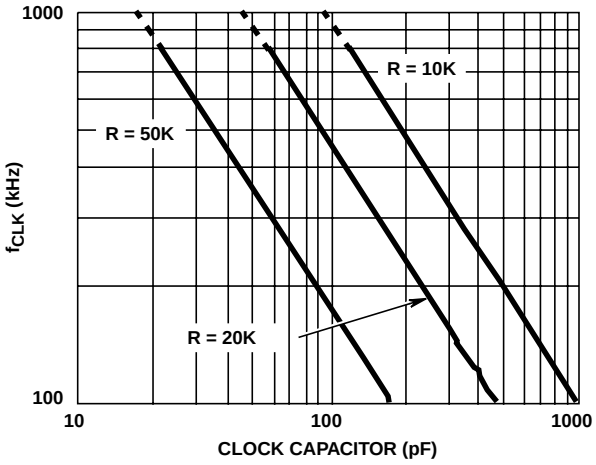


FIGURE 5. f_{CLK} vs CLOCK CAPACITOR

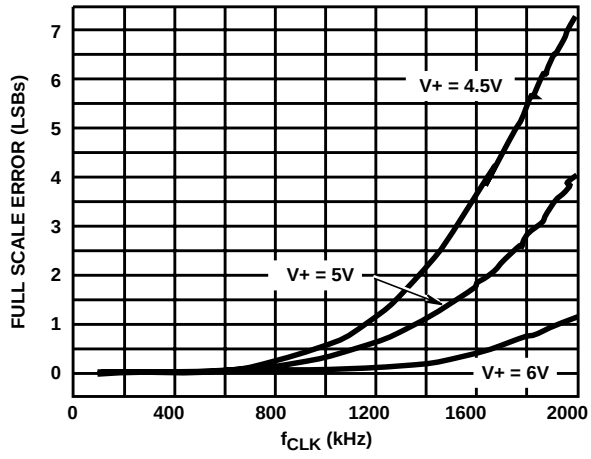


FIGURE 6. FULL SCALE ERROR vs f_{CLK}

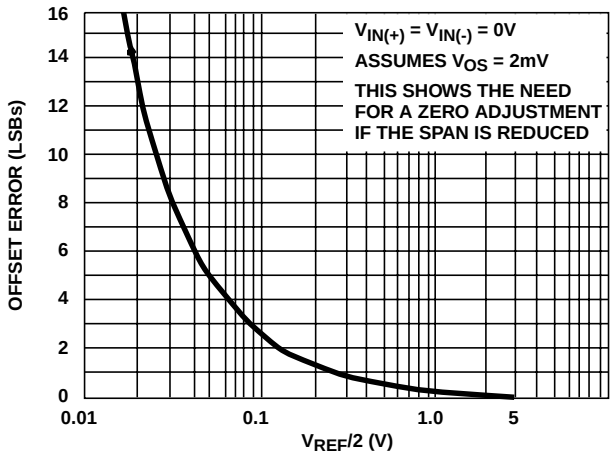


FIGURE 7. EFFECT OF UNADJUSTED OFFSET ERROR

Typical Performance Curves (Continued)

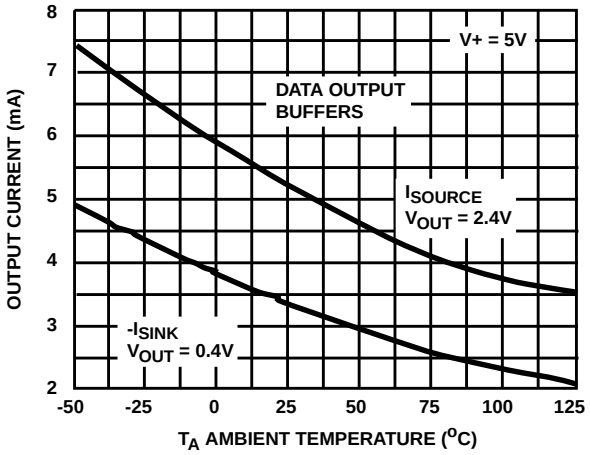


FIGURE 8. OUTPUT CURRENT vs TEMPERATURE

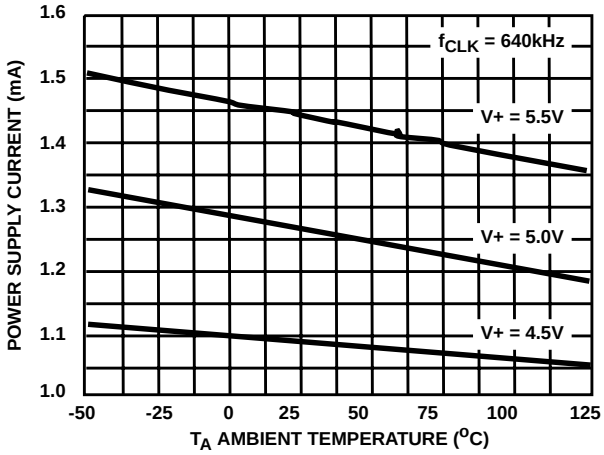


FIGURE 9. POWER SUPPLY CURRENT vs TEMPERATURE

Timing Diagrams

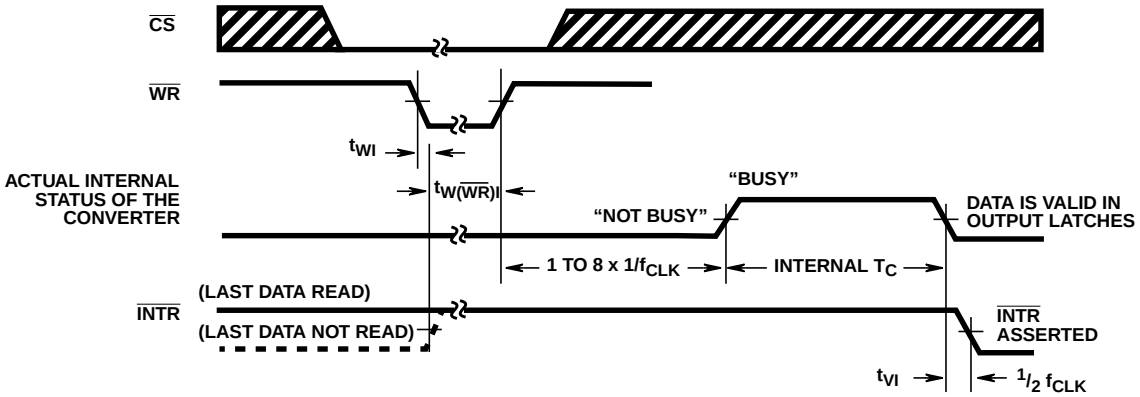


FIGURE 10A. START CONVERSION

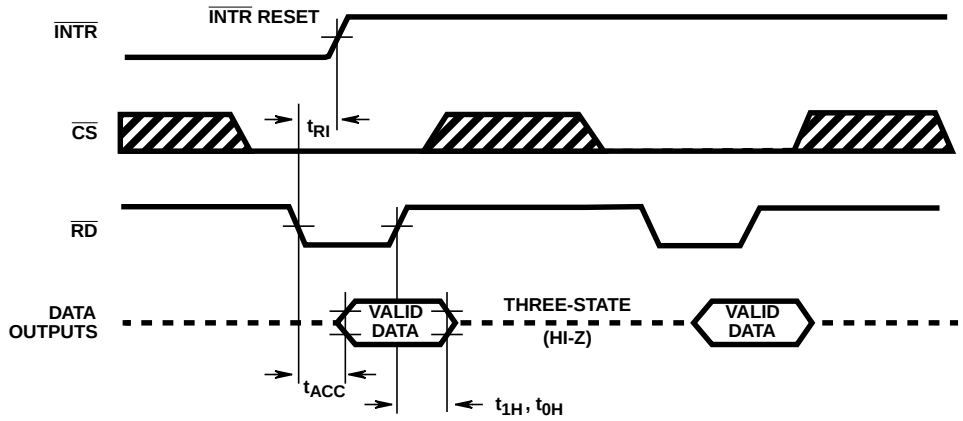


FIGURE 10B. OUTPUT ENABLE AND RESET INTR

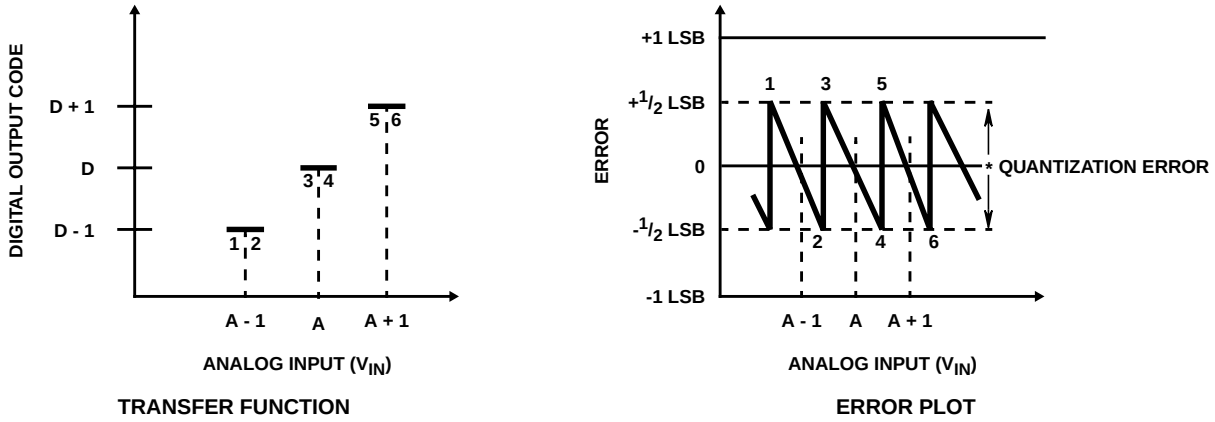


FIGURE 11A. ACCURACY = ±0 LSB; PERFECT A/D

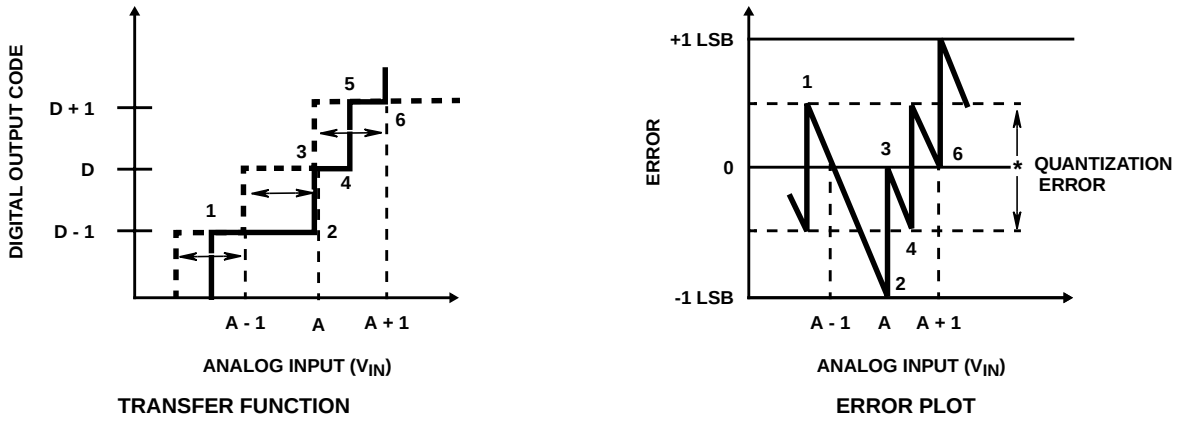


FIGURE 11B. ACCURACY = ±1/2 LSB

FIGURE 11. CLARIFYING THE ERROR SPECS OF AN A/D CONVERTER

Understanding A/D Error Specs

A perfect A/D transfer characteristic (staircase wave-form) is shown in Figure 11A. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D-1, D, and D+1. For the perfect A/D, not only will center-value (A - 1, A, A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located $\pm 1/2$ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend $\pm 1/2$ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

The error curve of Figure 11B shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 11A is $+1/2$ LSB because the digital code appeared $1/2$ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude, unless the device has missing codes.

Detailed Description

The functional diagram of the ADC0802 series of A/D converters operates on the successive approximation principle (see Application Notes AN016 and AN020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the WR input, the internal SAR latches and the shift-register stages are reset, and the INTR output will be set high. As long as the CS input and WR input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition. After the requisite number of clock pulses to complete the conversion, the INTR pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A RD operation (with CS low) will clear the INTR line high again.

The device may be operated in the free-running mode by connecting INTR to the WR input with CS = 0. To ensure start-up under all possible conditions, an external WR pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

Digital Operation

The converter is started by having CS and WR simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either WR or CS is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide CS and WR signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the Three-State output latches. When DFF2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the three-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs (CS, RD, and WR) meet standard TTL logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the CS input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the WR input (pin 3). The Output Enable function is achieved by an active low pulse at the RD input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by $^1/_2$ LSB (see Figure 11A).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA - 20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is $4^1/_2$ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_E(MAX) = (V_{PEAK})(2\pi f_{CM})\left[\frac{4.5}{f_{CLK}}\right]$$

where:

ΔV_E is the error voltage due to sampling delay,

V_{PEAK} is the peak value of the common-mode voltage,

f_{CM} is the common-mode frequency.

For example, with a 60Hz common-mode frequency, f_{CM}, and a 640kHz A/D clock, f_{CLK}, keeping this error to $^1/_4$ LSB (~5mV) would allow a common-mode voltage, V_{PEAK}, given by:

$$V_{PEAK} = \frac{\left[\Delta V_{E(MAX)(f_{CLK})}\right]}{(2\pi f_{CM})(4.5)},$$

or

$$V_{PEAK} = \frac{(5\times10^{-3})(640\times10^{3})}{(6.28)(60)(4.5)} \cong 1.9V.$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see Reference Voltage Span Adjust).

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and do not inherently cause errors as the on-chip comparator is strobed at the end of the clock perlod.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5μA. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$** pin for high resistance sources (>1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used will not cause errors since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor (≤1kΩ) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications (≤1kΩ), a 0.1μF bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5kΩ. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see Analog Input Current). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full scale adjustment of the A/D (see Full Scale Adjustment) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 12.

Notice that the reference voltage for the IC is either $^1/_2$ of the voltage which is applied to the V+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to $^1/_2$ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 13. For expanded scale inputs, the circuits of Figures 14 and 15 can be used.

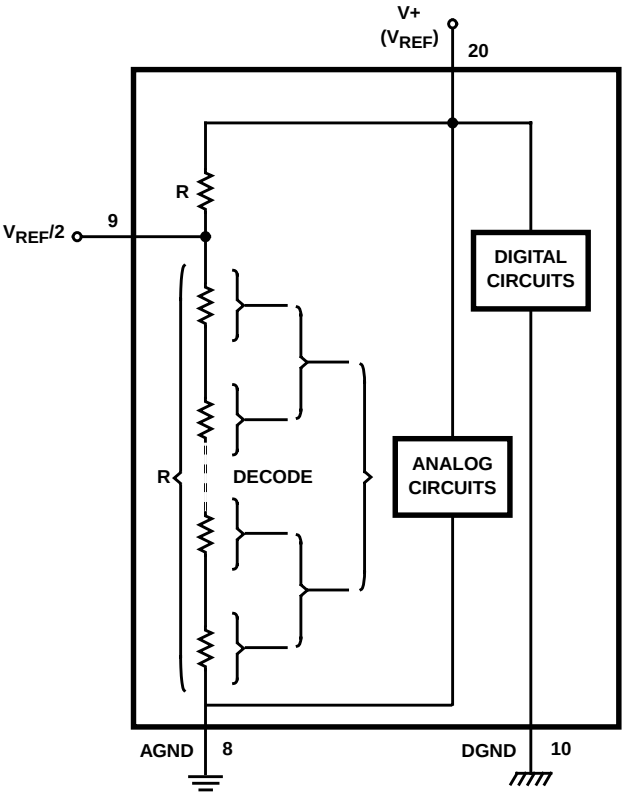


FIGURE 12. THE $V_{REFERENCE}$ DESIGN ON THE IC

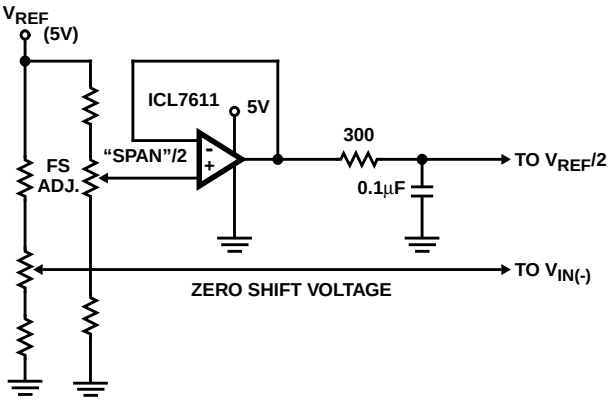


FIGURE 13. OFFSETTING THE ZERO OF THE ADC0802 AND PERFORMING AN INPUT RANGE (SPAN) ADJUSTMENT

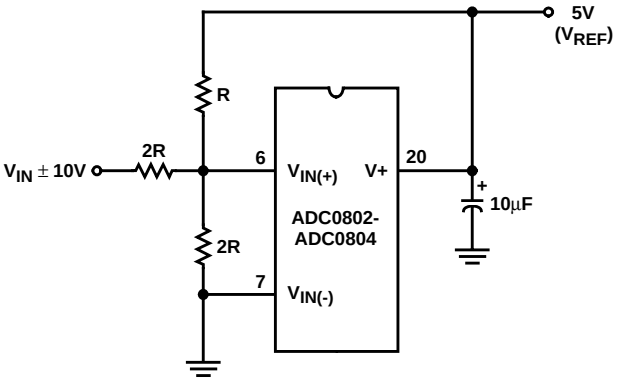


FIGURE 14. HANDLING ±10V ANALOG INPUT RANGE

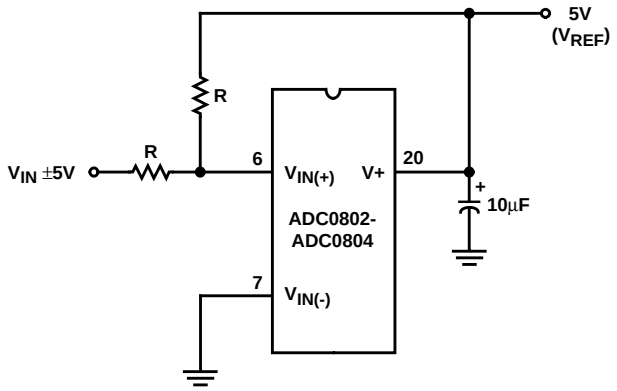


FIGURE 15. HANDLING ±5V ANALOG INPUT RANGE

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applicatIons, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of ±10mV will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1 LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal $^1/_2$ LSB value ($^1/_2$ LSB = 9.8mV for $V_{REF}/2$ = 2.500V).

Full Scale Adjust

The full scale adjustment can be made by applying a differential input voltage which is $1^1/_2$ LSB down from the desired analog full scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}f_{SADJ} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range,

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provIde self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 16.

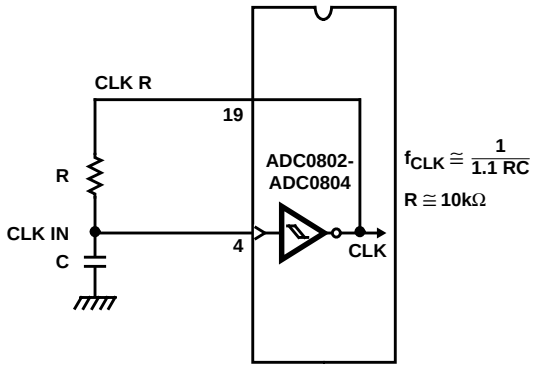


FIGURE 16. SELF-CLOCKING THE A/D

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 17 for details.

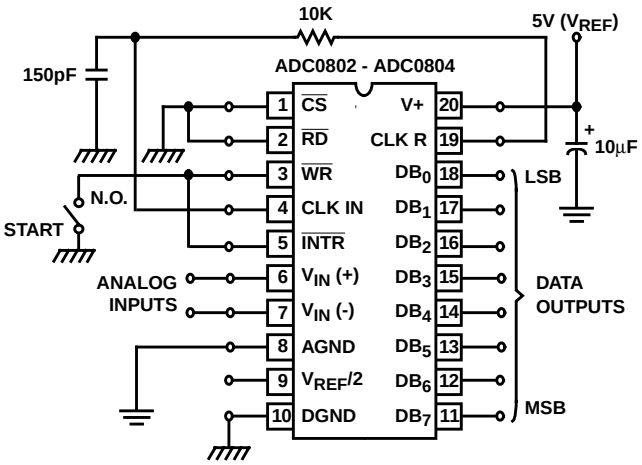


FIGURE 17. FREE-RUNNING CONNECTION

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in three-state (high-impedance mode). Back plane busing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see Typical Performance Curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be three-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V+ pin, and values of 1µF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clockIng capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of $^1/_4$ LSB can usually be traced to improper board layout and wiring (see Zero Error for measurement). Further information can be found in Application Note AN018.

Testing the A/D Converter

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 18.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full scale adjustment is to be made, an analog input voltage of 5.090V (5.120 - $1^1/_2$ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)V.$$

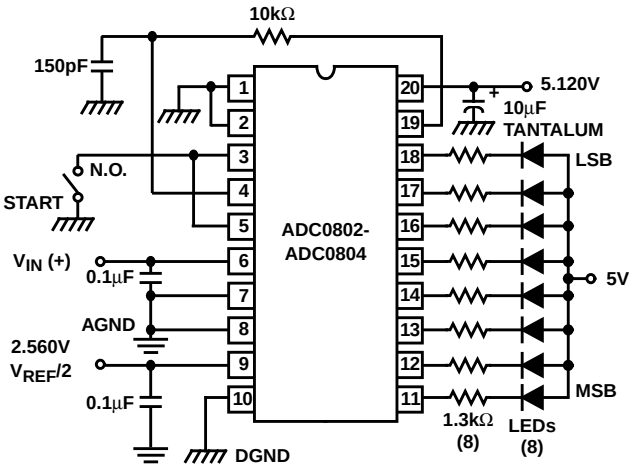


FIGURE 18. BASIC TESTER FOR THE A/D

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so:

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.64V.$$

Figures 19 and 20 show more sophisticated test circuits.

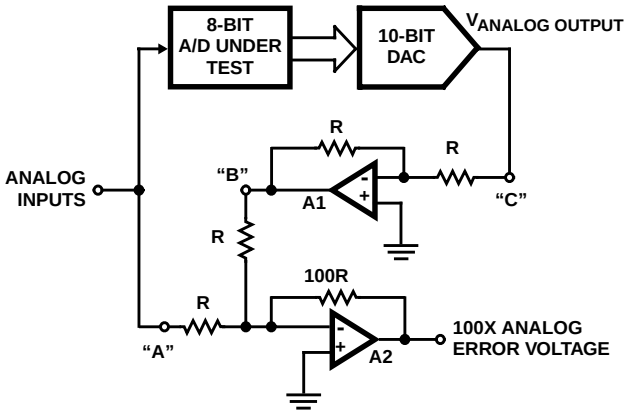


FIGURE 19. A/D TESTER WITH ANALOG ERROR OUTPUT. THIS CIRCUIT CAN BE USED TO GENERATE "ERROR PLOTS" OF FIGURE 11.

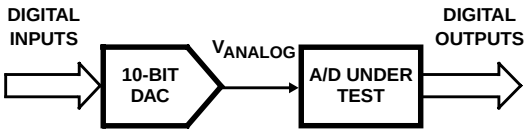


FIGURE 20. BASIC "DIGITAL" A/D TESTER

Typical Applications

Interfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The three-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/OR}$ and $\overline{I/OW}$ strobes and decoding the address bits A0 $\rightarrow$ A7 (or address bits A8 $\rightarrow$ A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See AN020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 21.

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 22. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 22 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO}$/M for an I/O-mapped connection.

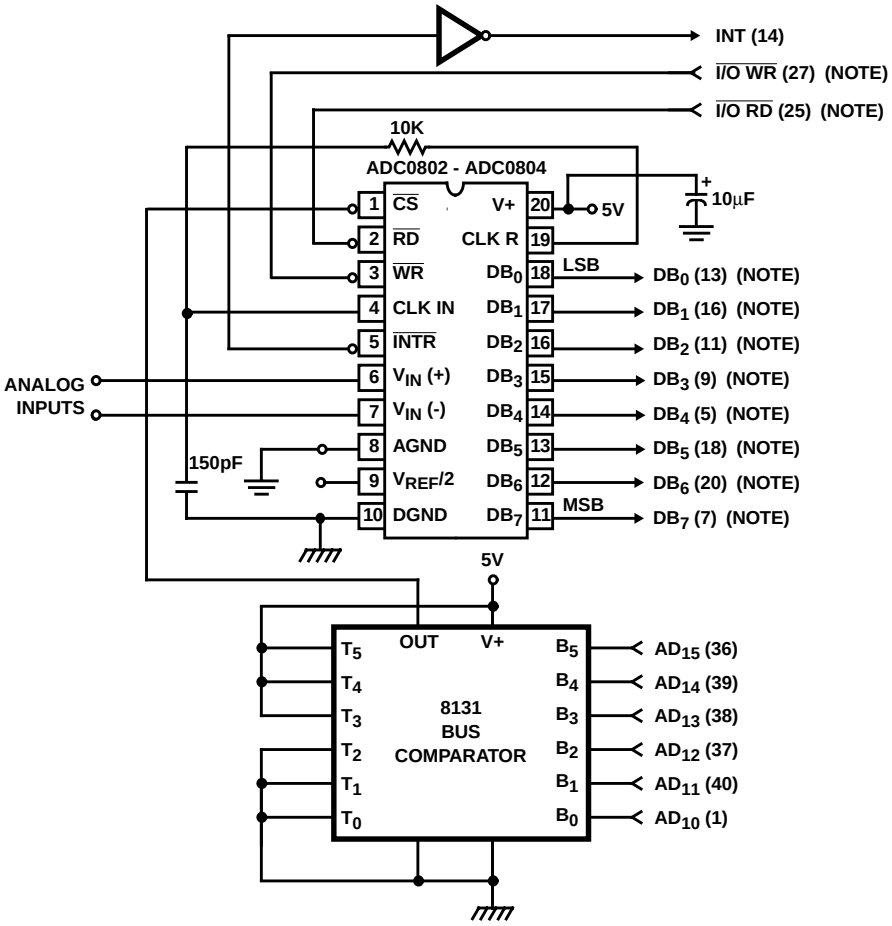
Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the RD and WR strobe signals. Instead it employs a single R/W line and additional timing, if needed, can be derived from the ϕ2 clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 23 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the CS decoding is shown using $^1/_2$ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the CS pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 24 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the CS pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no CS decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D RD pin can be grounded.

Application Notes

NOTE #	DESCRIPTION	AnswerFAX DOC. #
AN016	"Selecting A/D Converters"	9016
AN018	"Do's and Don'ts of Applying A/D Converters"	9018
AN020	"A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"	9020
AN030	"The ICL7104 - A Binary Output A/D Converter for Microprocessors"	9030



NOTE: Pin numbers for 8228 System Controller: Others are 8080A.

FIGURE 21. ADC0802 TO 8080A CPU INTERFACE

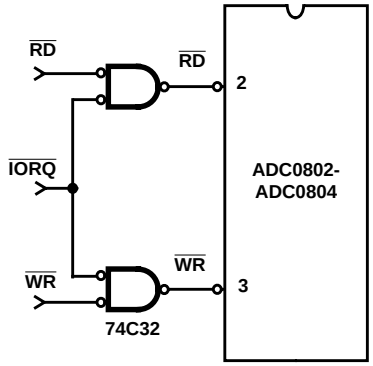
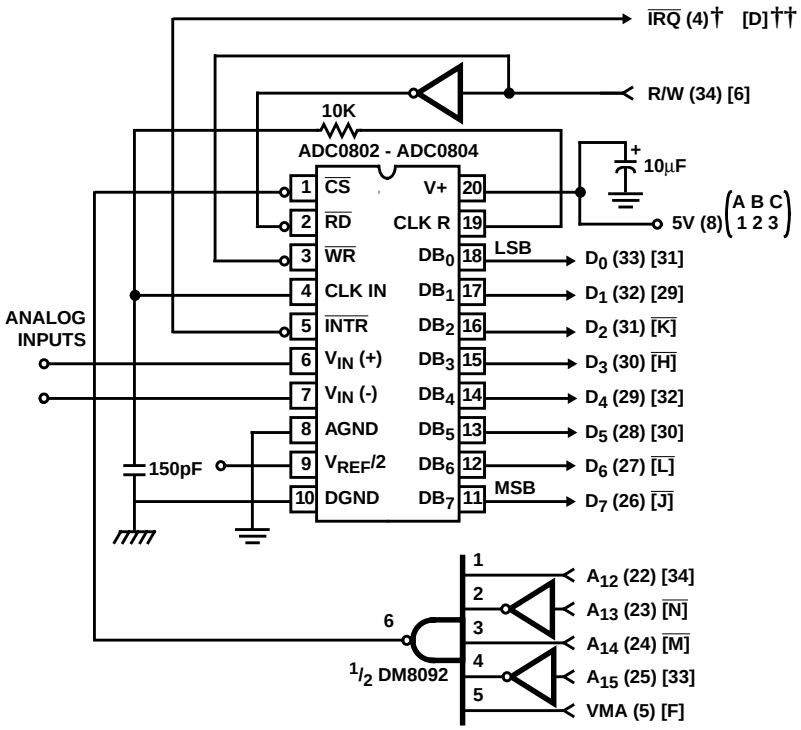


FIGURE 22. MAPPING THE A/D AS AN I/O DEVICE FOR USE WITH THE Z-80 CPU



† Numbers in parentheses refer to MC6800 CPU Pinout.
†† Numbers or letters in brackets refer to standard MC6800 System Common Bus Code.

FIGURE 23. ADC0802 TO MC6800 CPU INTERFACE

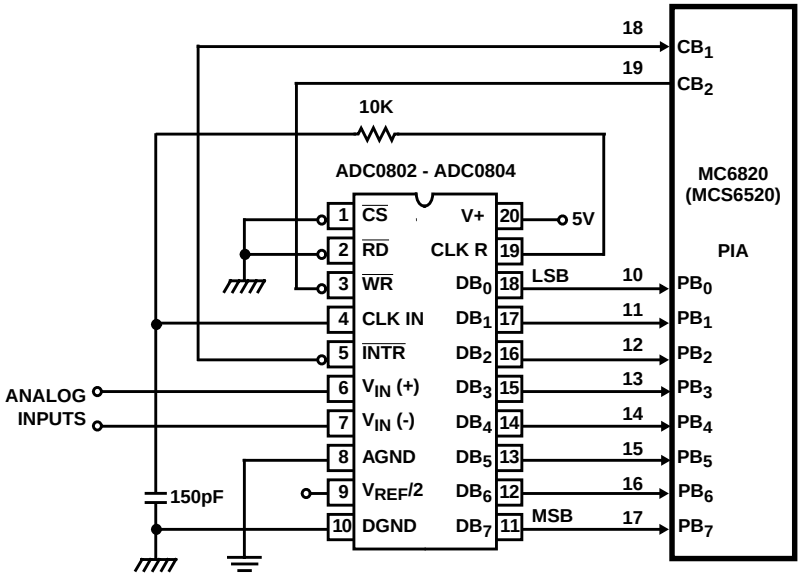


FIGURE 24. ADC0802 TO MC6820 PIA INTERFACE

Die Characteristics

DIE DIMENSIONS:

(101 mils x 93 mils) x 525µm x 25µm

METALLIZATION:

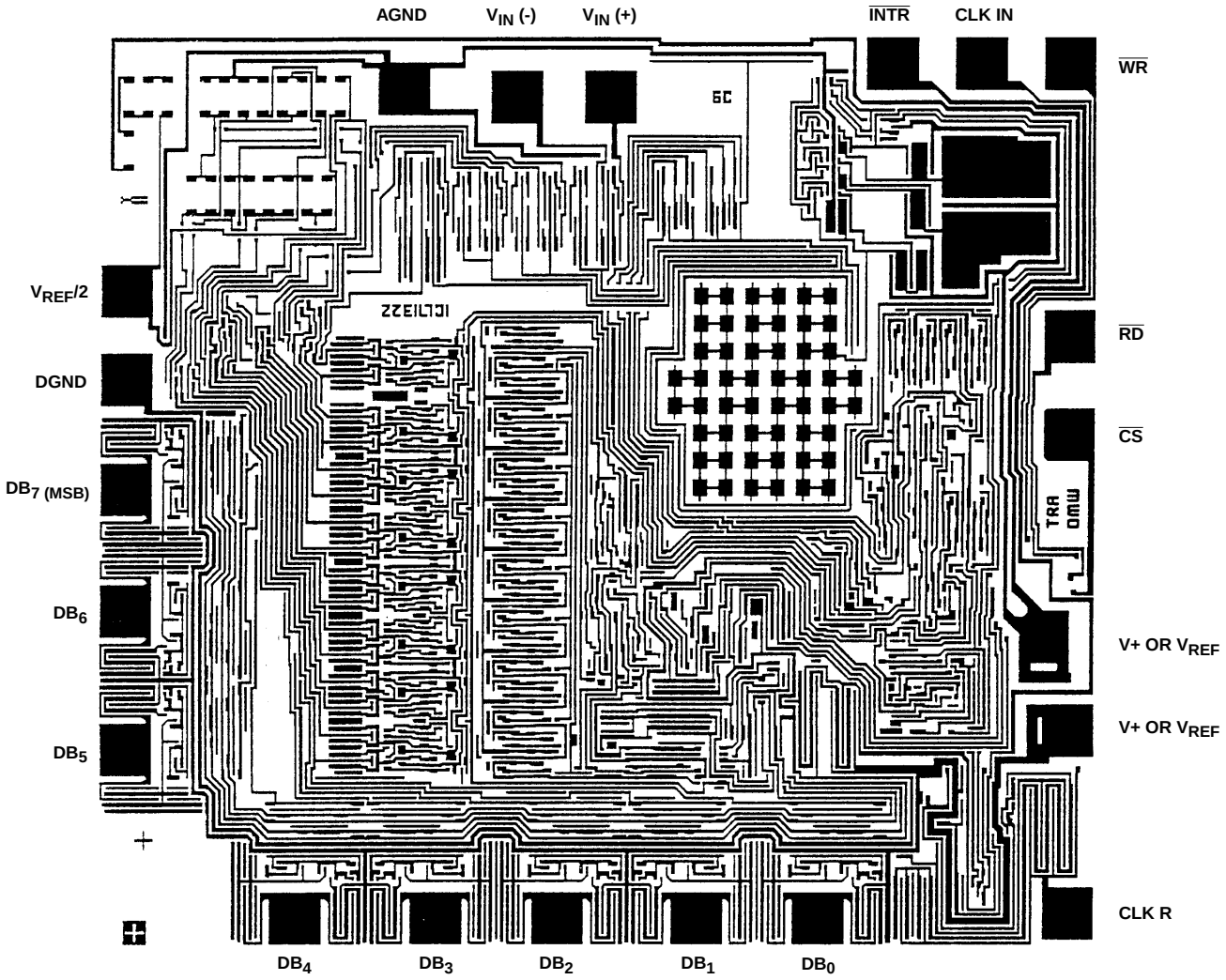
Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

Metallization Mask Layout

ADC0802, ADC0803, ADC0804



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National Semiconductor

October 1999

ADC0808/ADC0809
8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

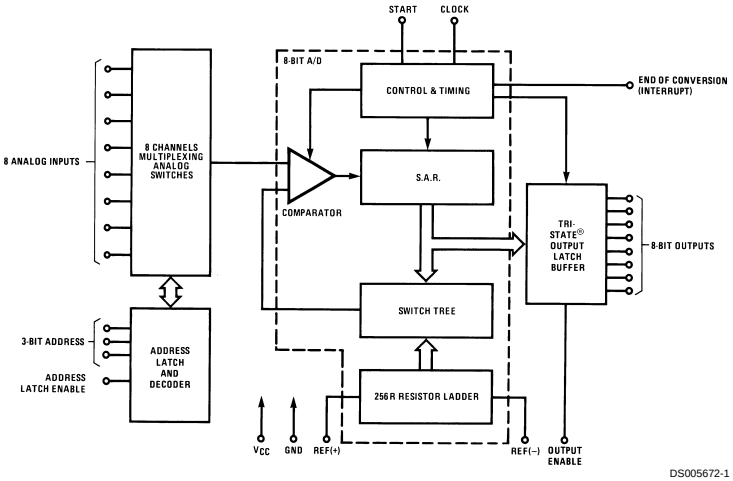
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

Block Diagram



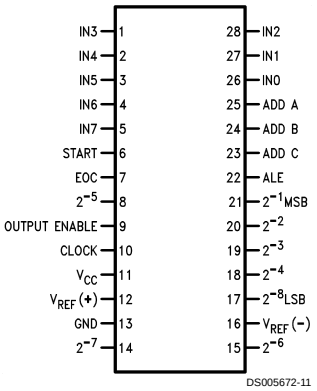
DS005672-1

See Ordering Information

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Connection Diagrams

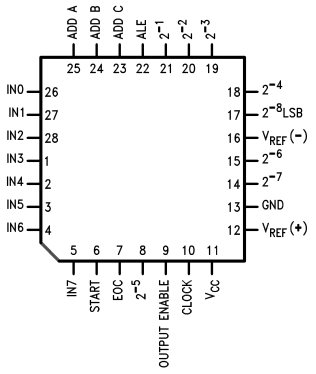
Dual-In-Line Package



DS005672-11

Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



DS005672-12

Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		−40˚C to +85˚C			−55˚C to +125˚C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC}+0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65˚C to +150˚C
Package Dissipation at T_A=25˚C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260˚C
Dual-In-Line Package (ceramic)	300˚C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1, 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CCN,ADC0809CCN	−40˚C≤T_A≤+85˚C
ADC0808CCV, ADC0809CCV	−40˚C ≤ T_A ≤ +85˚C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25˚C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0˚C to 70˚C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	µA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40˚C≤T_A≤+85˚C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25˚C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	µA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25˚C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			µA
CONTROL INPUTS						
$V_{IN(1)}$	Logical “1” Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical “0” Input Voltage				1.5	V
$I_{IN(1)}$	Logical “1” Input Current (The Control Inputs)	V_{IN}=15V			1.0	µA
$I_{IN(0)}$	Logical “0” Input Current (The Control Inputs)	V_{IN}=0	−1.0			µA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40^{\circ}C \le T_A \le +85^{\circ}C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA		**2.4** **4.5**		V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3	µA µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Mln	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_s	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_c	Conversion Time	f_c=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless othewise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3.* None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13.*

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 6*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1.

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

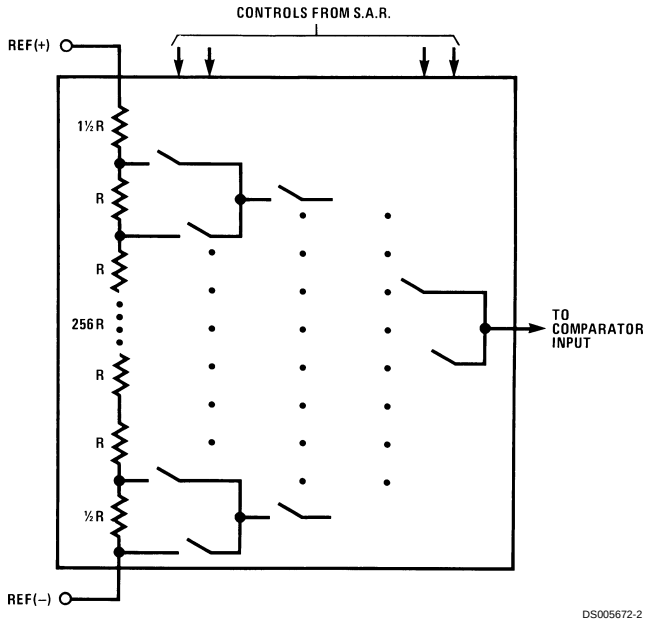


FIGURE 1. Resistor Ladder and Switch Tree

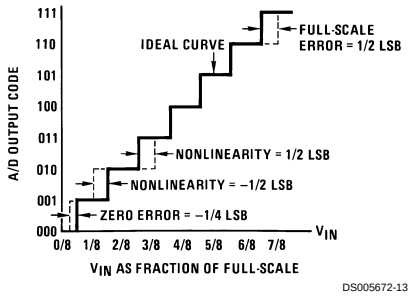


FIGURE 2. 3-Bit A/D Transfer Curve

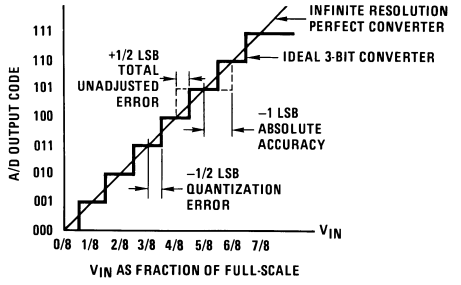


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

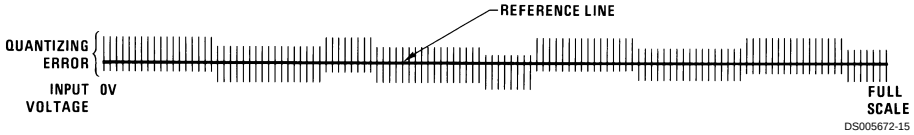


FIGURE 4. Typical Error Curve

Timing Diagram

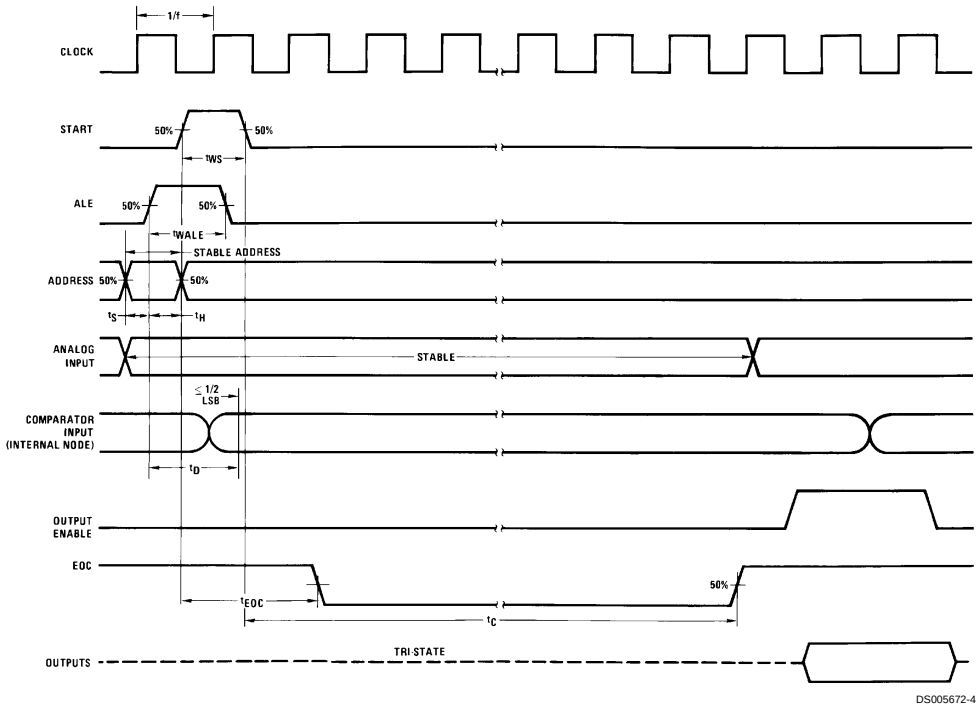


FIGURE 5.

Typical Performance Characteristics

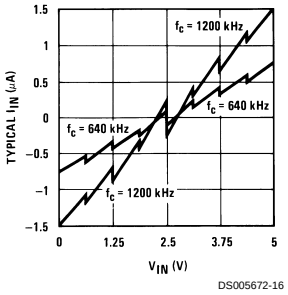


FIGURE 6. Comparator I_{IN} vs V_{IN} (V_{CC}=V_{REF}=5V)

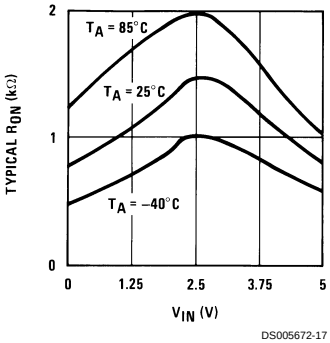


FIGURE 7. Multiplexer R_{ON} vs V_{IN} (V_{CC}=V_{REF}=5V)

TRI-STATE Test Circuits and Timing Diagrams

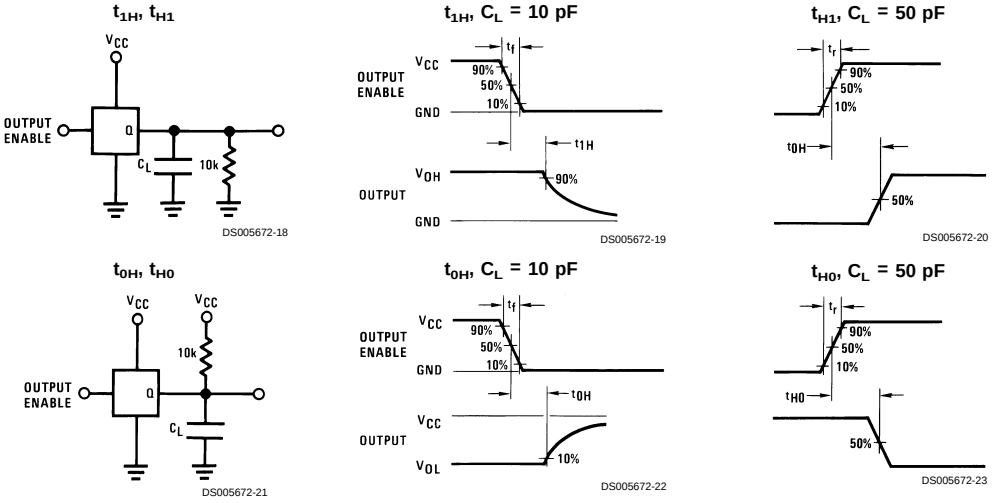


FIGURE 8.

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \qquad (1)$$

V_{IN}=Input voltage into the ADC0808

V_{fs}=Full-scale voltage

V_Z=Zero voltage

D_X=Data point being measured

D_{MAX}=Maximum data limit

D_{MIN}=Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a sys-

Applications Information (Continued)

tem reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

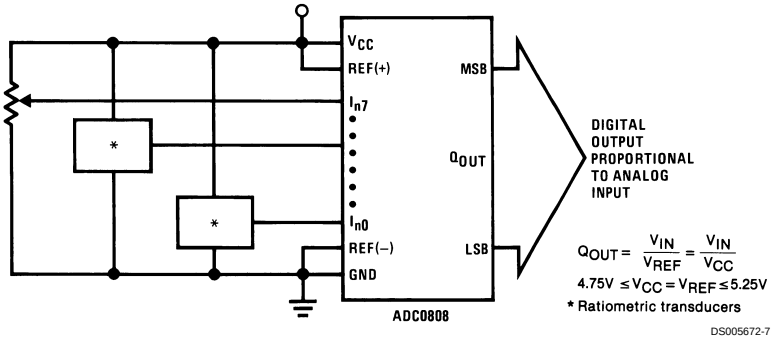
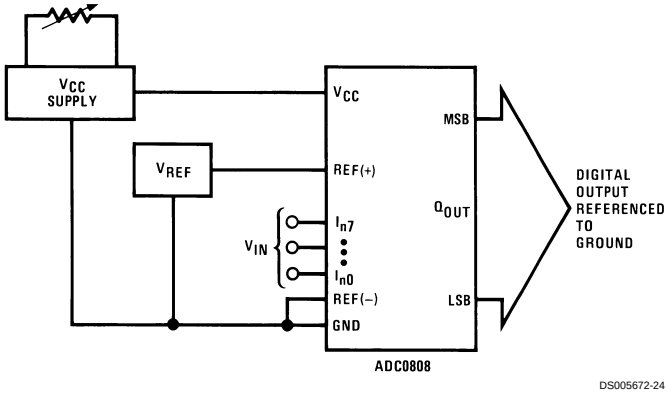


FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 µF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

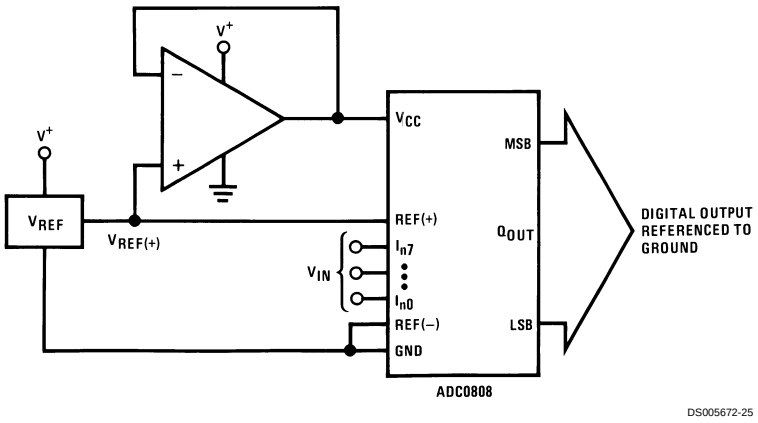
Applications Information (Continued)



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

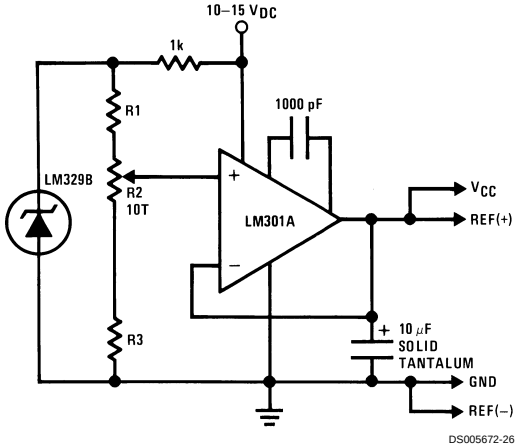
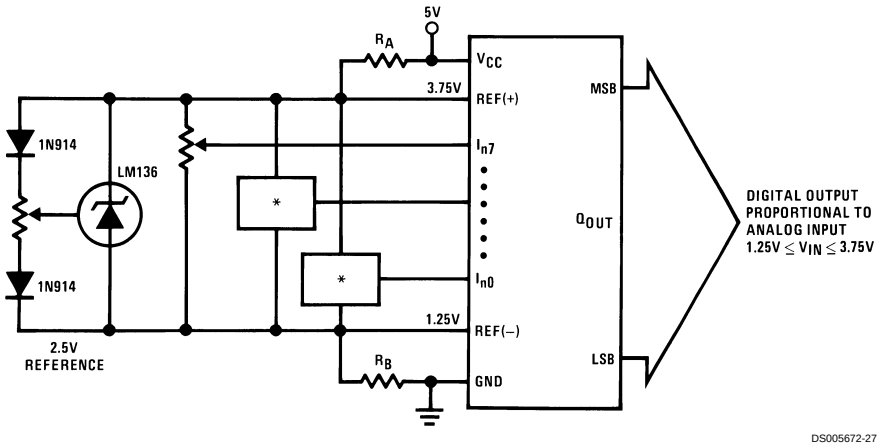


FIGURE 12. Typical Reference and Supply Circuit



$R_A = R_B$

*Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

Where: V_{IN}=Voltage at comparator input
$V_{REF(+)}$=Voltage at Ref(+)
$V_{REF(-)}$=Voltage at Ref(−)
V_{TUE}=Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

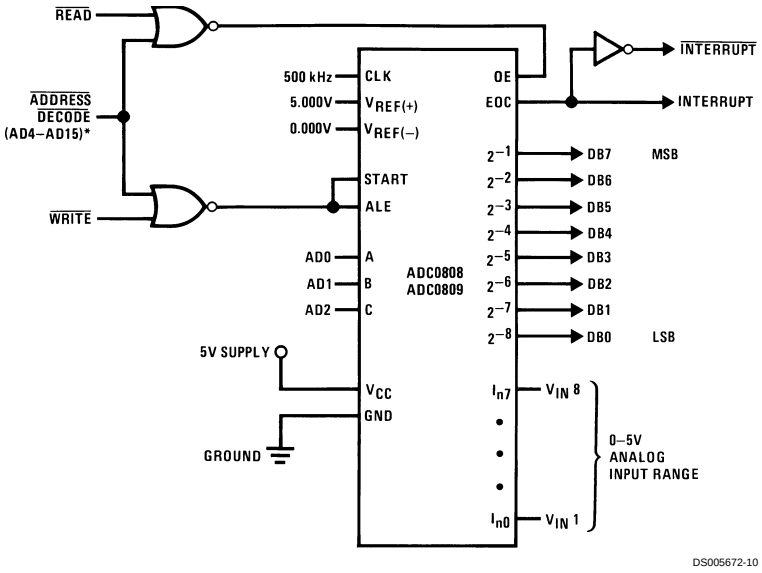
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application

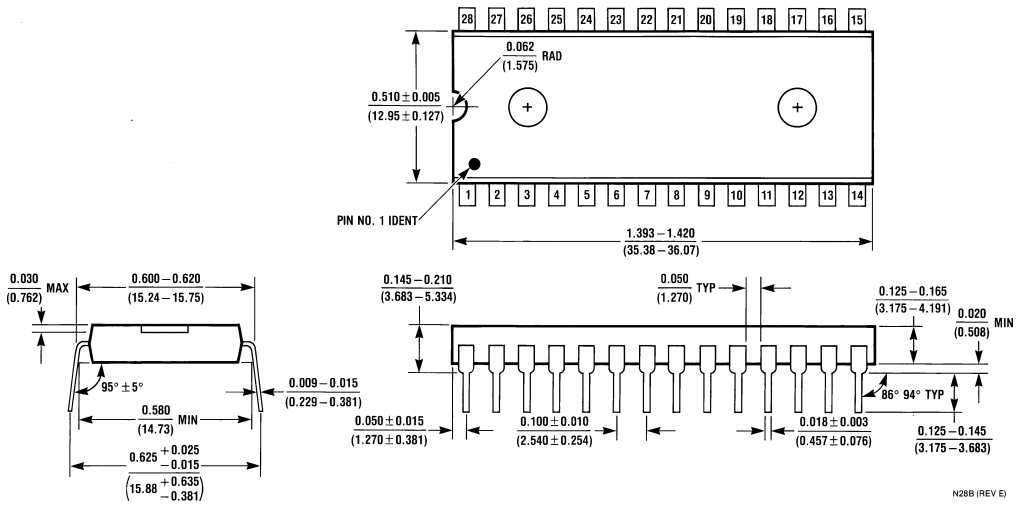


*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

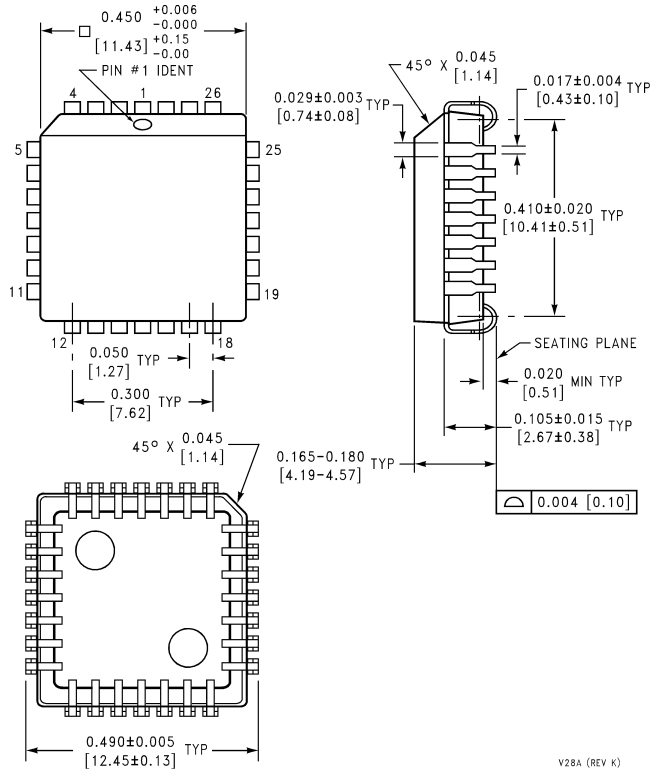
TABLE 2. Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ2•R/W	VMA•ϕ•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number ADC0808CCN or ADC0809CCN
NS Package Number N28B



Molded Chip Carrier (V)
Order Number ADC0808CCV or ADC0809CCV
NS Package Number V28A

Notes

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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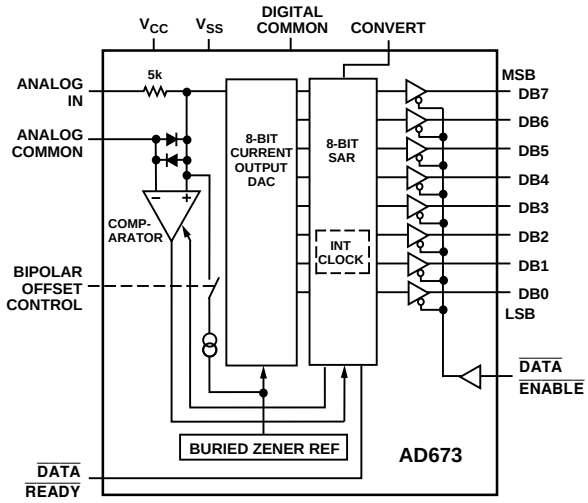
8-Bit A/D Converter

AD673*

FEATURES

Complete 8-Bit A/D Converter with Reference, Clock and Comparator
30 μs Maximum Conversion Time
Full 8- or 16-Bit Microprocessor Bus Interface
Unipolar and Bipolar Inputs
No Missing Codes Over Temperature
Operates on +5 V and –12 V to –15 V Supplies
MIL-STD-883 Compliant Version Available

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD673 is a complete 8-bit successive approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3-state output buffers—all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 20 μs.

The AD673 incorporates advanced integrated circuit design and processing technologies. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin-film resistor ladder network insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5 V and –12 V to –15 V, the AD673 will accept analog inputs of 0 V to +10 V or –5 V to +5 V. The trailing edge of a positive pulse on the CONVERT line initiates the 20 μs conversion cycle. $\overline{\text{DATA}}$ $\overline{\text{READY}}$ indicates completion of the conversion.

The AD673 is available in two versions. The AD673J as specified over the 0°C to +70°C temperature range and the AD673S guarantees ±1/2 LSB relative accuracy and no missing codes from –55°C to +125°C.

Two package configurations are offered. All versions are also offered in a 20-pin hermetically sealed ceramic DIP. The AD673J is also available in a 20-pin plastic DIP.

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690.**

PRODUCT HIGHLIGHTS

1. The AD673 is a complete 8-bit A/D converter. No external components are required to perform a conversion.
2. The AD673 interfaces to many popular microprocessors without external buffers or peripheral interface adapters.
3. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD673 adapts to either unipolar (0 V to +10 V) or bipolar (–5 V to +5 V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5 V and –12 V or –15 V supplies.
6. The AD673 is available in a version compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD673/883B data sheet for detailed specifications.

REV. A

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Tel: 617/329-4700 **Fax: 617/326-8703**

AD673—SPECIFICATIONS

(T_A = +25°C, V+ = +5 V, V– = –12 V or –15 V, all voltages measured with respect to digital common, unless otherwise noted)

Model	AD673J Min	AD673J Typ	AD673J Max	AD673S Min	AD673S Typ	AD673S Max	Units
RESOLUTION		8			8		Bits
RELATIVE ACCURACY,[1]			**±1/2**			**±1/2**	LSB
$T_A = T_{MIN}$ to T_{MAX}			**±1/2**			**±1/2**	LSB
FULL-SCALE CALIBRATION[2]		±2			±2		LSB
UNIPOLAR OFFSET			**±1/2**			**±1/2**	LSB
BIPOLAR OFFSET			**±1/2**			**±1/2**	LSB
DIFFERENTIAL NONLINEARITY,[3]	**8**			**8**			Bits
$T_A = T_{MIN}$ to T_{MAX}	**8**			**8**			Bits
TEMPERATURE RANGE	0		+70	–55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			**±1**			**±1**	LSB
Bipolar Offset			**±1**			**±1**	LSB
Full-Scale Calibration[2]			**±2**			**±2**	LSB
POWER SUPPLY REJECTION							
Positive Supply							
+4.5 ≤ V+ ≤ +5.5 V			**±2**			**±2**	LSB
Negative Supply							
–15.75 V ≤ V– ≤ –14.25 V			**±2**			**±2**	LSB
–12.6 V ≤ V– ≤ –11.4 V			**±2**			**±2**	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	–5		+5	–5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4 V max, T_{MIN} to T_{MAX})	**3.2**			**3.2**			mA
Output Source Current[4]							
(V_{OUT} = 2.4 V min, T_{MIN} to T_{MAX})	**0.5**			**0.5**			mA
Output Leakage			**±40**			**±40**	µA
LOGIC INPUTS							
Input Current			**±100**			**±100**	µA
Logic "1"	**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**	V
CONVERSION TIME, T_A and							
T_{MIN} to T_{MAX}	10	20	**30**	10	20	**30**	µs
POWER SUPPLY							
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V–	–11.4	–15	–16.5	–11.4	–15	**–16.5**	V
OPERATING CURRENT							
V+		15	**20**		15	**20**	mA
V–		9	**15**		9	**15**	mA

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full-scale calibration is guaranteed trimmable to zero with an external 200 Ω potentiometer in place of the 15 Ω fixed resistor.
Full scale is defined as 10 volts minus 1 LSB, or 9.961 V.

[3]Defined as the resolution for which no missing codes will occur.

[4]The data output lines have active pull-ups to source 0 5 mA. The $\overline{DATA}$ $\overline{READY}$ line is open collector with a nominal 6 kΩ internal pull-up resistor.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . 0 V to +7 V
V– to Digital Common . . . . . 0 V to –16.5 V
Analog Common to Digital Common . . . . . ±1 V
Analog Input to Analog Common . . . . . ±15 V
Control Inputs . . . . . 0 V to V+
Digital Outputs (High Impedance State) . . . . . 0 V to V+
Power Dissipation . . . . . 800 mW

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option[1]
AD673JN	0°C to +70°C	±1/2 LSB max	Plastic DIP (N-20)
AD673JD	0°C to +70°C	±1/2 LSB max	Ceramic DIP (D-20)
AD673SD[2]	–55°C to +125°C	±1/2 LSB max	Ceramic DIP (D-20)
AD673JP	0°C to +70°C	±1/2 LSB max	PLCC (P-20A)

NOTES
[1]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier.
[2]For details on grade and package offering screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook .

FUNCTIONAL DESCRIPTION

A block diagram of the AD673 is shown in Figure 1. The positive CONVERT pulse must be at least 500 ns wide. $\overline{DR}$ goes high within 1.5 µs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 8-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5 kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is more, the bit is turned off. After testing all bits, the SAR contains a 8-bit binary code which accurately represents the input signal to within (0.05% of full scale).

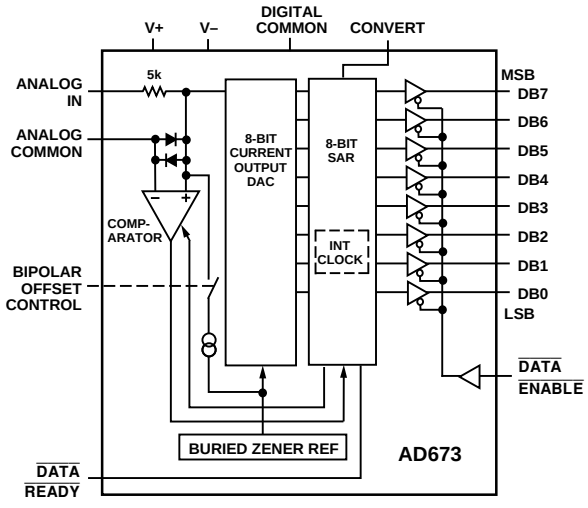


Figure 1. AD673 Functional Block Diagram

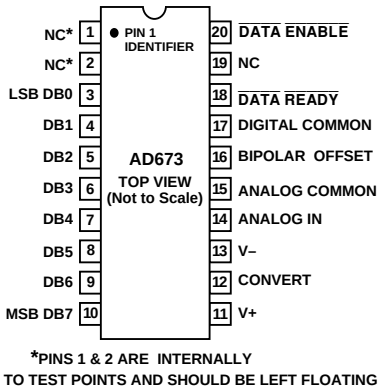
The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{DATA\ ENABLE}$ can then be activated to enable the 8-bits of data desired. $\overline{DATA\ ENABLE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less 1/2 LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 V to +10 V unipolar input range becomes a –5 V to +5 V range. The 5 kΩ thin-film input resistor is trimmed so that with a full-scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

UNIPOLAR CONNECTION

The AD673 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5 V and –12 V to –15 V), the analog input and the convert pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pinout is shown in Figure 2.

The standard unipolar 0 V to +10 V range is obtained by shorting the bipolar offset control pin (Pin 16) to digital common (Pin 17).



*PINS 1 & 2 ARE INTERNALLY CONNECTED TO TEST POINTS AND SHOULD BE LEFT FLOATING

Figure 2. AD673 Pin Connections

Full-Scale Calibration

The 5 kΩ thin-film input resistor is laser trimmed to produce a current which matches the full-scale current of the internal DAC-plus about 0.3%—when an analog input voltage of 9.961 volts (10 volts – 1 LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full-scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15 Ω resistor in series with the analog input to Pin 14. Typical full-scale calibration error will then be within ±2 LSB or ±0.8%. If more precise calibration is desired, a 200 Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 111111 10 and 11111111. Each LSB will then have a weight of 39.06 mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a weight of exactly 40.0 mV), a 100 Ω resistor and a 100 Ω trimmer (or a 200 Ω trimmer with good resolution) should be used. Of course, larger full-scale ranges can be arranged by using a larger input resistor, but linearity and full-scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5 kΩ Figure 3 illustrates the connections required for full-scale calibration.

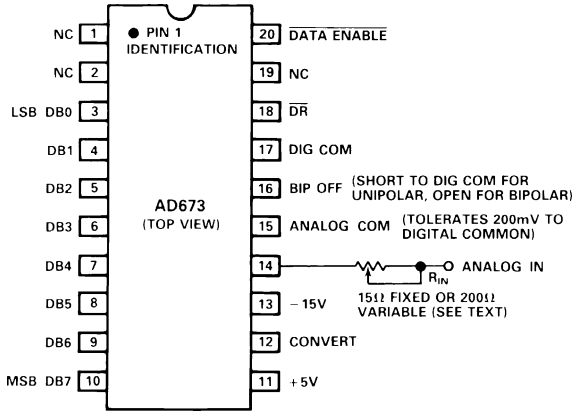


Figure 3. Standard AD673 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ±1/2 LSB for all versions of the AD673, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

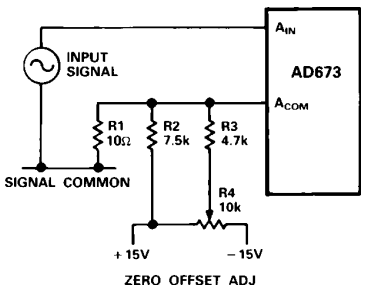


Figure 4a.

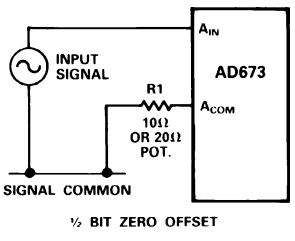


Figure 4b.

Figure 4. Unipolar Offset Trimming

Figure 4a shows how the converter zero may be offset to correct for initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

Figure 5 shows the nominal transfer curve near zero for an AD673 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

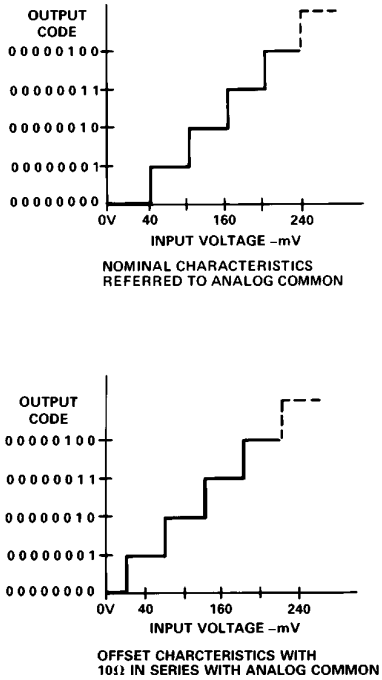


Figure 5. AD673 Transfer Curve—Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights % 39.06 mV)

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2 mA flows into the Analog Common terminal. A 10 Ω resistor in series with this terminal will result in approximately the desired l/2 bit offset of the transfer characteristics. The nominal 2 mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 20 Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full-scale transition point will also move. Thus, if an offset of 1/2 LSB is introduced, full scale trimming as described on the previous page should be done with an analog input of 9.941 volts.

NOTE: During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle appropriately during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar –5 V to +5 V range with an offset binary output code, the bipolar offset control pin is left open.

A –5.00 volt signal will give a 8-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and +4.961 volts at the input yields the 11111111 code. The nominal transfer curve is shown in Figure 6.

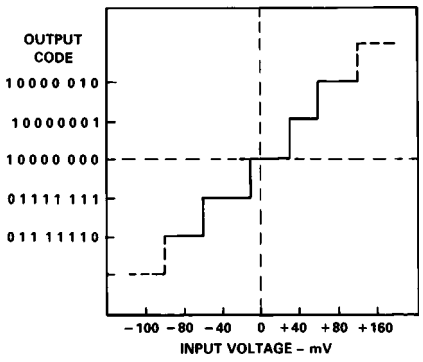


Figure 6. AD673 Transfer Curve—Bipolar Operation

Note that in the bipolar mode, the code transitions are offset 1/4 LSB such that an input voltage of 0 volts –5 mV to +35 mV yields the code representing zero (10000000). Each output code is then *centered* on its nominal input voltage.

Full-Scale Calibration

Full-Scale Calibration is accomplished in the same manner as in Unipolar operation except the full-scale input voltage is +4.61 volts.

Negative Full-Scale Calibration

The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally –5 V) which results in the 000000 00 code. R2 should be omitted to obtain a symmetrical range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 7.

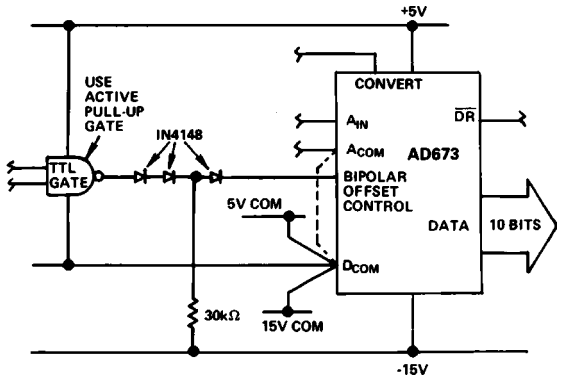


Figure 7. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0 V–10 V Input Range
Gate Output = 0 Bipolar ±5 V Input Range

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD673

Many situations in high-speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD673, a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD673 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10 μs with a droop rate less than 100 μV/ms.

$\overline{DR}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD673 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD673).

$\overline{DR}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10 μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

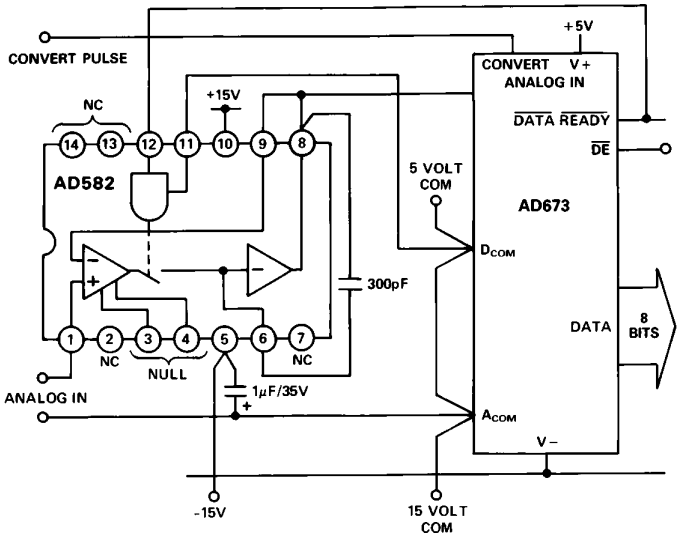


Figure 8. Sample-Hold Interface to the AD673

GROUNDING CONSIDERATIONS

The AD673 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200 mV of common-mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2 mA during a conversion. In addition a static current of about 2 mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD673

The operation of the AD673 is controlled by two inputs: CONVERT and $\overline{\text{DATA ENABLE}}$.

Starting a Conversion

The conversion cycle is initiated by a positive-going CONVERT pulse at least 500 ns wide. The rising edge of this pulse resets the internal logic, clears the result of the previous conversion, and sets $\overline{\text{DR}}$ high. The falling edge of CONVERT begins the conversion cycle. When conversion is completed $\overline{\text{DR}}$ returns low. During the conversion cycle, $\overline{\text{DE}}$ should be held high. If $\overline{\text{DE}}$ goes low during a conversion, the data output buffers will be enabled and intermediate conversion results will be present on the data output pins. This may cause bus conflicts if other devices in a system are trying to use the bus.

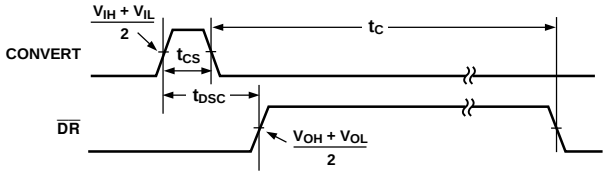


Figure 9. Convert Timing

Reading the Data

The three-state data output buffers is enabled by $\overline{\text{DE}}$. Access time of these buffers is typically 150 ns (250 maximum). The Data outputs remain valid until 50 ns after the enable signal returns high, and are completely into the high-impedance state 100 ns later.

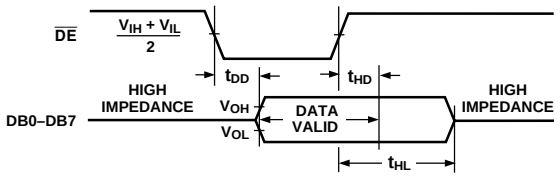


Figure 10. Read Timing

TIMING SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Units
CONVERT Pulse Width	t_{CS}	500	—	—	ns
$\overline{\text{DR}}$ Delay from CONVERT	t_{DSC}	—	1	1.5	µs
Conversion Time	t_C	10	20	30	µs
Data Access Time	t_{DD}	0	150	250	ns
Data Valid after $\overline{\text{DE}}$ High	t_{HD}	50	—	—	ns
Output Float Delay	t_{HL}	—	100	200	ns

MICROPROCESSOR INTERFACE CONSIDERATIONS—GENERAL

When an analog-to-digital converter like the AD673 is interfaced to a microprocessor, several details of the interface must be considered. First, a signal to start the converter must be generated; then an appropriate delay period must be allowed to pass before valid conversion data may be read. In most applications, the AD673 can interface to a microprocessor system with little or no external logic.

The most popular control signal configuration consists of decoding the address assigned to the AD673, then gating this signal with the system's WR signal to generate the CONVERT pulse, and gating it with RD to enable the output buffers. The use of a memory address and memory WR and RD signals denotes "memory-mapped" I/O interfacing, while the use of a separate I/O address space denotes "isolated I/O" interfacing.

Figure 11 shows a generalized diagram of the control logic for an AD673 interfaced to an 8-bit data bus, where an address ADC ADDR has been decoded. ADC ADDR starts the converter when written to (the actual data being written to the converter does not matter) and contains the high byte data during read operations.

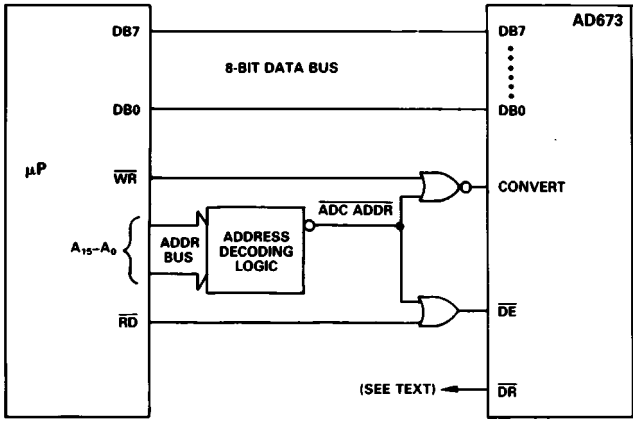


Figure 11. General AD673 Interface to 8-Bit Microprocessor

In systems where this read-write interface is used, at least 30 microseconds (the maximum conversion time) must be allowed to pass between starting a conversion and reading the results. This delay or "time-out" period can be implemented in a short software routine such as a countdown loop, enough dummy instructions to consume 30 microseconds, or enough actual useful instructions to consume the required time. In tightly-timed systems, the $\overline{DR}$ line may be read through an external three-state buffer to determine precisely when a conversion is complete. Higher-speed systems may choose to use $\overline{DR}$ to signal an interrupt to the processor at the end of a conversion.

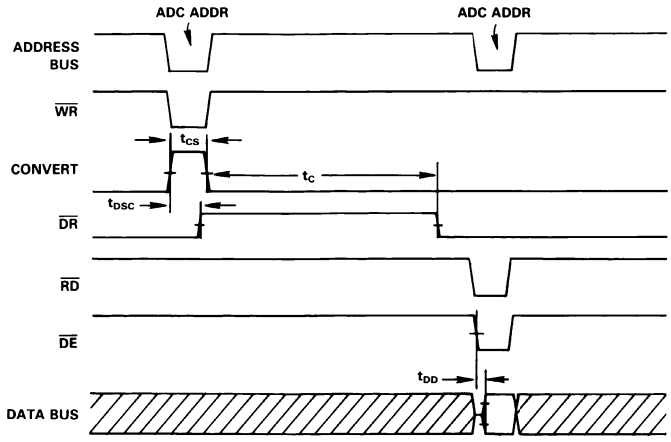


Figure 12. Typical AD673 Timing Diagram

CONVERT Pulse Generation

The AD673 is tested with a CONVERT pulse width of 500 ns and will typically operate with a pulse as short as 300 ns. However, some microprocessors produce active WR pulses which are shorter than this. Either of the circuits shown in Figure 13 can be used to generate an adequate CONVERT pulse for the AD673. In both circuits, the short low-going WR pulse sets the CONVERT line high through a flip-flop. The rising edge of $\overline{DR}$ (which signifies that the internal logic has been reset) resets the flip-flop and brings CONVERT low, which starts the conversion.

Note that t_{DSC} is slightly longer when the result of the previous conversion contains a Logic 1 on the LSB. This means that the actual CONVERT pulse generated by the circuits in Figure 13 will vary slightly in width.

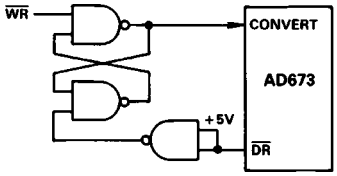


Figure 13a. Using 74LS00

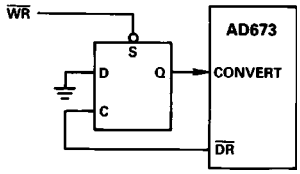
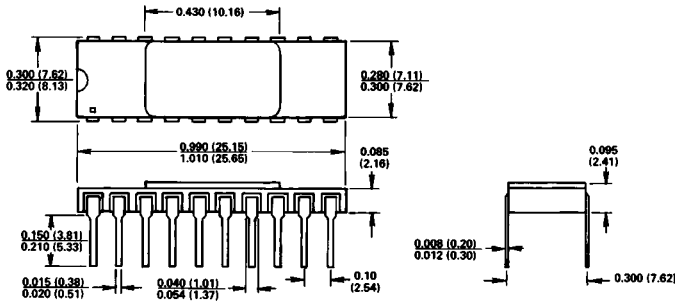


Figure 13b. Using 1/2 74LS74

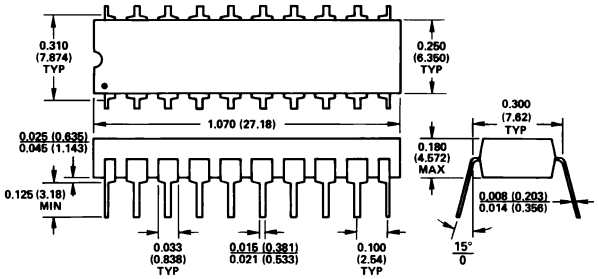
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Pin Ceramic DIP (D-20)



20-Pin Plastic DIP (N-20)



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PRINTED IN U.S.A.

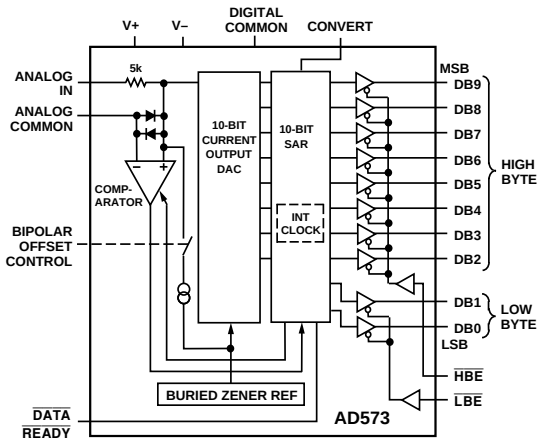
10-Bit A/D Converter

AD573*

FEATURES

Complete 10-Bit A/D Converter with Reference, Clock and Comparator
Full 8- or 16-Bit Microprocessor Bus Interface
Fast Successive Approximation Conversion—20 μs typ
No Missing Codes Over Temperature
Operates on +5 V and –12 V to –15 V Supplies
Low Cost Monolithic Construction

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD573 is a complete 10-bit successive approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and three state output buffers—all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 20 μs.

The AD573 incorporates advanced integrated circuit design and processing technologies. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin-film resistor ladder network insures high accuracy, which is maintained with a temperature compensated subsurface Zener reference.

Operating on supplies of +5 V and –12 V to –15 V, the AD573 will accept analog inputs of 0 V to +10 V or –5 V to +5 V. The trailing edge of a positive pulse on the CONVERT line initiates the 20 μs conversion cycle. DATA READY indicates completion of the conversion. HIGH BYTE ENABLE (HBE) and LOW BYTE ENABLE (LBE) control the 8-bit and 2-bit three state output buffers.

The AD573 is available in two versions for the 0°C to +70°C temperature range, the AD573J and AD573K. The AD573S guarantees ±1 LSB relative accuracy and no missing codes from –55°C to +125°C.

Three package configurations are offered. All versions are offered in a 20-pin hermetically sealed ceramic DIP. The AD573J and AD573K are also available in a 20-pin plastic DIP or 20-pin leaded chip carrier.

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690.**

PRODUCT HIGHLIGHTS

1. The AD573 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The AD573 interfaces to many popular microprocessors without external buffers or peripheral interface adapters. The 10 bits of output data can be read as a 10-bit word or as 8- and 2-bit words.
3. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD573 adapts to either unipolar (0 V to +10 V) or bipolar (–5 V to +5 V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5 V and –12 V or –15 V supplies.
6. The AD573 is available in a version compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B data sheet for detailed specifications.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD573—SPECIFICATIONS (@ T_A = +25°C, V+ = +5 V, V– = –12 V or –15 V, all voltages measured with respect to digital common, unless otherwise noted.)

Model	AD573J Min	AD573J Typ	AD573J Max	AD573K Min	AD573K Typ	AD573K Max	AD573S Min	AD573S Typ	AD573S Max	Units
RESOLUTION		10			10			10		Bits
RELATIVE ACCURACY[1]			**±1**			**±1/2**			**±1**	LSB
$T_A = T_{MIN}$ to T_{MAX}			**±1**			**±1/2**			**±1**	LSB
FULL-SCALE CALIBRATION[2]		±2			±2				**±2**	LSB
UNIPOLAR OFFSET			**±1**			**±1/2**			**±1**	LSB
BIPOLAR OFFSET			**±1**			**±1/2**			**±1**	LSB
DIFFERENTIAL NONLINEARITY[3]	**10**			**10**			**10**			Bits
$T_A = T_{MIN}$ to T_{MAX}	**9**			**10**			**10**			Bits
TEMPERATURE RANGE	0		+70	0		+70	–55		+125	°C
TEMPERATURE COEFFICIENTS[4]										
Unipolar Offset			**±2**			**±1**			**±2**	LSB
Bipolar Offset			**±2**			**±1**			**±2**	LSB
Full-Scale Calibration[2]			**±4**			**±2**			**±5**	LSB
POWER SUPPLY REJECTION										
Positive Supply										
+4.5 V ≤ V + ≤ +5.5 V			**±2**			**±1**			**±2**	LSB
Negative Supply										
–15.75 V ≤ V – ≤ –14.25 V			**±2**			**±1**			**±2**	LSB
–12.6 V ≤ V – ≤ –11.4 V			**±2**			**±1**			**±2**	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	–5		+5	–5		+5	–5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4 V max, T_{MIN} to T_{MAX})	**3.2**			**3.2**			**3.2**			mA
Output Source Current[5]										
(V_{OUT} = 2.4 V min, T_{MIN} to T_{MAX})	**0.5**			**0.5**			**0.5**			mA
Output Leakage			**±40**			**±40**			**±40**	µA
LOGIC INPUTS										
Input Current			**±100**			**±100**			**±100**	µA
Logic "1"	**2.0**			**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**			**0.8**	V
CONVERSION TIME										
$T_A = T_{MIN}$ to T_{MAX}	**10**	20	**30**	**10**	20	**30**	**10**	20	**30**	µs
POWER SUPPLY										
V+	**+4.5**	5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V–	**–11.4**	–15	**–16.5**	**+11.4**	–15	**–16.5**	**–11.4**	–15	**–16.5**	V
OPERATING CURRENT										
V+		15	**20**		15	**20**		15	**20**	mA
V–		9	**15**		9	**15**		9	**15**	mA

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full-scale calibration is guaranteed trimmable to zero with an external 50 Ω potentiometer in place of the 15 Ω fixed resistor. Full scale is defined as 10 volts minus 1 LSB, or 9.990 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]Change from +25°C value from +25°C to T_{MIN} or T_{MAX}.

[5]The data output lines have active pull-ups to source 0.5 mA. The $\overline{DATA}$ $\overline{READY}$ line is open collector with a nominal 6 kΩ internal pull-up resistor.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . 0 V to +7 V
V– to Digital Common . . . . . 0 V to –16.5 V
Analog Common to Digital Common . . . . . ±1 V
Analog Input to Analog Common . . . . . ±15 V
Control Inputs . . . . . 0 V to V+
Digital Outputs (High Impedance State) . . . . . 0 V to V+
Power Dissipation . . . . . 800 mW

ORDERING GUIDE[1]

Model	Package Option[2]	Temperature Range	Relative Accuracy
AD573JN	20-Pin Plastic DIP (N-20)	0°C to +70°C	±1 LSB max
AD573KN	20-Pin Plastic DIP (N-20)	0°C to +70°C	±1/2 LSB max
AD573JP	20-Pin Leaded Chip Carrier (P-20A)	0°C to +70°C	±1 LSB max
AD573KP	20-Pin Leaded Chip Carrier (P-20A)	0°C to +70°C	±1/2 LSB max
AD573JD	20-Pin Ceramic DIP (D-20)	0°C to +70°C	±1 LSB max
AD573KD	20-Pin Ceramic DIP (D-20)	0°C to +70°C	±1/2 LSB max
AD573 SD	20-Pin Ceramic DIP (D-20)	–55°C to +125°C	±1 LSB max

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier.

FUNCTIONAL DESCRIPTION

A block diagram of the AD573 is shown in Figure 1. The positive CONVERT pulse must be at least 500 ns wide. $\overline{DR}$ goes high within 1.5 µs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 10-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5 kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is more, the bit is turned off. After testing all bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within 1/2 LSB (0.05% of full scale).

The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{HBE}$ and $\overline{LBE}$ can then be activated to enable the upper 8-bit and lower 2-bit buffers as desired. $\overline{HBE}$ and $\overline{LBE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less 1/2 LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 V to +10 V unipolar input range becomes a –5 V to +5 V range. The 5 kΩ thin-film input resistor is trimmed so that with a full-scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

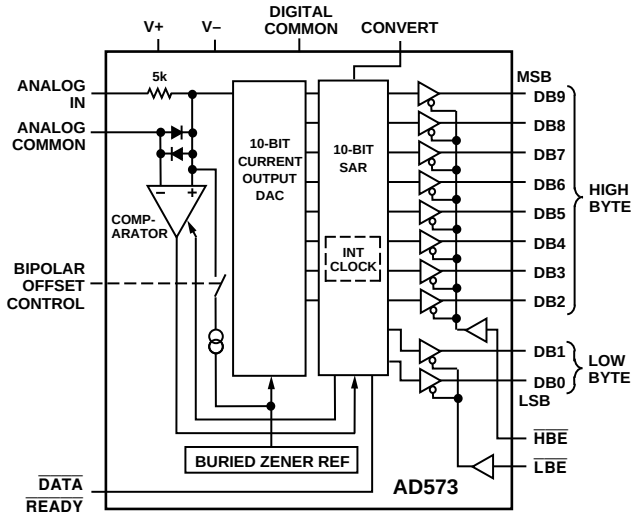


Figure 1. Functional Block Diagram

UNIPOLAR CONNECTION

The AD573 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5 V and –12 V to –15 V), the analog input and the convert pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pinout is shown in Figure 2.

The standard unipolar 0 V to +10 V range is obtained by shorting the bipolar offset control pin (Pin 16) to digital common (Pin 17).

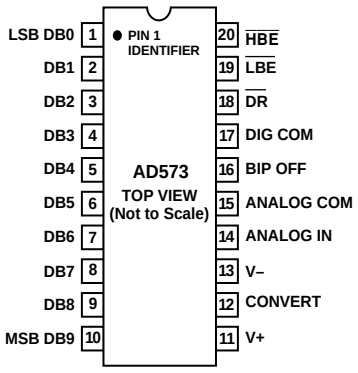


Figure 2. AD573 Pin Connections

Full-Scale Calibration

The 5 kΩ thin-film input resistor is laser trimmed to produce a current which matches the full-scale current of the internal DAC—plus about 0.3%—when an analog input voltage of 9.990 volts (10 volts – 1 LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full-scale input voltage can be trimmed down to match the DAC full-scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15 Ω resistor in series with the analog input to Pin 14. Typical full-scale calibration error will then be within ±2 LSB or ±0.2%. If more precise calibration is desired, a 50 Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 11111111 10 and 11111111 11. Each LSB will then have a weight of 9.766 mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a weight of exactly 10.00 mV), a 100 Ω resistor and a 100 Ω trimmer (or a 200 Ω trimmer with good resolution) should be used. Of course, larger full-scale ranges can be arranged by using a larger input resistor, but linearity and full-scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5 kΩ. Figure 3 illustrates the connections required for full-scale calibration.

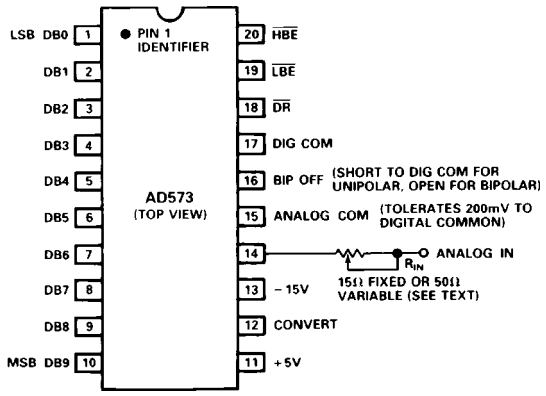


Figure 3. Standard AD573 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ±1 LSB for all versions of the AD573, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

Figure 4a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

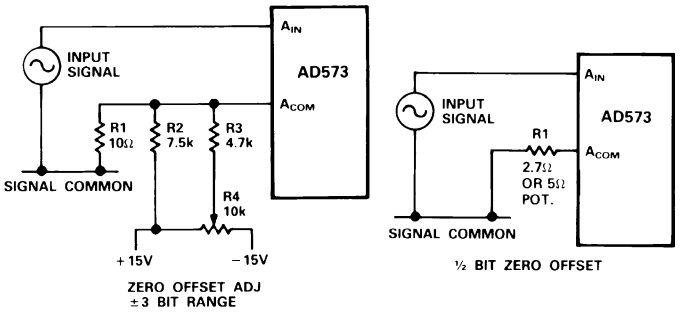


Figure 4a. *Figure 4b.*

Figure 4. Offset Trims

Figure 5 shows the nominal transfer curve near zero for an AD573 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

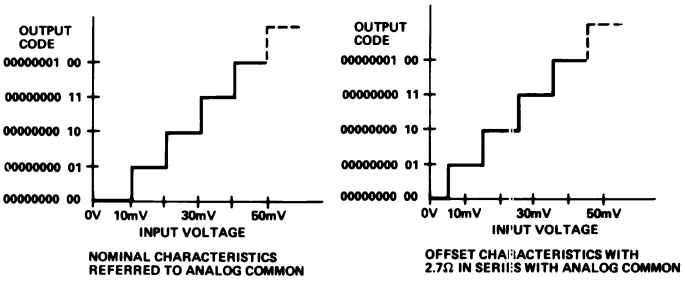


Figure 5. AD573 Transfer Curve—Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766 mV)

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2 mA flows into the Analog Common terminal. A 2.7 Ω resistor in series with this terminal will result in approximately the desired 1/2 bit offset of the transfer characteristics. The nominal 2 mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5 Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full-scale transition point will also move. Thus, if an offset of 1/2 LSB is introduced, full-scale trimming as described on the previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle appropriately during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar –5 V to +5 V range with an offset binary output code, the bipolar offset control pin is left open.

A –5.000 volt signal will give a 10-bit code of 00000000 00; an input of 0.000 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve is shown in Figure 6.

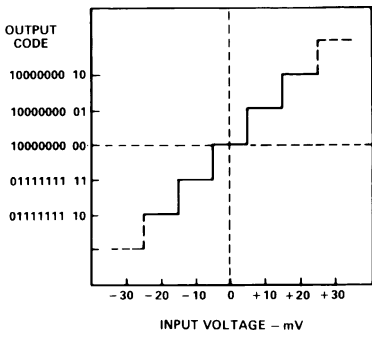


Figure 6. AD573 Transfer Curve— Bipolar Operation

Note that in the bipolar mode, the code transitions are offset 1/2 LSB such that an input voltage of 0 volts ±5 mV yields the code representing zero (10000000 00). Each output code is then *centered* on its nominal input voltage.

Full-Scale Calibration

Full-Scale Calibration is accomplished in the same manner as in unipolar operation except the full scale input voltage is +4.985 volts.

Negative Full-Scale Calibration

The circuit in Figure 4a can also be used in bipolar operation to offset the input voltage (nominally –5 V) which results in the 00000000 00 code. R2 should be omitted to obtain a symmetrical range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 7.

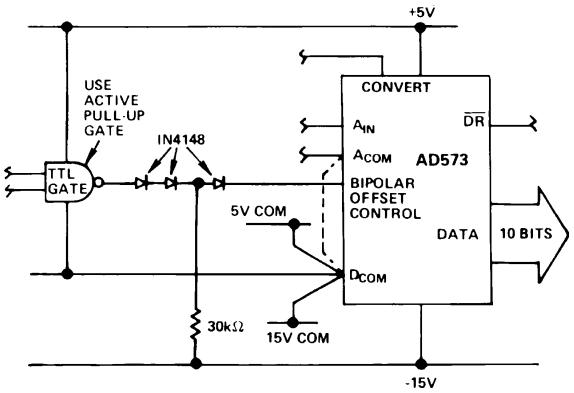


Figure 7. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0–10 V Input Range
Gate Output = 0 Bipolar ±5 V Input Range

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD573

Many situations in high speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A/D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD573, a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD573 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10 μs with a droop rate less than 100 μV/ms.

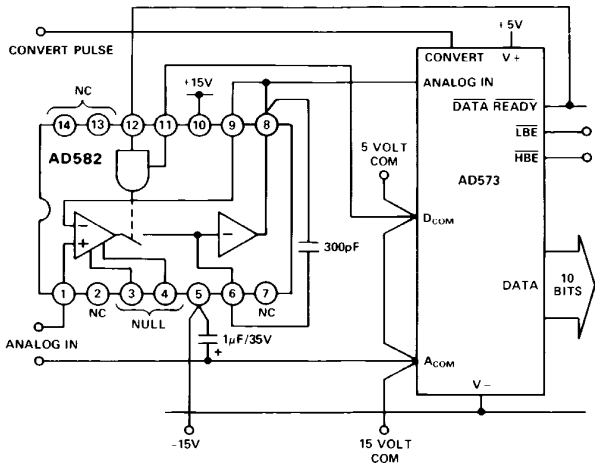


Figure 8. Sample-Hold Interface to the AD573

$\overline{DR}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD573 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD573).

$\overline{DR}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10 μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

GROUNDING CONSIDERATIONS

The AD573 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200 mV of common-mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2 mA during a conversion. In addition a static current of about 2 mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD573

The operation of the AD573 is controlled by three inputs: $\overline{\text{CONVERT}}$, $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$.

Starting a Conversion

The conversion cycle is initiated by a positive going CONVERT pulse at least 500 ns wide. The rising edge of this pulse resets the internal logic, clears the result of the previous conversion, and sets $\overline{\text{DR}}$ high. The falling edge of CONVERT begins the conversion cycle. When conversion is completed $\overline{\text{DR}}$ returns low. During the conversion cycle, $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ should be held high. If $\overline{\text{HBE}}$ or $\overline{\text{LBE}}$ goes low during a conversion, the data output buffers will be enabled and intermediate conversion results will be present on the data output pins. This may cause bus conflicts if other devices in a system are trying to use the bus.

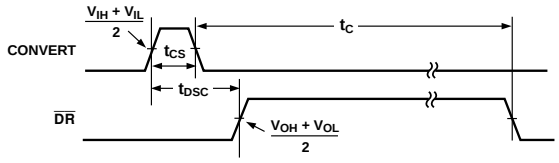


Figure 9. Convert Timing

Reading the Data

The three-state data output buffers are enabled by $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$. Access time of these buffers is typically 150 ns (250 maximum). The data outputs remain valid until 50 ns after the enable signal returns high, and are completely into the high impedance state 100 ns later.

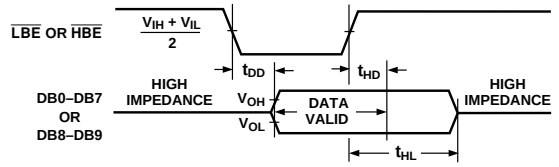


Figure 10. Read Timing

TIMING SPECIFICATIONS (All grades, $T_A = T_{MIN}$–T_{MAX})

Parameter	Symbol	Min	Typ	Max	Units
$\overline{\text{CONVERT}}$ Pulse Width	t_{CS}	500	–	–	ns
$\overline{\text{DR}}$ Delay from CONVERT	t_{DSC}	–	1	1.5	µs
Conversion Time	t_C	10	20	30	µs
Data Access Time	t_{DD}	0	150	250	ns
Data Valid after $\overline{\text{HBE}}$/$\overline{\text{LBE}}$ High	t_{HD}	50	–	–	ns
Output Float Delay	t_{HL}	–	100	200	ns

MICROPROCESSOR INTERFACE CONSIDERATIONS—GENERAL

When an analog-to-digital converter like the AD573 is interfaced to a microprocessor, several details of the interface must be considered. First, a signal to start the converter must be generated; then an appropriate delay period must be allowed to pass before valid conversion data may be read. In most applications, the AD573 can interface to a microprocessor system with little or no external logic.

The most popular control signal configuration consists of decoding the address assigned to the AD573, then gating this signal with the system's WR signal to generate the CONVERT pulse, and gating it with RD to enable the output buffers. The use of a memory address and memory WR and RD signals denotes "memory-mapped" I/O interfacing, while the use of a separate I/O address space denotes "isolated I/O" interfacing. In 8-bit bus systems, the 10-bit AD573 will occupy two locations when data is to be read; therefore, two (usually consecutive) addresses must be decoded. One of the addresses can also be used as the address which produces the CONVERT signal during WR operations.

Figure 11 shows a generalized diagram of the control logic for an AD573 interfaced to an 8-bit data bus, where two addresses (ADC ADDR and ADC ADDR + 1) have been decoded. ADC ADDR starts the converter when written to (the actual data being written to the converter does not matter) and contains the high byte data during read operations. ADC ADDR + 1 performs no function during write operations, but contains the low byte data during read operations.

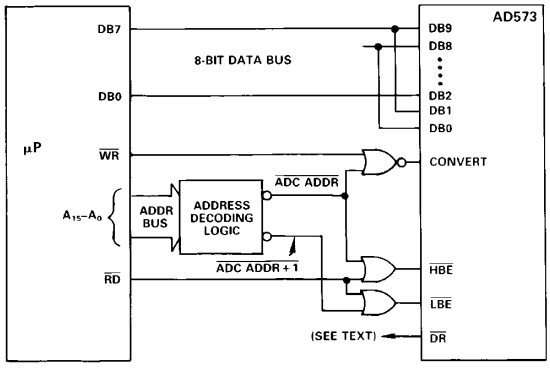


Figure 11. General AD573 Interface to 8-Bit Microprocessor

In systems where this read-write interface is used, at least 30 microseconds (the maximum conversion time) must be allowed to pass between starting a conversion and reading the results. This delay or "timeout" period can be implemented in a short software routine such as a countdown loop, enough dummy instructions to consume 30 microseconds, or enough actual useful instructions to consume the required time. In tightly-timed systems, the $\overline{\text{DR}}$ line may be read through an external three-state buffer to determine precisely when a conversion is complete. Higher speed systems may choose to use $\overline{\text{DR}}$ to signal an interrupt to the processor at the end of a conversion.

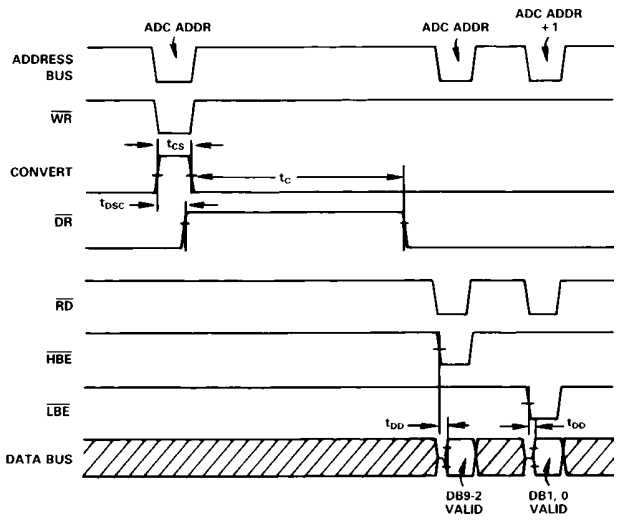


Figure 12. Typical AD573 Interface Timing Diagram

CONVERT Pulse Generation

The AD573 is tested with a CONVERT pulse width of 500 ns and will typically operate with a pulse as short as 300 ns. However, some microprocessors produce active WR pulses which are shorter than this. Either of the circuits shown in Figure 13 can be used to generate an adequate CONVERT pulse for the AD573.

In both circuits, the short low going WR pulse sets the CONVERT line high through a flip-flop. The rising edge of $\overline{DR}$ (which signifies that the internal logic has been reset) resets the flip-flop and brings CONVERT low, which starts the conversion.

Note that t_{DSC} is slightly longer when the result of the previous conversion contains a Logic 1 on the LSB. This means that the actual CONVERT pulse generated by the circuits in Figure 13 will vary slightly in width.

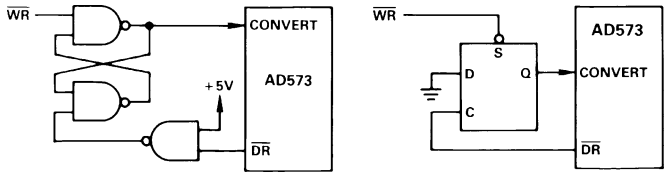


Figure 13a. Using 74LS00 *Figure 13b. Using 1/2 74LS74*

Output Data Format

The AD573 output data is presented in a left justified format. The 8 MSBs (DB9–DB2, Pins 10 through 3) are enabled by $\overline{HBE}$ (Pin 20) and the 2 LSBs (DB1, DB0—Pins 2 and 1) are enabled by $\overline{LBE}$ (Pin 19). This allows simple interface to 8-bit system buses by overlapping the 2 MSBs and the 2 LSBs. The organization of the data is shown in Figure 14.

When the least significant bits are read ($\overline{LBE}$ brought low), the six remaining bits of the byte will contain meaningless data. These unwanted bits can be masked by logically ANDing the byte with 11000000 (C0 hex), which forces the 6 lower bits to Logic 0 while preserving the two most significant bits of the byte.

Note that it is not possible to reconfigure the AD573 for right justified data.

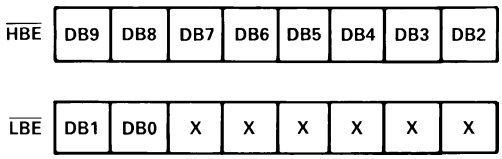


Figure 14. AD573 Output Data Format

In systems where all 10 bits are desired at the same time, $\overline{HBE}$ and $\overline{LBE}$ may be tied together. This is useful in interfacing to 16-bit bus systems. The resulting 10-bit word can then be placed at the high end of the 16-bit bus for left justification or at the low end for right justification.

It is also possible to use the AD573 in a "stand-alone" mode, where the output data buffers are automatically enabled at the end of a conversion cycle. In this mode, the $\overline{DR}$ output is wired to the $\overline{HBE}$ and $\overline{LBE}$ inputs. The outputs thus are forced into the high impedance state during the conversion period, and valid data becomes available approximately 500 ns after the $\overline{DR}$ signal goes low at the end of the conversion. The 500 ns delay allows propagation of the least significant bit through the internal logic.

This mode is particularly useful for bench-testing of the AD573, and in applications where dedicated I/O ports of peripheral interface adapter chips are available.

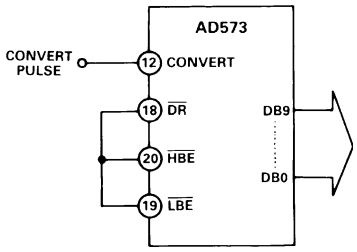


Figure 15. AD573 in "Stand-Alone" Mode (Output Data Valid 500 ns After $\overline{DR}$ Goes Low)

Apple II Microcomputer Interface

The AD573 can provide a flexible, low cost analog interface for the popular Apple II microcomputer. The Apple II, based on a 1 MHz 6502 microprocessor, meets all timing requirements for the AD573. Only a few TTL gates are required to decode the signals available on the Apple II's peripheral connector. The recommended connections are shown in Figure 16.

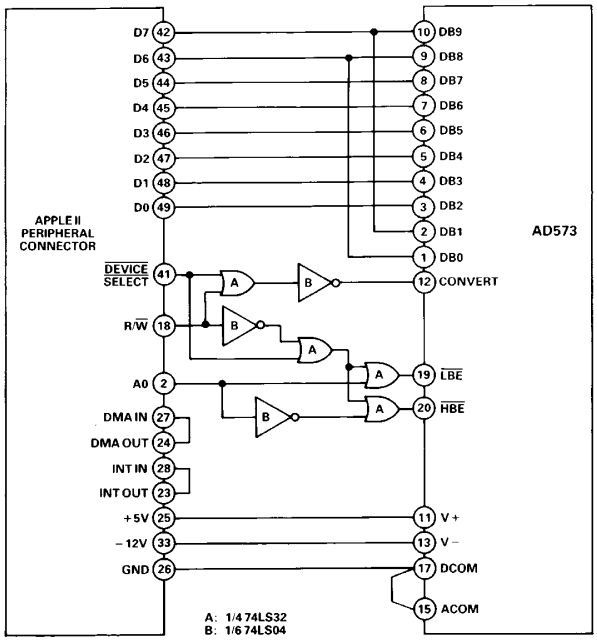


Figure 16. AD573 Interface to Apple II

The BASIC routine listed here will operate the AD573 circuit shown in Figure 16. The conversion is started by POKEing to the location which contains the AD573. The relatively slow execution speed of BASIC eliminates the need for a delay routine between starting and reading the converter. This routine assumes that the AD573 is connected for a ±5 volt input range. Variable I represents the integer value (from 0 to 1023) read from the AD573. Variable V represents the actual value of the input signal (in volts).

```
100 PRINT "WHICH SLOT IS THE A/D IN";:INPUT S
110 A=49280 + 16*S
120 POKE A,0
130 L=PEEK(A) :H=PEEK(A+1)
140 I =(4*H) + INT(L/64)
150 V=(I/1024)*10-5
160 PRINT "THE INPUT SIGNAL IS";V;"VOLTS."
```

It is also possible to write a faster-executing assembly-language routine to control the AD573. Such a routine will require a delay between starting and reading the converter. This can be easily implemented by calling the Apple's WAIT subroutine (which resides at location $FCA8) after loading the accumulator with a number greater than or equal to two.

8085-Series Microprocessor Interface

The AD573 can also be used with 8085-series microprocessors. These processors use separate control signals for RD and WR, as opposed to the single R/$\overline{W}$ control signal used in the 6800/6500 series processors.

There are two constraints related to operation of the AD573 with 8085-series processors. The first problem is the width of the CONVERT pulse. The circuit shown in Figure 17 (essentially the same as that shown in Figure 13) will produce a wide enough CONVERT pulse when the 8085 is running at 5 MHz. For 8085 systems running at slower clock rates (3 MHz), the flip-flop-based circuit can be eliminated since the $\overline{WR}$ pulse will be approximately 500 ns wide.

The other consideration is the access time of the AD573's three-state output data buffers, which is 250 ns maximum. It may be necessary to insert wait states during RD operations from the AD573. This will not be a problem in systems using memories with comparable access times, since wait states will have already been provided in the basic system design.

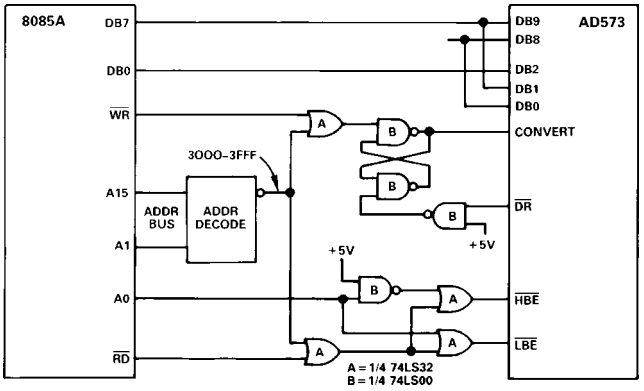


Figure 17. AD573–8085A Interface Connections

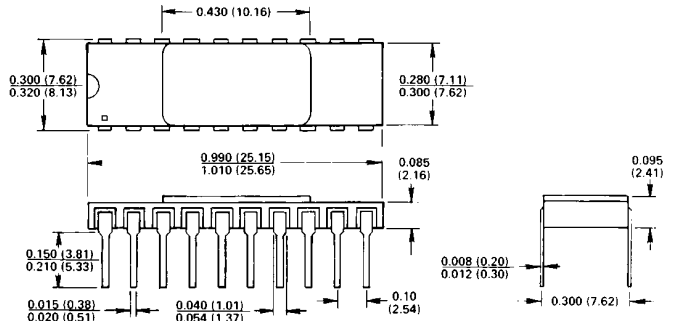
The following assembly-language subroutine can be used to control an AD573 residing at memory locations 3000_H and 3001_H. The 10 bits of data are returned (left-justified) in the DE register pair.

```
ADC:  LXI H, 3000  ; LOAD HL WITH AD573 ADDRESS
      MOV M, A     ; START CONVERSION
      MVI B, 06    ; LOAD DELAY PERIOD
LOOP: DCR B        ; DELAY LOOP
      JNZ LOOP     ;
      MOV A, M     ; READ LOW BYTE
      ANI C0       ; MASK LOWER 6 BITS
      MOV E, A     ; STORE CLEAN LOW BYTE IN E
      INR L        ; LOAD HIGH BYTE ADDRESS
      MOV D, M     ; MOVE HIGH BYTE TO D
      RET          ; EXIT
```

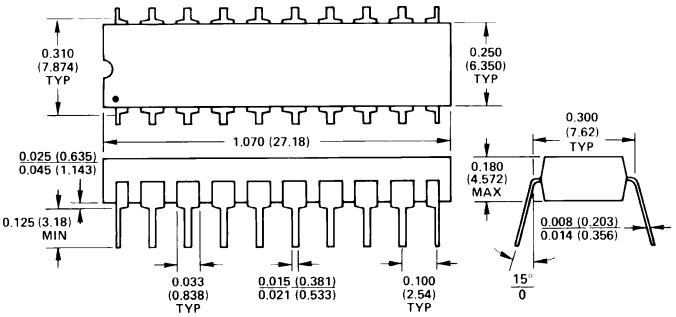
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

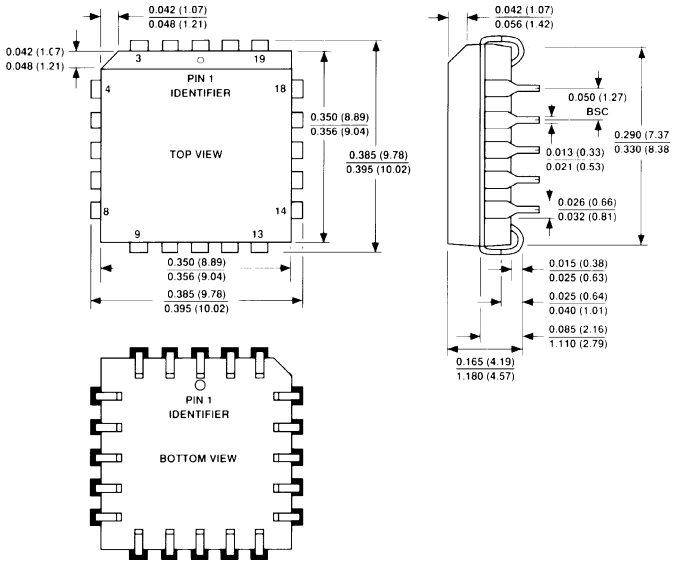
20-Pin Ceramic DIP Package ("D")



20-Pin Plastic DIP Package ("N")



P-20A PLCC



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19-0123; Rev. 4; 8/96

EVALUATION KIT AVAILABLE

Low-Power, 8-Channel, Serial 12-Bit ADCs

General Description

The MAX186/MAX188 are 12-bit data-acquisition systems that combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface together with high conversion speed and ultra-low power consumption. The devices operate with a single +5V supply or dual ±5V supplies. The analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™ and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320 family digital signal processors. The MAX186/MAX188 use either the internal clock or an external serial-interface clock to perform successive-approximation A/D conversions. The serial interface can operate beyond 4MHz when the internal clock is used.

The MAX186 has an internal 4.096V reference while the MAX188 requires an external reference. Both parts have a reference-buffer amplifier that simplifies gain trim .

The MAX186/MAX188 provide a hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes. Accessing the serial interface automatically powers up the devices, and the quick turn-on time allows the MAX186/MAX188 to be shut down between every conversion. Using this technique of powering down between conversions, supply current can be cut to under 10µA at reduced sampling rates.

The MAX186/MAX188 are available in 20-pin DIP and SO packages, and in a shrink small-outline package (SSOP), that occupies 30% less area than an 8-pin DIP. For applications that call for a parallel interface, see the MAX180/MAX181 data sheet. For anti-aliasing filters, consult the MAX274/MAX275 data sheet.

Applications

Portable Data Logging

Data-Acquisition

High-Accuracy Process Control

Automatic Testing

Robotics

Battery-Powered Instruments

Medical Instruments

SPI and QSPI are registered trademarks of Motorola.
Microwire is a registered trademark of National Semiconductor.

Features

- ♦ **8-Channel Single-Ended or 4-Channel Differential Inputs**
- ♦ **Single +5V or ±5V Operation**
- ♦ **Low Power: 1.5mA (operating mode)**
  2µA (power-down mode)
- ♦ **Internal Track/Hold, 133kHz Sampling Rate**
- ♦ **Internal 4.096V Reference (MAX186)**
- ♦ **SPI-, QSPI-, Microwire-, TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **20-Pin DIP, SO, SSOP Packages**
- ♦ **Evaluation Kit Available**

Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX186_CPP	0°C to +70°C	20 Plastic DIP
MAX186_CWP	0°C to +70°C	20 SO
MAX186_CAP	0°C to +70°C	20 SSOP
MAX186DC/D	0°C to +70°C	Dice*
MAX186_EPP	-40°C to +85°C	20 Plastic DIP
MAX186_EWP	-40°C to +85°C	20 SO
MAX186_EAP	-40°C to +85°C	20 SSOP
MAX186_MJP	-55°C to +125°C	20 CERDIP**

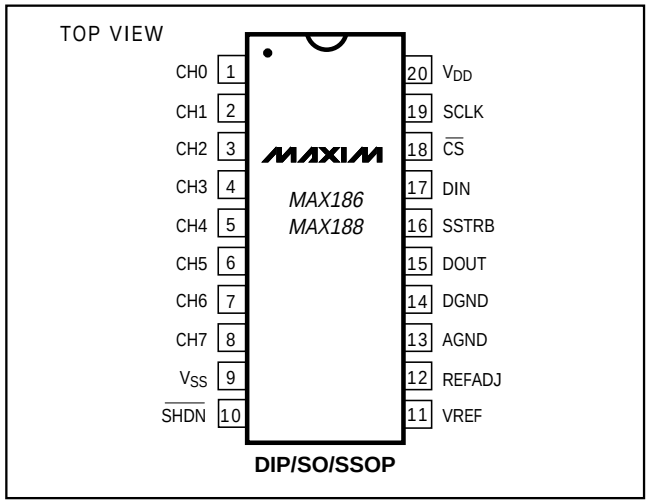
Ordering Information continued on last page.

† NOTE: Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade. Contact factory for availability of A-grade in SSOP package.

** Dice are specified at +25°C, DC parameters only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



Low-Power, 8-Channel, Serial 12-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{SS} to AGND .....+0.3V to -6V
V_{DD} to V_{SS} .....-0.3V to +12V
AGND to DGND .....-0.3V to +0.3V
CH0–CH7 to AGND, DGND .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
CH0–CH7 Total Input Current .....±20mA
VREF to AGND .....-0.3V to (V_{DD} + 0.3V)
REFADJ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX186_C/MAX188_C .....0°C to +70°C
MAX186_E/MAX188_E .....-40°C to +85°C
MAX186_M/MAX188_M .....-55°C to +125°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				12			Bits
Relative Accuracy (Note 2)		MAX186A/MAX188A				±0.5	LSB
		MAX186B/MAX188B				±0.5	
		MAX186C				±1.0	
		MAX188C				±0.75	
		MAX186D/MAX188D				±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature				±1	LSB
Offset Error		MAX186A/MAX188A				±2.0	LSB
		MAX186B/MAX188B				±3.0	
		MAX186C/MAX188C				±3.0	
		MAX186D/MAX188D				±3.0	
Gain Error (Note 3)		MAX186 (all grades)				±3.0	LSB
		External reference 4.096V (MAX188)	MAX188A			±1.5	
			MAX188B			±2.0	
			MAX188C			±2.0	
			MAX188D			±3.0	
Gain Temperature Coefficient		External reference, 4.096V			±0.8		ppm/°C
Channel-to-Channel Offset Matching					±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 4.096V_{P-P}, 133ksps, 2.0MHz external clock, bipolar input mode)							
Signal-to-Noise + Distortion Ratio	SINAD			70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD					-80	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		65kHz, V_{IN} = 4.096V_{P-P} (Note 4)			-85		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal Bandwidth		-3dB rolloff			4.5		MHz
Full-Power Bandwidth					800		kHz
CONVERSION RATE							
Conversion Time (Note 5)	t_{CONV}	Internal clock		5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion		6			
Track/Hold Acquisition Time	t_{AZ}					1.5	µs
Aperture Delay					10		ns
Aperture Jitter					<50		ps
Internal Clock Frequency					1.7		MHz
External Clock Frequency Range		External compensation, 4.7µF		0.1		2.0	MHz
		Internal compensation (Note 6)		0.1		0.4	
		Used for data transfer only			10		
ANALOG INPUT							
Input Voltage Range, Single-Ended and Differential (Note 9)		Unipolar, V_{SS} = 0V				0 to VREF	V
		Bipolar, V_{SS} = -5V				±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = ±5V			±0.01	±1	µA
Input Capacitance		(Note 6)			16		pF
INTERNAL REFERENCE (MAX186 only, reference buffer enabled)							
VREF Output Voltage		T_A = +25°C		4.076	4.096	4.116	V
VREF Short-Circuit Current						30	mA
VREF Tempco		MAX186A, MAX186B, MAX186C	MAX186_C		±30	±50	ppm/°C
			MAX186_E		±30	±60	
			MAX186_M		±30	±80	
		MAX186D			±30		
Load Regulation (Note 7)		0mA to 0.5mA output load			2.5		mV
Capacitive Bypass at VREF		Internal compensation		0			µF
		External compensation		4.7			
Capacitive Bypass at REFADJ		Internal compensation		0.01			µF
		External compensation		0.01			
REFADJ Adjustment Range					±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled, VREF = 4.096V)							
Input Voltage Range				2.50		V_{DD} + 50mV	V
Input Current					200	350	µA
Input Resistance				12	20		kΩ
Shutdown VREF Input Current					1.5	10	µA
Buffer Disable Threshold REFADJ				V_{DD} - 50mV			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain		MAX186		1.678		V/V
		MAX188		1.638		
REFADJ Input Current		MAX186			±50	µA
		MAX188			±5	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}		2.4			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{INH}	$\overline{SHDN}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{INL}	$\overline{SHDN}$ = 0V	-4.0			µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		1.5		V_{DD} -1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		2.75		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = open	-100		100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 5V (Note 6)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Negative Supply Voltage	V_{SS}			0 or -5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down		30	70	µA
		Full power-down		2	10	
Negative Supply Current	I_{SS}	Operating mode and fast power-down			50	µA
		Full power-down			10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Rejection (Note 8)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV
Negative Supply Rejection (Note 8)	PSR	V_{SS} = -5V ±5%; external reference, 4.096V; full-scale input		±0.01	±0.5	mV

Note 1: Tested at V_{DD} = 5.0V; V_{SS} = 0V; unipolar input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX186 – internal reference, offset nulled; MAX188 – external reference (VREF = +4.096V), offset nulled.
Note 4: Ground on-channel; sine wave applied to all off channels.
Note 5: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: External load should not change during conversion for specified accuracy.
Note 8: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only.
Note 9: The common-mode range for the analog inputs is from V_{SS} to V_{DD}.

TIMING CHARACTERISTICS

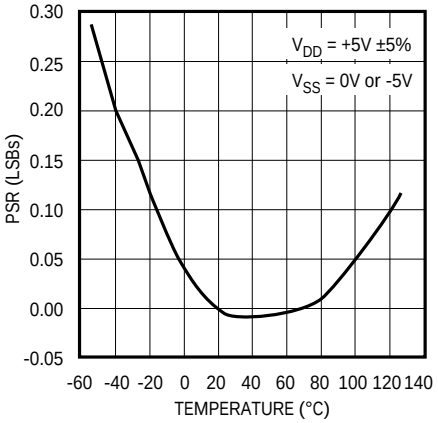
(V_{DD} = 5V ±5%; V_{SS} =0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{AZ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	MAX18_ _C/E	20		150	ns
			MAX18_ _M	20		200	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	External clock mode only, C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	External clock mode only, C_{LOAD} = 100pF				200	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Internal clock mode only		0			ns

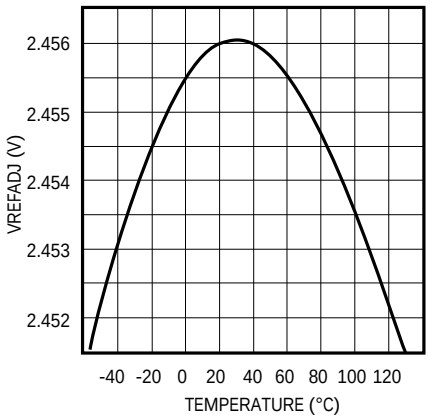
Low-Power, 8-Channel, Serial 12-Bit ADCs

Typical Operating Characteristics

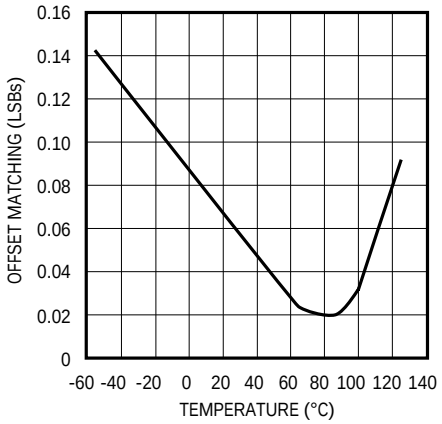
POWER-SUPPLY REJECTION vs. TEMPERATURE



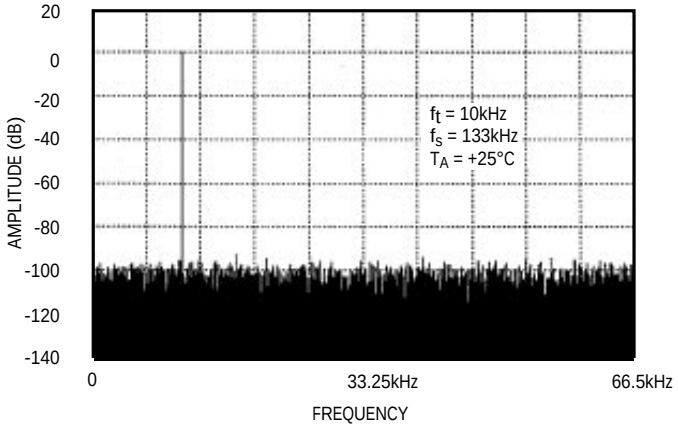
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



MAX186/MAX188 FFT PLOT – 133kHz



Pin Description

PIN	NAME	FUNCTION
1-8	CH0-CH7	Sampling Analog Inputs
9	V_{SS}	Negative Supply Voltage. Tie to -5V ±5% or AGND
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX186/MAX188 down to 10µA (max) supply current, otherwise the MAX186/MAX188 are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference Voltage for analog-to-digital conversion. Also, Output of the Reference Buffer Amplifier (4.096V in the MAX186, 1.638 x REFADJ in the MAX188). Add a 4.7µF capacitor to ground when using external compensation mode. Also functions as an input when used with a precision external reference.

Pin Description (continued)

PIN	NAME	FUNCTION
12	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
13	AGND	Analog Ground. Also IN- Input for single-ended conversions.
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX186/MAX188 begin the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60% in external clock mode.)
20	V_{DD}	Positive Supply Voltage, +5V ±5%

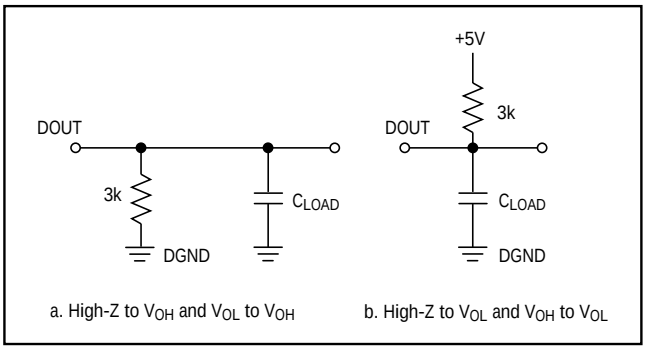


Figure 1. Load Circuits for Enable Time

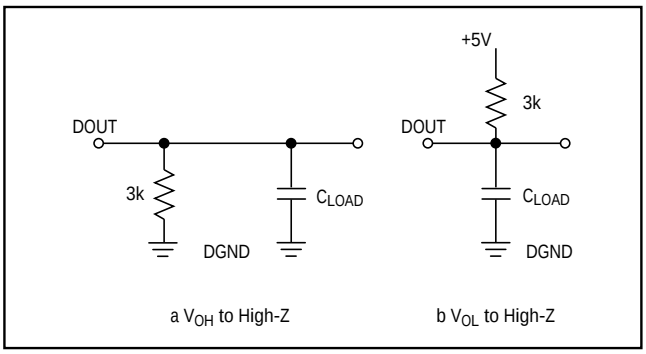


Figure 2. Load Circuits for Disabled Time

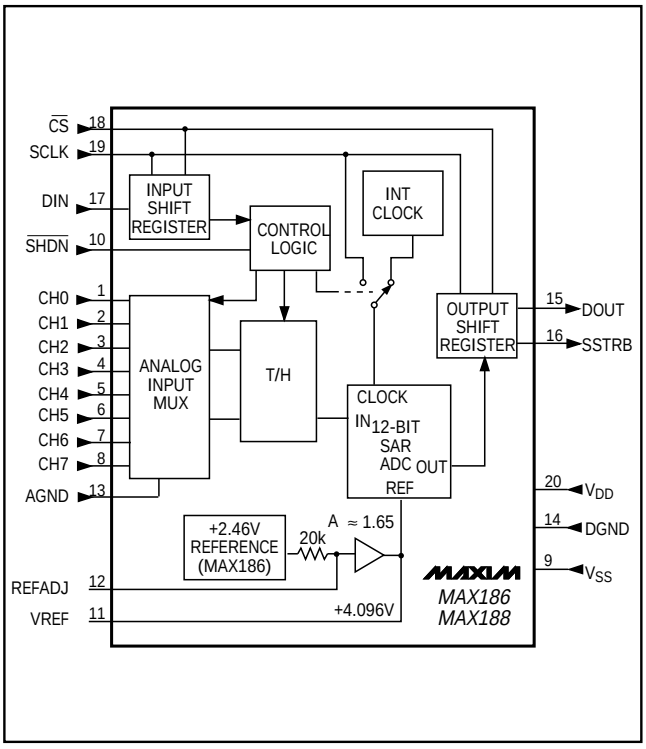


Figure 3. Block Diagram

Low-Power, 8-Channel, Serial 12-Bit ADCs

Detailed Description

The MAX186/MAX188 use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors. No external hold capacitors are required. Figure 3 shows the block diagram for the MAX186/MAX188.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0-CH7 and IN- is switched to AGND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5 and CH6/CH7. Configure the channels with Table 3 and Table 4.

In differential mode, IN- and IN+ are internally switched to either one of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. Accomplish this by connecting a 0.1µF capacitor from AIN- (the selected analog input, respectively) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply AGND. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN}+) - (V_{IN}-)]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. The T/H enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to AGND, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

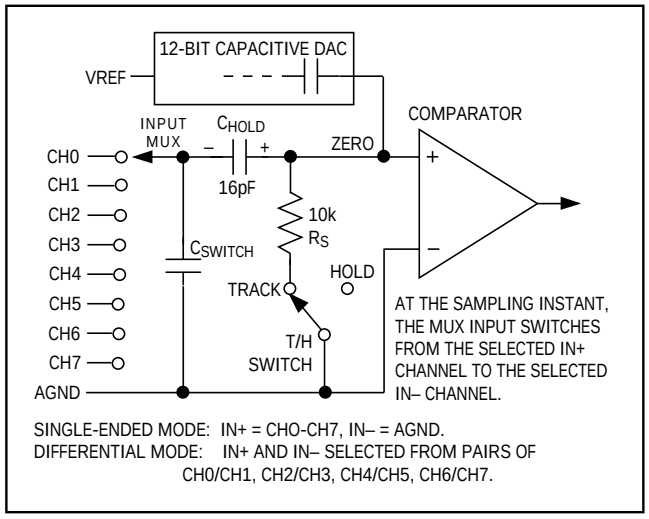


Figure 4. Equivalent Input Circuit

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{AZ} = 9 \times (R_S + R_{IN}) \times 16pF,$$

where R_{IN} = 5kΩ, R_S = the source impedance of the input signal, and t_{AZ} is never less than 1.5µs. Note that source impedances below 5kΩ do not significantly affect the AC performance of the ADC. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

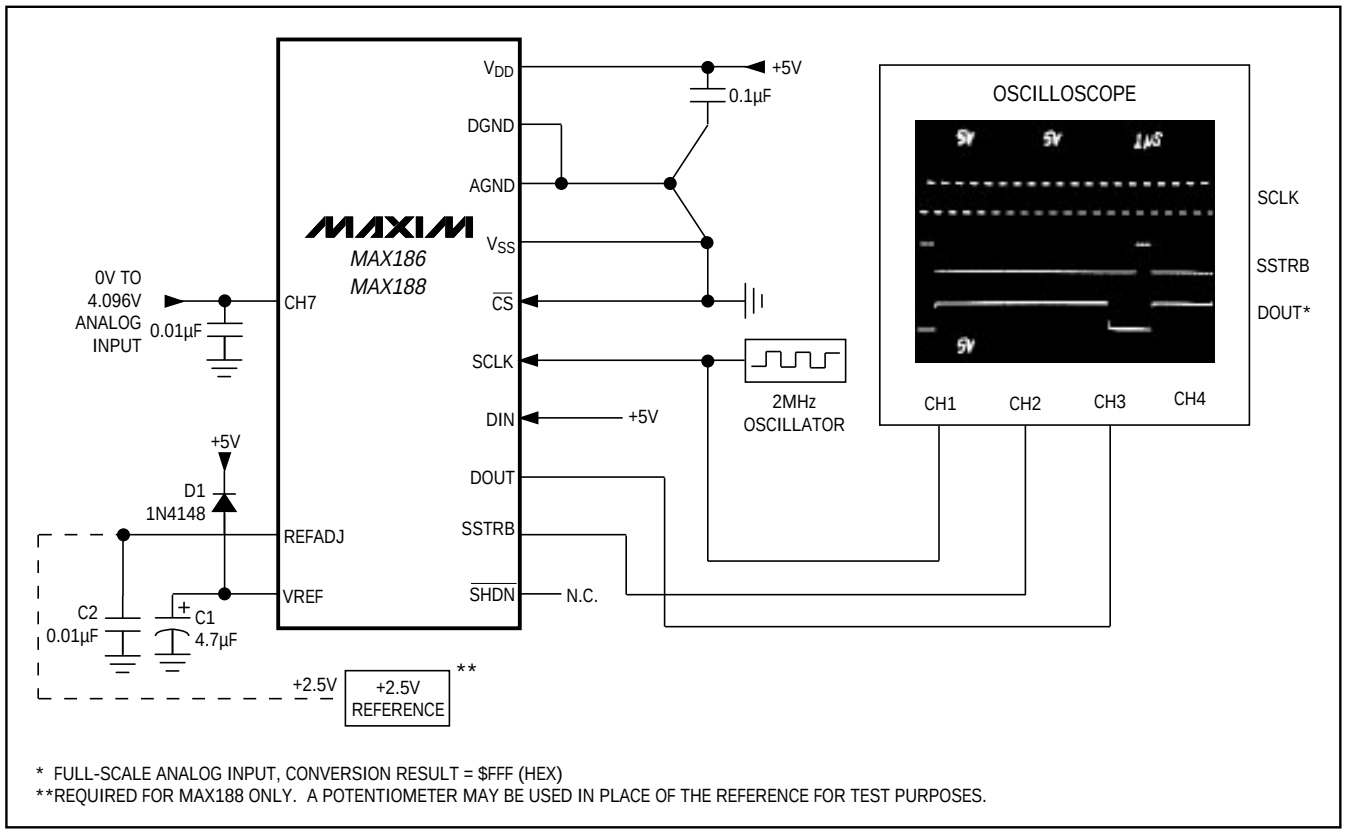


Figure 5. Quick-Look Circuit

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{SS}, allow the channel input pins to swing from V_{SS} - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than V_{SS} by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off-channels over two milliamperes, as excessive current will degrade the conversion accuracy of the on-channel.

The full-scale input voltage depends on the voltage at VREF. See Tables 1a and 1b.

Quick Look

To evaluate the analog performance of the MAX186/MAX188 quickly, use the circuit of Figure 5. The MAX186/MAX188 require a control byte to be written to DIN before each conversion. Tying DIN to +5V feeds in control bytes of $FF (HEX), which trigger

Table 1a. Unipolar Full Scale and Zero Scale

Reference	Zero Scale	Full Scale
Internal Reference (MAX186 only)	0V	+4.096V
External Reference at REFADJ	0V	V_{REFADJ} x A*
at VREF	0V	VREF

** A = 1.678 for the MAX186, 1.638 for the MAX188*

Table 1b. Bipolar Full Scale, Zero Scale, and Negative Full Scale

Reference	Negative Full Scale	Zero Scale	Full Scale
Internal Reference (MAX186 only)	-4.096V/2	0V	+4.096V/2
External Reference at REFADJ	-1/2V_{REFADJ} x A*	0V	+1/2V_{REFADJ} x A*
at VREF	-1/2 VREF	0V	+1/2 VREF

** A = 1.678 for the MAX186, 1.638 for the MAX188*

single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result comes out of DOUT. Varying the analog input to CH7 should alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started on the MAX186/MAX188 by clocking a control byte into DIN. Each rising edge on SCLK, with $\overline{CS}$ low, clocks a bit from DIN into the MAX186/MAX188's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 2 shows the control-byte format.

The MAX186/MAX188 are fully compatible with Microwire and SPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire and SPI both transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result).

Example: Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode, call it TB1. TB1 should be of the format: 1XXXXX11 Binary, where the Xs denote the particular channel and conversion-mode selected.

Table 2. Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

Bit	Name	Description
7(MSB)	START	The first logic "**1**" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion. See Tables 3 and 4.
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to AGND. In differential mode, the voltage difference between two channels is measured. See Tables 3 and 4.
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode **0** **0** Full power-down (I_Q = 2µA) **0** **1** Fast power-down (I_Q = 30µA) **1** **0** Internal clock mode **1** **1** External clock mode

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIFF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 4. Channel Selection in Differential Mode (SGL/$\overline{DIFF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ on the MAX186/MAX188 low.
3) Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB2.
5) Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB3.
6) Pull $\overline{CS}$ on the MAX186/MAX188 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of dead time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (see Figure 15). For bipolar inputs, the output is twos-complement (see Figure 16). Data is clocked out at the falling edge of SCLK in MSB-first format.

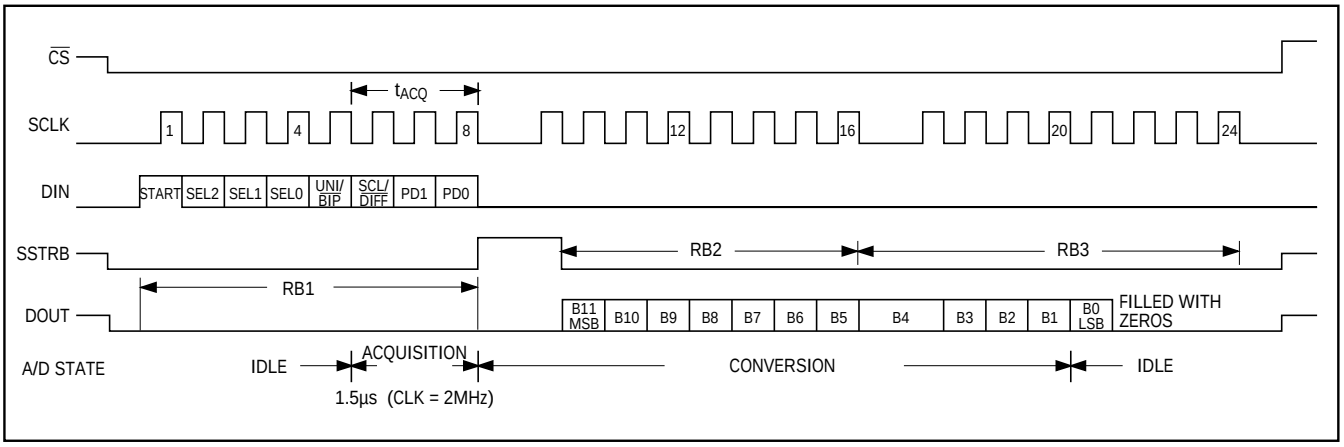


Figure 6. 24-Bit External Clock Mode Conversion Timing (SPI, QSPI and Microwire Compatible)

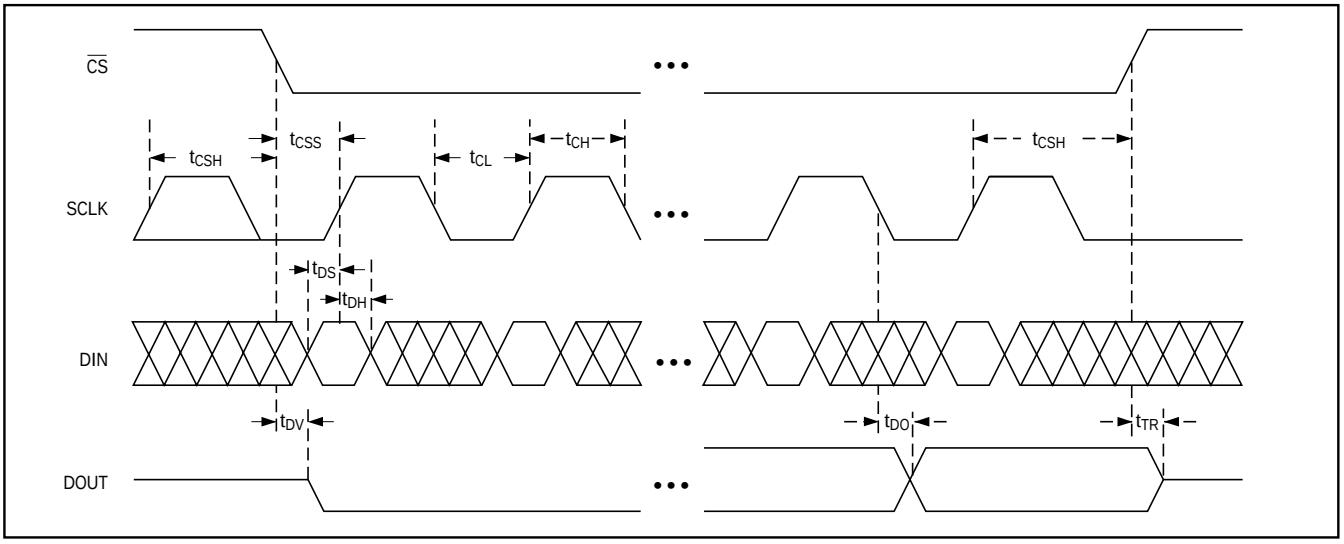


Figure 7. Detailed Serial-Interface Timing

Internal and External Clock Modes

The MAX186/MAX188 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX186/MAX188. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7 through 10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (see Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or else droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the clock period exceeds 10µs, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

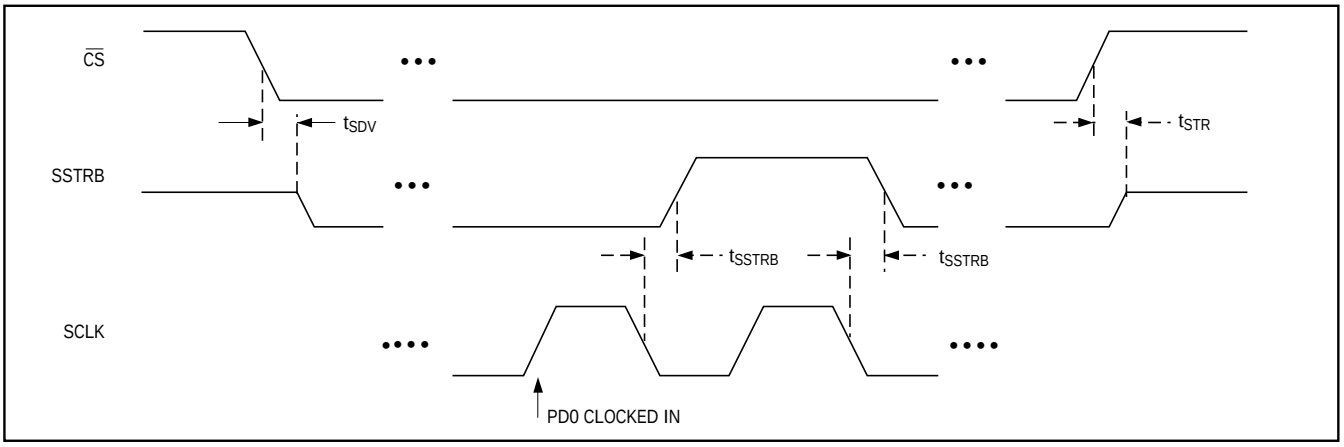


Figure 8. External Clock Mode SSTRB Detailed Timing

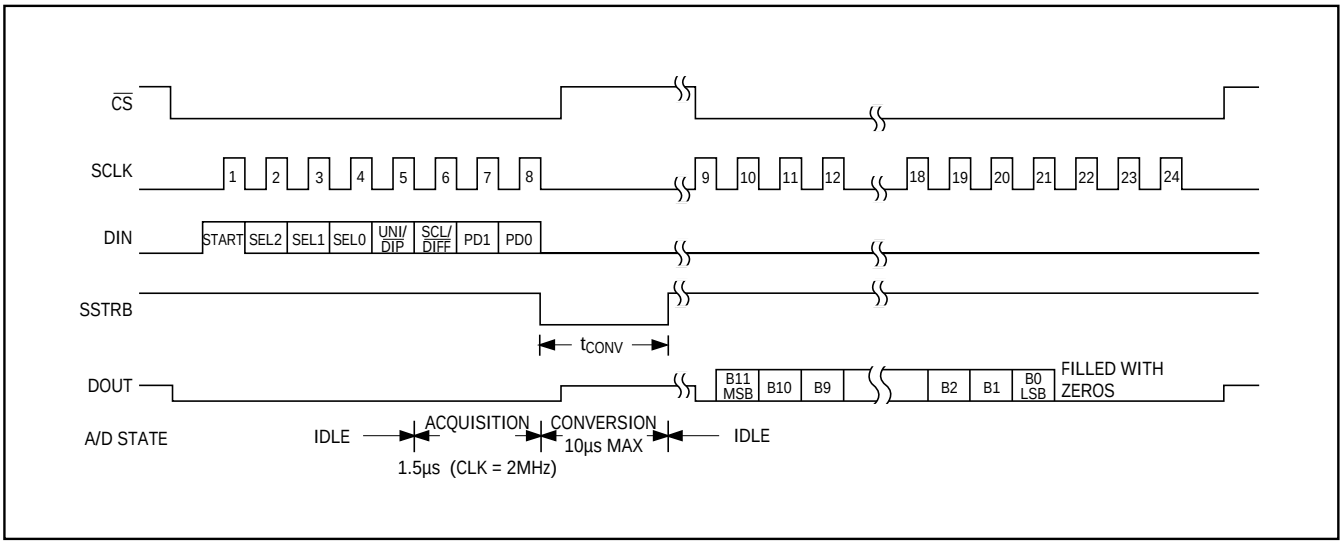


Figure 9. Internal Clock Mode Timing

Internal Clock

In internal clock mode, the MAX186/MAX188 generate their own conversion clock internally. This frees the microprocessor from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to typically 10MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (see Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX186/MAX188 and three-states DOUT, but it does not adversely effect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In internal clock mode, data can be shifted in and out of the MAX186/MAX188 at clock rates exceeding 4.0MHz, provided that the minimum acquisition time, t_{AZ}, is kept above 1.5µs.

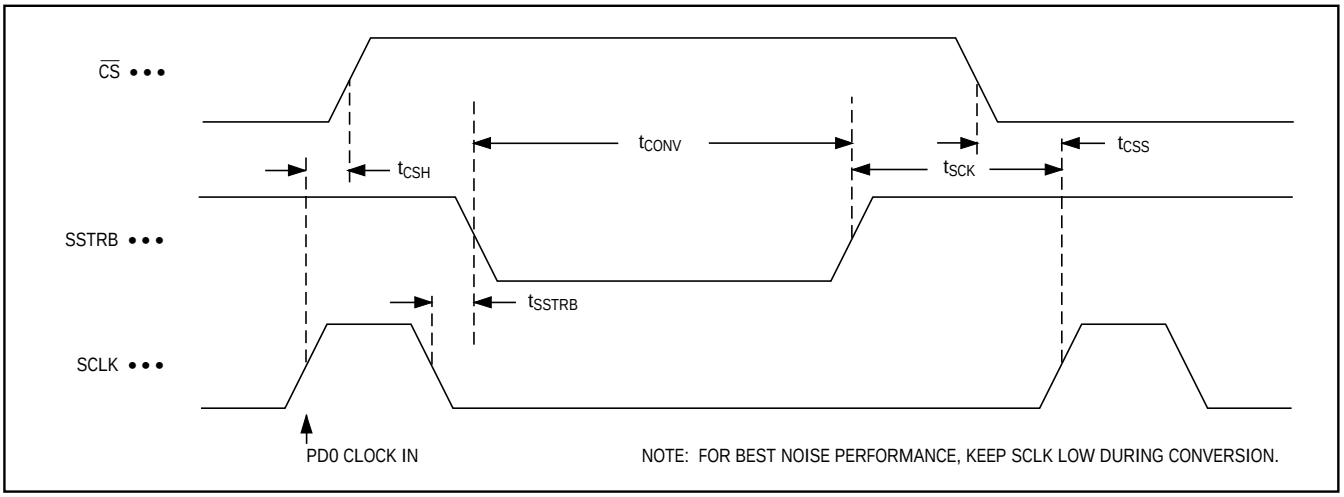


Figure 10. Internal Clock Mode SSTRB Detailed Timing

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX186/MAX188. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle, e.g. after V_{CC} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If a falling edge on $\overline{CS}$ forces a start bit before bit 5 (B5) becomes available, then the current conversion will be terminated and a new one started. Thus, the fastest the MAX186/MAX188 can run is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX186/MAX188. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX186/MAX188 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 100µs and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, the $\overline{SHDN}$ pin also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

To select external compensation, float $\overline{SHDN}$. See the *Typical Operating Circuit*, which uses a 4.7µF capacitor at VREF. A value of 4.7µF or greater ensures stability and allows operation of the converter at the full clock speed of 2MHz. External compensation increases power-up time (see the *Choosing Power-Down Mode* section, and Table 5).

Internal compensation requires no external capacitor at VREF, and is selected by pulling $\overline{SHDN}$ high. Internal compensation allows for shortest power-up times, but is only available using an external clock and reduces the maximum clock rate to 400kHz.

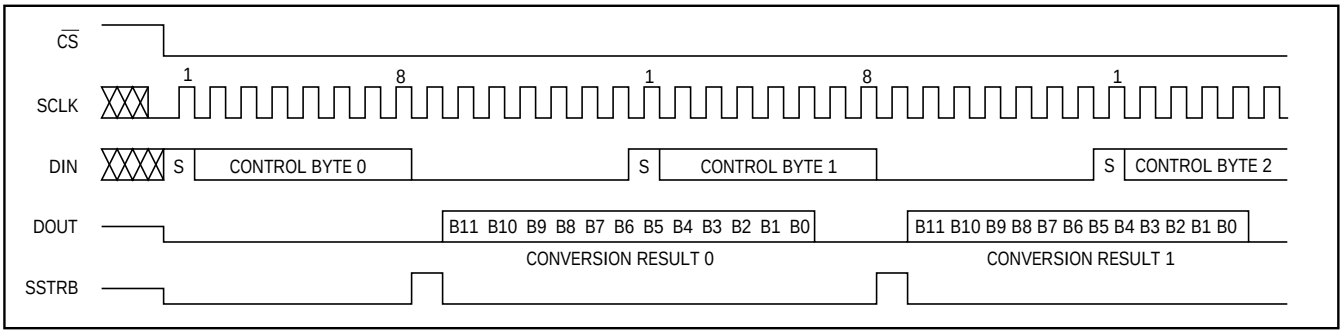


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

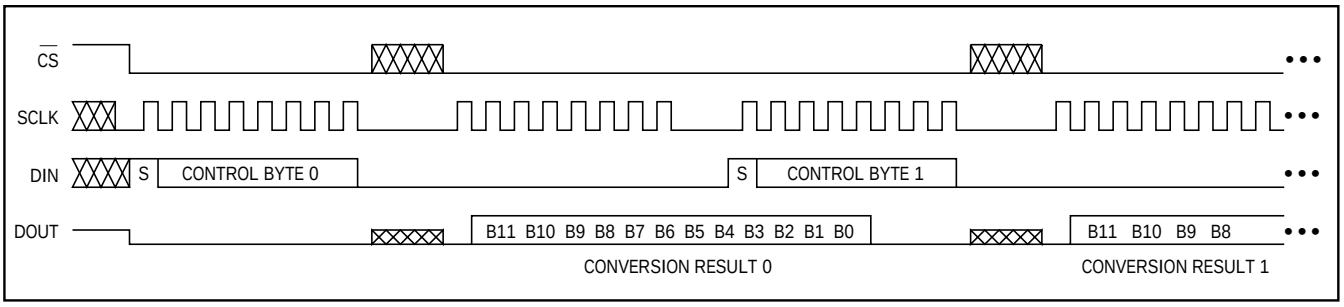


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

Power-Down

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 7 and 8 of the DIN control byte with $\overline{SHDN}$ high or floating (see Tables 2 and 6). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 7 and 8 of DIN word (see Table 7).

Full power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} and I_{SS} typically to 2µA.

Fast power-down mode turns off all circuitry except the bandgap reference. With the fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

In both software shutdown modes, the serial interface remains operational, however, the ADC will not convert. Table 5 illustrates how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate.

In external compensation mode, the power-up time is 20ms with a 4.7µF compensation capacitor (200ms with a 33µF capacitor) when the capacitor is fully discharged. In fast power-down, you can eliminate start-up time by using low-leakage capacitors that will not discharge more than 1/2LSB while shut down. In shutdown, the capacitor has to supply the current into the reference (1.5µA typ) and the transient currents at power-up.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out while the MAX186/MAX188 have already entered a software power-down.

The first logical 1 on DIN will be interpreted as a start bit, and powers up the MAX186/MAX188. Following the start bit, the data input word or control byte also determines clock and power-down modes. For example, if the DIN word contains PD1 = 1, then the chip will remain powered up. If PD1 = 0, a power-down will resume after one conversion.

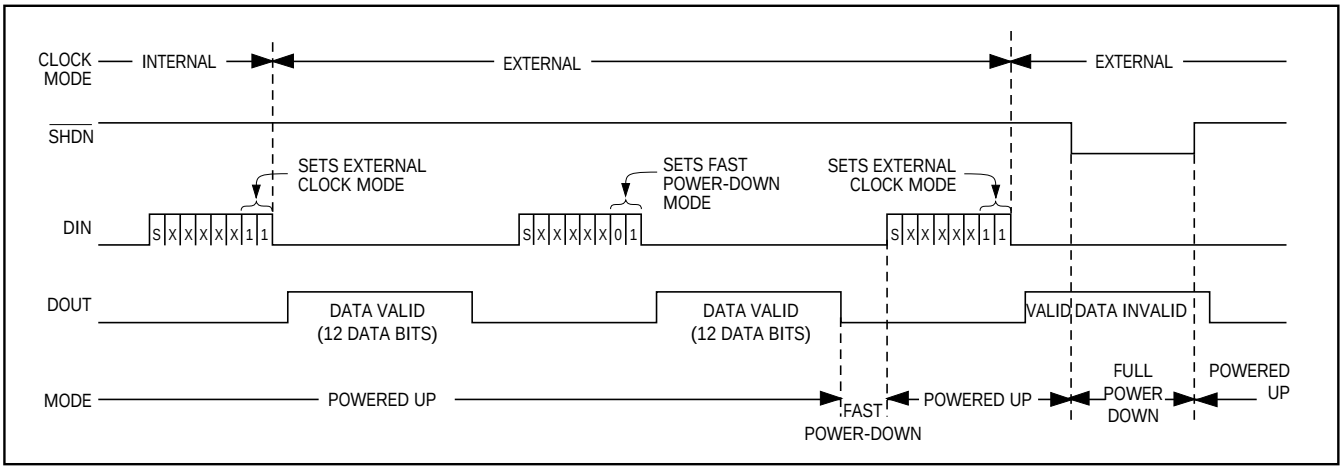


Figure 12a. Timing Diagram Power-Down Modes, External Clock

Table 5. Typical Power-Up Delay Times

Reference Buffer	Reference-Buffer Compensation Mode	VREF Capacitor (µF)	Power-Down Mode	Power-Up Delay (sec)	Maximum Sampling Rate (ksps)
Enabled	Internal		Fast	5µ	26
Enabled	Internal		Full	300µ	26
Enabled	External	4.7	Fast	See Figure 14c	133
Enabled	External	4.7	Full	See Figure 14c	133
Disabled			Fast	2µ	133
Disabled			Full	2µ	133

Table 6. Software Shutdown and Clock Mode

PD1	PD0	Device Mode
1	1	External Clock Mode
1	0	Internal Clock Mode
0	1	Fast Power-Down Mode
0	0	Full Power-Down Mode

Table 7. Hard-Wired Shutdown and Compensation Mode

$\overline{SHDN}$ State	Device Mode	Reference-Buffer Compensation
1	Enabled	Internal Compensation
Floating	Enabled	External Compensation
0	Full Power-Down	N/A

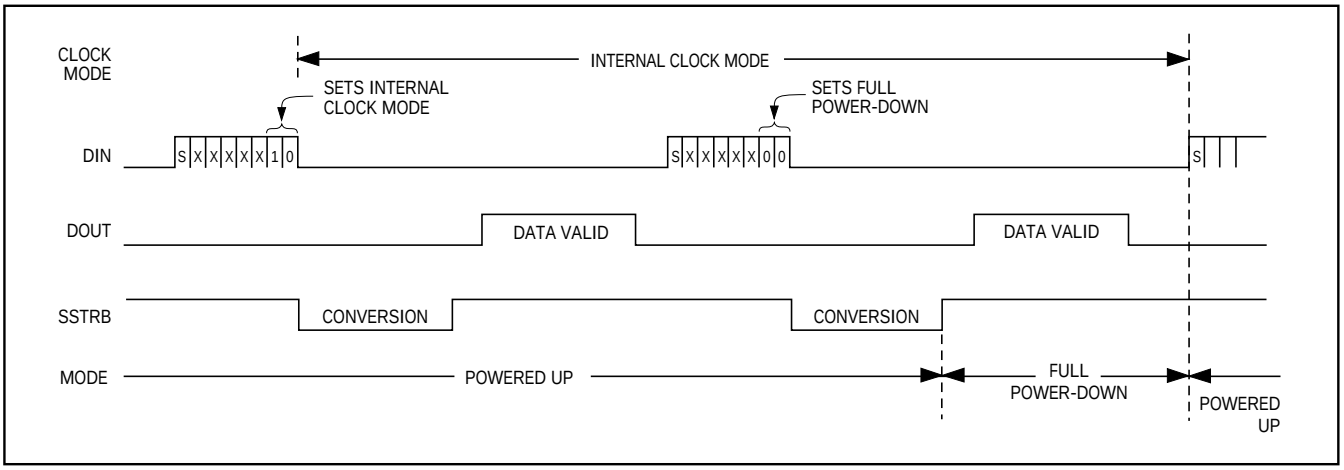


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Hardware Power-Down

The $\overline{SHDN}$ pin places the converter into the full power-down mode. Unlike with the software shut-down modes, conversion is not completed. It stops coincidentally with $\overline{SHDN}$ being brought low. There is no power-up delay if an external reference is used and is not shut down. The $\overline{SHDN}$ pin also selects internal or external reference compensation (see Table 7).

Power-Down Sequencing

The MAX186/MAX188 auto power-down modes can save considerable power when operating at less than maximum sample rates. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples illustrate two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 14a depicts the MAX186 power consumption for one or eight channel conversions utilizing full power-down mode and internal reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 12-bit accuracy, 10 time constants or 2ms are required after power-up. Waiting 2ms in FASTPD mode instead of full power-up will reduce the power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 13.

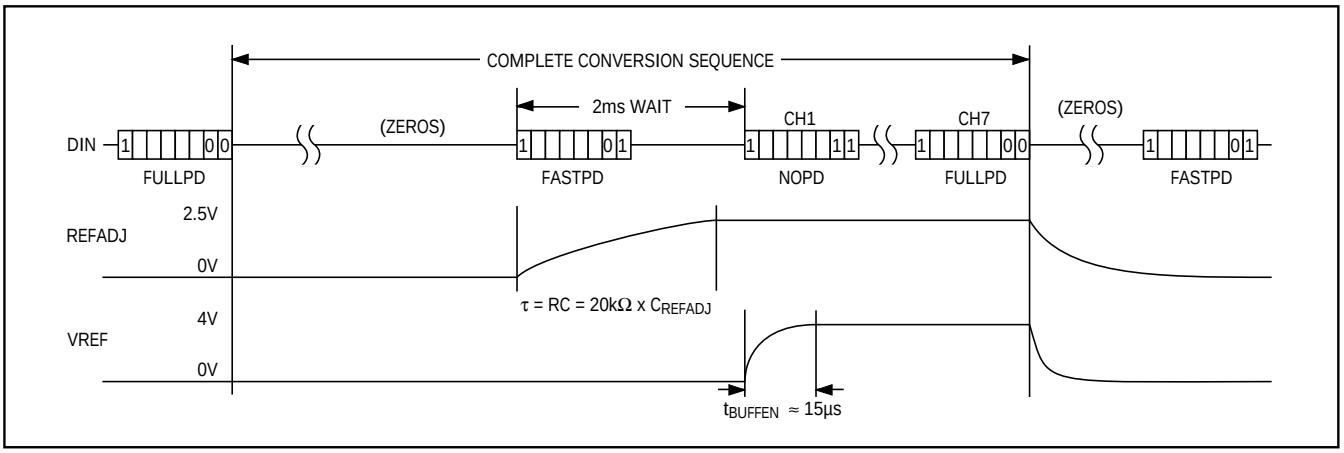


Figure 13. MAX186 FULLPD/FASTPD Power-Up Sequence

Low-Power, 8-Channel, Serial 12-Bit ADCs

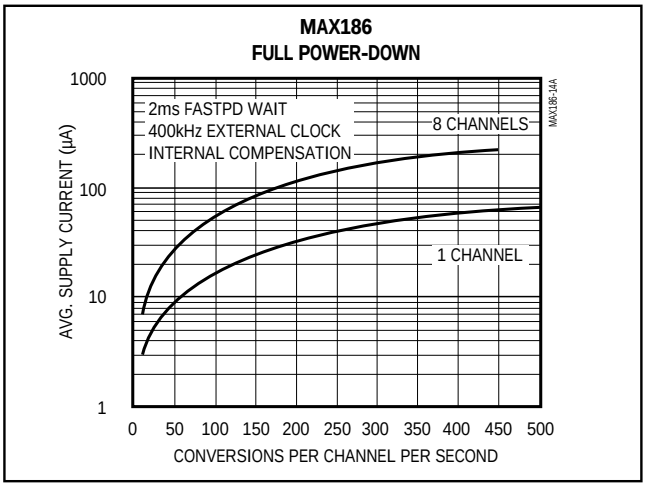


Figure 14a. MAX186 Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

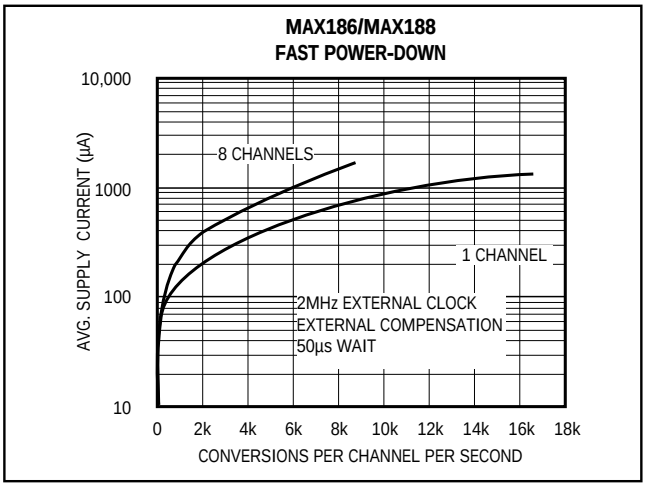


Figure 14b. MAX186/MAX188 Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

Lowest Power at Higher Throughputs

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 50µs wait after power-up, accomplished by 75 idle clocks after a dummy conversion. This circuit combines fast multi-channel conversion with lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX186/MAX188 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

External and Internal References

The MAX186 can be used with an internal or external reference, whereas an external reference is required for the MAX188. Diode D1 shown in the *Typical Operating Circuit* ensures correct start-up. Any standard signal diode can be used. For both parts, an external reference can either be connected directly at the VREF terminal or at the REFADJ pin.

An internal buffer is designed to provide 4.096V at VREF for both the MAX186 and MAX188. The MAX186's internally trimmed 2.46V reference is buffered with a gain of 1.678. The MAX188's buffer is trimmed with a buffer gain of 1.638 to scale an external 2.5V reference at REFADJ to 4.096V at VREF.

MAX186 Internal Reference

The full-scale range of the MAX186 with internal reference is 4.096V with unipolar inputs, and ±2.048V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the Reference-Adjust Circuit of Figure 17.

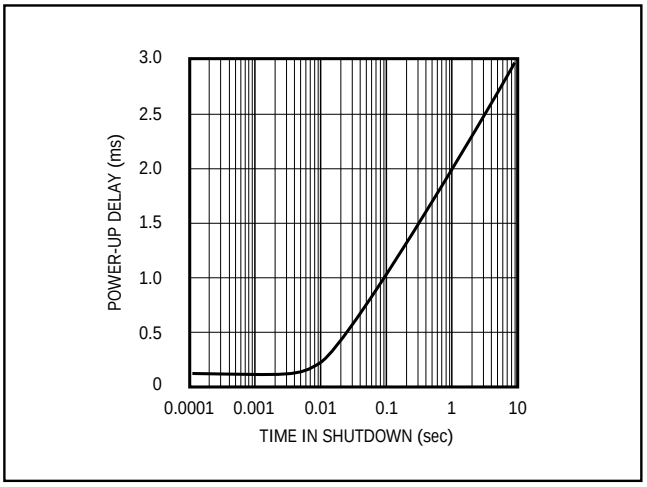


Figure 14c. Typical Power-Up Delay vs. Time in Shutdown

External Reference

With both the MAX186 and MAX188, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX186 and higher than 100kΩ for the MAX188, where the internal reference is omitted. At VREF, the input impedance is a minimum of 12kΩ for DC currents. During conversion, an external reference at VREF must be able to deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

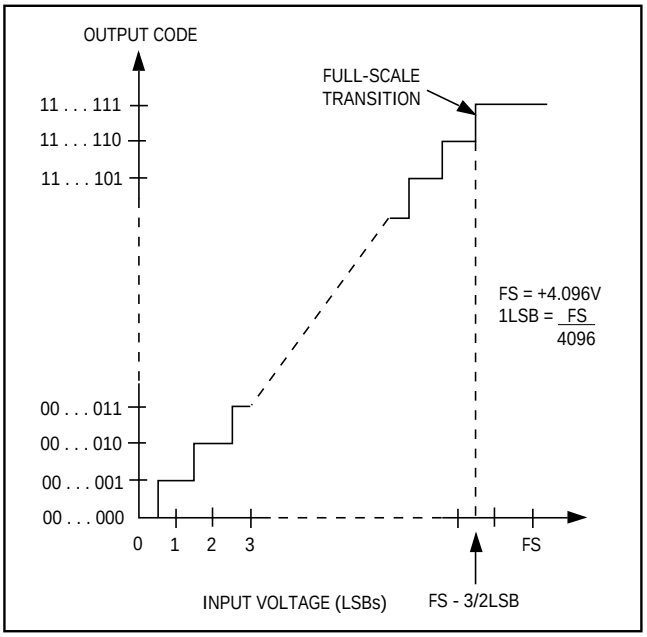


Figure 15. MAX186/MAX188 Unipolar Transfer Function, 4.096V = Full Scale

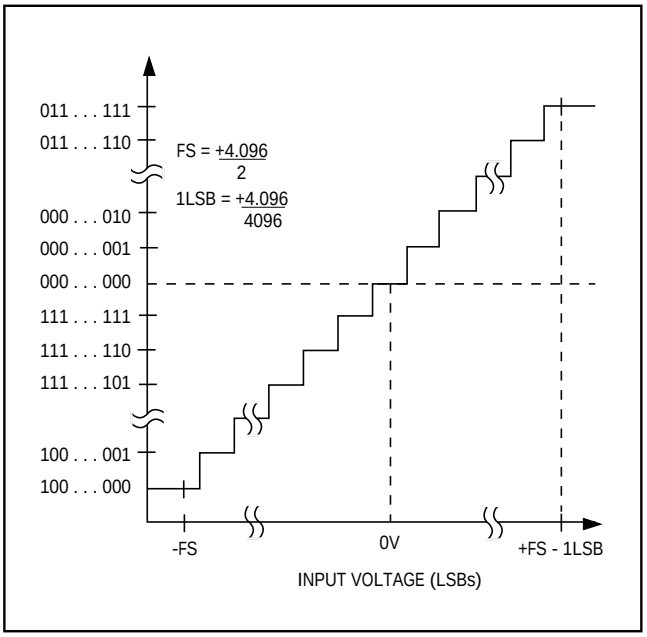


Figure 16. MAX186/MAX188 Bipolar Transfer Function, ±4.096V/2 = Full Scale

Using the buffered REFADJ input avoids external buffering of the reference. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}.

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the bipolar input/output transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary with 1 LSB = 1.00mV (4.096V/4096) for unipolar operation and 1 LSB = 1.00mV ((4.096V/2 - -4.096V/2)/4096) for bipolar operation.

Figure 17, the MAX186 Reference-Adjust Circuit, shows how to adjust the ADC gain in applications that use the internal reference. The circuit provides ±1.5% (±65LSBs) of gain adjustment range.

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. All other analog grounds

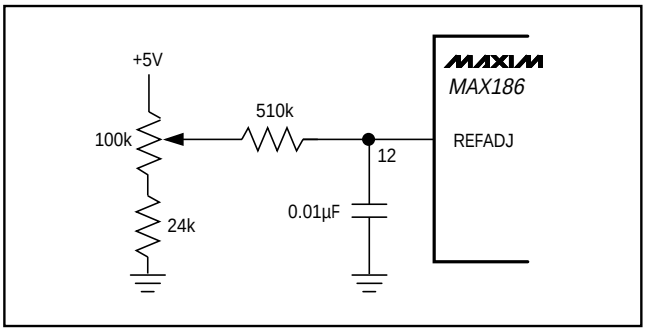


Figure 17. MAX186 Reference-Adjust Circuit

and DGND should be connected to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX186/MAX188. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a low-pass filter, as shown in Figure 18.

Low-Power, 8-Channel, Serial 12-Bit ADCs

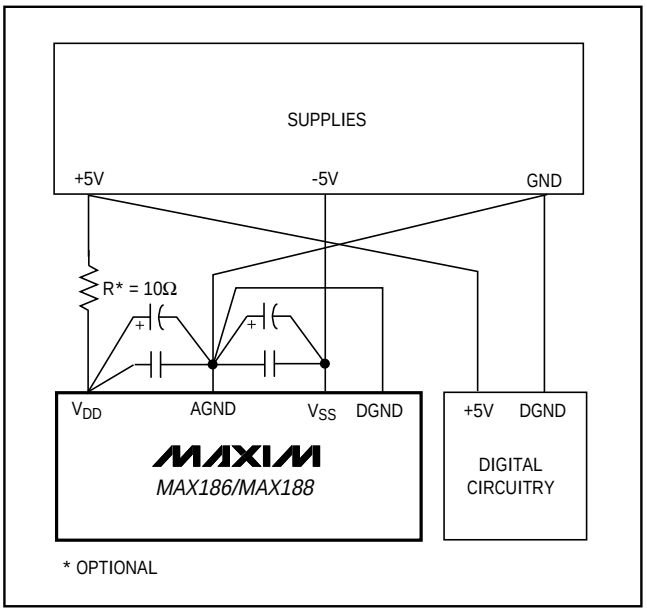


Figure 18. Power-Supply Grounding Connection

High-Speed Digital Interfacing with QSPI

The MAX186/MAX188 can interface with QSPI at high throughput rates using the circuit in Figure 19. This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU since QSPI incorporates its own micro-sequencer. Figure 19 depicts the MAX186, but the same circuit could be used with the MAX188 by adding an external reference to VREF and connecting REFADJ to V_{DD}.

Figure 20 details the code that sets up QSPI for autonomous operation. In external clock mode, the MAX186/MAX188 perform a single-ended, unipolar conversion on each of their eight analog input channels. Figure 21, QSPI Assembly-Code Timing, shows the timing associated with the assembly code of Figure 20. The first byte clocked into the MAX186/MAX188 is the control byte, which triggers the first conversion on CH0. The last two bytes clocked into the MAX186/MAX188 are all zero and clock out the results of the CH7 conversion.

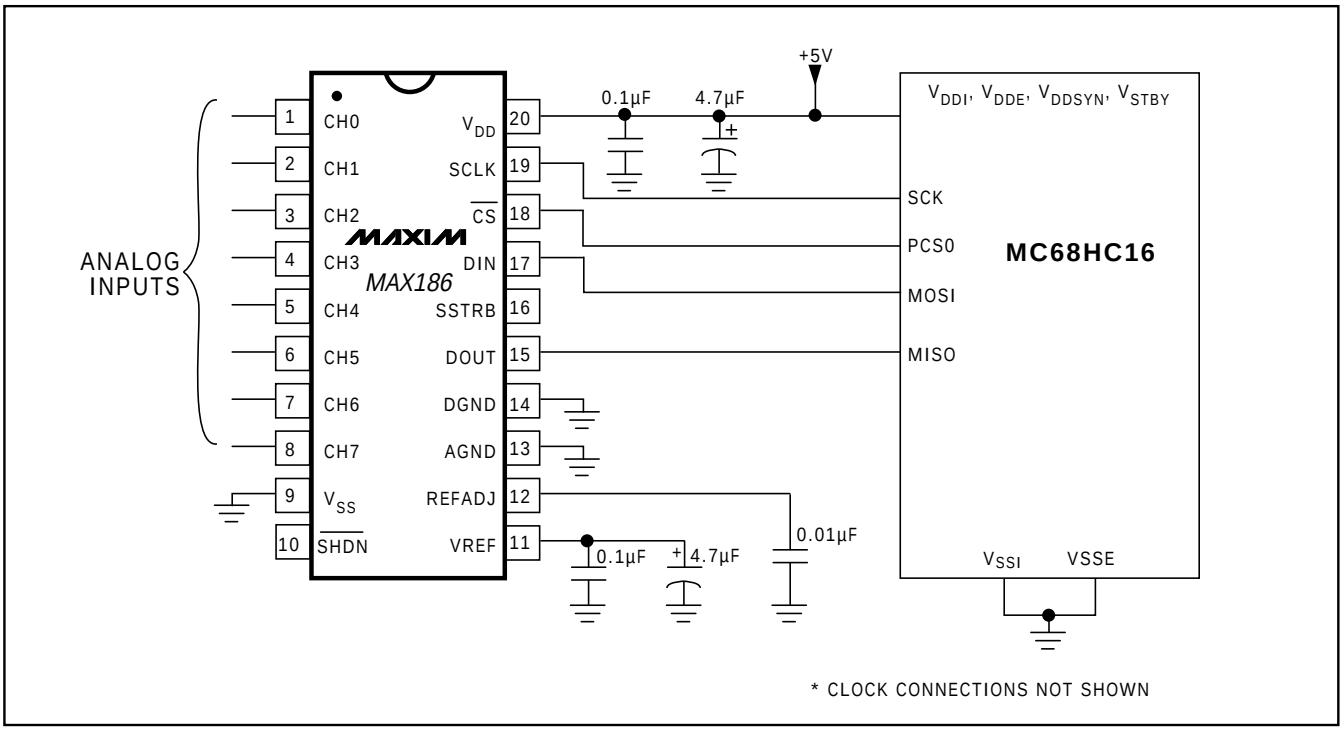


Figure 19. MAX186 QSPI Connection

```
*Title : MAX186.ASM
* Description :
*             This is a shell program for using a stand-alone 68HC16 without any external memory. The internal 1K RAM
*             is put into bank $0F to maintain 68HC11 code compatibility. This program was written with software
*             provided in the Motorola 68HC16 Evaluation Kit.
*
*  Roger J.A. Chen, Applications Engineer
*  MAXIM Integrated Products
*  November 20, 1992
*
*****************************************************************************************************************************************************************
      INCLUDE      'EQUATES.ASM'   ;Equates for common reg addrs
      INCLUDE      'ORG00000.ASM'  ;initialize reset vector
      INCLUDE      'ORG00008.ASM'  ;initialize interrupt vectors
      ORG    $0200                 ;start program after interrupt vectors
      INCLUDE  'INITSYS.ASM'       ;set EK=F,XK=0,YK=0,ZK=0
                                   ;set sys clock at 16.78 MHz, COP off
      INCLUDE  'INITRAM.ASM'       ;turn on internal SRAM at $10000
                                   ;set stack (SK=1, SP=03FE)
MAIN:
      JSR    INITQSPI
MAINLOOP:
      JSR    READ186
WAIT:
      LDAA   SPSR
      ANDA   #$80
      BEQ    WAIT                  ;wait for QSPI to finish
      BRA MAINLOOP
ENDPROGRAM:

INITQSPI:

;This routine sets up the QSPI microsequencer to operate on its own.
;The sequencer will read all eight channels of a MAX186/MAX188 each time
;it is triggered. The A/D converter results will be left in the
;receive data RAM. Each 16 bit receive data RAM location will
;have a leading zero, 12 bits of conversion result and three zeros.
;
;Receive RAM Bits 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
;A/D Result           0   MSB                                LSB 0   0   0
*****  Initialize the QSPI Registers   ******
      PSHA
      PSHB
      LDAA   #%01111000
      STAA   QPDR              ;idle state for PCS0-3 = high
      LDAA   #%01111011
      STAA   QPAR              ;assign port D to be QSPI
      LDAA   #%01111110
      STAA   QDDR              ;only MISO is an input
      LDD    #$8008
      STD    SPCR0             ;master mode,16 bits/transfer,
                               ;CPOL=CPHA=0,1MHz Ser Clock
      LDD    #$0000
      STD    SPCR1             ;set delay between PCS0 and SCK,
```

Figure 20. MAX186/MAX188 Assembly-Code Listing

```
                                ;set delay between transfers
      LDD    #$0800
      STD    SPCR2              ;set ENDQP to $8 for 9 transfers
*****  Initialize QSPI Command RAM  *****

      LDAA   #$80          ;CONT=1,BITSE=0,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD40          ;store first byte in COMMAND RAM
      LDAA   #$C0          ;CONT=1,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD41
      STAA   $FD42
      STAA   $FD43
      STAA   $FD44
      STAA   $FD45
      STAA   $FD46
      STAA   $FD47
      LDAA   #$40          ;CONT=0,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD48
*****  Initialize QSPI Transmit RAM *****

      LDD    #$008F
                                STD    $FD20
      LDD    #$00CF
                                STD    $FD22
      LDD    #$009F
                                STD    $FD24
      LDD    #$00DF
                                STD    $FD26
      LDD    #$00AF
                                STD    $FD28
      LDD    #$00EF
                                STD    $FD2A
      LDD    #$00BF
                                STD    $FD2C
      LDD    #$00FF
                                STD    $FD2E
      LDD    #$0000
                                STD    $FD30
      PULB
      PULA
      RTS

READ186:
;This routine triggers the QSPI microsequencer to autonomously
;trigger conversions on all 8 channels of the MAX186. Each
;conversion result is stored in the receive data RAM.
      PSHA
      LDAA   #$80
      ORAA   SPCR1
      STAA   SPCR1          ;just set SPE
      PULA
      RTS

*****  Interrupts/Exceptions  *****

BDM: BGND               ;exception vectors point here
```

Figure 20. MAX186/MAX188 Assembly-Code Listing (continued)

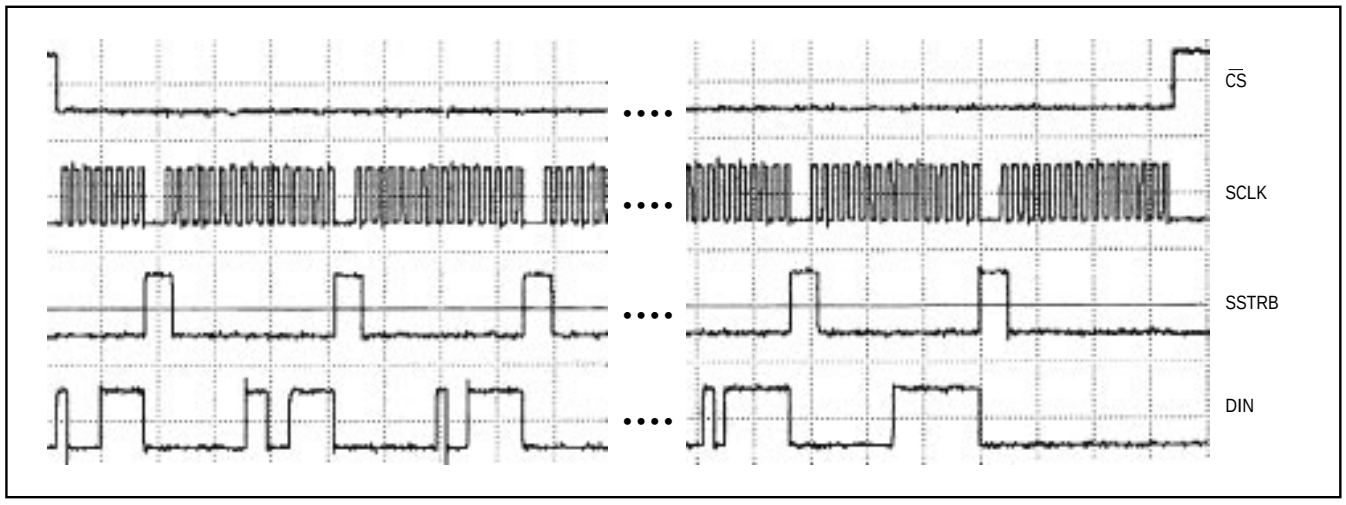


Figure 21. QSPI Assembly-Code Timing

TMS320C3x to MAX186 Interface

Figure 22 shows an application circuit to interface the MAX186/MAX188 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 23.

Use the following steps to initiate a conversion in the MAX186/MAX188 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR of the TMS320 are tied together with the SCLK input of the MAX186/MAX188.
2) The MAX186/MAX188 $\overline{CS}$ is driven low by the XF_ I/O port of the TMS320 to enable data to be clocked into DIN of the MAX186/MAX188.
3) An 8-bit word (1XXXXX11) should be written to the MAX186/MAX188 to initiate a conversion and place the device into external clock mode. Refer to Table 2 to select the proper XXXXX bit values for your specific application.
4) The SSTRB output of the MAX186/MAX188 is monitored via the FSR input of the TMS320. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX186/MAX188.

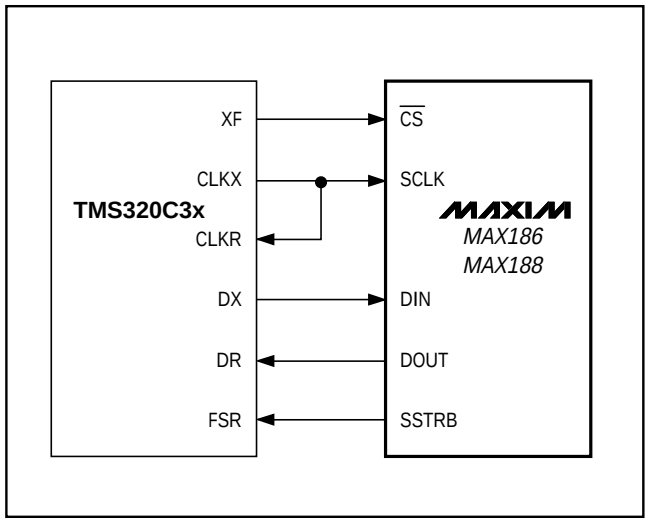


Figure 22. MAX186/MAX188 to TMS320 Serial Interface

5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX186/MAX188 until the next conversion is initiated.

Low-Power, 8-Channel, Serial 12-Bit ADCs

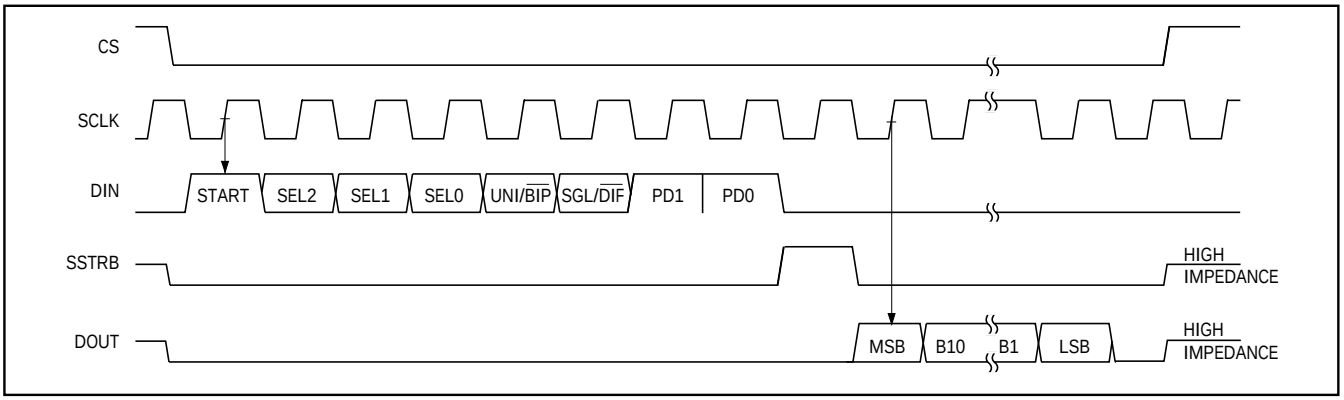
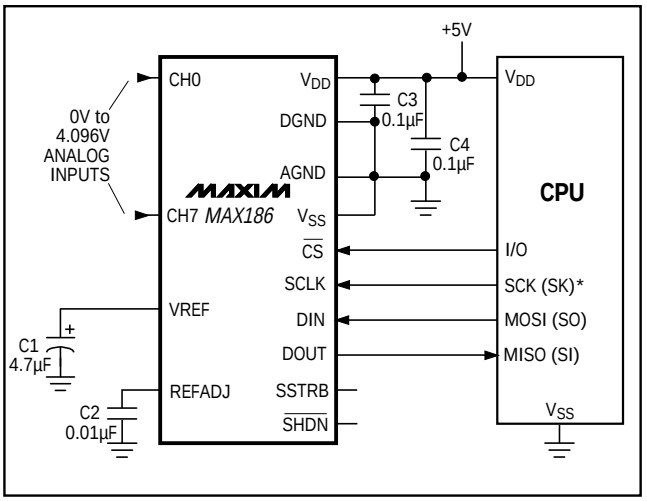
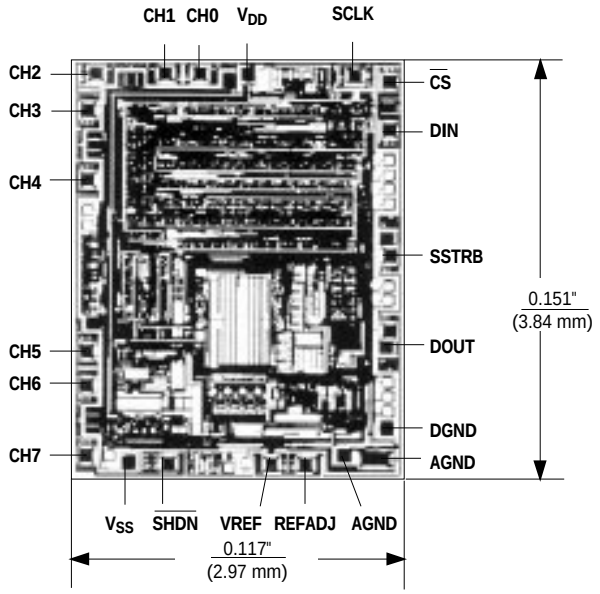


Figure 23. TMS320 Serial Interface Timing Diagram

Typical Operating Circuit



Chip Topography



MAX186/MAX188

TRANSISTOR COUNT: 2278;
SUBSTRATE CONNECTED TO V_{DD}

Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE
MAX188_CPP	0°C to +70°C	20 Plastic DIP
MAX188_CWP	0°C to +70°C	20 SO
MAX188_CAP	0°C to +70°C	20 SSOP
MAX188DC/D	0°C to +70°C	Dice*
MAX188_EPP	-40°C to +85°C	Plastic DIP
MAX188_EWP	-40°C to +85°C	20 SO
MAX188_EAP	-40°C to +85°C	20 SSOP
MAX188_MJP	-55°C to +125°C	20 CERDIP**

PART	TEMP. RANGE	BOARD TYPE
MAX186EVKIT-DIP	0°C to +70°C	Through-Hole

† NOTE: Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade.
** Dice are specified at +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

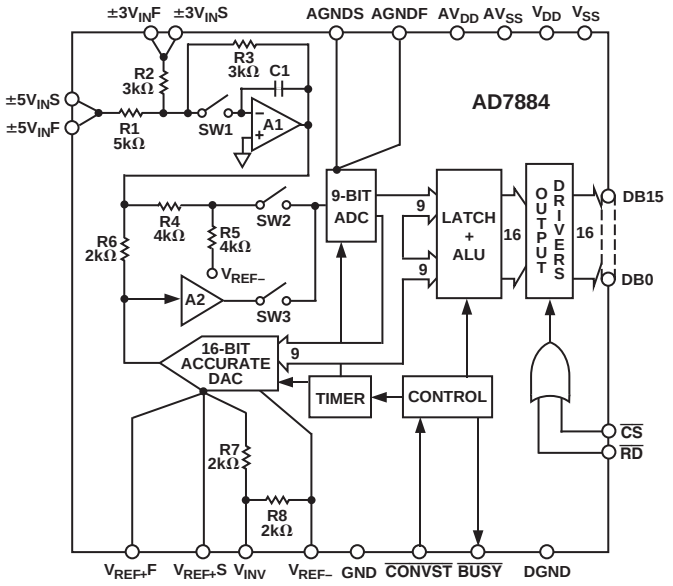
LC²MOS
16-Bit, High-Speed Sampling ADCs

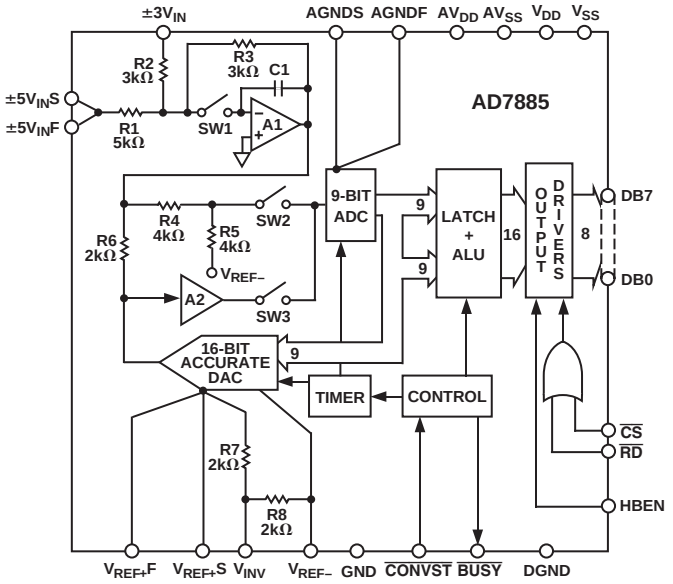
AD7884/AD7885

FEATURES
Monolithic Construction
Fast Conversion: 5.3 μs
High Throughput: 166 kSPS
Low Power: 250 mW

APPLICATIONS
Automatic Test Equipment
Medical Instrumentation
Industrial Control
Data Acquisition Systems
Robotics

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7884/AD7885 is a 16-bit monolithic analog-to-digital converter with internal sample-and-hold and a conversion time of 5.3 μs. The maximum throughput rate is 166 kSPS. It uses a two-pass flash architecture to achieve this speed. Two input ranges are available: ±5 V and ±3 V. Conversion is initiated by the $\overline{\text{CONVST}}$ signal. The result can be read into a microprocessor using the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs on the device. The AD7884 has a 16-bit parallel reading structure while the AD7885 has a byte reading structure. The conversion result is in two's complement code.

The AD7884/AD7885 has its own internal oscillator which controls conversion. It runs from ±5 V supplies and needs a V_{REF+} of 3 V.

The AD7884 is available in a 40-lead Cerdip package and in a 44-lead PLCC package.

The AD7885 is available in a 28-lead Cerdip package and the AD7885A is available in a 44-lead PLCC package.

REV. D

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Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD7884/AD7885/AD7885A–SPECIFICATIONS (V_{DD} = 5 V ± 5%, V_{SS} = –5 V ± 5%, V_{REF}+S = 3 V; AGND = DGND = GND = 0 V; f_{SAMPLE} = 166 kHz. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	J Version[1, 2, 3]	A Version[1, 2, 3]	B Versions[1, 2, 3]	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution	16	16	16	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	16	16	16	Bits	
Integral Nonlinearity			±0.0075	% FSR max	Typically 0.003% FSR
Positive Gain Error	±0.1	±0.03	±0.03	% FSR typ	AD7885AN/BN: 0.1% typ
Positive Gain Error			±0.05	% FSR max	AD7885BN: 0.2% max
Gain TC[4]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero Error	±0.05	±0.05	±0.05	% FSR typ	
Bipolar Zero Error			±0.15	% FSR max	
Bipolar Zero TC[4]	±8	±8	±8	ppm FSR/°C typ	
Negative Gain Error	±0.1	±0.03	±0.03	% FSR typ	AD7885AN/BN: 0.1% typ
Negative Gain Error			±0.05	% FSR max	AD7885BN: 0.2% max
Offset TC[4]	±2	±2	±2	ppm FSR/°C typ	
Noise	120	120	120	µV rms typ	78 µV rms typical in ±3 V Input Range
DYNAMIC PERFORMANCE					
Signal to (Noise + Distortion) Ratio	82	84	84	dB min	Input Signal: ±5 V, 1 kHz Sine Wave, Typically 86 dB
	82	82	82	dB typ	Input Signal: ±5 V, 12 kHz Sine Wave
Total Harmonic Distortion	–84	–88	–88	dB max	Input Signal: ±5 V, 1 kHz Sine Wave
	–84	–84	–84	dB typ	Input Signal: ±5 V, 12 kHz Sine Wave
Peak Harmonic or Spurious Noise	–88	–88	–88	dB max	Input Signal: ±5 V, 1 kHz Sine Wave
Intermodulation Distortion (IMD)					
Second Order Terms	–84	–84	–84	dB typ	f_A = 11.5 kHz, f_B = 12 kHz, f_{SAMPLE} = 166 kHz
Third Order Terms	–84	–84	–84	dB typ	f_A = 11.5 kHz, f_B = 12 kHz, f_{SAMPLE} = 166 kHz
CONVERSION TIME					
Conversion Time	5.3	5.3	5.3	µs max	
Acquisition Time	2.5	2.5	2.5	µs max	
Throughput Rate	166	166	166	kSPS max	There is an overlap between conversion and acquisition.
ANALOG INPUT					
Voltage Range	±5	±5	±5	Volts	
	±3	±3	±3	Volts	
Input Current	±4	±4	±4	mA max	
REFERENCE INPUT					
Reference Input Current	±5	±5	±5	mA max	V_{REF+}S = 3 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	Input Level = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB15–DB0					
Floating-State Leakage Current	10	10	10	µA max	
Floating-State Output Capacitance[4]	15	15	15	pF max	
POWER REQUIREMENTS					
V_{DD}	5	5	5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	35	35	35	mA max	Typically 25 mA
I_{SS}	30	30	30	mA max	Typically 25 mA
Power Supply Rejection Ratio					
$\Delta Gain/\Delta V_{DD}$	86	86	86	dB typ	
$\Delta Gain/\Delta V_{SS}$	86	86	86	dB typ	
Power Dissipation	325	325	325	mW max	Typically 250 mW

NOTES

[1]Temperature ranges are as follows: J, A, B Versions: –40°C to +85°C.

[2]V_{IN} = ±5 V.

[3]The AD7885AAP has the same specs as the AD7884AP. The AD7885ABP has the same specs as the AD7884BP.

[4]Sample tested to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = GND = 0 V. See Figures 2, 3, 4, and 5.)

Parameter	Limit at 25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (A, B, and J Versions)	Unit	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulsewidth
t_2	100	100	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Low Delay
t_3	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_4	60	60	ns min	$\overline{RD}$ Pulsewidth
t_5	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	57	57	ns max	Data Access Time After $\overline{RD}$
t_7[3]	5	5	ns min	Bus Relinquish Time After $\overline{RD}$
	50	50	ns max	
t_8	40	40	ns min	New Data Valid before Rising Edge of $\overline{BUSY}$
t_9	10	80	ns min	HBEN to $\overline{RD}$ Setup Time
t_{10}	25	25	ns min	HBEN to $\overline{RD}$ Hold Time
t_{11}	60	60	ns min	HBEN Low Pulse Duration
t_{12}	60	60	ns min	HBEN High Pulse Duration
t_{13}	55	70	ns max	Propagation Delay from HBEN Falling to Data Valid
t_{14}	55	70	ns max	Propagation Delay from HBEN Rising to Data Valid

NOTES

[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_7, quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

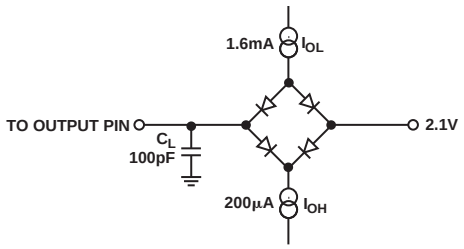


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

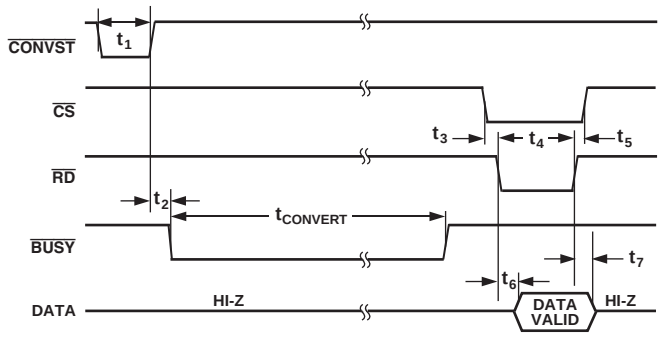


Figure 2. AD7884 Timing Diagram, Using $\overline{CS}$ and $\overline{RD}$

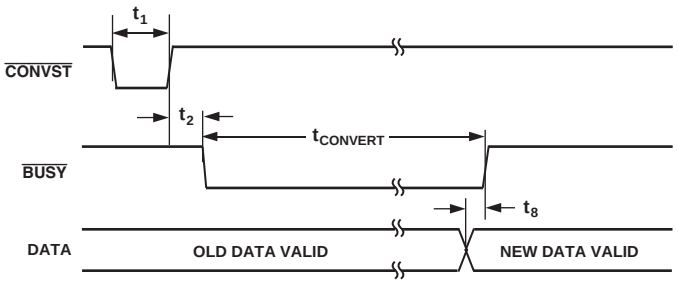


Figure 3. AD7884 Timing Diagram, with $\overline{CS}$ and $\overline{RD}$ Permanently Low

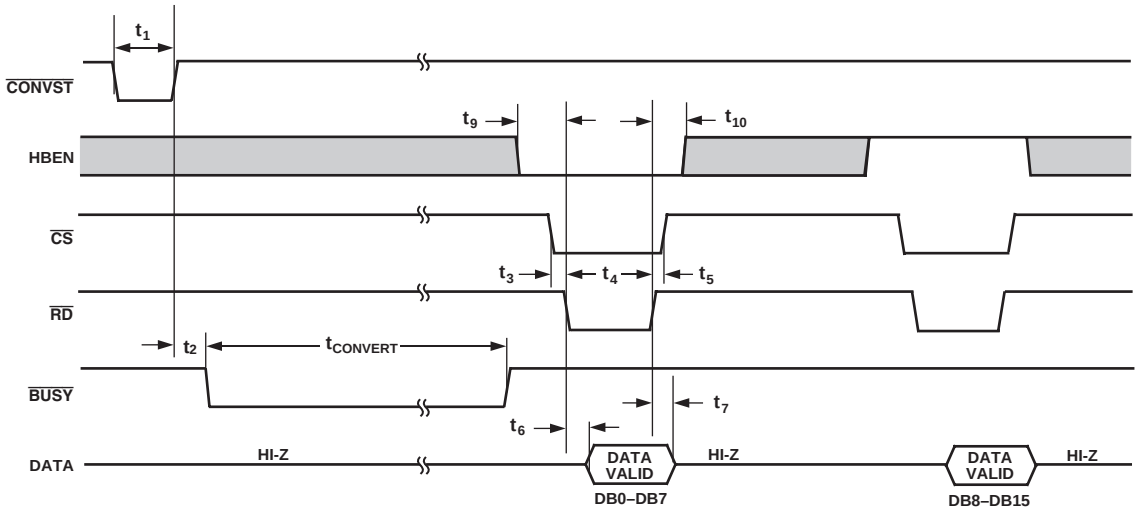


Figure 4. AD7885 Timing Diagram, Using $\overline{CS}$ and $\overline{RD}$

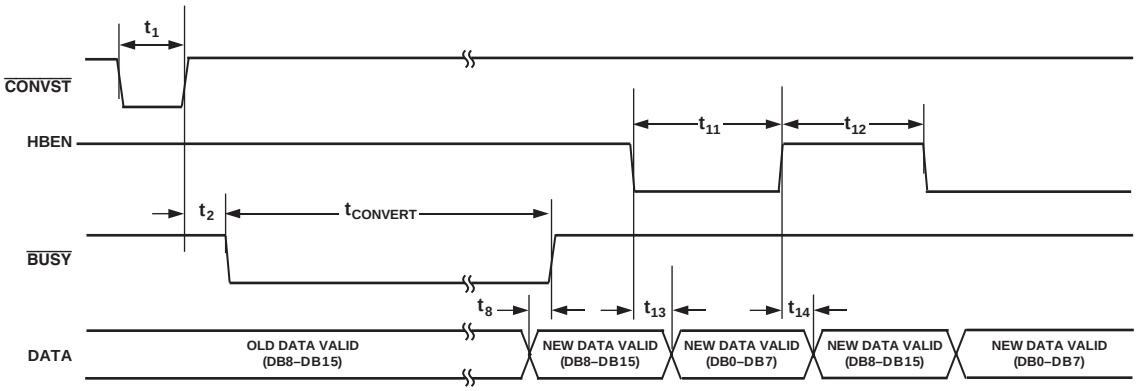


Figure 5. AD7885 Timing Diagram, with $\overline{CS}$ and $\overline{RD}$ Permanently Low

ORDERING GUIDE

Model	Linearity Temperature Range	Error (% FSR)	SNR (dB)	Package Option
AD7884AP	–40°C to +85°C		84	P-44A
AD7884BP	–40°C to +85°C	±0.0075	84	P-44A
AD7885AAP	–40°C to +85°C		84	P-44A
AD7885ABP	–40°C to +85°C	±0.0075	84	P-44A
AD7884AQ	–40°C to +85°C		84	Q-40
AD7884BQ	–40°C to +85°C	±0.0075	84	Q-40
AD7885JQ	–40°C to +85°C		82	Q-28
AD7885AQ	–40°C to +85°C		84	Q-28
AD7885BQ	–40°C to +85°C	±0.0075	84	Q-28

NOTE
P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to AGND . . . . . –0.3 V to +7 V
AV_{DD} to AGND . . . . . –0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to –7 V
AV_{SS} to AGND . . . . . –0.3 V to –7 V
AGND Pins to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
AV_{DD} to V_{DD}[2] . . . . . –0.3 V to +7 V
AV_{SS} to V_{SS}[2] . . . . . +0.3 V to –7 V
GND to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
$V_{IN}S$, $V_{IN}F$ to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
V_{REF+} to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
$V_{REF–}$ to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
V_{INV} to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial Plastic (A, B Versions) . . . . . –40°C to +85°C
  Industrial Cerdip (J, A, B Versions) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
28-Lead Cerdip
  θ_{JA} Thermal Impedance . . . . . 50.9°C/W
  θ_{JC} Thermal Impedance . . . . . 8.3°C/W
40-Lead Cerdip
  θ_{JA} Thermal Impedance . . . . . 44.5°C/W
44-Lead PLCC
  θ_{JA} Thermal Impedance . . . . . 47.7°C/W
  θ_{JC} Thermal Impedance . . . . . 17.5°C/W
Power Dissipation (Any Package) to 75°C . . . . . 1000 mW
Degradation above 75°C by . . . . . 10 mW/°C

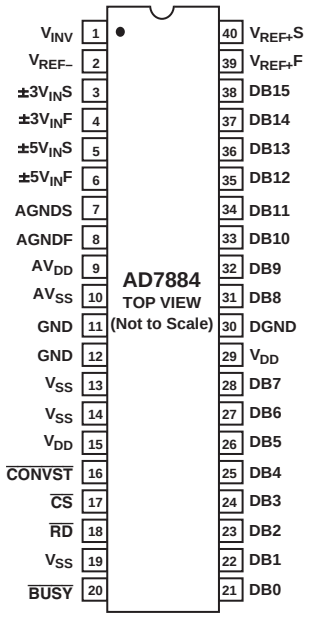
NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]If the AD7884/AD7885 is being powered from separate analog and digital supplies, AV_{SS} should always come up before V_{SS}. See Figure 12 for a recommended protection circuit using Schottky diodes.

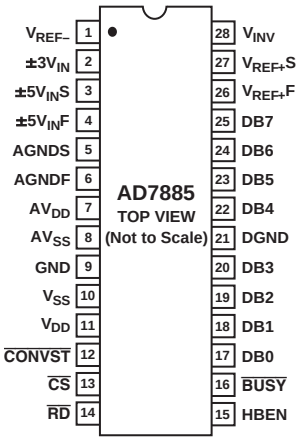
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7884/AD7885 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

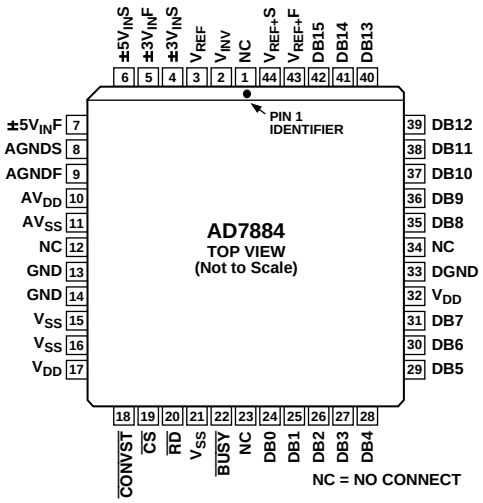
PIN CONFIGURATIONS

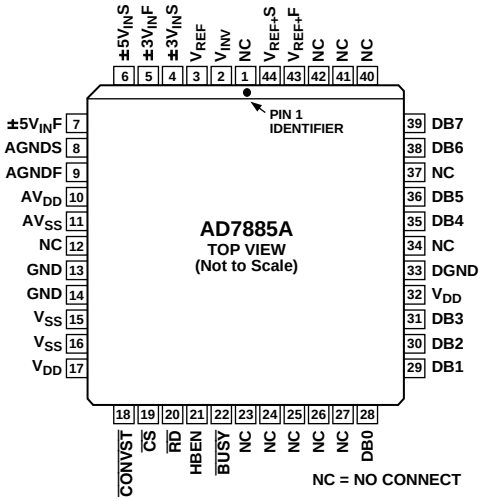
CERDIP





PLCC





PIN FUNCTION DESCRIPTION

AD7884	AD7885	AD7885A	Description
V_{INV}	V_{INV}	V_{INV}	This pin is connected to the inverting terminal of an op amp, as in Figure 6, and allows the inversion of the supplied 3 V reference.
V_{REF-}	V_{REF-}	V_{REF-}	This is the negative reference input, and it can be obtained by using an external amplifier to invert the positive reference input. In this case, the amplifier output is connected to V_{REF-}. See Figure 6.
±3 V_{IN}S	–	±3 V_{IN}S	This is the analog input sense pin for the ±3 volt analog input range on the AD7884 and AD7885A.
±3 V_{IN}F	–	±3 V_{IN}F	This is the analog input force pin for the ±3 volt analog input range on the AD7884 and AD7885A. When using this input range, the ±5 V_{IN}F and ±5 V_{IN}S pins should be tied to AGND.
–	±3 V_{IN}	–	This is the analog input pin for the ±3 volt analog input range on the AD7885. When using this input range, the ±5 V_{IN}F and ±5 V_{IN}S pins should be tied to AGND.
±5 V_{IN}S	±5 V_{IN}S	±5 V_{IN}S	This is the analog input sense pin for the ±5 volt analog input range on both the AD7884, AD7885 and AD7885A.
±5 V_{IN}F	±5 V_{IN}F	±5 V_{IN}F	This is the analog input force pin for the ±5 volt analog input range on both the AD7884, AD7885 and AD7885A. When using this input range, the ±3 V_{IN}F and ±3 V_{IN}S pins should be tied to AGND.
AGNDS	AGNDS	AGNDS	This is the ground return sense pin for the 9-bit ADC and the on-chip residue amplifier.
AGNDF	AGNDF	AGNDF	This is the ground return force pin for the 9-bit ADC and the on-chip residue amplifier.
AV_{DD}	AV_{DD}	AV_{DD}	Positive analog power rail for the sample-and-hold amplifier and the residue amplifier.
AV_{SS}	AV_{SS}	AV_{SS}	Negative analog power rail for the sample-and-hold amplifier and the residue amplifier.
GND	GND	GND	This is the ground return for sample-and-hold section.
V_{SS}	V_{SS}	V_{SS}	Negative supply for the 9-bit ADC.
V_{DD}	V_{DD}	V_{DD}	Positive supply for the 9-bit ADC and all device logic.
$\overline{CONVST}$	$\overline{CONVST}$	$\overline{CONVST}$	This asynchronous control input starts conversion.
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	Chip Select control input.
$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	Read control input. This is used in conjunction with $\overline{CS}$ to read the conversion result from the device output latch.
–	HBEN	HBEN	High Byte Enable. Active high control input for the AD7885. It selects either the high or the low byte of the conversion for reading.
$\overline{BUSY}$	$\overline{BUSY}$	$\overline{BUSY}$	Busy output. The Busy output goes low when conversion begins and stays low until it is completed, at which time it goes high.
DB0–DB15	–	–	Sixteen-bit parallel data word output on the AD7884.
–	DB0–DB7	DB0–DB7	Eight-bit parallel data byte output on the AD7885.
DGND	DGND	DGND	Ground return for all device logic.
V_{REF+}F	V_{REF+}F	V_{REF+}F	Reference force input.
V_{REF+}S	V_{REF+}S	V_{REF+}S	Reference sense input. The device operates from a 3 V reference.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Error

This is the deviation of the midscale transition (all 0s to all 1s) from the ideal (AGND).

Positive Gain Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (+V_{REF+}S – 1 LSB), after Bipolar Zero Error has been adjusted out.

Negative Gain Error
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal (–V_{REF+}S + 1 LSB), after Bipolar Zero Error has been adjusted out.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for an ideal 16-bit converter, this is 98 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7884/AD7885, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7884/AD7885 is tested using the CCIFF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Power Supply Rejection Ratio
This is the ratio, in dBs, of the change in positive gain error to the change in V_{DD} or V_{SS}. It is a dc measurement.

OPERATIONAL DIAGRAM

An operational diagram for the AD7884/AD7885 is shown in Figure 6. It is set up for an analog input range of ±5 V. If a ±3 V input range is required, A1 should drive ±3 V_{IN}S and ±3 V_{IN}F with ±5 V_{IN}S, ±5 V_{IN}F being tied to system AGND.

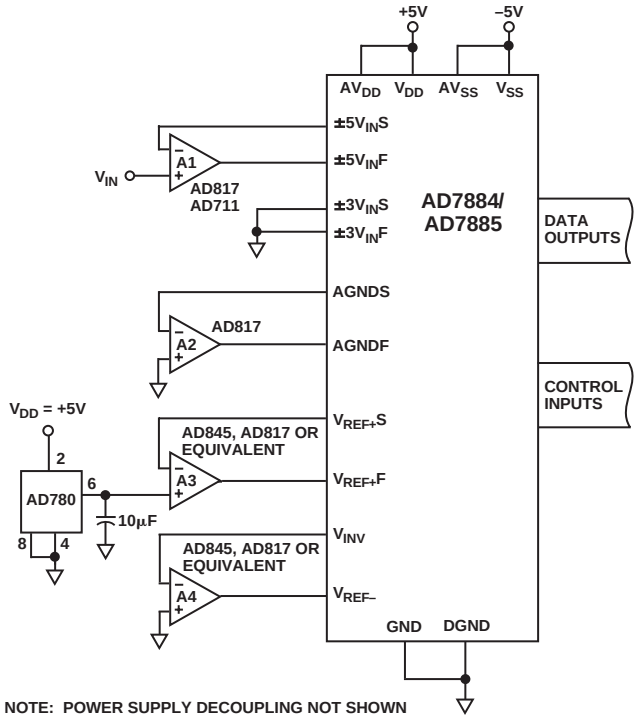


Figure 6. AD7884/AD7885 Operational Diagram

The chosen input buffer amplifier (A1) should have low noise and distortion and fast settling time for high bandwidth applications. Both the AD711 and the AD845 are suitable amplifiers.

A2 is the force, sense amplifier for AGND. The AGNDS pin should be at zero potential. Therefore, the amplifier must have a low input offset voltage and good noise performance. It must also have the ability to deal with fast current transients on the AGNDS pin. The AD817 has the required performance and is the recommended amplifier.

If AGNDS and AGNDF are simply tied together to Star Ground instead of buffering, the SNR and THD are not significantly degraded. However, dc specifications like INL, Bipolar Zero and Gain Error will be degraded.

The required 3 V reference is derived from the AD780 and buffered by the high-speed amplifier A3 (AD845, AD817 or equivalent). A4 is a unity gain inverter which provides the –3 V negative reference. The gain setting resistors are on-chip and are factory trimmed to ensure precise tracking of V_{REF+}. Figure 6 shows A3 and A4 as AD845s or AD817s. These have the ability to respond to the rapidly changing reference input impedance.

CIRCUIT DESCRIPTION

Analog Input Section

The analog input section of the AD7884/AD7885 is shown in Figure 7. It contains both the input signal conditioning and sample-and-hold amplifier. Note that the analog input is truly benign. When SW1a goes open circuit to put the SHA into the hold mode, SW1b is closed. This means that the input resistors, R1 and R2 are always connected to either virtual ground or true ground.

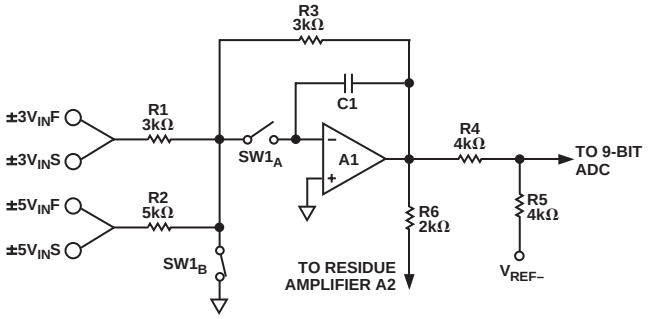


Figure 7. AD7884/AD7885 Analog Input Section

When the ±3 V_{IN}S and ±3 V_{IN}F inputs are tied to 0 V, the input section has a gain of –0.6 and transforms an input signal of ±5 volts to the required ±3 volts. When the ±5 V_{IN}S and ±5 V_{IN}F inputs are grounded, the input section has a gain of –1 and so the analog input range is now ±3 volts. Resistors R4 and R5, at the amplifier output, further condition the ±3 volts signal to be 0 volt to –3 volts. This is the required input for the 9-bit A/D converter section.

With SW1a closed, the output of A1 follows the input (the sample-and-hold is in the track mode). On the rising edge of the $\overline{\text{CONVST}}$ pulse, SW1a goes open circuit, and capacitor C1 holds the voltage on the output of A1. The sample-and-hold is now in the hold mode. The aperture delay time for the sample-and-hold is nominally 50 ns.

A/D Converter Section

The AD7884/AD7885 uses a two-pass flash technique in order to achieve the required speed and resolution. When the $\overline{\text{CONVST}}$ control input goes from low to high, the sample-and-hold amplifier goes into the hold mode and a 0 V to –3 V signal is presented to the input of the 9-bit ADC. The first phase of conversion generates the 9 MSBs of the 16-bit result and transfers these to the latch and ALU combination. They are also fed back to the 9 MSBs of the 16-bit DAC. The 7 LSBs of the DAC are permanently loaded with 0s. The DAC output is subtracted from the analog input with the result being amplified and offset in the Residue Amplifier Section.

The signal at the output of A2 is proportional to the error between the first phase result and the actual analog input signal, and is digitized in the second conversion phase. This second phase begins when the 16-bit DAC and the Residue Error Amplifier have both settled. First, SW2 is turned off and SW3 is turned on. Then, the SHA section of the Residue Amplifier goes into hold mode. Next SW2 is turned off and SW3 is turned on. The 9-bit result is transferred to the output latch and ALU. An error correction algorithm now compensates for the offset inserted in the Residue Amplifier Section and errors introduced in the first pass conversion and combines both results to give the 16-bit answer.

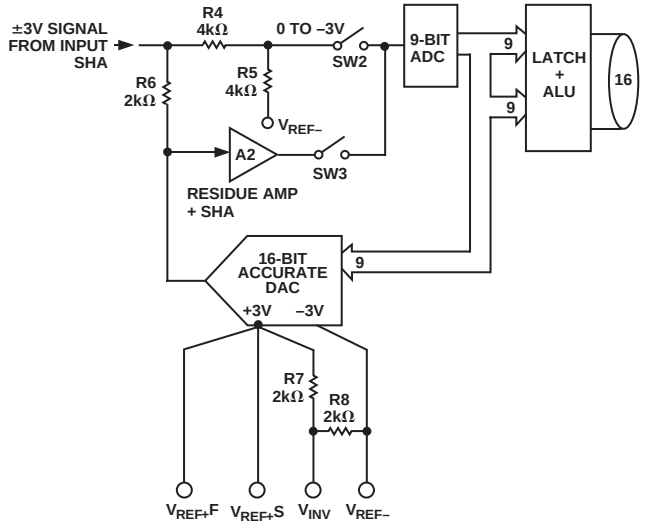


Figure 8. A/D Converter Section

Timing and Control Section

Figure 9 shows the timing and control sequence for the AD7884/AD7885. When the part receives a $\overline{\text{CONVST}}$ pulse, the conversion begins. The input sample-and-hold goes into the hold mode 50 ns after the rising edge of $\overline{\text{CONVST}}$ and $\overline{\text{BUSY}}$ goes low. This is the first phase of conversion and takes 3.35 µs to complete. The second phase of conversion begins when SW2 is turned off and SW3 turned on. The Residue Amplifier and SHA section (A2 in Figure 8) goes into hold mode at this point and allows the input sample-and-hold to go back into sample mode. Thus, while the second phase of conversion is ongoing, the input sample-and-hold is also acquiring the input signal for the next conversion. This overlap between conversion and acquisition allows throughput rates of 166 kSPS to be achieved.

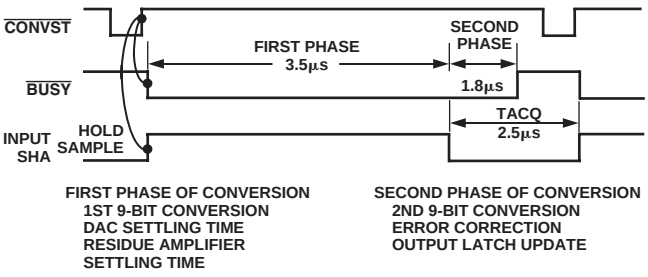


Figure 9. Timing and Control Sequence

USING THE AD7884/AD7885 ANALOG INPUT RANGES

The AD7884/AD7885 can be set up to have either a ±3 volts analog input range or a ±5 volts analog input range. Figures 10 and 11 show the necessary corrections for each of these. The output code is two's complement and the ideal code table for both input ranges is shown in Table I.

Table I. Ideal Output Code Table for the AD7884/AD7885

Analog Input			
In Terms of FSR[2]	±3 V Range[3]	±5 V Range[4]	Digital Output Code Transition[1]
+FSR/2 – 1 LSB	2.999908	4.999847	011 . . . 111 to 111 . . . 110
+FSR/2 – 2 LSBs	2.999817	4.999695	011 . . . 110 to 011 . . . 101
+FSR/2 – 3 LSBs	2.999726	4.999543	011 . . . 101 to 011 . . . 100
AGND + 1 LSB	0.000092	0.000153	000 . . . 001 to 000 . . . 000
AGND	0.000000	0.000000	000 . . . 000 to 111 . . . 111
AGND – 1 LSB	–0.000092	–0.000153	111 . . . 111 to 111 . . . 110
–(FSR/2 – 3 LSBs)	–2.999726	–4.999543	100 . . . 011 to 100 . . . 010
–(FSR/2 – 2 LSBs)	–2.999817	–4.999695	100 . . . 010 to 100 . . . 001
–(FSR/2 – 1 LSB)	–2.999908	–4.999847	100 . . . 001 to 100 . . . 000

NOTES
[1]This table applies for $V_{REF+}S$ = 3 V.
[2]FSR (Full-Scale Range) is 6 volts for the ±3 V input range and 10 volts for the ±5 V input range.
[3]1 LSB on the ±3 V range is FSR/2^{16} and is equal to 91.5 μV.
[4]1 LSB on the ±5 V range is FSR/2^{16} and is equal to 152.6 μV.

Reference Considerations

The AD7884/AD7885 operates from a ±3 volt reference. This can be derived simply using the AD780 as shown in Figure 6.

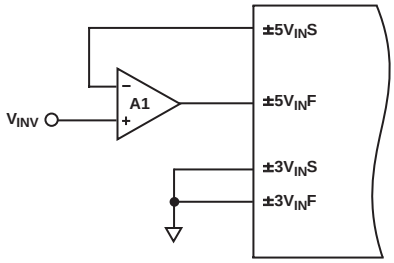


Figure 10. ±5 V Input Range Connection

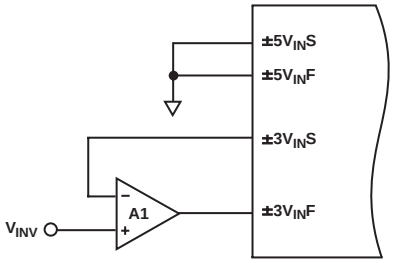


Figure 11. ±3 V Input Range Connections

The critical performance specification for a reference in a 16-bit application is noise. The reference pk-pk noise should be insignificant in comparison to the ADC noise. The AD7884/AD7885 has a typical rms noise of 120 μV. For example a reasonable target would be to keep the total rms noise less than 125 μV. To do this the reference noise needs to be less than 35 μV rms. In the 100 kHz band, the AD780 noise is less than 30 μV rms, making it a very suitable reference.

The buffer amplifier used to drive the device V_{REF+} should have low enough noise performance so as not to affect the overall system noise requirement. The AD845 and AD817 achieve this.

Decoupling and Grounding

The AD7884 and AD7885A have one AV_{DD} pin and two V_{DD} pins. They also have one AV_{SS} pin and three V_{SS} pins. The AD7885 has one AV_{DD} pin, one V_{DD} pin, one AV_{SS} pin and one V_{SS} pin. Figure 6 shows how a common +5 V supply should be used for the positive supply pins and a common –5 V supply for the negative supply pins.

For decoupling purposes, the critical pins on both devices are the AV_{DD} and AV_{SS} pins. Each of these should be decoupled to system AGND with 10 μF tantalum and 0.1 μF ceramic capacitors right at the pins. With the V_{DD} and V_{SS} pins, it is sufficient to decouple each of these with ceramic 1 μF capacitors.

AGNDS, AGNDF are the ground return points for the on-chip 9-bit ADC. They should be driven by a buffer amplifier as shown in Figure 6. If they are tied directly together and then to ground, there will be a marginal degradation in linearity performance.

The GND pin is the analog ground return for the on-chip linear circuitry. It should be connected to system analog ground.

The DGND pin is the ground return for the on-chip digital circuitry. It should be connected to the ground terminal of the V_{DD} and V_{SS} supplies. If a common analog supply is used for AV_{DD} and V_{DD} then DGND should be connected to the common ground point.

Power Supply Sequencing

AV_{DD} and V_{DD} are connected to a common substrate and there is typically 17 Ω resistance between them. If they are powered by separate 5 V supplies, then these should come up simultaneously. Otherwise, the one that comes up first will have to drive 5 V into a 17 Ω load for a short period of time. However, the standard short-circuit protection on regulators like the 7800 series will ensure that there is no possibility of damage to the driving device.

AV_{SS} should always come up either before or at the same time as V_{SS}. If this cannot be guaranteed, Schottky diodes should be used to ensure that V_{SS} never exceeds AV_{SS} by more than 0.3 V. Arranging the power supplies as in Figure 6 and using the recommended decoupling ensures that there are no power supply sequencing issues as well as giving the specified noise performance.

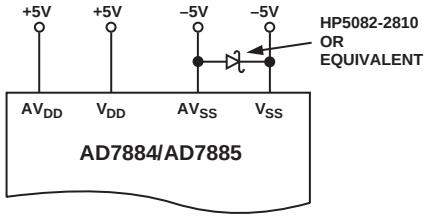


Figure 12. Schottky Diodes Used to Protect Against Incorrect Power Supply Sequencing

AD7884/AD7885 PERFORMANCE

Linearity

The linearity of the AD7884/AD7885 is determined by the on-chip 16-bit D/A converter. This is a segmented DAC which is laser trimmed for 16-bit DNL performance to ensure that there are no missing codes in the ADC transfer function. Figure 13 shows a typical INL plot for the AD7884/AD7885.

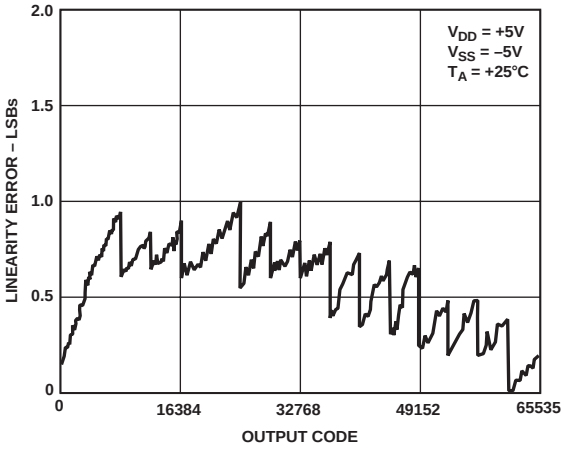


Figure 13. AD7884/AD7885 Typical Linearity Performance

Noise

In an A/D converter, noise exhibits itself as code uncertainty in dc applications and as the noise floor (in an FFT, for example) in ac applications.

In a sampling A/D converter like the AD7884/AD7885, all information about the analog input appears in the baseband from dc to 1/2 the sampling frequency. An antialiasing filter will remove unwanted signals above $f_S/2$ in the input signal but the converter wideband noise will alias into the baseband. In the AD7884/AD7885, this noise is made up of sample-and-hold noise and A/D converter noise. The sample-and-hold section contributes 51 μV rms and the ADC section contributes 59 μV rms. These add up to a total rms noise of 78 μV. This is the input referred noise in the ±3 V analog input range. When operating in the ±5 V input range, the input gain is reduced to –0.6. This means that the input referred noise is now increased by a factor of 1.66 to 120 μV rms.

Figure 14 shows a histogram plot for 5000 conversions of a dc input using the AD7884/AD7885 in the ±5 V input range. The analog input was set as close as possible to the center of a code transition. All codes other than the center code are due to the ADC noise. In this case, the spread is six codes.

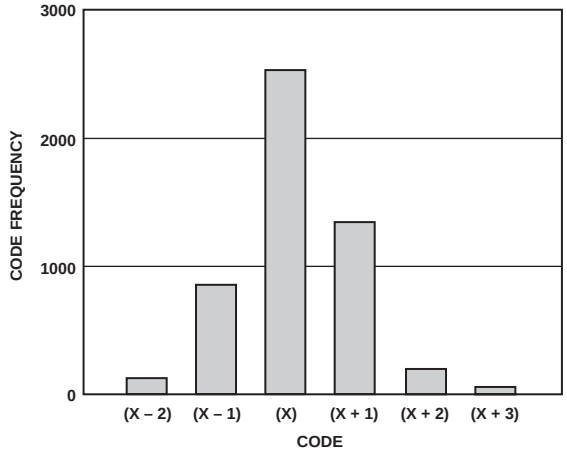


Figure 14. Histogram of 5000 Conversions of a DC Input

If the noise in the converter is too high for an application, it can be reduced by oversampling and digital filtering. This involves sampling the input at higher than the required word rate and then averaging to arrive at the final result. The very fast conversion time of the AD7884/AD7885 makes it very suitable for oversampling. For example, if the required input bandwidth is 40 kHz, the AD7884/AD7885 could be oversampled by a factor of 2. This yields a 3 dB improvement in the effective SNR performance. The noise performance in the ±5 volt input range is now effectively 85 μV rms and the resultant spread of codes for 2500 conversions will be four. This is shown in Figure 15.

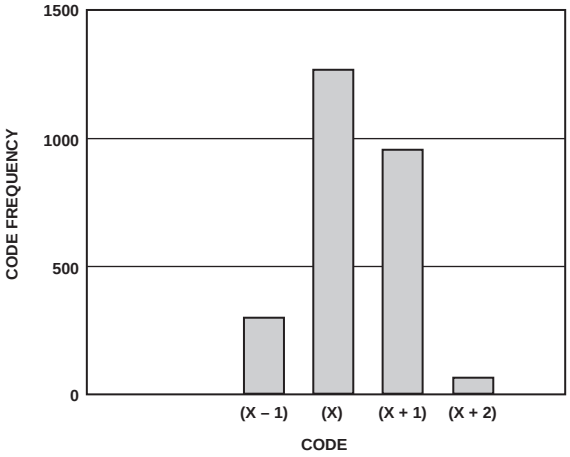


Figure 15. Histogram of 2500 Conversions of a DC Input Using a ×2 Oversampling Ratio

Dynamic Performance

With a combined conversion and acquisition time of 6 µs, the AD7884/AD7885 is ideal for wide bandwidth signal processing applications. Signal to (Noise + Distortion), Total Harmonic Distortion, Peak Harmonic or Spurious Noise and Intermodulation Distortion are all specified. Figure 16 shows a typical FFT plot of a 1.8 kHz, ±5 V input after being digitized by the AD7884/AD7885.

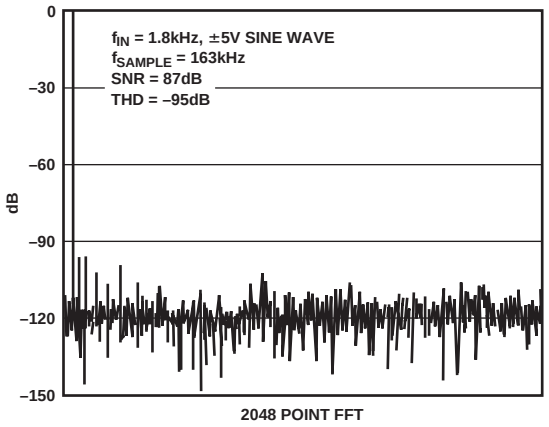


Figure 16. AD7884/AD7885 FFT Plot

Effective Number of Bits

The formula for SNR (see Terminology section) is related to the resolution or number of bits in the converter. Rewriting the formula, below, gives a measure of performance expressed in effective number of bits (N).

$$N = (SNR - 1.76)/6.02$$

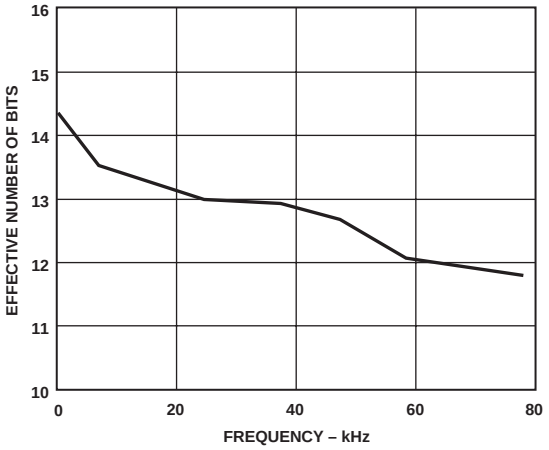


Figure 17. Effective Number of Bits vs. Frequency

The effective number of bits for a device can be calculated from its measured SNR. Figure 17 shows a typical plot of effective number of bits versus frequency for the AD7884. The sampling frequency is 166 kHz.

MICROPROCESSOR INTERFACING

The AD7884/AD7885 is designed on a high speed process which results in very fast interfacing timing (Data Access Time of 57 ns max). The AD7884 has a full 16-bit parallel bus, and the AD7885 has an 8-bit wide bus. The AD7884, with its parallel interface, is suited to 16-bit parallel machines whereas the AD7885, with its byte interface, is suited to 8-bit machines. Some examples of typical interface configurations follow.

AD7884 to MC68000 Interface

Figure 18 shows a general interface diagram for the MC68000, 16-bit microprocessor to the AD7884. In Figure 18, conversion is initiated by bringing $\overline{CSA}$ low (i.e., writing to the appropriate address). This allows the processor to maintain control over the complete conversion process. In some cases it may be more desirable to control conversion independent from the processor. This can be done by using an external sampling timer.

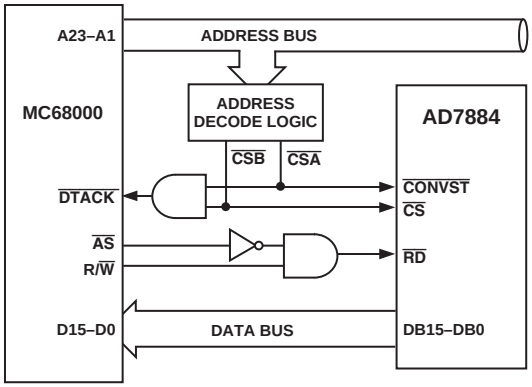


Figure 18. AD7884 to MC68000 Interface

Once conversion has been started, the processor must wait until it is completed before reading the result. There are two ways of ensuring this. The first way is to simply use a software delay to wait for 6.5 µs before bringing $\overline{CS}$ and $\overline{RD}$ low to read the data.

The second way is to use the $\overline{BUSY}$ output of the AD7884 to generate an interrupt in the MC68000. Because of the nature of its interrupts, the MC68000 requires additional logic (not shown in Figure 18) to allow it to be interrupted correctly. For full information on this, consult the MC68000 User's Manual.

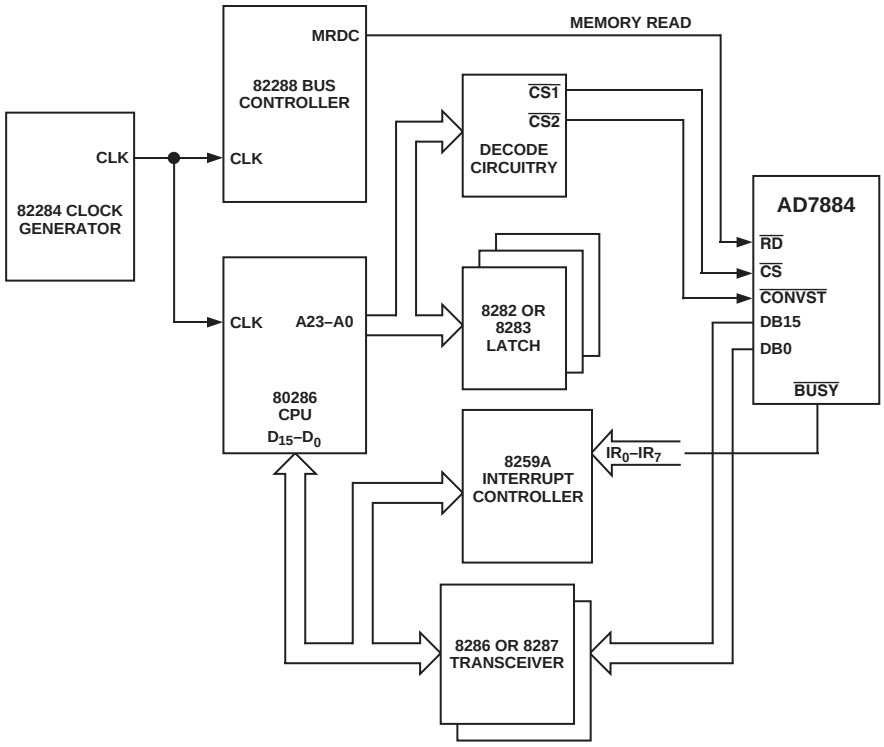


Figure 19. AD7884 Interfacing to Basic iAPX 286 System

AD7884 to 80286 Interface

The 80286 is an advanced high performance processor with special capabilities aimed at multiuser and multitasking systems.

Figure 19 shows an interface configuration for the AD7884 to such a system. Note that only signals relevant to the AD7884 are shown. For the full 80286 configuration refer to the iAPX 286 data sheet (Basic System Configuration).

In Figure 19 conversion is started by writing to a selected address and causing it $\overline{CS2}$ to go low. When conversion is complete, $\overline{BUSY}$ goes high and initiates an interrupt. The processor can then read the conversion result.

AD7885 to 8088 Interface

The AD7885, with its byte (8 + 8) data format, is ideal for use with the 8088 microprocessor. Figure 20 is the interface diagram. Conversion is started by enabling $\overline{CSA}$. At the end of conversion, data is read into the processor. The read instructions are:

```
MOV AX, C001   Read 8 MSBs of data
MOV AX, C000   Read 8 LSBs of data
```

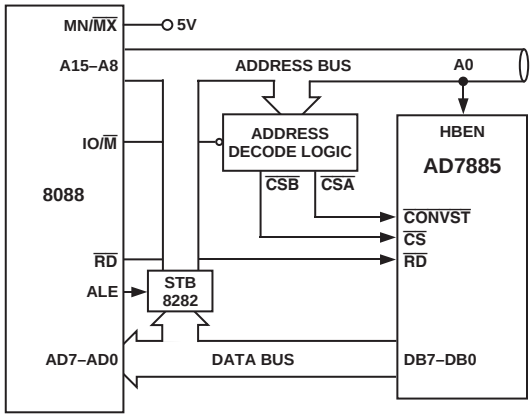


Figure 20. AD7885 to 8088 Interface

AD7884 to ADSP-2101 Interface

Figure 21 shows an interface between the AD7884 and the ADSP-2101. Conversion is initiated using a timer which allows very accurate control of the sampling instant. The AD7884 $\overline{BUSY}$ line provides an interrupt to the ADSP-2101 when conversion is completed. The $\overline{RD}$ pulsewidth of the processor can be programmed using the Data Memory Wait State Control Register. The result can then be read from the ADC using the following instruction:

MR0 = DM (ADC)

where MR0 is the ADSP-2101 MR0 register, and ADC is the AD7884 address.

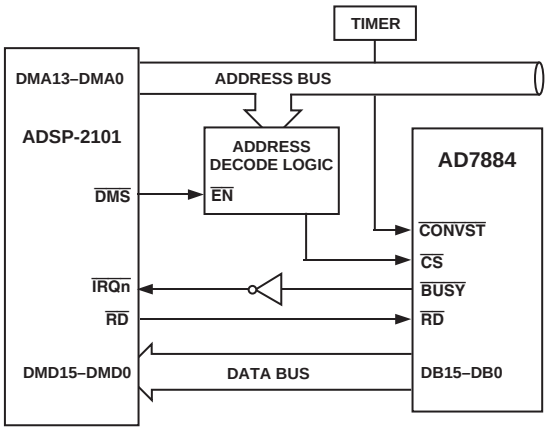


Figure 21. AD7884 to ADSP-2101 Interface

Stand-Alone Operation

If $\overline{CS}$ and $\overline{RD}$ are tied permanently low on the AD7884, then, when a conversion is completed, output data will be valid on the rising edge of $\overline{BUSY}$. This makes the device very suitable for stand-alone operation. All that is required to run the device is an external $\overline{CONVST}$ pulse which can be supplied by a sample timer. Figure 22 shows the AD7884 set up in this mode with the $\overline{BUSY}$ signal providing the clock for the 74HC574 3-state latches.

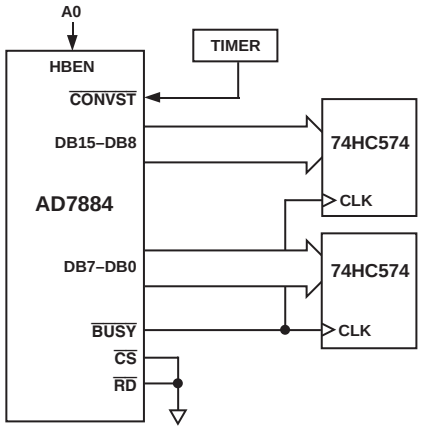


Figure 22. Stand-Alone Operation

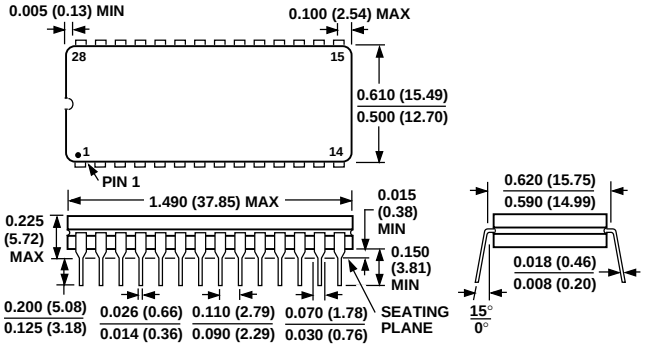
Digital Feedthrough from an Active Bus

It is very important when using the AD7884/AD7885 in a microprocessor-based system to isolate the ADC data bus from the active processor bus while a conversion is being executed. This will yield the best noise performance from the ADC. Latches like the 74HC574 can be used to do this. If the device is connected directly to an active bus then the converter noise will typically increase by a factor of 30%.

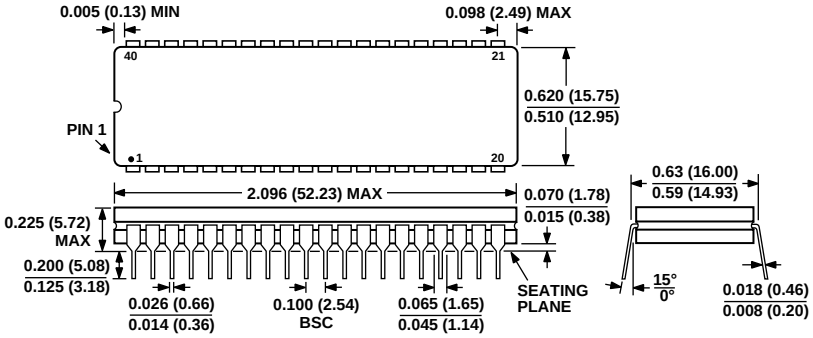
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

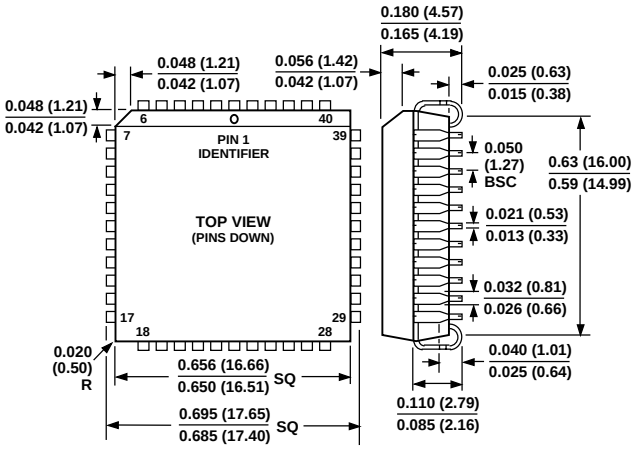
28-Lead Cerdip
(Q-28)



40-Lead Plastic DIP
(Q-40)



44-Lead PLCC
(P-44A)



Revision History

Location	Page
Data Sheet changed from REV. C to REV. D.	
Addition of Cerdip package to GENERAL DESCRIPTION	1
"J" Column added to Specifications	2
Cerdip added to ORDERING GUIDE	5
Edit to ABSOLUTE MAXIMUM RATINGS	5
Addition of Q-28 Outline Dimensions	15

C01353–0–2/02(0)

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Digital to Analog Converters
- D/A Converters
- Audio D/A Converters
- Digital Potentiometers
- Video Encoders

All Product Categories
- Amplifiers and Comparators
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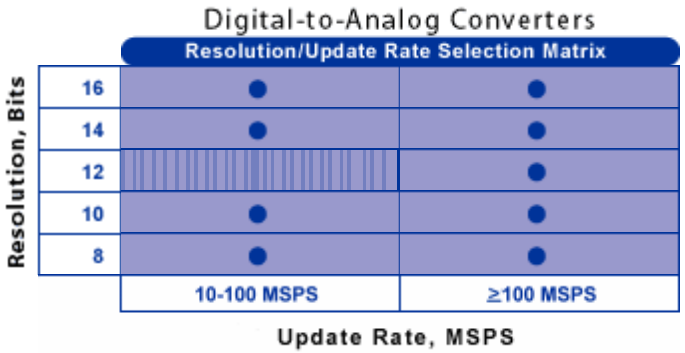
As the world's leading supplier of data converters, Analog Devices enables new system architectures with digital to analog converters that deliver breakthrough combinations of performance and function. Analog Devices' DACs are unmatched in their ability to deliver the low power, small footprint, and low cost requirements today's systems demand. ADI's D/A converters provide superior value for high-volume applications in cost-sensitive markets.

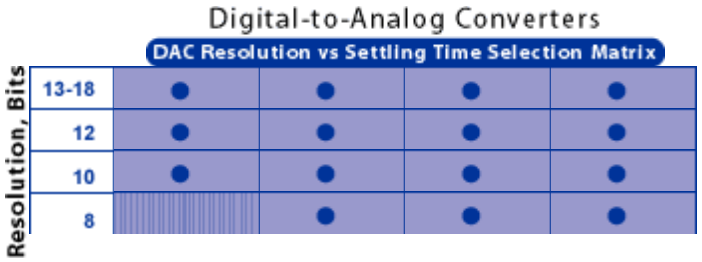
Parametric Search

All DACs

Resolution/Throughput Matrix



Resolution vs Settling Time Matrix



New D/A Converters

AD5063 - 2.7V-5.5V, Full Accurate 16-Bit Vout *nano*DAC™ Converter, Unbuffered, in a MSOP

AD5620 - 3 V/5 V, 12-Bit *nano*DAC™ Converter with 10 ppm/°C Max On-Chip Reference in Sot-23

AD5640 - 3 V/5 V, 14-Bit *nano*DAC™ Converter with 10 ppm/°C Max On-Chip Reference in Sot-23

AD5662 - 2.7-5.5V, 16-Bit *nano*DAC™ Converter in a Sot-23

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Harmonic Images in Digital to Analog Conversion

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Power Dissipation vs. Die Temperature

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≥10 µs	10 µs-1 µs	1 µs-100 ns	100 ns-10 ns

Settling Time

Resources
Overview
Selection Tables
Product Highlights
More...

Les Convertisseurs Analogiques /Numériques *: CAN*

6 - Les paramètres des CAN

Certaines caractéristiques d'un CAN sont définies de manières identique à celle du CNA à savoir: la résolution, les erreurs de décalage, de gain, de linéarité, la vitesse de conversion, les grandeurs d'influence. On définie en plus l'erreur d'hysteresis et l'erreur de quantification.

6.1 Erreur d'hystéresis :

Cette erreur provient du comparateur; elle ne doit pas dépasser $\pm\frac{q}{2}$ (q représente le quantum)

6 .2 Erreur de quantification

La caractéristique de transfert du CAN est en marches d'escalier comme le montre la figure 6.1 .

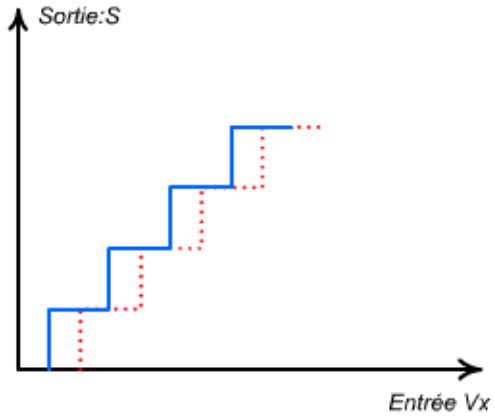

Figure 6.1: Caractéristique de transfert du CAN et quantification du signal

La quantification introduit une erreur systématique. Cette erreur peut être centrée (trait plein) ou par défaut (trait pointillé).

Dans le cas d'un signal analogique V_x évolue sous forme d'une rampe de tension, l'erreur $\varepsilon(t)=S(t)-V_x(t)$ est représentée sur la figure 6.2 .

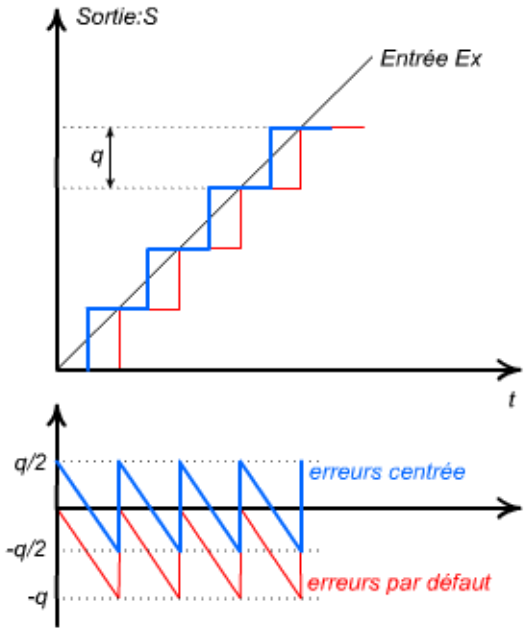

Figure 6.2: Erreurs de quantification

Cette erreur est considérée comme un bruit dynamique superposé au signal. On montre que sa valeur quadratique moyenne est égale à: $\frac{q^2}{12}$ (erreur centrée) et $\frac{q^2}{3}$ (erreur par défaut).

6.3 Réjection des signaux parasites

La réjection des signaux parasites constitue dans certaines applications de l'appareil une spécification importante, car la précision de la mesure peut être gravement affectée par ces signaux. On distingue deux catégories de bruits:

- les bruits série superposés en série au signal utile,
- les bruits de mode commun interviennent spécialement dans l'utilisation des entrées flottantes.

Les Convertisseurs Analogiques /Numériques : CAN

7- Exemples d'utilisation des CNA

Organisation d'un filtre numérique

La figure 77 illustre l'organisation d'un filtre numérique, a chaque instant t = KTe, le signal e(t) est converti en un nombre e(k) par le CAN. Te est la période d'échantillonnage. A la sortie du CAN, on obtient le nombre e(k) codé en binaire sur un nombre de bits. Cette conversion nécessite une durée de quelques dizaines de microsecondes; ceci implique l'utilisation d'un échantillonneur bloquer. La séquence issue du CAN constitue la grandeur d'entrée du filtre numérique. L'utilisation de calcul, qui comporte des opérations addition, multiplication et retard est programmée pour calculer la valeur de s(k) d'une séquence de nombres qui constitue la grandeur de sortie du filtre. Les nombres s(k) sont convertis en un signal analogique s(k.Te) grâce à un CNA. le filtre passe bas restitue le signal continu du temps s(t).

figure 77 : Organisation d'un filtre numérique

D'une manière générale, l'algorithme d'un filtre numérique est la relation de récurrence suivante:
ou h(k) est la réponse impulsionnelle du filtre.
On suppose que le filtre est non récursif; le filtre détermine la séquence S(i) transformée d'une séquence e(i) donnée. La connaissance de la fonction de transfert F(z) du filtre permet de calculer les coefficients de la relation de récurrence et donc de programmer l'unité de calcul pour Vxécution de l'algorithme.

Exemple pratique

Supposons que F(z) soit connue:
F(z) =EQ \F(S(z);E(z)) = EQ \F(z2+1;z2-2z+1) avec F(z) = Laplace(f*(t)) et t= eTp

S'z) et E(z) sont respectivement la transformée en Z de la sortie et de l'entrée. On peut écrire.
z2S(z) - 2zS(z) + S(z) = z2E(z) + E(z)
Recherchons l'original de chaque terme
S(i-2) - 2S(i-1) + S(i) = E(i-2) + E(i)
On obtient la relation de récurrence:
S(i) = E(i-2) + E(i) - S(i-2) + 2S(i-1)
On note que le filtre est caractérisé par sa réponse impulsionnelle et que F(z) est obtenue à partir de cette réponse. Il existe une grande variété de méthodes allant de la simple utilisation des résultats analytiques jusqu'à des méthodes algorithmiques assistées par ordinateur.

Constitution d'une chaîne d'oscilloscope à mémoire numérique

L'oscilloscope à mémoire à tube à rayon cathodique (TRC) est loin de répondre aux Vxigences actuelles. L'oscilloscope à mémoire numérique (Digital Storage Oscilloscope D.S.O) , qui non seulement évité les inconvénients de l'appareil précédent (coût élevé de l'enregistrement de l'information mémorisée, impossibilité de dilater le signal mémorisé en vue d'une analyse détaillée, impossibilité de visualiser les événements précédent le point de déclenchement, ect) offre de nouvelles possibilités: il fournit par Vxemple des sorties numériques pour la programmation à distance et le transfert de données dans les deux sens, il fournit également des interfaces standards ordinateurs dont la plus connue et la plus demandé est le GPIB/ IEE 488 qui permet d'incorporer le DSO à un système automatique d'instrumentation.
La figure 78 représente une voie de la chaîne d'oscilloscope à mémoire numérique.

figure78: Schéma bloc d'une chaîne d'oscilloscope à mémoire numérique

La numération est assurée par un CAN précédé d'un échantillonneur bloqueur. Les données sont ensuite stockées sous contrôle de la logique. Cette opération se répète jusqu'au remplissage complet de la mémoire. On procède ensuite à la lecture non destructive de cette dernière; le signal est reconstitué à l'aide du CNA

suivi d'un filtre car le signal fourni par le filtre est sous forme de niveaux discrets. Le CAN utilisé doit être très rapide (convertisseur flash ou à approximations successives) car la durée de conversion doit être faible pour ne pas limiter le fonctionnement en haute fréquence des DSO.
La capacité de la mémoire exprime la résolution horizontale. Une mémoire de 4K peut stoker 4096 points de données. La résolution horizontale est de 4096 points. si la mémoire est partagée en deux zones d'enregistrement, la résolution sera divisée par deux. une résolution horizontale de N points peut donc être imaginée par un élastique portant N perles espacées figure 79 . Le réglage de la base de temps correspond à l'Vxtension de l'élastique et à l'espacement entre les perles. Si l'Vxtension est égale à tVx secondes, l'espacement entre perles est de EQ \F(tex;N), et tout signal de durée inférieur à EQ \F(tex;N)sera entièrement perdu.
pour une vitesse de balayage donnée, la capacité mémoire d'un DSO détermine sa bande passante et son temps de montée.
1 - la bande passante est égale à SYMBOL 68 \f "Symbol"f = EQ \F(Fe;n)
Fe est la fréquence d'échantillonnage et n le nombre d'échantillons nécessaires pour reconstituer un signal pur (d'après le théorème de SHANON , F est égale à 2 fois la fréquence du signal étudié).
La fréquence d'échantillonnage du DSO dépend de la vitesse de balayage V et du nombre de points de la mémoire N: Fe = EQ \F(N;v).

figure 79 : Points d'échantillonnage nécessaires pour reconstituer le signal

La vitesse de balayage est choisie en fonction de l'application alors que le nombre de points est fixe car il est défini par la taille de la mémoire. pour une vitesse de balayage donnée, la fréquence d'échantillonnage, donc la bande passante, est proportionnelle à la capacité mémoire. Il est intéressant d'observer que, si la

fréquence d'échantillonnage est importante pour élargir la bande passante, elle ne prime que sur la vitesse de balayage très élevées. Sur la courbe représentant la bande passante en fonction de la vitesse de balayage, on constate que, pour des vitesses de balayage usuelles, l'intérêt de la capacité de la mémoire devient prédominante.

2- le temps de montée est d'autant rapide que le nombre de points N est grand. Il dépend aussi de la disposition des points d'échantillonnage par rapport au signal. L'Vxemple de la figure80 indique le cas le plus défavorable ou il est égale à:

figure 80 : Temps de montée dans le cas le plus défavorable

Tr = 1.6. intervalles d'échantillonnage

Tr = EQ \F(1;Fe) = 1.6 EQ \F(V;N)

Ici encore, on voit que le rôle de la capacité de la mémoire est primordial.

Le signal mémoire peut contenir des phénomènes rapides. l'Vxpansion horizontale après mémorisation permet d'observer ces phénomènes en détail. Une grande capacité de la mémoire et une grande Vxpansion associées équivalent à l'effet de loupe d'une double base de temps.

Le DSO peut être doté de la propriété de visualisation en temps réel permettant de suivre l'évolution du phénomène et d'agir sur les paramètres du système étudié tout en jugeant de leurs effets. Le défilement peut être arrêté à tout instant pour une analyse détaillée utilisant l'effet de loupe.

Liens vers d'autres cours similaires

Conversion Analogique-Numérique et Numérique-Analogique	Auteur
Conversion numérique-analogique et analogique-numérique	**Michel Hubin**
Convertisseurs Analogique / Numérique	**Ecole polytechnique fédérale de Lausanne**
Convertisseurs Numérique / Analogique	**Ecole polytechnique fédérale de Lausanne**
Convertisseurs N/A et A/N	**Dominique Chevalier**
Convertisseurs N/A et Convertisseurs A/N	**D. Piot**
Les Conversions D.A.C. et A.D.C.	**NeT_TroniquE**
Les technologies de CAN (simple & double rampes, à approx.) + TD	**CeLtiX**
Convertisseurs A/N et N/A " un bit " sigma delta	**Pierre-Louis Corrieu**
Conversion numérique analogique	**Patrick Dubief**

Liens

http://transdata.free.fr/cna.html	Ce site expose brièvement le principe de la Conversion Numérique Analogique et présente divers types de convertisseurs
http://www2.egr.uh.edu/~glover/	Il s'agit du site web d'un professeur à l'université de Houston, spécialisé entre autre, dans la conversion analogique-numérique. (Site en Anglais)
http://www.iut.u-bordeaux1.fr/geii/Cours/Ccouturie/cours3.pdf	Ce site présente en détail le principe de la conversion analogique numérique tant du point de vue éléctronique que du point de vue traitement du signal.
http://perso.wanadoo.fr/e-lektronik/LEKTRONIK/annexes/conversion.htm	Une page qui présente de façon assez complète la conversion analogique numérique.
http://www.jhu.edu/~signals/index.html	Divers applets Java ayant, plus ou moins, attrait à la conversion analogique numérique.