TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

Page

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LIST OF ABREVIATIONS

AlN	Aluminium nitride
ASIC	Application specific integrated circuit
BAN	Body area network
CBS	Checkerboard straight
CBT	Checkerboard trapezoidal
CMOS	Complementary metal-oxide-semiconductor
DRIE	Deep reactive ion etching
DUT	Device under test
GSM	Global system for mobile communications
IoT	Internet of Things
MEMS	Microelectromechanical systems
PCB	Printed circuit board
PCE	Power conversion efficiency
PZT	Lead zirconate titanate
QFN	Quad flat no-lead
SiP	System in Package
TPMS	Tire pressure monitoring system
VNA	Vector Network Analyzer
WLAN	Wireless local area network
WSN	Wireless Sensor Node

LIST OF SYMBOLS

ζ	Damping ratio
δ	Mechanical strain
σ	Mechanical stress
Y	Young's modulus
d_{ij}	Piezoelectric strain coefficient
ρ	Material density
ω_n	Natural frequency
E	Electric field
D	Electrical displacement (charge density)
Θ	System coupling coefficient
γ	Body effect parameter
φ_f	Surface potential

INTRODUCTION

Motivation

In recent years, massive amounts of data has been required to refine deep learning algorithms and provide smart systems. The global trend is to use more and more sensors to increase the amount of data collected. Accordingly, most objects around us will collect and communicate data. In the internet of things (IoT) world, everything will eventually become a sensor (Libelium, 2019) and wireless sensor networks will become prevalent. Wireless sensors are found today in a wide range of different applications (e.g. health, automotive, aerospace, industry, housing…) as shown in Fig. 0.1. These devices have limited lifetimes because of their operating power requirements. It is expected by the year 2020 that 33 billion IoT devices will be deployed (Razavi, 2015). An important question is how to power these compact sensors? Many researchers are investigating energy harvesting or renewable power "scavenging" technologies to extend battery life efficiently. Even eliminating the battery completely from some systems is highly desired due to its size, cost and environmental impact.

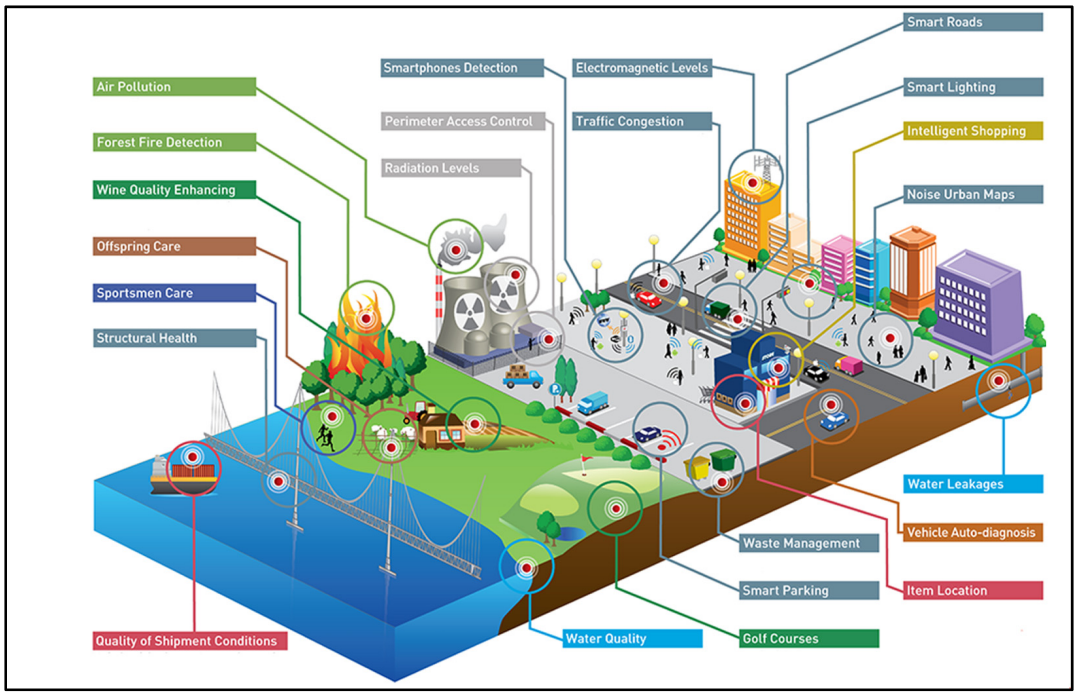

Figure 0.1 Sensors everywhere in the IoT
Taken from Libelium (2019)

Energy harvesting is the conversion of energy present in the ambient environment into electrical energy. Energy harvesting for autonomous wireless sensor nodes applications can recharge and extend the battery life or even provide the required power allowing the wireless sensor nodes to perform their sensing functions and wireless communication with minimal supervision and maintenance. There are different energy harvesting approaches but not all of them are suitable for wireless sensor nodes due to size constraints and power generated. From a paper by Texas Instruments, Table 0.1 lists some of the energy sources available in the ambient with an estimate of how much power can be harvested (Raju et Grazier, 2008). It can be noticed that relatively sizable power can be harvested from industrial vibrations. With the growth of MEMS devices, compact energy harvesting from motion and vibration has become possible. Vibration energy harvesters have the advantage that they can be readily implemented with MEMS technology. The ability to fabricate the converters with silicon based MEMS technology improves the level of integration possible with silicon based microelectronics. Furthermore, voltages within the usable range can be generated avoiding the need for large inductor based power management circuits and making all integrated solutions possible.

Table 0.1 Energy Harvesting Estimates
Taken from Raju et Grazier (2008)

Energy Source	Harvested Power
Vibration / Motion	
Human	4 $\mu W/cm^2$
Industry	100 $\mu W/cm^2$
Temperature Difference	
Human	25 $\mu W/cm^2$
Industry	1-10 mW/cm^2
Light	
Indoor	10 $\mu W/cm^2$
Outdoor	10 mW/cm^2
RF	
GSM	0.1 $\mu W/cm^2$
WiFi	0.001 $\mu W/cm^2$

Research Problem

The limited lifetime of batteries has been a challenge that has required extensive research by scientists to find alternative solutions. Among the possibilities is harvesting energy from the ambient. The global emerging energy harvesting market at the wireless module level grew from $19 M in 2012 to $227 M in 2017, meaning a growth of 51 % per year (Yole, 2012). However, this impressive growth would have been much bigger if it was not limited by various design challenges.

Piezoelectric materials can provide a transduction mechanism to convert signals from mechanical to electrical domains and vice versa. Piezoelectric materials are used for energy harvesting cantilevers due to their high output power density and energy conversion efficiency and they are very suitable for miniaturization. Therefore, this has led to a growing interest in piezoelectric thin films for MEMS applications and this requires an in depth understanding of these materials. However, the use of a commercial technology limits the choice of these materials. This requires more innovative design techniques to overcome this limitation.

Ambient vibrations are present all around us wherever there is an activity related to mechanical oscillations such as those created by machines, household appliances, human walking and many more. However, in most of the practical cases, the vibration in the environment is totally random with the energy distributed in a wide spectrum. For maximum power, the resonant frequency of the harvester should match that of the vibrations. It is favored that these harvesters have low resonant frequencies to respond to these low level vibrations. In addition to the geometry of the harvester, the proof mass geometry along with the piezoelectric materials to be used, has to be looked at to solve the problem of lowering the resonant frequency of these harvesters which is preferably to be paired with an increase in the output voltage. Also broadening the bandwidth of these harvesters is favorable. Many techniques for widening this frequency range are investigated by researchers (Dibin Zhu, 2010; Huan, Yuantai et Qing-Ming, 2008b; Tang, Yang et Soh, 2010). For broadband piezoelectric energy harvesting device, varying the mass or varying the dimensions of a cantilever are among the most used techniques

(Ferrari et al., 2008). Those techniques used to widen the bandwidth are based on multi frequency response of cantilever structures. Piezoelectric cantilevers of different lengths, with the width and thickness kept constant could achieve the wide range of frequency desired (Swee-Leong et al., 2011).

The output of an energy harvester is not directly suited as a power supply for circuits because of variations in its power and voltage over time as it varies with the ambient condition. Therefore a power management circuit is required to convert this volatile electrical power to a regulated power source. The main block in a power management circuit, for converting harvested power is the DC-DC converter or a charge pump with a variable number of stages that performs the DC/DC conversion.

This DC/DC conversion in the power management circuit can be implemented using a linear regulator, an inductor based DC-DC converter or a switched-capacitor DC-DC converter. Power consumption, efficiency, reconfigurability and integration are key features of the prospective design. Most inductor based DC-DC converters require a bulky off chip inductor and the voltage supplied by a linear regulator cannot be higher than the input voltage. Alternatively, switched-capacitor DC-DC converters can be reconfigurable and can be fully integrated in standard CMOS processes in addition to low power and low cost operation. Therefore, the design of a switched capacitor based circuit could be considered. These kind of circuits are highly demanded for biasing of electrostatic MEMS actuators. A challenge that faces electrostatic MEMS actuators (e.g. micromirrors, electrostatic MEMS oscillators or even an electrostatic MEMS harvesters), this requires relatively high configurable voltages to increase the integration level and agility of the circuitry designed.

Research Objectives

The ultimate goal of this thesis is to work towards autonomous wireless senor nodes. The work presents alternative solutions to batteries that do not offer a viable solution to power IoT devices in the future as the wireless sensor nodes are the key building blocks for realizing the

IoT. This thesis enables energy efficiency strategies for longer battery life and better performance. Moreover, it may be possible to power simple systems by the harvested energy stored in super capacitors. This will have substantial environmental benefits.

Autonomous wireless sensors are found today in a wide range of different applications. The Nintendo Wii is an example of the use of wireless sensors for gaming applications (Nintendo). Tire pressure monitoring systems (TPMSs) are examples of wireless sensor nodes (WSNs) used for safety (Yu et al., 2007). Body area network (BAN) with wireless sensors, will provide users with information and various reporting capabilities for medical, lifestyle, assisted living, sports, or entertainment purposes (Honeine et al., 2011).

These devices have limited lifetimes because of their operating power requirements. Vibrational MEMS energy harvesters present a solution to the power operating requirements associated to the batteries limited lifetimes. Low level vibrations occur in many environments including: large commercial buildings, automobiles, aircraft, ships, trains, and industrial environments. Vibration energy harvesters have the advantage that they can be more easily implemented with MEMS technology. The main energy harvesters based on vibrations that are used for small scale energy harvesters are piezoelectric devices.

Piezoelectric materials are materials that physically deform in the presence of an electric field, or conversely, produce an electrical charge when mechanically deformed. Generally, the piezoelectric material can be used in different modes like 33 mode and 31 mode depending on the direction of the voltage generated in response to an applied strain in an xyz-plane. The 31 mode is of interest, meaning that the voltage acts in the 3 or z-direction, and the mechanical stress / strain acts in the 1or x-direction. An advantage of this operation is the large strain in the 1 direction which is developed due to bending (Roundy, 2003). Unimorphs are to be considered, a common type of 31 elements, in which the piezoelectric material is centered in between two metal layers, at the top and bottom. As the beam bends, the piezo layer is in tension or in compression and an alternating current is generated.

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The rate of the harvested energy varies with ambient condition. DC-DC converters are among the most desired circuitry due to their wide range of applications. Therefore, a power management circuit is required to provide a regulated power source for sensor circuits. To realize a complete integrated solution, it is necessary to consider the integration of the MEMS harvester with its power management circuitry in a single package.

Accordingly, the main objectives of this thesis on MEMS energy harvesters can be summed as follows:

1. To analyze cantilever based piezoelectric vibrational energy harvesting. The proof mass effects leading to design tuning strategies to meet specifications and lowering the resonant frequency based on T-shaped designs is the recommended path.
2. To explore an optimal design of a MEMS harvester based on piezoelectric coupling and using the commercial technology PiezoMUMPs. Such devices as piezoelectric benders that exploit the d31 mode of operation will be considered after understanding the geometry effects to maximize the output power based on trapezoidal T-shaped beams.
3. To design and fabricate a DC-DC circuit or charge pump with the ability to generate multiple voltage levels from a fixed input voltage. The system would be highly efficient across the operating range, with accurate output voltage regulation and small size to achieve high integration and could be a significant component to condition the output power of vibration energy harvesters or for MEMS electrostatic actuation.
4. To achieve an optimal vibration energy harvester design that paves the way towards autonomous systems by proposing cross-shaped structures.

Contributions

The main contributions of this work are as follows:

1. A design tuning of the frequency for T-shaped energy harvester structures by varying the proof mass geometry in order to achieve the lowest frequency possible.

Using a commercial technology to fabricate the energy harvesters has various advantages including a precise control over the structure dimensions in order to ensure optimal performance, repeatability and mass production. However, this implies design challenges to work with what the technology is offering. The proof mass has a significant impact in lowering the frequency of the harvester. Therefore, the first contribution of the work was to present design strategies to lower these resonant frequencies by proposing the mass as a planar T–shaped cantilever. This comes with the advantage of the reduction of the device thickness and simpler fabrication and assembly. This work has led to the publication entitled effects of proof mass geometry on piezoelectric vibrational energy harvesters in Sensors (Alameh et al., 2018b).

2. A method for increasing the power output of the energy harvester without significantly sacrificing the resonant frequency by using trapezoidal T-shaped cantilevers.

Different applications limit the area and volume available. Accordingly, the scaling down of the harvesters to fit into small volumes implies various design challenges. This leads to an increase in the resonant frequency and increases the challenge in order to maintain sufficient power output. For that, after being able to present solutions to tune the frequency, the second contribution of the work is to optimize this power output without significantly affecting the frequency by using T-shaped trapezoidal beams instead of rectangular ones. This is due to a better strain distribution which translates to higher currents. The balancing of the strain has to be done carefully as this can have a negative impact. All of this is presented in an article submitted to the IEEE Sensors Journal (Alameh, Gratuze et Nabki, 2019).

3. A novel reconfigurable DC-DC converter charge pump architecture.

MEMS energy harvesters should be accompanied with their power management circuitry. In this case, the circuit design has to satisfy two conditions: First an agile DC-DC circuit and secondly to generate high voltages from low voltages. For that purpose, a novel reconfigurable charge pump has been proposed and fabricated in 0.13 μm CMOS technology. This was

presented in the work published in TVLSI (Alameh et Nabki, 2017a) and focused on the MEMS electrostatic actuation application.

With an increasing demand to higher actuation voltages, recommendations to widening the voltage range were presented in ICECS (Alameh, Bouchami et Nabki, 2016). This proposed architecture satisfies the condition of reconfigurability required and is suitable for energy harvesting, and therefore we propose adapting it to energy harvesting power conditioning circuits.

4. Novel checkerboard piezoelectric vibrational energy harvesting structures for maximal output power and lower resonant frequency

Novel optimal energy harvesting structures are proposed. This is based on the previous studies and is in the direction towards an integrated energy harvesting system to power wireless sensor nodes. The MEMS checkerboard harvester, a new geometry for a MEMS harvester, has been proposed that meets the requirements of a low and wider band frequency and higher power generation. This original work has been presented at ICECS (Alameh et al., 2018a). To extract the power from the harvester, rectification circuits are fabricated in a 0.35 µm CMOS technology based on the work presented in MWSCAS (Alameh et Nabki, 2017b). This contribution directly leads to some of the proposed future work.

Thesis Outline

This thesis is a manuscript based thesis. Hence, chapters 2, 3 and 4 presents one journal paper each. The thesis is organized as follows:

Chapter 1 covers the literature review on various energy harvesting sources, focusing on vibrational energy harvesting. Rectifier circuits and charge pumps within a power management circuit are addressed towards an integrated energy harvesting system.

Chapter 2 studies the effects of proof mass geometry on piezoelectric energy harvesters. In T-shaped structures the mass geometry has significant impact on performance and this is what has been addressed in this chapter through models based on fabrications and measurements. It is based on the paper published in (Alameh et al., 2018b).

Chapter 3 goes further than studying the mass geometry, rather studies the impact of beam geometry on the performance of cantilever based piezoelectric energy harvesters. Namely, rectangular and tapered beams are compared. The advantages of tapered beams are discussed and recommendations are presented. It is based on the paper submitted in (Alameh, Gratuze et Nabki, 2019).

Chapter 4 presents a dynamically reconfigurable charge pump for electrostatic MEMS actuation. The need and advantages of DC-DC conversion, namely agility has been addressed where the benefits can be extended beyond electrostatic actuation to energy harvesting. It is based on the paper published in (Alameh et Nabki, 2017a).

Chapter 5 describes the steps towards an integrated energy harvesting system for IoT sensor nodes. Optimized cross-shaped designs and power management circuits are designed, fabricated, measured and discussed.

The thesis ends with a conclusion and recommendations. A summary of the thesis, relisting the main contributions, a list of published papers, and a glimpse of the future work, both short and long term concludes this thesis.

In Appendix I, other promising work that has been performed on charge pumps is described. This work has been put on hold due to the discontinuation of the fabrication technology used (i.e., GlobalFoundries CMOS 0.13µm technology), however it will be adapted to an alternative technology in future work.

CHAPTER 1

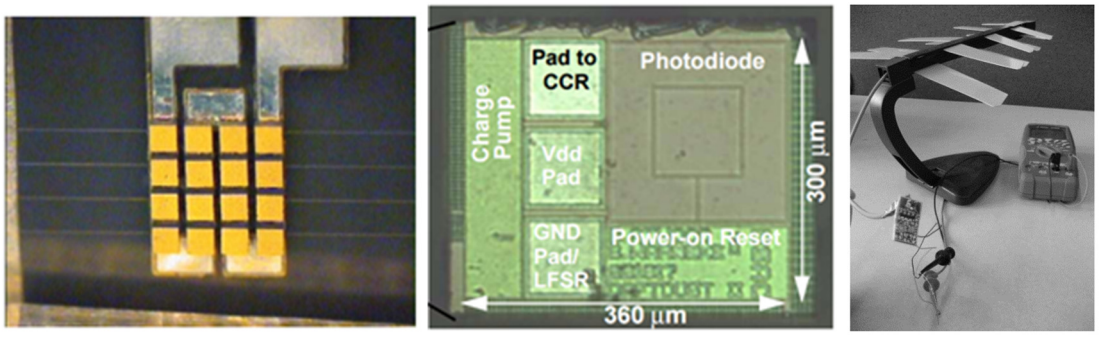
LITERATURE REVIEW

1.1 Introduction

The limited lifetime of batteries has been a hindrance that has spurred extensive research in alternative solutions to batteries. Many researchers have been investigating energy harvesting or energy scavenging technologies as they can provide a clean source of energy. Working towards an energy harvesting system this chapter starts with the different energy harvesting sources, this leads to the choice of vibrational energy harvesting, particularly piezoelectric vibrational energy harvesters. Support circuits including AC-DC rectifiers and DC-DC converters are discussed leading towards integrated energy harvesting systems.

1.2 MEMS Energy Harvesting Sources

A MEMS device is a micrometer scaled system made using microfabrication techniques that is used to sense or control physical events. MEMS applications are limitless, from optics to RF components to lab-on-chip and many more. Among the sensing applications is the use of these micro devices for energy harvesting.



(a) (b) (c)

Figure 1.1 (a) A 4x4 thermoelectric module (Watkins, Shen et Venkatasubramanian, 2005) (b) Photodiode used to power an IC (Warneke, Atwood et Pister, 2001) (c) Harvesting ambient energy from a nearby TV tower (Sample et Smith, 2009)

There are many stray energies in our living space that can be used as energy sources. The mature research on large-scale application of environment energy is not applicable and cannot be used to harvest and store these natural energies in small-scale applications such as wireless sensor nodes. Hence, many research work is approaching energy harvesting technologies for these applications. There are different harvesting approaches that includes thermal, photovoltaic, RF and vibrational harvesting.

1.2.1 Thermal

Thermal energy harvesters are often based on the Seebeck effect in which the temperature difference between two dissimilar conductors produces a voltage difference. They are widely used, however for micro scale solutions the thermoelectric materials have to be chosen to be compatible with clean room processing for their integration into MEMS devices. Superlattices have been used. Figure 1.1(a) presents a 4×4 couple thermo electric module fabricated for energy harvesting using superlattice thermoelectrics for applications in implantable medical devices and sensors (Watkins, Shen et Venkatasubramanian, 2005) with power density ranges from 0-6 mW/cm^2 depending on the temperature gradient.

1.2.2 Photovoltaic

Photovoltaic technology is very well developed on macroscale. Photovoltaic cells convert incoming photons into electricity. Outdoors, there is sufficient energy unlike indoors where illumination levels are much lower where the energy density drops to about 10 $\mu W/cm^2$. Figure 1.1(b) shows photovoltaic cells used as energy scavengers in the Smart Dust Program at the University of California, Berkley (Warneke, Atwood et Pister, 2001). Dye sensitized solar cells in energy harvesting have been presented as a promising solution, the dyes absorbs light and much higher power can be produced (Hardin et al., 2009; Li et al., 2006).

1.2.3 Radio Frequency

RF energy harvesting from that available through public telecommunication services (e.g. GSM and WLAN frequencies) is hindered by very low power density levels. An example of harvesting energy from a TV tower by Intel was demonstrated by (Sample et Smith, 2009) and can be seen in Fig. 1.1(c). The tower transmitted energy that was used to power a temperature sensor. However with a relatively large antenna area (30 cm by 20 cm), 60 μW of energy was harvested (energy density 0.1 $\mu W/cm^2$).

1.2.4 Vibrations

On the other hand, vibration energy harvesters have the advantage that they can be more easily implemented with MEMS technology. They rely on a more common energy source which is vibrations. The ability to fabricate the converters with silicon based MEMS technology improves the level of integration possible with silicon based microelectronics. Vibration energy harvesting converts mechanical displacement present in the environment into electrical energy. It provides high power densities, low cost, compact in size and more easily implemented with MEMS technology. This will be discussed in the following section.

1.3 Vibrational Energy Harvesters

Three main converters enable to turn mechanical energy into electricity: electrostatic devices, piezoelectric devices and electromagnetic devices. Figure 1.2 shows the number of publications on piezoelectric, electrostatic, and electromagnetic energy harvesters indexed in Web of Science between years 2003 and 2013 (Toprak et Tigli, 2014). It shows a growing interest in piezoelectricity especially in recent years. In general, the output voltage tends to be too low in the case of electromagnetic transducers and too high in the case of electrostatic transducers. The highest power output is achieved with piezoelectric conversion for MEMS energy harvesters (Vullers et al., 2010b; Vullers et al., 2009). The electrostatic and piezoelectric harvesters are easy to fabricate with small sizes (1-10 mm), while electromagnetic

energy harvesting devices are relatively larger. A few µW of power and up to several mW can be achieved depending on the transducer type. An overview of the operating principle of each will be introduced briefly with examples of other works about each of these three are added in the following subsections.

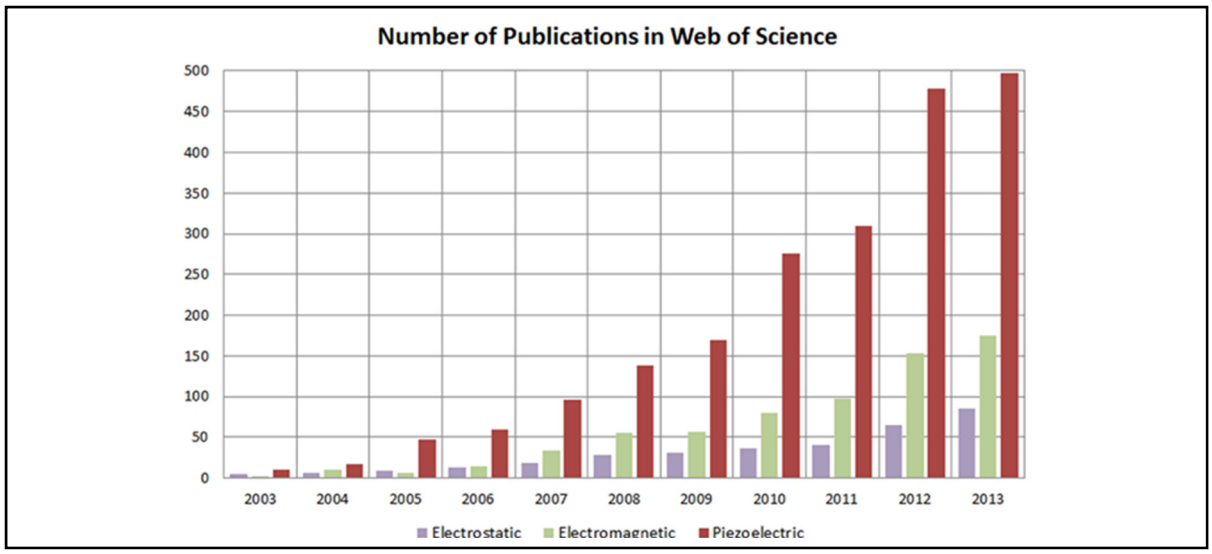


Figure 1.2 Number of publications on piezoelectric, electromagnetic, and electrostatic energy harvesters in Web of Science between years 2003 and 2013
Taken from Toprak et Tigli (2014)

1.3.1 Electromagnetic Energy Harvesters

Electromagnetic induction is based on the motion of an electrical conductor in a magnetic field, and an electric current is generated. Usually it is done by means of a permanent magnet, a coil and a resonating cantilever. A micromachined electromagnetic energy harvester has been presented in (Kulkarni et al., 2007) by moving a magnet in between two microfabricated coils. The device volume is 150 mm^3 and it generated about 586 nW of power across 110 ohm load when excited by an acceleration of 8.829 m/s^2 at 60 Hz. While a macroscopic electromagnetic harvester, shown in Fig. 1.3, based around two magnets coupled to a coil attached to a cantilever have achieved 37 µW at 322 Hz (0.84 cm^3) (Glynne-Jones et al., 2004).

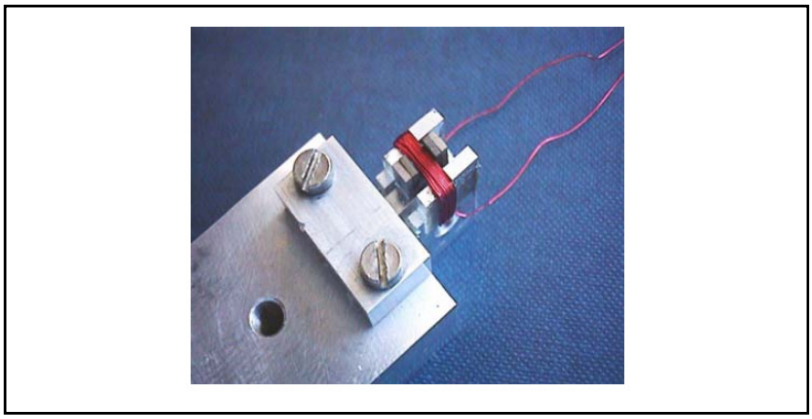


Figure 1.3 Photograph of electromagnetic generator geometry
Taken from Glynne-Jones et al. (2004)

1.3.2 Electrostatic Energy Harvesters

Electrostatic energy harvesters are capacitive devices made of two plates separated by a dielectric material. As the two plates move relative to each other, this generates a capacitance variation and consequently electric charges. Electrostatic converters are of two types: electret free and electret-based. Electret-free electrostatic converters use conversion cycles made of charges and discharges of the capacitor while the others use electrets, giving them the ability to directly convert mechanical power into electricity (Lin et al., 2015). These converters are based on a variable capacitive structure where different capacitor shapes can be employed.

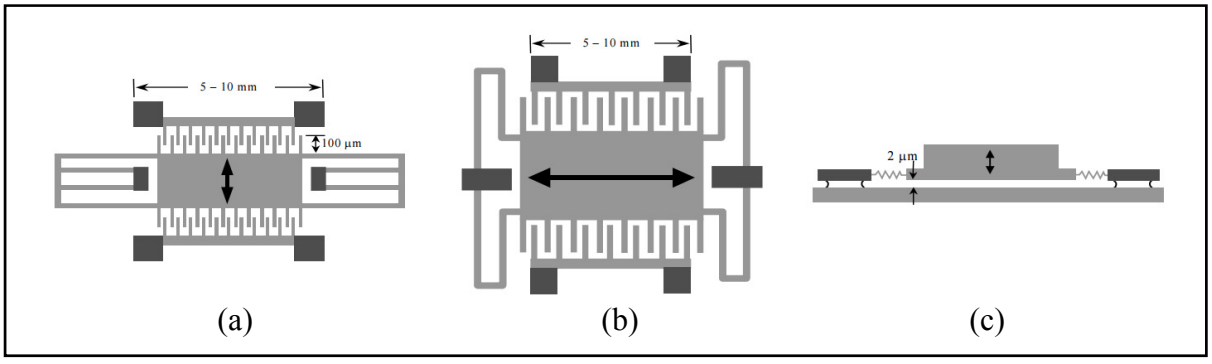


Figure 1.4 Three topologies for micromachined electrostatic converters (a) In-plane overlap (b) In-plane gap closing and (c) Out-of-plane gap closing
Taken from Roundy, Wright et Pister (2002)

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Detailed models of three different electrostatic vibration energy harvester design concepts are developed in (Roundy, Wright et Pister, 2002). The three design concepts: in-plane overlap (capacitance changes by changing overlap area of fingers), in-plane gap closing (capacitance changes by changing gap between fingers), and out-of-plane gap closing (capacitance changes by changing gap between two large plates), shown in Fig. 1.4, are evaluated and compared based on simulations and practical considerations. Their simulations indicate that the highest power density is achieved with in-plane gap closing converters, followed by out-of-plane gap closing converters, and finally by in-plane overlap converters.

A formal optimization of the in-plane gap closing topology is performed in that article, taking some physical constraints into consideration. Test devices have been designed for a DRIE process that etches MEMS structures into the top layer of a SOI wafer. The silicon DRIE process for which this converter is designed has a maximum aspect ratio of about 50. The maximum aspect ratio of the features, and if the total volume has to be less the 1 cm^3, will limit the maximum achievable power output. A final design is produced using the optimal design parameters, Table 1.1. Simulations of the optimized design show that an output power density of 116 $\mu W/cm^3$ is possible from input vibrations of 2.25 m/s^2 at 120 Hz. The following design parameters have to be optimized within the space and aspect ratio constraints: the input voltage (Vin), total length and width of the device, device thickness, length of the interdigitated fingers, and nominal gap between fingers. The 116 μW output power is based on simulations. It has to be proven by measurements.

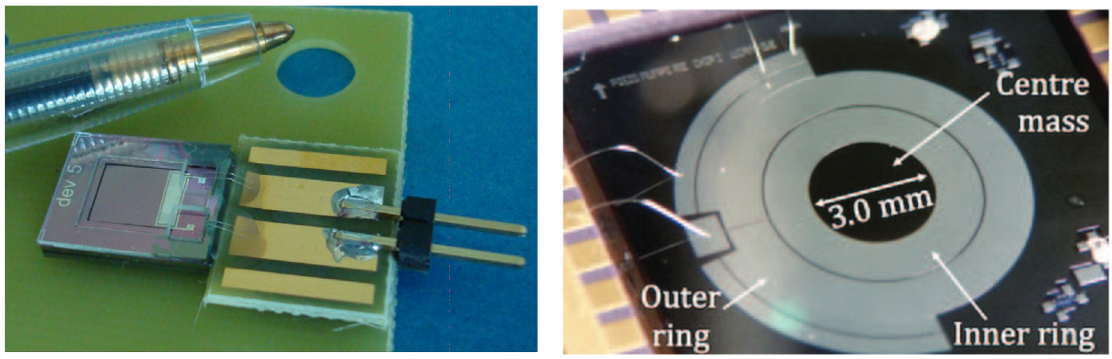
Table 1.1 Design Parameters and Power Output
for an In-plane Gap Closing Design

Vars	**Description of Variable**	**0.25 μm min gap**
W	Width of shuttle mass	10 mm
L	Length of shuttle mass	9 mm
L_{fin}	Length of fingers	530 μm
T	Device thickness	200μm
Vin	Input voltage	10V
Gap	Nominal dielectric gap	50μm
Pout	Output power	116μW

The best structure for electrostatic devices was proved to be in-plane gap closing and this has been confirmed in the work (Boisseau, Despesse et Seddik, 2012). However these electrostatic devices require relatively high actuation voltages which can limit there application and this is part of the research in this work.

1.3.3 Piezoelectric Energy Harvesters

The interest in piezoelectric energy harvesting has grown since the early 2000s, though the piezoelectric effect has been discovered much before. The research focused on the concept of converting mechanical strain into electric voltage or current using piezoelectricity has went in different directions. Some work focused on studying piezoelectric materials and creating new materials with superior characteristics to the ones currently available. Mostly materials such as single crystal (e.g. quartz), piezoceramic (e.g. lead zirconate titanate PZT), thin film (e.g. zinc oxide) and polymeric materials (e.g. polyvinylidenefluoride PVDF). Other works looked into hybrid designs with piezoelectric harvesters combined with other energy harvesting phenomena like electromagnetic for instance (Yang et al., 2010). On the other hand, most of the research focused on exploring new design architectures to create these resonant structures. The first of these structures that is still dominant is the use of a simple beam structure (Shen et al., 2008) (Aramaki et al., 2017) (Wang et al., 2017). Often a mass is being attached to the cantilever beam (Marzencki, Ammar et Basrour, 2007) (Elfrink et al., 2009). For e.g. the piezoelectric harvester in (Marzencki, Ammar et Basrour, 2007) achieved 40 μW when measured on a PZT based harvester with beam dimensions of 400 μm × 800 μm and mass volume of 800 μm × 800 μm × 400 μm and the one in (Elfrink et al., 2009) 60 μW on an AlN based harvester with beam dimensions of 1mm × 5 mm and mass volume 5mm×5mm×400 μm. Both where relatively large designs with Figure 1.5 showing the latter. Some variations has been reported to the shape of the beam, like S-shaped (Shmulevich et Elata, 2015), T-shaped (Minh et al., 2013), Trapezoidal (Miller et al., 2011), Triangular (Kherbeet et al., 2015) and other different geometries (Jia, Du et Seshia, 2016). All these different types, aim at having the best possible specifications. This research will investigate some of these different options through studies and comparisons to present recommendations for optimal designs.



(a) (b)

Figure 1.5 Piezoelectric energy harvester (a) rectangular beam (Elfrink et al., 2009) and (b) disk membrane (Jia, Du et Seshia, 2016)

1.4 Support Circuits

In this section, rectifying circuits and DC-DC converters are discussed. Charge pump techniques for microenergy harvesting can be extended to provide biasing voltages for electrostatic actuators.

1.4.1 AC/DC converters

Full bridge rectifiers are among the most common rectifying circuits used in energy harvesting mainly for their simplicity. Diode connected transistors have been used for integrated solutions. However, the low level output voltage that can be generated from the harvester could be less than that required to operate the diode. The use of a Schottky diode would be a favorable choice to achieve a large power conversion efficiency (PCE), but it is not compatible with the conventional CMOS technology and requires costly fabrication processes. Some other approaches are presented in the literature, however they do not fit with the targeted integration approach mainly due to the use of bulky inductors. For instance, improvements to full bridge rectifiers have been proposed by (Ramadass et Chandrakasan, 2010), based on the approach that uses switched magnetic components along with controllers. Many variations of these circuits have been adapted in the literature. While these circuits are much more efficient, however to use them enough power has to be generated in order to accommodate the use of

these controllers. The same argument holds with active diodes which can be used for lower input voltages, but do not fit with the power budget targeted herein.

1.4.2 DC/DC converters

At the heart of every power management circuit is a DC-DC converter. They play a crucial role to convert the variable DC input voltages to a regulated DC output voltage, with either a larger or a smaller magnitude. Broadly DC converters can be classified into three categories: linear regulators, switch mode power converters and switched capacitor power converters. Linear regulators exhibit relatively small area and can be fully integrated in standard CMOS processes. The voltage supplied cannot be higher than the input voltage. For example, (Shenck et Paradiso, 2001) uses a low dropout (LDO) linear regulator in the power conditioning circuit for the shoe powered RF tag system which has led to a low efficiency for the DC-DC converter. Inductor based DC-DC converter are efficient but they often require a bulky off-chip inductor in μH range. Very high frequency require inductors in nH range but that increases the current leading to low efficiency at low output power levels. The associated size penalty limits their use in certain applications (Yi-Chun et Otis, 2011). An example of an inductor based energy harvesting system has been proposed in (Torres et Rincon-Mora, 2009; 2010). They present an electrostatic energy-harvesting and battery-charging CMOS system prototype. It is a voltage-constrained system, i.e. the voltage of the harvested energy storage battery limits the maximum voltage of the capacitor. In their paper, a prototype circuit that precharges, detects, and synchronizes to a variable voltage-constrained capacitor validates experimentally electrostatically energy harvesting from vibrations. The experimental results show that, on average (excluding gate-drive and control losses), the system harvests 9.7 nJ/cycle by investing 1.7 nJ/cycle, yielding a net energy gain of approximately 8 nJ/cycle at an average of 1.6 μW (in typical applications) for every 200 pF variation. Projecting and including reasonable gate-drive and controller losses reduces the net energy gain to 6.9 nJ/cycle at 1.38 μW.

Alternatively, switched-capacitor (SC) DC-DC converters have high efficiency at low current levels and can be fully integrated in standard CMOS processes. Therefore, we consider the

design of a switched-capacitor based power management circuit for energy harvesting applications.

The major advantage of SC power converters and what makes them of interest for researchers is their capability for monolithic integration at low power levels (Vaisband, Saadat et Murmann, 2015). Several power management circuits based on switched capacitor architecture have been published lately. Reference (Ma et Bondade, 2013) describes a design for sub-mW application to extract the maximum power from a thermoelectric source, but it does not regulate the output voltage. Reference (Ng, August 2011) describes the design of a reconfigurable charge pump, but it targets a maximum output power of just 10 μW and the reported peak efficiency is only 65%. Reference (Le, Sanders et Alon, 2011) presents a reconfigurable switched-capacitor DC-DC converter with variable frequency, but is designed for operation with a fixed input voltage (1.2 V). Reference (Chowdhury et Ma, 2009) demonstrates a reconfigurable charge pump converter operating efficiently over a wide input voltage range, but is designed for load currents in the range of several tens of mA. Many reconfigurable switched-capacitor converters are based on optimization heuristics (Saadat, 2015).

1.4.3 Charge Pumps for Micro Energy Harvesting and More

Charge pumps can be used to step-up the rectified AC voltage from the harvester. In a review of charge pump topologies for micro energy harvesting systems (Mi et al., 2016), different topologies had been studied and compared. The cross-coupled architecture was found to have the versatility and suitability to meet the requirements as it can be used as a rectifier, step-up converter and as a step-down converter. There is a need for DC-DC circuits that are reconfigurable in order to respond to variable inputs and to generate a regulated output, or can be used to generate from a fixed input, multiple regulated outputs. The latter is of high interest to the actuation of electrostatic MEMS devices. Electrostatic MEMS require relatively high and variable DC voltages for their actuation. The advantage of charge pumps with respect to conventional switching converters is that magnetic passive components are not needed. These

high voltages could be achieved by cascading the stages with the first stage acting as a rectifier and the remaining stages as voltage doublers. This will yield higher voltages limited only by the breakdown voltages of the used trasistors.

Traditionally switched capacitor step up charge pumps in which the pumping capacitors step-up the voltage in sequence have been preferred. That is, ideally the output will be 2Vin, 3Vin… (N+1)Vin. The main advantage of this topology is that the bottom plate parasitic capacitor experiences a voltage swing of just Vin, however a disadvantage is that it provides a fixed input voltage source.

Another topology is the series parallel, it is easier to provide multiple and fractional gains. The series parallel can be used for wireless sensor node applications. In certain applications, these self-powered microsystems need both step-up and step down conversion in the power stage, since battery voltages can decline over its operating lifetime, as the power is drained. Hence, an interesting reconfigurable Step-Up and Step-Down switched capacitor dc-dc power converter is presented in (Ma et Bondade, 2013). It operates with a pair of complimentary phases, two pumping capacitors and 11 switches to employ the power stage seen in Fig. 1.6. This allows the converter to be reconfigured with 5 different conversion gains 1/2, 2/3, 1, 3/2, 2, depending on the switching schemes for the different configurations of the SC power converter.

With these conversion gains ranging from 1/2 (step-down) to 2 (step-up), this circuit could be used in power conditioning circuits. It can respond to the variable voltages from the harvester whether they are high or low to obtain a regulated supply (e.g. 1.2 V). However, realizing this circuit in standard CMOS technologies presents a challenge at the level of implementing the switches and their control to achieve the different conversion gains with limited power budget. The closed loop operation of the feedback controller for the step-up/down SC power converter has to be identified. Adapting a solution to these short comings could result in an enhanced form of the design to suit desired applications.

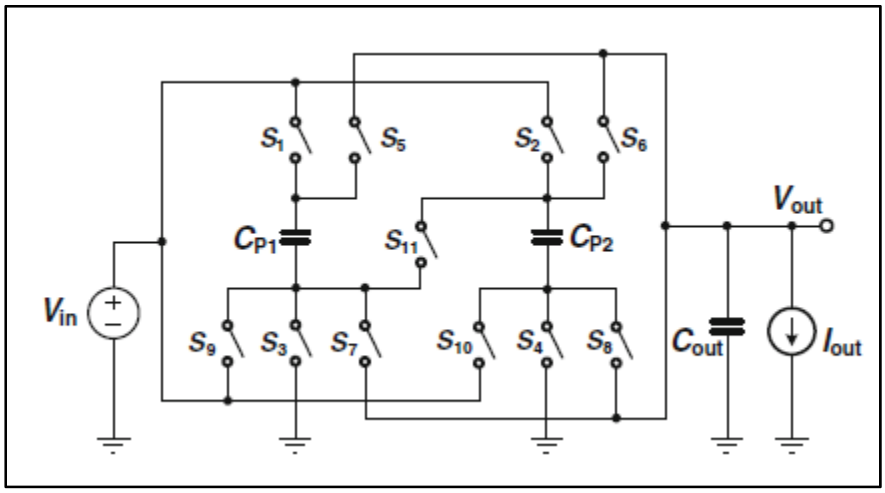


Figure 1.6 The reconfigurable step-up and step-down SC power stage
Taken from Ma et Bondade (2013)

1.5 Energy Harvesting Systems

A MEMS energy harvester design has a mechanical and an electrical part. In the literature, few works present the system as a whole in order to verify the functionality of the signal paths from the mechanical structures to the electrical circuits. There have been independent solutions in optimizing the design of the mechanical harvester or its power management circuitry but few coupled works that cover the harvesting MEMS and the required circuits together.

From this few, an integrated power harvesting system including a MEMS generator and a power management circuit has been presented in (Marzencki, Ammar et Basrour, 2007). The MEMS generator and the power management circuit are realized as a System On a Package (SoP). The mechanical transduction is performed using the piezo electric effect of a thin layer of Aluminium Nitride (AlN) which is deposited on an SOI substrate. This material has been chosen because its deposition is simple, compatible with microelectronics and does not require polarisation. Figure 1.7(a) presents the fabricated device using microfabrication techniques.

The power management circuit consists of an AC/DC converter which rectifies the alternative signal generated and a DC/DC converter to meet the voltage levels of the storage element. A Villard voltage doubler has been used, which uses ideal diodes and capacitors. While this kind

of converters has the great benefit of simplicity, its output has very poor ripple characteristics. The effectiveness of the AC/DC and DC/DC converters for charging the micro batteries or super capacitors has to be improved.

The proposed system of 5 mm^3 incorporates a MEMS power generator that delivers very low powers (in the nW range) at voltages often inferior to 200 mV. The proposed SoP is shown in Fig 1.7(b).

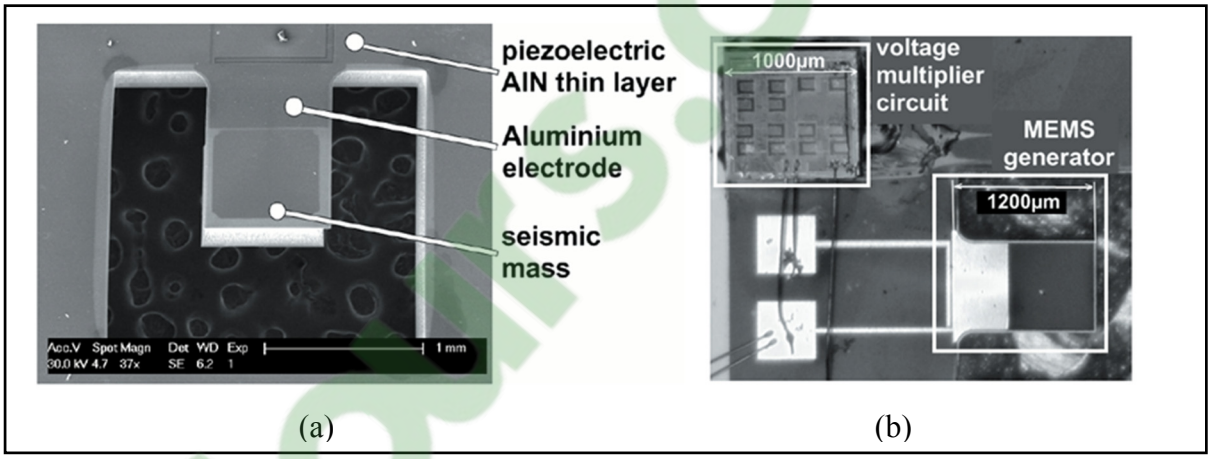


Figure 1.7 (a) SEM image of piezoelectric harvester (b) Proposed system
Taken from Marzencki, Ammar et Basrour (2007)

The structure of this system is interesting. Upon analysing it and addressing some of its shortcomings, an optimized system would positively benefit from a customized adaptation of this design. Their proposed system could benefit from exploring other piezoelectric materials (for e.g. PZT which has better coupling coefficients) or other geometries for the harvester. Another limitation is the use of a controlled vibration source, while in energy harvesting applications the harvested energy is random and unpredictable and the system has to respond to that. Widening the frequency bandwidth of the energy harvester by targeting multi mode energy harvesters could present a better solution.

Another work by (Elfrink et al., 2010) attempted at designing a low power wireless autonomous sensor system. While the paper details the fabrication and the performance of the

energy harvester, the information presented about the power management circuits was scarce. Discrete components have been used to provide a continuous DC power of 10 µW with a rectification efficiency of about 60 % to power an in-house-built low power wireless sensor system.

In their work (Yu et al., 2014), they present an array of five cantilever beams with unit dimensions of about 3×2.4×0.05 mm^3 and a mass dimension of about 8×12.4×0.5 mm^3 connected in series to produce a power output of 66.75 µW. A bulky design with a power conditioning circuit realized using discrete components, seen in Fig. 1.8, achieves an efficiency of 65%.

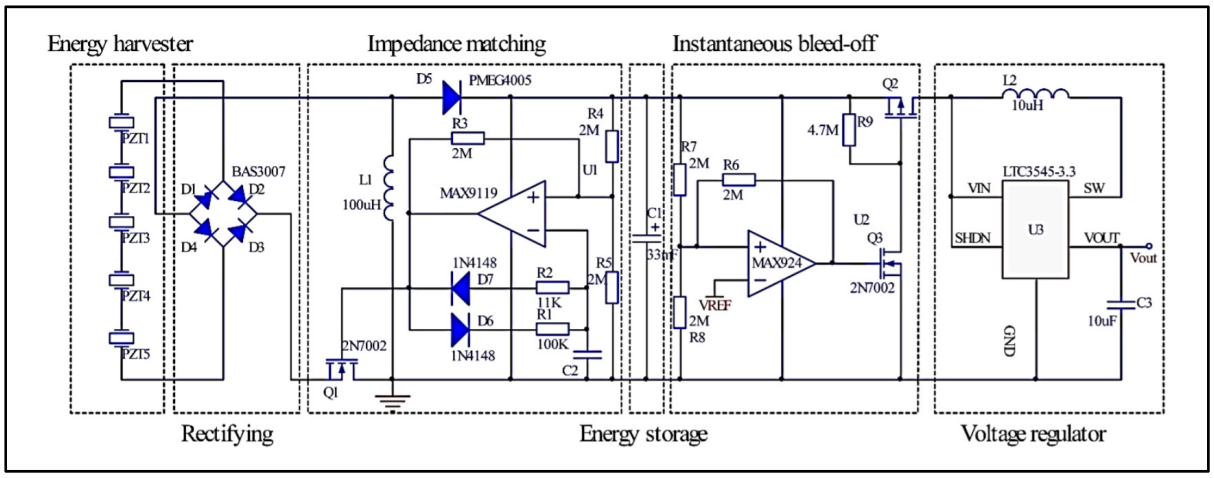


Figure 1.8 Power conditioning circuit
Taken from Yu et al. (2014)

1.6 Design Approach and Procedures

Apart from the previous literature survey, in this work designing an energy harvesting system follows an iterative process. The cycle can be summarized as follows: the best design architectures are identified to position the work within the state-of-the-art, followed by design implementations and simulations, then fabrication and testing. This is presented in the form of three manuscripts in chapters 2, 3 and 4. Chapter 5 and Appendix I compliment the work.

To perform the design choices and establish architectures, different kinds of harvesters including piezoelectric ones were investigated. Different electrode placements to allow for different modes of piezoelectric energy harvesting were studied. Complete information about their merits and demerits is gathered. In addition, the ways to fabricate and package state-of-the-art energy harvesters in which the process technology plays a vital role (e.g. cost, CMOS compatibility) is examined. This is used to establish key specifications that will be targeted at the system-level to define the performance metrics of the energy harvesters and power management circuit.

The designs and FEM simulations of the MEMS energy harvester structures are performed so that an accurate behavioral model is created using COMSOL Multiphysics and then implement the design using a commercial technology; specifically MEMSCAP PiezoMUMPs. MEMS fabrication technologies to implement the harvester are studied briefly as necessary to understand the micro-fabrication limitations. The extracted specifications of the harvester model are used to define the power management circuit targeted specifications.

A first MEMS harvester chip was submitted for fabrication at an early stage. Various T-shaped designs were investigated to verify resonance frequency and output power levels. This helped refine the simulation models. The PiezoMUMPs process used is a 5-mask level SOI patterning and etching process derived from work performed at MEMSCAP. In the fabricated chip, the piezoelectric layer AlN is sandwiched between the Si (below) and Al (top) on which the two metal pads have to be placed. The fabricated rectangular T-shaped MEMS harvesters were studied and tested and their performance was analyzed. The published results are presented in Chapter 2. Based on the performance metrics attained, improvements have been needed, models were revised and a second device was fabricated on trapezoidal T-shaped harvesters with results presented in Chapter 3. The advantages of T-shaped designs combined with an idea attempting to trench under the silicon and use the substrate as a mass resulted in the checkerboard designs. This third device was fabricated and the results are presented in Chapter 5. The test results were used to help verify the power management specifications and in creating the models of the system when needed.

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The fabricated MEMS chips have been tested. In general, a MEMS transducer is a device that converts mechanical stimuli (such as force) into an electrical signal (usually current) or vice versa. To characterize the MEMS resonance behavior, a vector network analyzer (VNA) has been used to measure the resonant frequency, bandwidth and the Q-factor. A vibration exciter is a machine which produces mechanical vibratory motion. The exciter produces a range of time dependent excitation force and displacement through a given range of frequencies. This machine was used to excite the MEMS resonator at its resonance frequency, and the maximum harvested voltage was monitored on an oscilloscope. In addition, a vibrometer has been used to measure the mechanical and electrical responses as a function of velocity.

Understanding diverse power conditioning methods (e.g. rectifying, DC/DC conversion, energy storage) which can be based on the harvester's output and comparing them based on the target specifications has been performed. This was extended to meet the requirements of MEMS electrostatic actuation. Furthermore, DC/DC conversion or charge pumps for MEMS electrostatic actuation has been studied. To support a wide multiple output voltage range, the switched capacitor converter should be reconfigurable. Referring to the literature is an ongoing process that has been revisited at every step to help position the work and mitigate problems.

Circuit level design and simulation was carried out in commercial integrated circuits technologies (0.13 and 0.35 μm CMOS) using the Cadence CAD environment. This included the design of the biasing integrated circuits for electrostatic MEMS (i.e. dc-dc converters or charge pumps) and the conditioning circuits for harvesters (i.e. ac-dc efficient circuits that can shape the ill-shaped output of the harvester into a stable low-noise DC bias). Layout and post layout simulations were performed and the first charge pump chip was fabricated. The fabricated chip was tested to extract performance metrics and determine improvements required. Results are published in Chapter 4. Based on the results from testing, more analysis was carried out and the charge pump circuit was improved. Second charge pump was designed, however the technology used was discontinued. The results are presented in Appendix I in the form of a conference paper. Then, a third chip, designed to be integrated with the checkerboard energy harvesters was fabricated. This chip included two rectifier versions of the power

management circuitry and also considered integration aspects which are important for the implementation of an integrated energy harvesting microsystem. Results as well are presented in Chapter 5.

To test the fabricated IC chips, they had to be packaged and wire bonded. For that a 48 pin QFN (quad-flat-no leads) package from Spectrum Semiconductors was considered. The bonding of the die in the package has to be carefully distributed to minimize parasitic interference. A test PCB is designed using Altium Designer software and fabricated to suit the testing needs. A socket was used to connect the packaged chip. The socket chosen from the Textool™ Series from 3M™, specifically an open top socket for 48 pin QFN applications. DC supplies were used to power the IC and sinusoidal and square wave signals were generated from the function generator to provide the signals. An oscilloscope was used to measure output voltages and the switching transients of the fabricated circuit and a digital voltmeter was used to monitor voltages throughout the testing process.

1.7 Conclusion

This chapter presented a literature review on MEMS energy harvesting and their power conditioning circuits. It also presented a few works on integrated harvesting systems. This propels the work in terms of design decisions and considerations. In each of the coming chapters, the literature review is considered in the front matter of each paper. The design approach and procedures followed in this work are briefly detailed in order to compliment the journal papers that are reproduced in chapters 2, 3 and 4.

CHAPTER 2

EFFECTS OF PROOF MASS GEOMETRY ON PIEZOELECTRIC VIBRATION ENERGY HARVESTERS

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Abstract:

Piezoelectric energy harvesters have proven to have the potential to be a power source in a wide range of applications. As the harvester dimensions scale down, the resonance frequencies of these devices increase drastically. Proof masses are essential in micro scale devices in order to decrease the resonance frequency and increase the strain along the beam to increase the output power. In this work, the effects of proof mass geometry on piezoelectric energy harvesters are studied. Different geometrical dimension ratios have significant impact on the resonance frequency, e.g., beam to mass lengths, and beam to mass widths. A piezoelectric energy harvester has been fabricated and tested operating at a frequency of about 4 kHz within the audible range. The responses of various prototypes were studied, and an optimized T-shaped piezoelectric vibration energy harvester design is presented for improved performance.

Keywords: Energy harvester, piezoelectric transducer, geometry, proof mass, resonant frequency.

2.1 Introduction

Piezoelectric energy harvesters present a solution to the power requirements of many devices, and can provide an alternative power source to batteries in a wide range of applications. For

instance, the research community has been investigating their use in implantable and portable electric devices due to their high output power density and energy conversion efficiency, suitability for miniaturization, and CMOS compatibility (Erturk et Inman, 2011). Micromachined piezoelectric vibrational energy harvesters have been reported in many applications such as medical energy harvesting (e.g. cardiac pacemakers), automotive applications (e.g., tire pressure monitoring systems), industrial applications, military applications, wireless sensor nodes, and many others (van Schaijk et al., 2013; Vullers et al., 2010a; Xu, Hansen et Wang, 2010; Yu et al., 2014).

However, the scaling down of these harvesters implies various design challenges in order to maintain sufficient power output and well-suited resonance frequencies to match those of ambient vibration sources that, depending on application, can be optimal below 500 Hz. For this purpose, researchers have been looking for new ways in optimizing harvester designs (Jia et Seshia, 2016a; Sriramdas et Pratap, 2017). In this work, the energy harvester designs presented operate over a range of resonant frequencies ranging from 2 to 5 kHz, and the effect of geometry variations on the resonant frequency of these devices is studied. This frequency range was selected as a trade-off between silicon area of the harvester designs and their resonant frequency in order to fabricate these devices in a commercial MEMS process. It is important to note that the results of this study can be scaled to lower frequency ranges if larger size piezoelectric energy harvesters are considered. In this case, the analysis and optimizations presented here would still apply and enable more efficient designs.

Many studies have been performed on piezoelectric energy harvesting, and models have been presented, notably for the cantilever geometry (Erturk et Inman, 2009; Miller et al., 2011). Some studies have focused on the impact of the position and geometry of the proof mass on the resonance frequency, however the mass has always been presented as a 3D proof mass placed on the tip of the harvester. In this work a different approach is presented, by considering the mass as a planar T-shaped cantilever. The main advantage with the mass being planar, is the reduction of the device thickness, and the simpler fabrication and assembly. This allows the use of commercial MEMS technologies which provide relatively precise control over the

structure dimensions in order to ensure optimal performance and repeatability. In this work, a study on the effects of the proof mass geometry on the resonance frequency is presented in order to reduce it and achieve the maximum amount of harvested energy. Finite element methods (FEM) simulations have been performed and analyzed to study effect of the beam width to length ratio, proof mass area, and proof mass to cantilever mass ratio, based on the measurement results of fabricated prototypes.

This paper is structured as follows: first, the operating principle of a piezoelectric harvester with a proof mass is detailed and then FEM simulation results are presented, followed by an optimized T-shaped design, the process flow for the fabrication technology, measurement results, and a conclusion.

2.2 Operating Principle of a Piezoelectric Energy Harvester with a Proof Mass

The MEMS piezoelectric energy harvesters studied here have the shape of a cantilever, clamped at one end and with a T-shaped proof mass attached at the free end, as depicted in Figure 2.1(a). The piezoelectric layer is sandwiched between two electrode layers and excited such that the d31 piezoelectric coefficient is used, yielding an induced voltage across the electrodes in response to strain along the beam axis. The model of vibrational resonant structures is similar to the traditional mechanical resonator (Beeby, 2015). External accelerations stemming from vibrations are transmitted to a suspended mass causing a relative displacement. The material, geometry and location of the proof mass affect the resonance mode and consequently the overall system performance. The lumped parameter model of a piezoelectric harvester would consist of a mechanical spring, K_m; an equivalent mass, M_{eq}; and a damper C_m as shown in Figure 2.1(b).

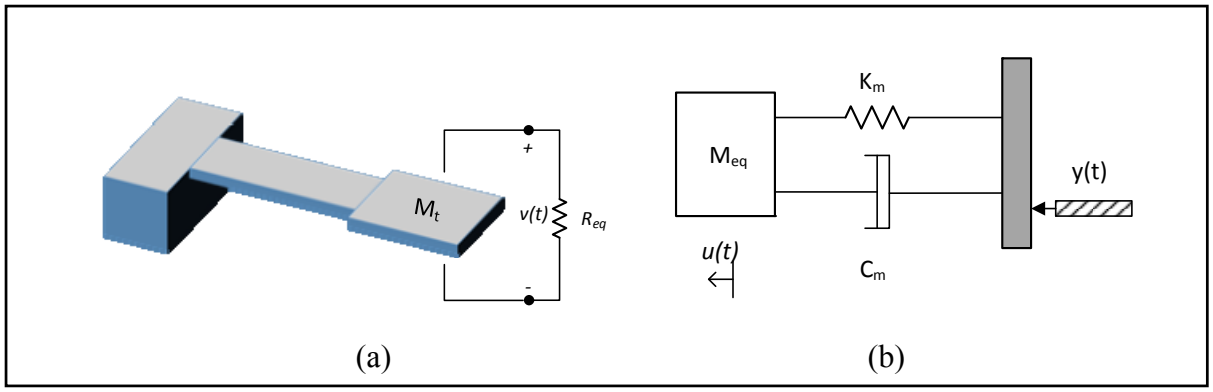

Figure 2.1 (a) Energy harvester; (b) mass-spring-damper model

Inertia based energy harvesters are reduced to a second-order spring-mass-damper system with equations based on Newton's second law:

$$f_{in}(t) = M_{eq}.a(t) \text{ or } F_{in}(jw) = M_{eq}.A(jw) \tag{2.1}$$

where M_{eq} is the equivalent mass, f_{in}, a, F_{in} and A are the force and acceleration in time and frequency domains, respectively. External vibrations of amplitude $y(t)$ are transmitted to a suspended mass causing a relative displacement $u(t)$. The harvester dynamics, based on the above equation to derive the mechanical domain equation with a single degree of freedom, can be represented by (Dompierre, Vengallatore et Fréchette, 2010):

$$M_{eq}\ddot{u}(t) + C_m\dot{u}(t) + K_m u(t) - \theta v(t) = -M_{eq}\ddot{y}(t)\mu \tag{2.2}$$

where K_m is the mechanical stiffness, C_m is the mechanical damping and Θv is the coupling force with Θ is the system coupling coefficient which is proportional to d_{31}. Both Θ and K_m depend on the geometry and strain distribution of the mode shape. All of these terms comprise mainly mechanical mode shapes and their derivatives (Miso et al., 2010). Thus, by changing the mass, the mode shape is altered affecting all of these effective constants. The material, geometry and location of a proof mass affect the modal analysis and consequently the analysis of the entire system. A correction factor μ has been added in (2.2) to evaluate the effect of the mass. Its value ranges from 1 with a large tip mass to 1.566 with no tip mass (Erturk et Inman,

2008). When the center of gravity of the tip mass has an offset to the end of the piezo beam, an improved and detailed modelling of piezoelectric power harvesters with proof mass offset can be found in (Lumentut et Howard, 2014). This can result in a more accurate expression of the mass matrix and dynamic force vector. This can provide a more practical design, which can avoid the use of material around the end of the piezoelectric length which can be damaged because of its brittle nature. In addition, note that the finite element equations proposed in (Lumentut et Howard, 2014) have been validated in (Lumentut et Howard, 2017).

The equivalent electrical circuit, shown in Figure 2.2(a), can be seen as a mechanical spring mass system coupled to an electrical domain through a transformer that converts a strain to current. In the mechanical domain, the input stress is represented by σ_{IN}, the mechanical mass by L_M, the mechanical stiffness by C_M and the mechanical losses by R_M. The piezoelectric coupling is modelled as a transformer, and C_P represents the electrical domain plate capacitor composed by the piezoelectric material (Roundy, Wright et Rabaey, 2012). At resonance, the whole circuit can be transposed to the electrical domain. In the electrical domain, the cantilever based piezoelectric harvester can be modelled as a current source in parallel with a parasitic capacitor and parasitic resistor as illustrated in Figure 2.2(b). Applying Kirchhoff circuit laws to the equivalent electrical circuit to determine the electrical domain equation yields:

$$\theta\dot{u}(t) + C_P\dot{v}(t) + \frac{V(t)}{R_{eq}} = 0 \tag{2.3}$$

where $\theta\dot{u}$ is the current, v is the voltage and R_{eq} is the external load.

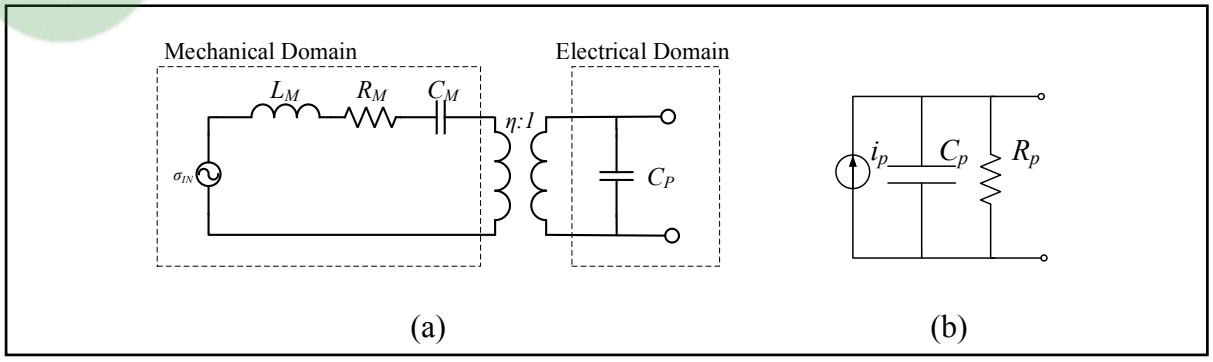

Figure 2.2 Piezoelectric harvester (a) coupled model and (b) uncoupled model

The natural frequency of a spring mass system, considering a stiffness K, is expressed as:

$$\omega_n = \sqrt{\frac{K}{M_{eq}}} \tag{2.4}$$

where K varies depending on the structures. For a cantilever beam, $K = 3EI/L^3$ where E is Young's modulus of elasticity, I is the moment of inertia and L is the length of the beam. E is the ratio of stress to strain while I depends on the beam width and thickness.

If the harvester is driven by a harmonic base excitation $y(t) = Ysin(\omega t)$, then the inertial mass M_{eq} moves and the mechanical power which is to be converted to electrical power by the piezomaterial is given by (Roundy, Wright et Rabaey, 2012):

$$P_m = \frac{M_{eq}\zeta Y^2 \left(\frac{\omega}{\omega_n}\right)^3 \omega^3}{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + \left[2\zeta\left(\frac{\omega}{\omega_n}\right)\right]^2} \tag{2.5}$$

where ζ is the damping ratio. For maximum energy conversion efficiency, the driving frequency of the harvester, ω, has to match its resonance frequency, ω_n. The maximum output power occurs at $\omega = \omega_n$, and is given by (Roundy, Wright et Rabaey, 2012):

$$P_{max} = \frac{M_{eq}Y^2{\omega_n}^3}{4\zeta} \tag{2.6}$$

Maximizing the power by operating at the natural frequency emphasizes the selection of piezomaterial and dimensions. The power delivered is proportional to the inertial mass. While the damping affects the Q-factor and bandwidth of the harvester, any variation in the excitation frequency results in a sharp drop-off in the power harvested. Note that (2.5) and (2.6) do not consider the effect of the piezomaterial on the output power. This depends on the energy transduction of the strain across the piezomaterial. It has been shown in (Roundy, Wright et

Rabaey, 2012) that the output power depends on the strain experienced in the piezoelectric layer, its dimensions, and its piezoelectric coefficient.

2.3 Simulation Results

The MEMS energy harvester features a central beam that is connected to a proof mass. The design has six design degrees of freedom, namely, the beam length (Beam_L), the beam width (Beam_W), the beam height (Beam_H), the mass length (Mass_L), the mass width (Mass_W), and the mass height (Mass_H), as illustrated in Figure 2.3. When the beam height equals the mass height, a planar T-shape is achieved. Eigen frequency simulation through COMSOL Multiphysics was used to assess the effect of varying these variables on the device performance.

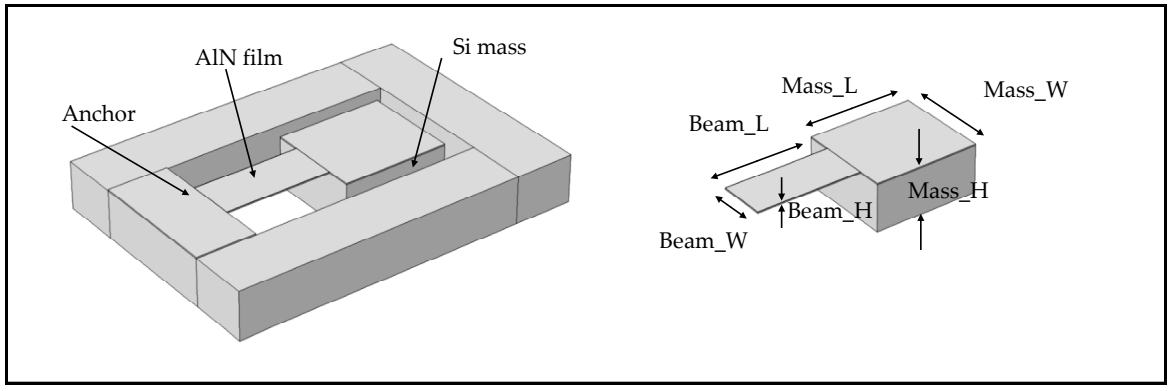

Figure 2.3 T-shaped harvester with the representation of the dimensions

In order to get the most accurate results, a model has been created in COMSOL in which a triangular swept mesh was used. In order to compare the results between experimental and simulation results, the beam was anchored to the surrounding silicon substrate and an air bubble around the device was used to take into consideration air damping effects. The structures were fabricated in a commercial MEMS technology: PiezoMumps from MEMSCAP. For this reason, the studies were limited to the structures that could be realized using this process. Therefore, a limitation on the values of the parameters, due to the fixed thicknesses of the materials used, has been considered. The value of Beam_H has been defined

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as 10 µm, and Mass_H can only take two different values 10 µm or 400 µm, the latter possible if the handle portion of the substrate is kept below the T-shaped mass. The piezoelectric material used is aluminum nitride (AlN). The design variations in the dimension ratios of the mass length to the beam length and the mass width to the beam width is illustrated in Figure 2.4.

2.3.1 The Effect of Beam_L and Mass_L over a Structure of a Fixed Length

In a set of simulations, the total length of the structure (Structure_L = Beam_L + Mass_L) and thickness (Beam_H and Mass_H) of the silicon structure are kept to 1700 µm and 10 µm, respectively. The length of the mass to length of the structure ratio (Mass_L / Structure_L) is varied from 0.01 to 0.98 by setting Mass_L from 20 to 1680 µm. Beam_W is selected to be half of Mass_W which makes their values 300 µm and 600 µm, respectively. The total area of the proof mass (Mass_L * Mass_W) changes from 0.012 mm^2 to 1.008 mm^2, while the total area of the beam (Beam_L * Beam_W) changes from 0.504 mm^2 to 0.006 mm^2. This results in a ratio between the surface areas of the mass and the beam varying from 0.02 to 168, and the active area to available area ratio varying from 50.4% to 99.7%. These changes allowed for a reduction of 1.2 kHz on the value of the fundamental mode frequency as shown in Figure 2.5(a).

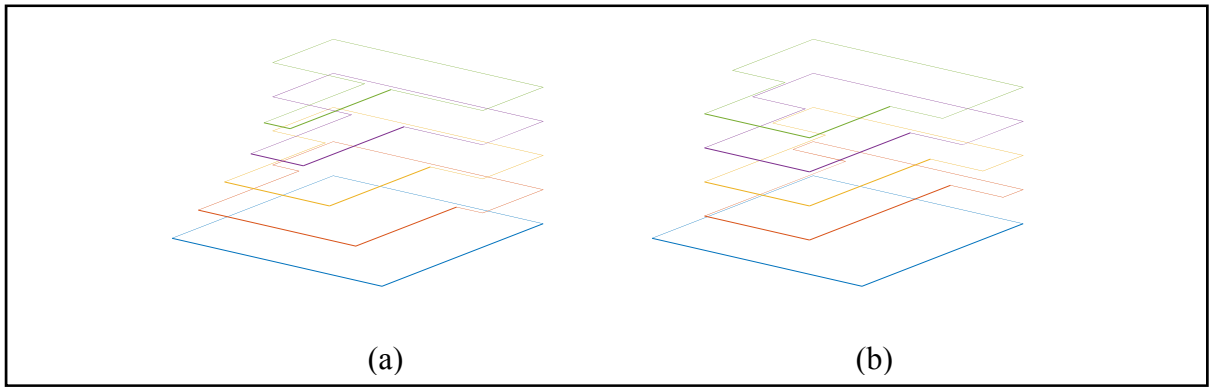


Figure 2.4 Overlay illustration of the variation of ratio of (a) the mass length (Mass_L) to the beam length (Beam_L) and (b) the mass width (Mass_W) to the beam width (Beam_W)

Another set of simulations was carried-out with the following parameters: the total length of the structure (Structure_L) and thickness (Beam_H and Mass_H) of the silicon structure are kept to 2000 µm and 10 µm respectively. The length of the mass to length of the structure ratio (Mass_L / (Mass_L + Beam_L)) changes from 0.01 to 0.99 by setting Mass_L from 20 to 1980 µm. Beam_W was chosen to be equal to half of Mass_W (i.e., 400 µm and 800 µm respectively). As a result, in that case, the total area of the proof mass (Mass_L * Mass_W) changed from 0.016 mm^2 to 1.584 mm^2, while the total area of the beam (Beam_L * Beam_W) changed from 0.792 mm^2 to 0.008 mm^2, therefore changing the surface mass to surface beam ratio from 0.02 to 198. Consequently, the ratio of surface used to available surface went from 50.5% to 99.5%. These changes allowed for a reduction of 0.9 kHz of the first Eigen frequency, as shown in Figure 2.5(b).

Both these sets of simulations show that the lowest frequency is obtained when the length of the beam to length of the structure ratio is equal to 0.5. When the length of the beam is equal to the length of the mass, the best result is obtained. Moreover, the results are almost symmetric, for e.g. if the length of the mass to length of the structure ratio is equal to 30% or 70%, similar results are attained.

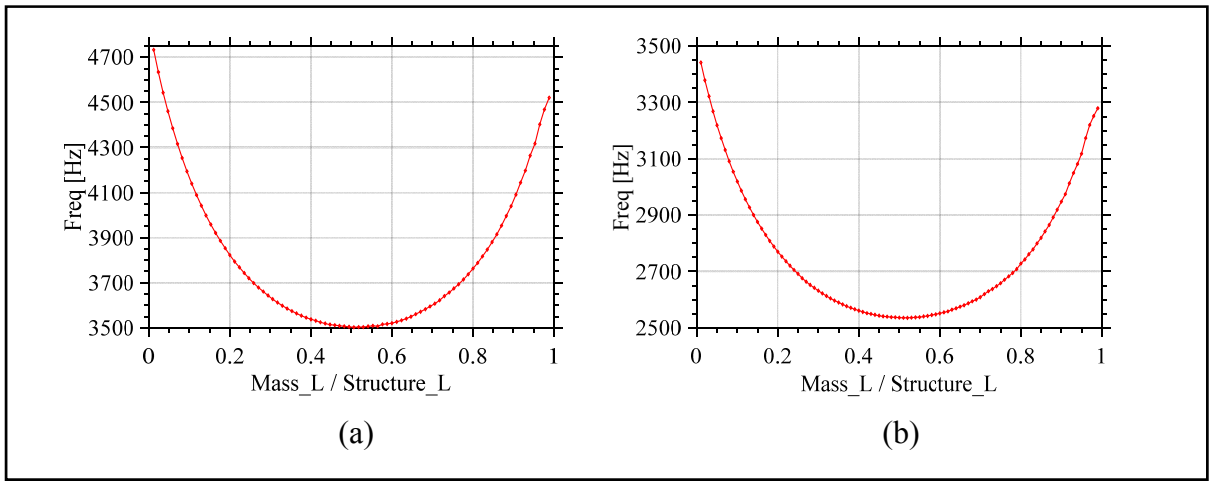


Figure 2.5 Effects of the variation of ratio of the mass length (Mass_L) to the total structure length (Structure_L) on the value of the first Eigen frequency for structure length of (a) 1700 µm and (b) 2000 µm

The variation of the ratio of the length of the mass over the total length of the structure allows for a reduction in the resonant frequency of the design. However, this reduction depends on other parameters, and the effect of a variation of Beam_W and Mass_W was investigated as well.

2.3.2 The Effect of Beam_W / Mass_W

In this set of simulations, the total length of the structure (Structure_L) and thickness (Beam_H and Mass_H) of the silicon structure are kept to 1700 μm and 10 μm, respectively. The length of the mass to length of the structure ratio (Mass_L / Structure_L) is varied from 0.01 to 0.98 by setting Mass_L from 20 to 1680 μm. Regarding the value of Mass_W, it was kept at 600 μm while using the value of Beam_W to explore different ratios for Beam_W / Mass_W such as 1/6, 1/3, 1/2, 2/3, 5/6, and 1, which results in Beam_W values of 100, 200, 300, 400, 500, and 600 μm, respectively. These different ratios allow a reduction of up to 2.2, 1.7, 1.2, 0.7, 0.3, and 0 kHz, respectively. The maximum reduction is reached when the length of the beam represents half of the total length of the structure for each given Beam_W, as seen in Figure 2.6(a).

A second set of simulations was carried out with once again different values for the Beam_W/Mass_W ratio. The total length of the structure (Beam_L + Mass_L) and thickness (Beam_H and Mass_H) of the silicon structure are kept to 2000 μm and 10 μm respectively. The length of the mass to length of the structure ratio (Mass_L/Mass_L + Beam_L) changes from 0.01 to 0.99 by setting Mass_L from 20 to 1980 μm. The value of Mass_W was chosen to be equal 800 μm while using the value of Beam_W is varied to explore different ratios for Beam_W/Mass_W such as 1/8, 1/4, 3/8, 1/2, 5/8, 3/4, 7/8 and 1 so respectfully 100, 200, 300, 400, 500, 600, 700 and 800 μm. These different ratios allow a reduction of up to 1.7, 1.4, 1.1, 0.9, 0.6, 0.4, 0.2 and 0 kHz respectively. The maximum of the reduction is reached when the length of the beam represents half of the total length of the structure, as seen in Figure 2.6(b). Table 2.1 summarizes the above simulations as a percentage frequency reduction corresponding to beam width to mass width percentage.

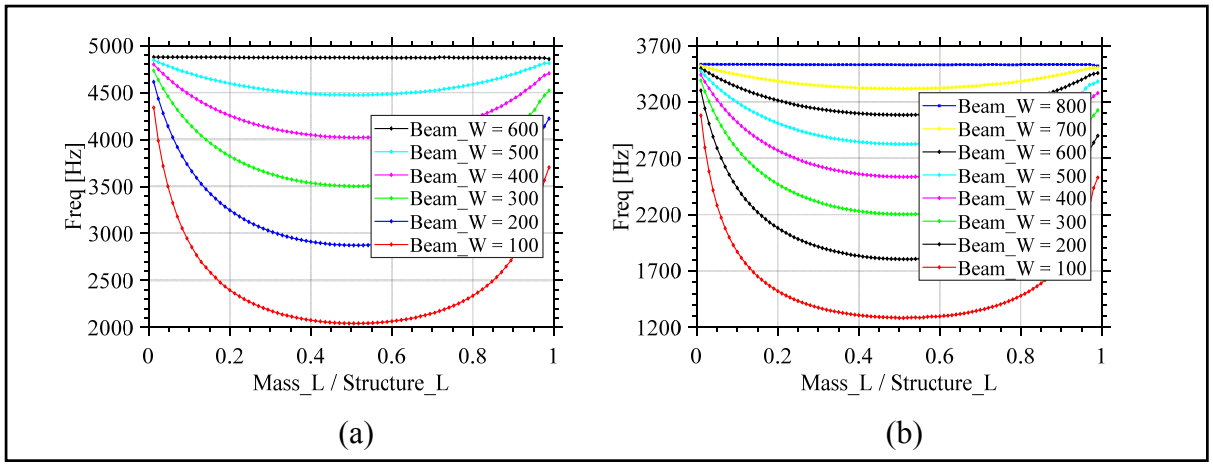


Figure 2.6 Effects of the variation of ratio of the mass length to the total structure length on the value of the first Eigen frequency for different Beam_W / Mass_W ratios, while conserving a total structure length of (a) 1700 µm and (b) 2000 µm

According to the data presented, there is no optimal geometry stemming from reducing the beam width. However, while reducing the beam width allows for a reduction in the resonant frequency of the structure, this also reduces the surface available on which the piezoelectric material will be deposited, impacting output power. The structural integrity of the realized structure is also affected by reducing the beam width. Note that the targeted first out-of-plane flexural mode of the T-shaped device is of interest in this work. This mode is typically at a lower frequency than the torsional mode. However, the scaling down of the beam width can lower the torsional mode resonance frequency so that it overlaps or interferes with the targeted resonance operation. This should be considered in the device design when reducing the beam width, in addition to considering fracture and the reduced piezoelectric area.

Table 2.1 Summary of the Effect of Beam_W / Mass_W on the Resonant Frequency

Beam_W / Mass_W (%)	12.5	25	37.5	50	62.5	75	87.5	100
Reonant frqeuency reduction[1] (%)	48	40	31	25	17	11	6	0

[1] Beam_L = Mass_L

When combining the two effects, it is noticed the change in frequency due to changing the Mass_L / Structure_L ratio is less significant when the width of the beam is near that of the mass, as seen in Figure 2.6.

2.3.3 Addition of a Proof Mass Using the Wafer Substrate

The impact of using the silicon wafer substrate as a proof mass to increase the mass depth was studied by performing similar simulations with a 400 µm-deep proof mass located under the mass portion of the structure. This allows a further reduction of the value of the resonant frequencies. As seen in Figure 2.7, a ratio of 0.5 between the length of the mass and the length of the structure still provides the best operating point. However, the change in frequency will be negligible from a Mass_L / Strucure_L ratio of 0.3 to 0.7 in comparison to the reduction in frequency observed when this ratio changes from 0 to 0.3 or from 1 to 0.7.

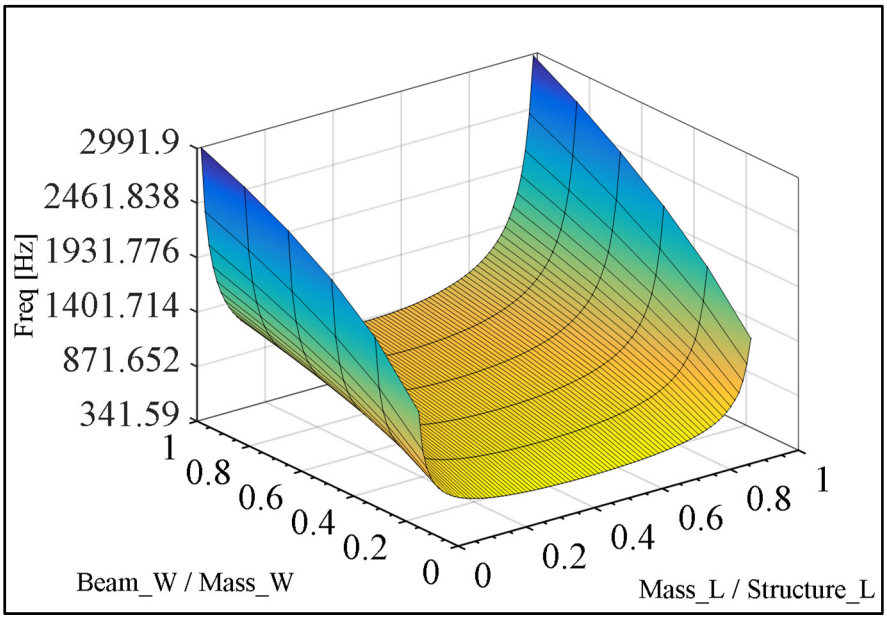


Figure 2.7 Effects of the variation of the Mass_L / Structure_L ratio on the value of the first Eigen frequency for different Beam_W / Mass_W ratios. Note that here the wafer substrate is used as a proof mass

2.3.4 Addition of a Fixed-Area Mass

If a fixed-area mass is to be added to the cantilever in order to lower the resonant frequency, then once again the mass geometry has to be studied carefully. For this set of simulations, the length (Beam_L), width (Beam_W) and thickness (Beam_H and Mass_H) of the silicon structure are set to 2000 µm, 500 µm and 10 µm respectively. To this beam, a mass is added, having a constant surface area of 1 mm2. Figure 2.8 shows the effect of adding a mass which will result in a range of possible frequencies depending on the mass geometry, namely mass length and width, while keeping height constant. When the mass length is longer, and consequently the mass width shorter, the resonance frequency is reduced. Note that, based on Figure 8, one can conclude that the addition of a proof mass of given area must be carried-out by carefully selecting the mass geometry in addition to the beam geometry.

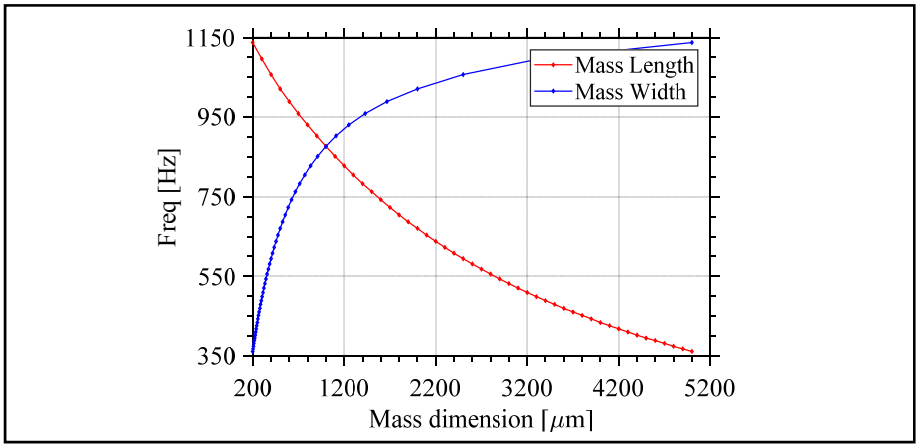


Figure 2.8 Effects of varying the length or the width of a constant-area (1 mm^2) mass on the value of the first Eigen frequency of the structure

2.3.5 Discussion

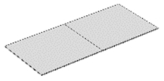
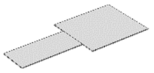
As a result of the study of the effects of the geometry of the mass, the following conclusions are noted: i) If the substrate is not used to increase the mass, a beam length that is equal to the mass length will yield the lowest resonant frequency. ii) If the substrate is added to the proof mass, then if the length of the mass is between 30 to 70% of the total structure length, the

lowest resonant frequency will be attained. iii) In both cases, the ratio of the beam width over the mass width must be kept as small as possible in order to maintain a low resonant frequency, keeping in mind that the reduction of beam width will also reduce the harvested power, because of limited piezoelectric area. iv) Finally, care must be taken when considering a fixed mass geometry as this will result in a range of resonant frequencies (i.e., the longer its length, and consequently the shorter its width, the lower the resonant frequency).

2.4 T-shaped Optimized Design

Based on the conclusions reached from the simulation results, an optimized T-shaped design is proposed. To compare the effects of the change in mass geometry, a rectangular cantilever beam will be used as a comparison point. All the dimensions are presented in Table 2.2. The T-shaped design will follow the recommendations in considering a mass of the same thickness as the beam, a mass length equals to that of the beam, and a narrow beam width (within the laminations of the process technology). COMSOL frequency domain simulations were used to analyze output power as a function of the vibration frequency, with a given electrical load and the harmonic acceleration amplitude.

Table 2.2 Proposed Design Parameters

Design	L_B (μm)	W_B (μm)	H_B (μm)	L_M (μm)	W_M (μm)	H_M (μm)	Freq (Hz)	
Rectangular (reference)	900	800	10	900	800	10	4355	
T-shaped (optimized)	900	300	10	900	800	10	2710	

The first Eigen frequency of the T-structure is of 2710 Hz. The reference beam structure has a resonant frequency of 4350 Hz. Therefore, the proposed structure allows a reduction of 1640 Hz in resonant frequency. Figure 2.9(a) and (b) show the output voltage and power for both designs. Here, an acceleration of 1 g along the z-axis and a resistive load of 100 kΩ are used in the simulations. The at-resonance voltage difference in the two designs of 69 mV (beam

design) and 146mV (T-shaped design) translates to an output power of 24 nW for the reference beam design to 107 nW for the optimized T-shaped design. The output power at resonance, for both designs versus the acceleration is depicted in Figure 2.9(c), for a load of 100 kΩ. For instance, at an acceleration of 5g, the T-shaped design has an electric power output of about 2.5 µW compared to 0.5 µW for the cantilever, an improvement by a factor of 5. The output voltage as a function of the electrical load resistance at a harmonic acceleration amplitude of 1g at the resonant frequency of the devices is shown in Figure 2.9(d). The T-shaped designs outputs more voltage at a given load and can sustain a smaller load resistance. This information can be used for the selection of a power conditioning circuit such that its load on the harvester is optimal.

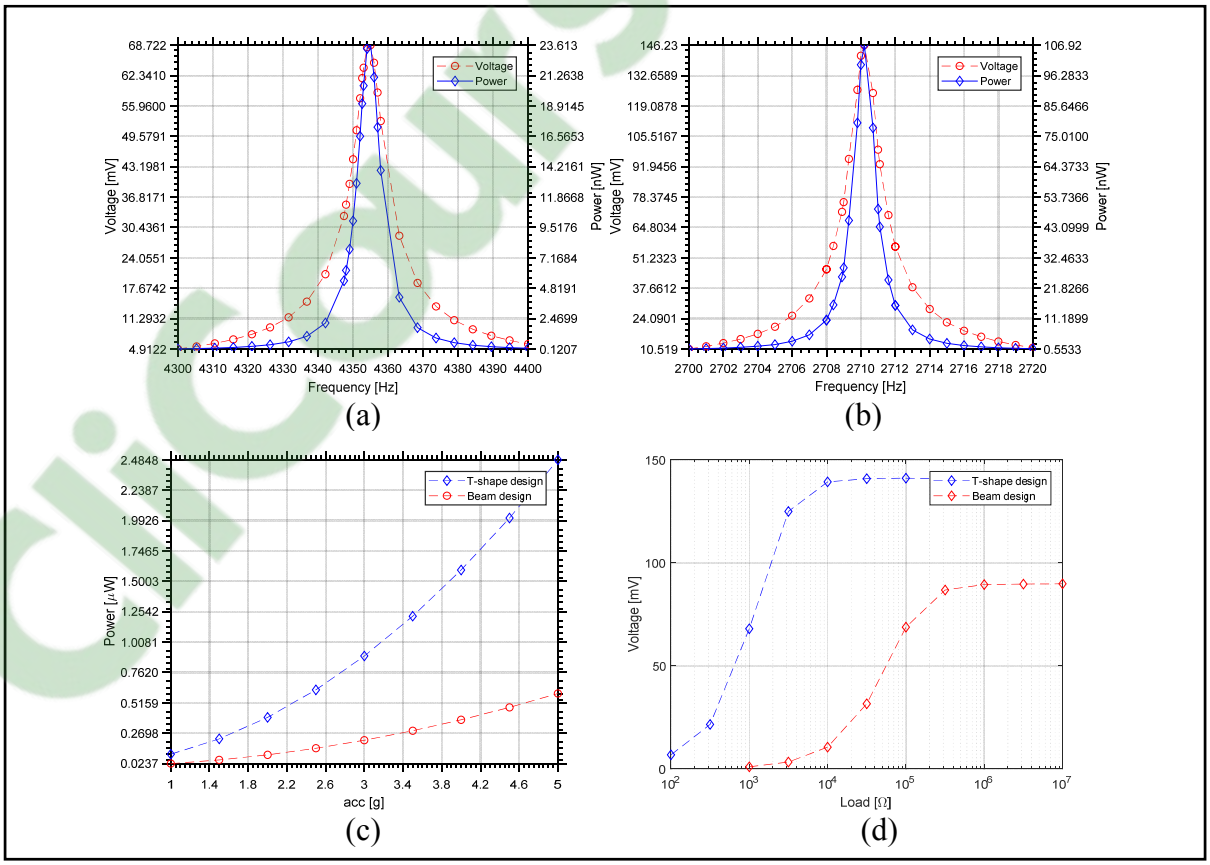


Figure 2.9 Simulation of the frequency response of the proposed design without using the substrate as a proof mass: (a) output voltage and power of the reference beam design, (b) output voltage and power of the T-shaped optimized design, (c) output power of the designs vs. acceleration, and (d) output voltage vs. resistive load value for both designs

While the T-shaped design proposed occupies smaller area than the reference beam design, it compares favorably and features various advantages, namely a lower resonant frequency, increased voltage and power output for a similar acceleration, and support for a smaller load resistance at a given acceleration. Accordingly, it is important to carefully dimension a cantilever-based energy harvester to ensure that the harvested power is optimal for a given available area.

2.5 Fabrication Process and Designs' Dimensions

The T-shape prototype designs were fabricated using the PiezoMumps process from MEMSCAP. PiezoMUMPs is a piezoelectric-based MEMS process that provides cost-effective access to MEMS prototyping. The fabrication process includes a 5 mask layer etching and patterning process briefly outlined in Figure 2.10 and has been detailed in (Cowen et al., 2014). The process is carried out on an N-type double-side polished silicon-on-insulator (SOI) wafer, used as the starting substrate (Figure 2.10(a)). First, the 10 µm silicon layer is doped using a phosphosilicate glass layer (PSG); that is deposited and then removed by wet etching; to increase its conductivity. Then, a layer of silicon dioxide is patterned on the SOI wafer (Figure 2.10(b)). The silicon device layer is connected to the electrical ground and the 0.2 µm oxide isolates the signal pads from the ground plane (Figure 2.10(c)). A 0.5 µm thick layer of piezoelectric aluminum nitride (AlN) is then deposited and patterned (Figure 2.10(d)). A 1.02 µm metal stack of 20 nm-thick chromium (Cr) for adhesion and 1 µm aluminum (Al) is deposited to form the electrical interconnects and the pads (Figure 2.10(e)). Lastly, the 400 µm substrate is etched from the backside to form release trenches (Figure 2.10(f)). Note that a portion of the substrate can remain below a given portion of the cantilever if the mask geometry is designed accordingly.

The SEM micrographs of two of the fabricated devices, labelled Design 1 and Design 2, are shown in Figure 2.11. These fabricated designs were conceived in order to better characterize and model this vibrational piezoelectric energy harvester geometry. As such, the dimensions of the fabricated devices are presented in Table 2.3. In order to achieve higher energy outputs, interdigitated electrode designs have been proposed in the literature (Caliò et al., 2014; Li,

Tian et Deng, 2014), in which an array of narrow positive and negative electrodes are placed on the piezoelectric surface when it is fabricated. The fabricated structures are such that Design 2 is interdigitated while Design 1 is not. It can be noticed that the intrinsic stresses in the thin films are responsible for the out-of-plane upwards bending behaviour. This stems from the difference between the intrinsic stress of the deposited thin films and the crystalline silicon structure that has very low intrinsic stress. This deformation was not observed to have a significant impact on the resonant frequency of the devices characterized in this work as measurements of identical structures showed a good stability of the resonance frequency between devices and a close match to the results obtained in simulations.

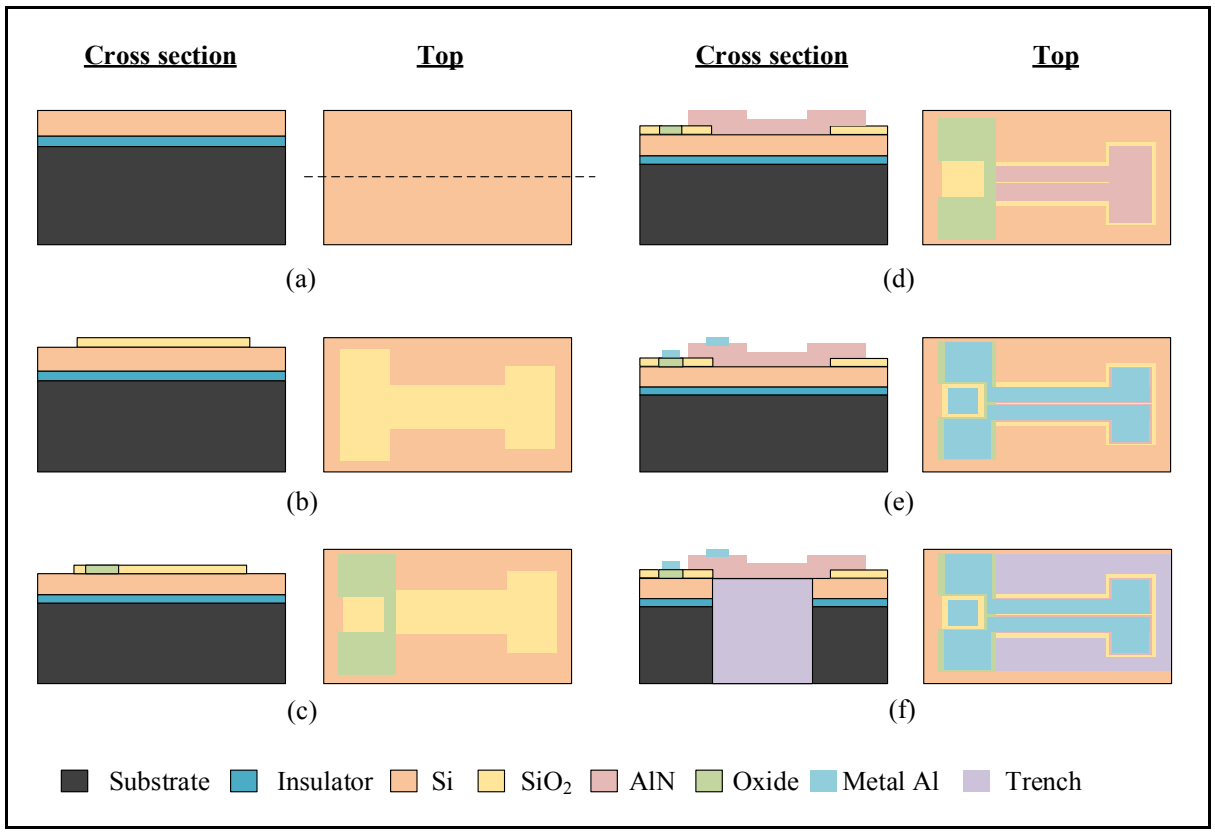


Figure 2.10 Overview of the PiezoMUMPs fabrication process flow

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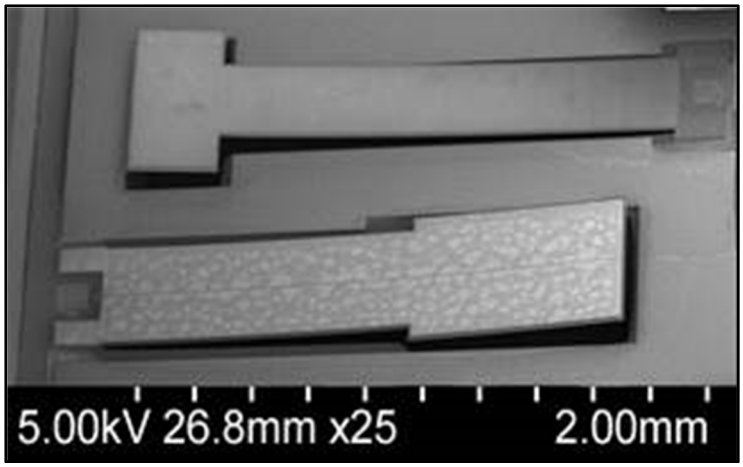


Figure 2.11 SEM micrograph of the fabricated harvesters Design 1 (bottom) and Design 2 (top)

Using FEM simulation, these devices have been recreated and simulated to extract their expected resonant frequencies and frequency response to a z-axis acceleration. The experimental data stemming from these designs allowed to tune the model in order to get a more accurate simulation of these designs. This was done by optimizing the material properties, anchoring, meshing and damping of the FEM model. While the model allowed to get an accurate representation of the behavior of the system, the variations of the process accounted for a resonant frequency variation of up to 4.5%, if only Design 1 and Design 2 are considered. The value of that acceleration and of the damping of the surrounding air have been set to match the measurements made on the physically realized structures during the development of the model. This ensures that the extracted Q-factor from simulation matches that of the measurements.

Table 2.3 Fabricated Design Parameters

Design	L_B (μm)	W_B (μm)	H_B (μm)	L_M (μm)	W_M (μm)	H_M (μm)	Simulated Resonant Frequency (Hz)
Design 1	1000	400	10	700	500	10	4397
Design 2	1500	325	10	300	600	10	3591

2.6 Measurement Results

To test the fabricated prototype devices and acquire experimental data, the following process has been followed. The first step was to study the Eigen frequencies of the structures using COMSOL in order to gain insight into the expected resonance frequency of the devices. Then, using a vector network analyzer (VNA), Model E5061B from Keysight, the value of the resonant frequencies were measured. The block diagram of the test setup is shown Figure 2.12, while the experimental test setup is shown in Figure 2.13.

The two designs are such that the mass length is larger than the width in Design 1 while the mass width is larger than the length in Design 2. The average measured resonance frequency of Design 1 is of 4.6 kHz and that of Design 2 is 3.5 kHz. It is worth noting that the fabrication process is responsible for a small variation of the resonant frequencies of the devices from simulations, even after model tuning.

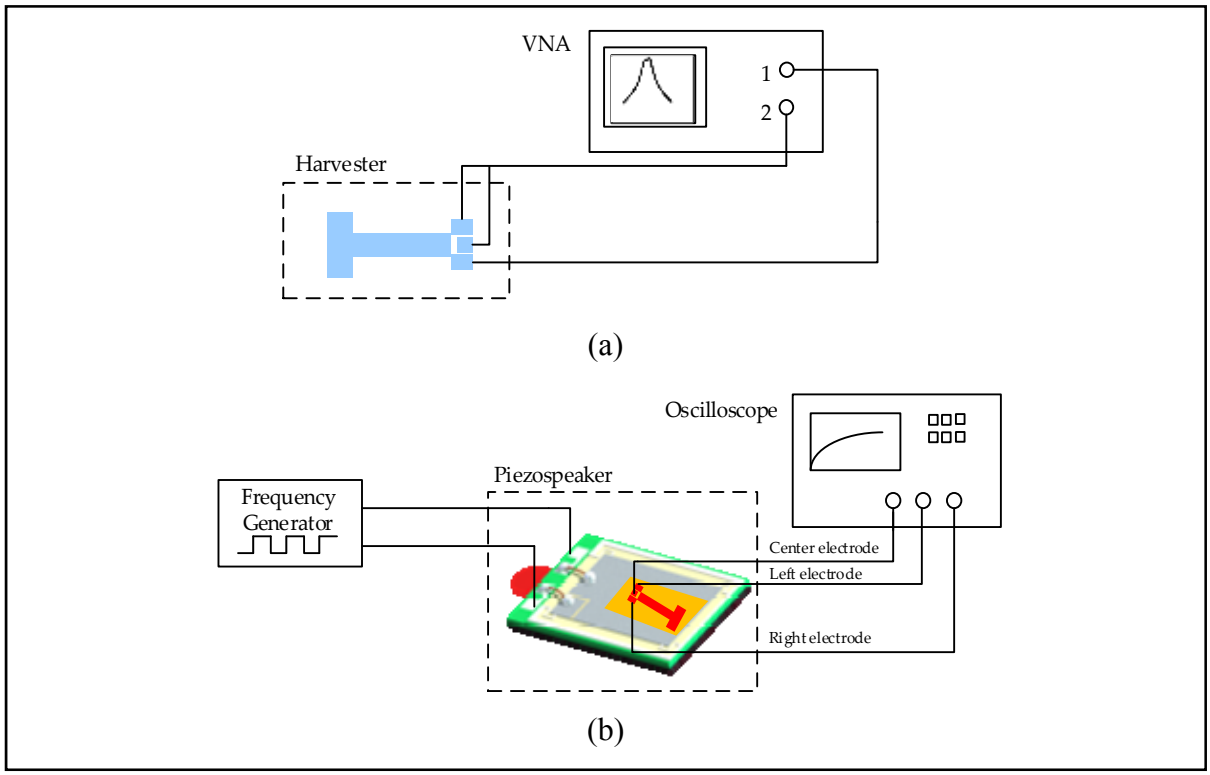
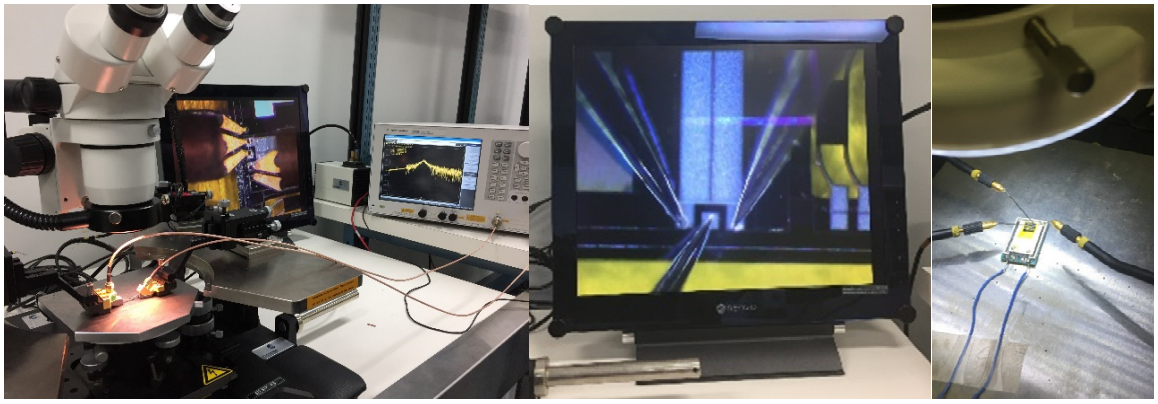


Figure 2.12 (a) Resonance test setup and (b) output power test setup



(a) (b) (c)

Figure 2.13 Photos of (a) the experimental test setup (b) the device with the electrical probe tips, and (c) the piezospeaker setup with the device under test attached to it

As mentioned earlier, Design 2 is interdigitated while Design 1 is not. However in measurements no significant differences have been noticed, thus electrical tests focused only on Design 1. The output response of Design 1 measured with the VNA is shown in Figure 2.14, outlining the resonance frequency, bandwidth and the Q-factor. The bandwidth is measured to be about 63.3 Hz with a resonant frequency of 4.6 kHz and quality factor 72.7. The damping ratio is calculated to be $\zeta = 1 / 2Q = 0.007$. Note that the characterization of the damping in such a system can be complex. For further information, a more detailed overview on damping characterization is presented in (Lumentut et Howard, 2014).

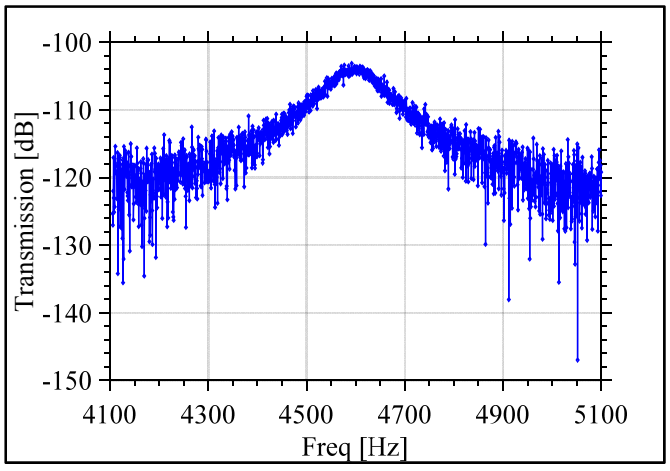


Figure 2.14 Measured frequency response of Design 1

A piezo-speaker has been used to characterize the power output of this device providing a cost effective method of testing. Piezo speaker APS2509S-T-R from PUI Audio was used (Audio), on which the devices were taped using kapton tape to generate the frequencies needed to measure their frequency response. This piezo speaker, has a frequency range from 300 Hz to 20 kHz, therefore the tests were limited to excitation frequencies below 20 kHz. The mechanical motion of the piezo speaker is used here to vibrate the harvester device. In order to measure the voltages generated, probes connected directly to an oscilloscope without using an impedance matching circuit were used. The oscilloscope has been used as a load in this measurement.

The response of the system when subjected to a sinusoidal excitation at a given frequency was characterized. An accelerometer from PCB Piezotronics (model 352C65) was used to quantify the acceleration of the piezo speaker. The sinusoidal excitation of the piezo speaker has an amplitude of 10 V and a frequency 4350 Hz. This resulted in an acceleration 8.4g of the piezo speaker, and the generated power across the 1 MΩ oscilloscope load was measured to be 62 nW. The output voltage for the left, right and center electrodes are shown in Figure 2.15. The left and right outputs expectedly show near identical responses. When combined, these outputs yield a maximum output voltage of 252 mVp-p.

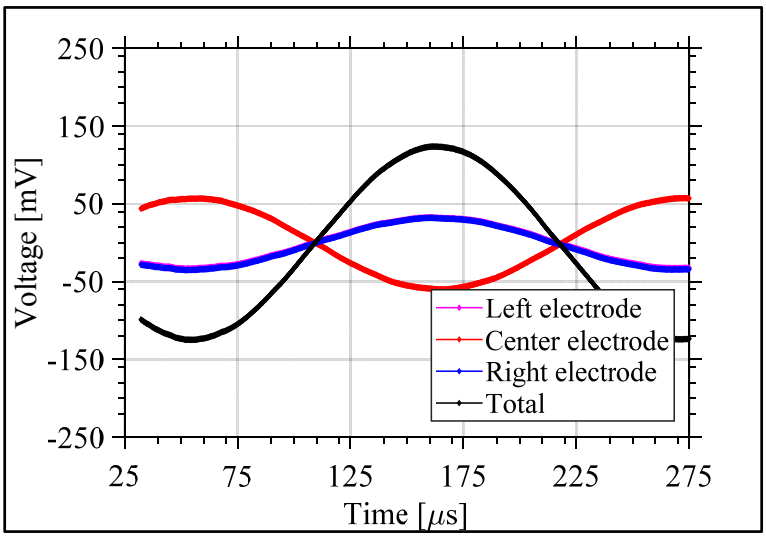


Figure 2.15 Output voltage of Design 1 in response to harmonic excitation at each electrode, along with the total combined output

Figure 2.16(a) shows the output voltage corresponding to three input vibrations of different amplitudes and their corresponding simulations. As can be seen, the simulation results are in good agreement with the measurements. The piezo speaker used has a maximum input of 16 Vp-p, however a limitation of 10 V max was imposed by the function generator used (Keysight 3320A function generator). The three input voltage amplitudes used on the piezo speaker are 5, 7.5 and 10 V. Figure 2.16(b) shows the generated voltages of three different dies of the same design outlining the process variation in terms of performance with an excitation voltage amplitude of 10 V with respect to simulation results, also showing a good correspondence with the measurements. Based on the measurement data received, the models had been revisited and optimizations had been performed for more accuracy in the fabrication of the prospective designs.

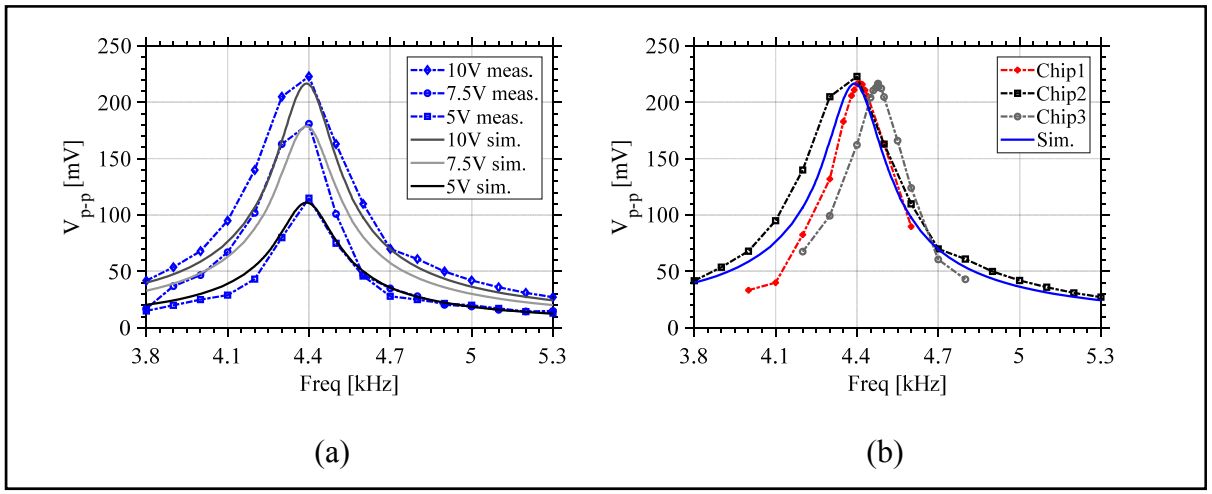


Figure 2.16 (a) Measured output voltage of Design 1 while varying the piezo speaker excitation voltage, and (b) variation between different dies of Design 1

2.7 Conclusion

In this paper, a study on the effects of the geometry on piezoelectric energy harvester characteristics was presented. As discussed, improvements to the geometry of the harvester has an impact on the performance, in which dimension ratios have to be chosen carefully for optimal design performance. A study on T-shape harvesters has showed that the lowest

frequency can be achieved when the length of the mass to the length of the structure ratio is 0.5, while keeping the beam width to mass width as small as possible.

An optimized T-shape design was proposed, and measurement results from prototypes used to validate the simulation model used to design the optimized T-shape device were presented. The optimized design stemming from the measured prototypes, simulation model and study presented in this paper will be implemented for characterization and will then be integrated with a power conditioning circuit. While this study has allowed for device dimensions that lower the resonant frequency and increasing the output power, this can be further optimized by applying the technique to other beam geometries (e.g., (Roundy et al., 2005)). Future work will investigate such structures in order to further increase the harvested power and lower the resonant frequencies within the 100 Hz to 1 kHz range.

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Author Contributions: A.A. and M.E. designed the devices. A.A. and M.G. designed the test setups and performed the experimental testing. M.E. and F.N. supervised the work and provided expertise. All authors contributed to the writing of the paper.

Conflicts of Interest: The authors declare no conflict of interest.

CHAPTER 3

IMPACT OF GEOMETRY ON THE PERFORMANCE OF CANTILVER-BASED PIEZOELECTRIC VIBRATION ENERGY HARVESTERS

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Abstract:

This paper aims at comparing micromachined cantilever structures with the purpose of providing design guidelines towards high performance energy harvesters such that they provide a good output power, resonant frequency and volume trade-off, while considering microfabrication process limitations. Increasing the power output of piezoelectric energy harvesters by tapering the beams has been presented as promising solution in the literature. This paper investigates the power output of several geometric variations of cantilever beams, and examines the advantages of balancing the strain distribution throughout the beam. A comparison of the impact of different geometries is presented, and recommendations are given. Namely, eight rectangular and trapezoidal T-shaped designs are fabricated and benchmarked. Their resonant frequencies and power outputs are compared for the same available area (1800 μm× 800 μm). Measurements show that the trapezoidal designs can have a higher output power depending on the beam length to mass length ratio, in comparison to the rectangular T-designs that have lower frequencies. Resonant frequencies ranging from 2.9 to 7.2 kHz and power outputs ranging from 2.2 to 7.1 nW are reported.

Index Terms: Vibration energy harvesting, piezoelectric, transducer, cantilever, geometry, resonant frequency, strain, output power.

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3.1 Introduction

Energy harvesting based on vibration is of interest in a wide range of sensing applications, ranging from powering structural health monitoring sensors to powering tire pressure sensors. Cantilever piezoelectric vibration energy harvesters are among the most common designs used (Jia et Seshia, 2016a; Liu et al., 2011; Marzencki, Defosseux et Basrour, 2009), despite many different energy harvesting techniques studied in the literature (Beeby et al., 2007; Vullers et al., 2010a). The use of piezoelectric materials has been favored because of their relatively good energy density and conversion efficiency when subjected to small displacements, their suitability for miniaturization and their potential for CMOS integration (Aktakka et Najafi, 2014; Caliò et al., 2014; Kim, Priya et Kanno, 2012). Different factors characterize the harvesters' performance, among which responding to the right frequency and efficiently generating the maximum output power within a given device volume (Roundy et al., 2005). Scaling up the size of these harvesters is favorable as this yields lower resonant frequencies and higher output powers at the cost of larger volume, which can be detrimental. Accordingly, an output power, resonant frequency and volume trade-off exists.

Modified cantilever beam geometries have been proposed to improve performance with structures such as the rectangular and trapezoidal T-shapes being reported (Montazer et Sarma, 2018). The rectangular T-shape includes a tip mass that is wider than the beam width, and the trapezoidal T-shape features an anchored beam width that is larger than its end, and can include a mass at the tip as well. The intent of this paper is to outline the advantages that T-shaped harvesters, rectangular or trapezoidal, can bring over the typical cantilever beam harvester. The work specifically covers planar mass designs when adding a thick proof mass below or above the cantilever tip is not an option. It will be presented that within a fixed area, these shapes can result in significant differences in characteristics. While this work focuses on structures without proof masses, the study presented in this work can still apply if proof mass structures are added to the cantilever in order to achieve lower resonant frequencies and higher output powers.

Accordingly, this paper is a comprehensive study that provides guidelines on how to design the harvester in order to achieve a good output power, resonant frequency and device volume trade-off. The work also considers the limitations of the microfabrication process used to implement the harvesters in proposing these guidelines, which in this case is the MEMSCAP PiezoMUMPs process. While the harvester geometry types touched on herein can be found in the literature, the impact of geometry variations on the performance trade-off of the designs is not often tackled in other works. Notably, this is the case when solely a planar proof mass is an option (i.e., limiting the minimum resonant frequency and output power). Adding a large proof mass to the harvester can be a challenge in commercial processes, because of packaging and/or microfabrication limitations and can result in a lower yield. However, such commercial processes ensure repeatability and low-cost implementation of the harvesters. As such, T-shape devices with a planar mass can be beneficial to devise, however these need to be carefully designed to overcome the limitations of the proof mass removal on the performance trade-offs.

Relatively large scale cantilevers were investigated in previous works to understand tip mass size effects on performance (Miso et al., 2010). On a microscale, in (Jia et Seshia, 2016a) only rectangular beams were considered. The portion of the cantilever length that the end mass can occupy was studied and the best results were achieved with a 5 mm^3 mass. In (Kim et al., 2011), the effect of the proof mass size on the mechanical behavior of micron-scale cantilevers was investigated, with frequencies in the tens of kHz reported. On the other hand, not many works have studied T-shaped MEMS energy harvesters. Previous works on T-shaped harvesters have not focused on the optimal geometry dimensions or provided performance-focused design methodologies. The work in (Miller et al., 2011) proposed rectangular and trapezoidal beams, but did not provide a performance comparison. In (Montazer et Sarma, 2018), a trapezoidal PVDF piezoelectric film occupying an area of 125 mm^2 is presented. While most of the previous works (e.g., (Andosca et al., 2012), (Lumentut et Howard, 2014)) have focused on cantilevers with a thicker mass at the tip (i.e., proof mass), as was previously stated, the work presented here considers a mass that is of similar thickness than that of the beam (i.e., planar mass). Effects of the proof mass size and geometry specifically on the

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resonant frequency of piezoelectric vibrational energy harvesters was studied in our prior work (Alameh et al., 2018b).

In this paper, T-shape energy harvester geometry optimizations are studied and validated through fabrication results that match theory and simulations. The focus of the paper is to investigate the variations in resonant frequency and power output of the harvesters stemming the beam to mass area and the beam geometry. Recommendations on beam to mass length and beam to mass width are given. This yields a better understanding on how to optimize the dimensions of T-shaped vibration energy harvesters. Eight designs have been fabricated and tested using the PiezoMUMPs fabrication process from MEMSCAP. This process is commercially available which ensures the repeatability and reliability of the presented results.

The paper is structured as follows: the theoretical design aspects are summarized in section II, section III presents simulation results, section IV describes the fabrication process, and section V reports on the measurement results and is followed by a conclusion.

3.2 Design Considerations

Figure 3.1 shows a general representation of a T-shaped piezoelectric cantilever structure. The piezoelectric material is in between upper and lower electrodes along the beam. It is excited in the d31 mode where the induced voltage is across the beam thickness and the strain along the beam axis. In general, piezoelectric materials respond to an applied mechanical stress to generate an electric charge. The constitutive relations of the piezoelectric material are (Park, Park et Lee, 2010):

$$\begin{aligned} \delta &= \sigma / Y + dE, \text{ and} \\ D &= d\sigma + \varepsilon E, \end{aligned} \tag{3.1}$$

where δ is the mechanical strain, σ is the mechanical stress, Y is the Young's modulus, d is the piezoelectric strain coefficient, E is the electric field, D is the electrical displacement (charge density), and ε is the dielectric constant of the piezoelectric material. Relevant work on the

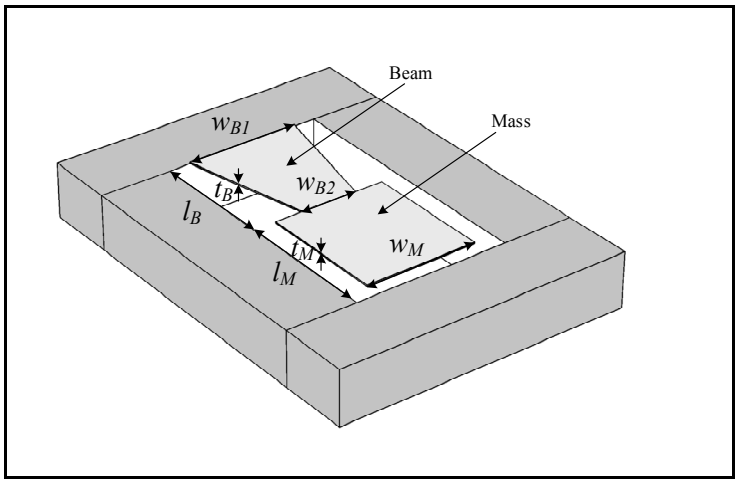

Figure 3.1 Illustration of the T-shaped harvester

modeling of piezoelectric energy harvesters can be found in (Dompierre, Vengallatore et Fréchette, 2013; Miller et al., 2011; Miso et al., 2010). Euler-Bernoulli beam theory for clamped-free cantilever geometries best describes the beam characteristics. The undamped resonant frequency is given by (Priya et Inman, 2008):

$$\omega_i = \frac{k_i^2}{L^2}\sqrt{\frac{YI}{\rho A}} \tag{3.2}$$

where k_i is a factor that depends on the vibration mode, L is the length of the cantilever, ρ is the material density, I is the moment of inertia and A is the cross-sectional area. For a rectangular beam of mass m, length l_B and width $w_{B1} = w_{B2}$, the fundamental mode frequency, ω_0, is given by:

$$\omega_0 = 1.875^2\sqrt{\frac{YI}{l_B^3 m}} \tag{3.3}$$

In general, the fundamental mode frequency depends on $\sqrt{K_{eff} / M_{eq}}$ where K_{eff} is the effective stiffness and M_{eq} is the equivalent mass of the cantilever, both calculated for a lumped-element model. For a rectangular T-shape structure, a tip mass M is added to the end of a beam. The

effective stiffness is defined as $K_{eff} = 3YI / L_{eff}^3$ where L_{eff} is the effective length. The first resonant frequency can then be expressed as (Wen-Hsien et al., 2004):

$$\omega_0 = \sqrt{\frac{3YI}{L_{eff}^3 M_{eq}}} \tag{3.4}$$

where the equivalent mass is $M_{eq} = 0.2427m + M$, the effective cantilever length is $L_{eff} = l_B + 0.5l_M$ and the moment of inertia is $I = \frac{1}{12} w_{B1} t_B^3$. Consequently:

$$\omega_0 = \frac{1}{2}\sqrt{\frac{Y w_{B1} t_B^3}{(0.2427m + M) L_{eff}^3}} \tag{3.5}$$

Assuming that the density of the cantilever material, ρ, is the same for the beam and the mass, and they both approximately have the same thickness (i.e., $t_b = t_M$) then the resonant frequency equation can be rewritten as:

$$\omega_0 = \frac{1}{2}\sqrt{\frac{Y}{\rho}} t_B \sqrt{\frac{w_{B1}}{L_{eff}{}^3 \left(\frac{33}{140}(l_B \times w_{B1}) + l_M \times w_M \right)}} \tag{3.6}$$

Based on (3.6), the resonant frequency depends on the width, thickness, length, mass and the material of the cantilever. Figure 3.2(a) illustrates the variation of the resonance frequency of the T-shaped structure as a function of the beam length while keeping all the other variables constant including the total length, $l_B + l_M$. These variations will be further investigated in section 3.3.

When the piezoelectric material is excited with a harmonic motion, strain is induced across the piezoelectric layer. The generated electrical charge q and peak power output P can be estimated by the following equations (Jia et Seshia, 2016a):

$$q = d_{31}\varepsilon_{av} Y w_p l_p \text{, and} \tag{3.7}$$

$$P = \frac{\omega q^2}{C} = \frac{\omega h_p q^2}{\varepsilon_0 \varepsilon_r w_p l_p} = \frac{\varepsilon_{av}^2 \omega d_{31}^2 Y^2 (w_p l_p h_p)}{\varepsilon_0 \varepsilon_r},$$

where d_{31} is the piezoelectric charge constant, ε_{av} is the average piezoelectric strain, w_p, l_p, h_p are the piezoelectric layer dimensions, ω is the vibration frequency and C is the capacitance of the piezoelectric layer.

As seen in (3.7), the output power is dependent on the harvester geometry, frequency and the induced strain in the piezoelectric layer. In other words, the impact of the tip mass is significant on the harvester's performance, as it alters all of these parameters. Figure 3.2(b) shows the output power variation as a function of beam length, while all other parameters are kept constant. Design optimizations to increase output power include an increase in mass, the use of higher density materials, reduced mechanical and electrical damping and a resonant frequency that is near the vibration frequency. However, an optimal design may not be practically realizable because of limitations on the geometry dimensions.

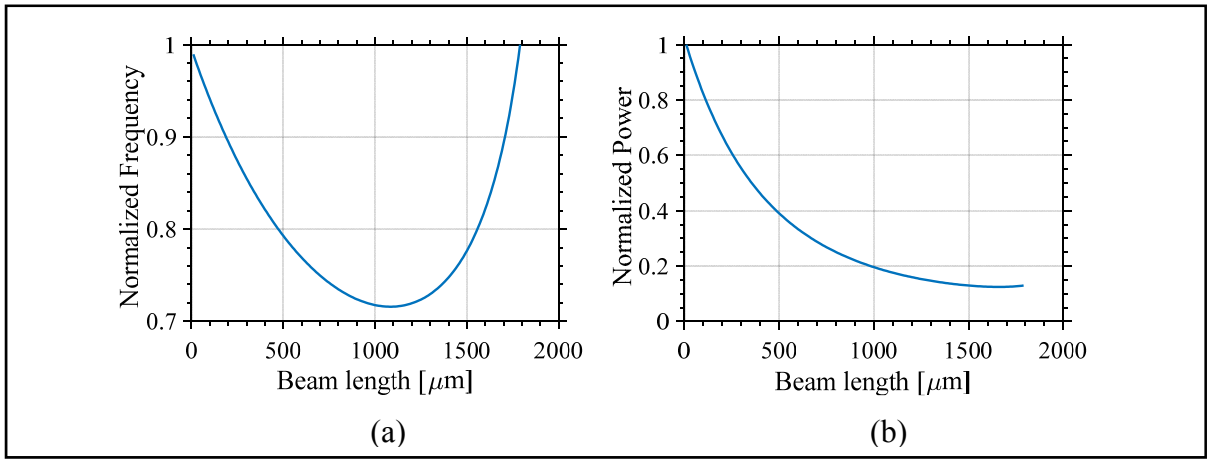

Figure 3.2 Analytical normalized (a) frequency and (b) output power variations vs. beam length of the T-shaped structure for a fixed total length.
All the other parameters are kept constant

Equations (3.6) and (3.7) govern the performance of rectangular piezoelectric energy harvesters. These equations imply that if the total length of the design is increased, then its

resonant frequency will decrease, while the output power will be higher. However, for a representative comparison, in this work the total length has been selected to be the same for all of the devices, and only the relative beam to mass lengths are modified.

3.3 Simulation Results

Two beam geometries are studied in this work: the rectangular beam and the trapezoidal beam. These will be considered with and without a tip mass to form T-shape structures. The resonant frequency and the stain distribution of the structures are considered (Miller et al., 2009). This is essential because as shown previously in (7), the output power scales with these parameters. The geometries of the cantilevers studied here are based on Fig. 3.1.

The harvesters were designed with different dimensions to compare their performance. Table 3.1 summarizes dimensions of the fabricated designs shown in Fig. 3.3. Rectangular beams are labeled as “B” designs, and trapezoidal beams are labeled as “T” designs. B1 is a reference rectangular design, B2 has a mass that occupies thirty percent of the total length and a beam width that is half that of the mass width, B3 has a mass that occupies fifty percent of the total length and a beam width that is half that of the mass width, and B4 has a mass that occupies fifty percent of the total length and beam width that is three eighths that of the mass width. T1 has a non-anchored width that is half that of the anchored side, T2 has a non-anchored width that is one eighth that of the anchored side, T3 has a mass occupying thirty percent of the total length and a beam width at the mass that is half that at the anchor side, and T4 has a mass occupying fifty percent of the total length and a beam width at the mass that is half that at the anchor.

While the goal here is to better understand the behaviors by sweeping through different parameter values, these dimensions have been selected as a compromise to ensure good fabrication yield and reliability, based on prior experience with the fabrication process. The total available fabrication area was of 4.3 × 4.3 mm, and was another design size constraint.

In order to study the structures, a model has been developed using the COMSOL finite element simulation software. As the structures were fabricated using the commercial PiezoMUMPS fabrication technology, studies were limited to structures that could be realized with this process. Therefore, some limitations were imposed on the values of the parameters, due to the thicknesses of the materials used. The beam thickness was defined as 11.5 μm (10 μm Si, 0.5 μm AlN, 1 μm Al) and the mass thickness 10 μm (Si only).

Table 3.1 Design Dimensions

Design Variants (B: rect., T: trap.)	Beam Dimensions l_B, w_{B1}, w_{B2}, t_B (μm)	Mass Dimensions l_M, w_M, t_M (μm)
B1	1800, 800, 800, 11.5	-
B2	1260, 400, 400, 11.5	540, 800, 10
B3	900, 400, 400, 11.5	900, 800, 10
B4	900, 300, 300, 11.5	900, 800, 10
T1	1800, 800, 400, 11.5	-
T2	1800, 800, 100, 11.5	-
T3	1260, 800, 400, 11.5	540, 800, 10
T4	900, 800, 400, 11.5	900, 800, 10

3.3.1 Strain Distribution

As shown in the constitutive equations presented in section 3.2, the piezoelectric effect converts a mechanical strain to an electric current in response to a mechanical stress. Figure 3.3 shows the simulated von Mises stress distribution of the different designs. The trapezoidal beams show better stress distribution that translates into higher strains. Several aspects need to be addressed to maximize the strain distribution, including the piezoelectric material. The more trapezoidal the shape of the beam, the more even the strain distribution, and therefore the more energy is generated per unit volume of piezoelectric material (Baker, Roundy et Wright, 2005). However, this results in a higher resonant frequency. Another advantage of the trapezoidal designs are their increased resistance to shocks compared with rectangular beams (Frank et Peter, 2008). They are more reliable with higher yields, and have an increased resistance to fracture due to the fact that the highest stress in a cantilever beam is at the base, such that increasing the width of the beam at the base allows the force to be distributed over a larger

area. Cantilever designs with a rectangular geometry experience strains mostly on the portion of the beam near the anchored end.

Figure 3.4 shows FEM simulated strain response for the rectangular designs along a cut line straight through the middle across the total structure length (i.e., arc length). The narrower the rectangular beam width with respect to the mass width, the more the strain is increased. However, the reduced width required for large strain and the concentration of the strain at the anchored portion of the beam reduce the effective piezoelectric material area to generate charge. As seen in (3.7), the output power is proportional to the applied mechanical strain, the piezoelectric area and the resonant frequency. With most of the strain energy accumulated where the beam is clamped and almost no stress on the other parts, using trapezoidal beams instead of rectangular beams allows to maximize the piezoelectric material area and augments the harvested power without affecting the resonant frequencies significantly (Baker, Roundy et Wright, 2005).

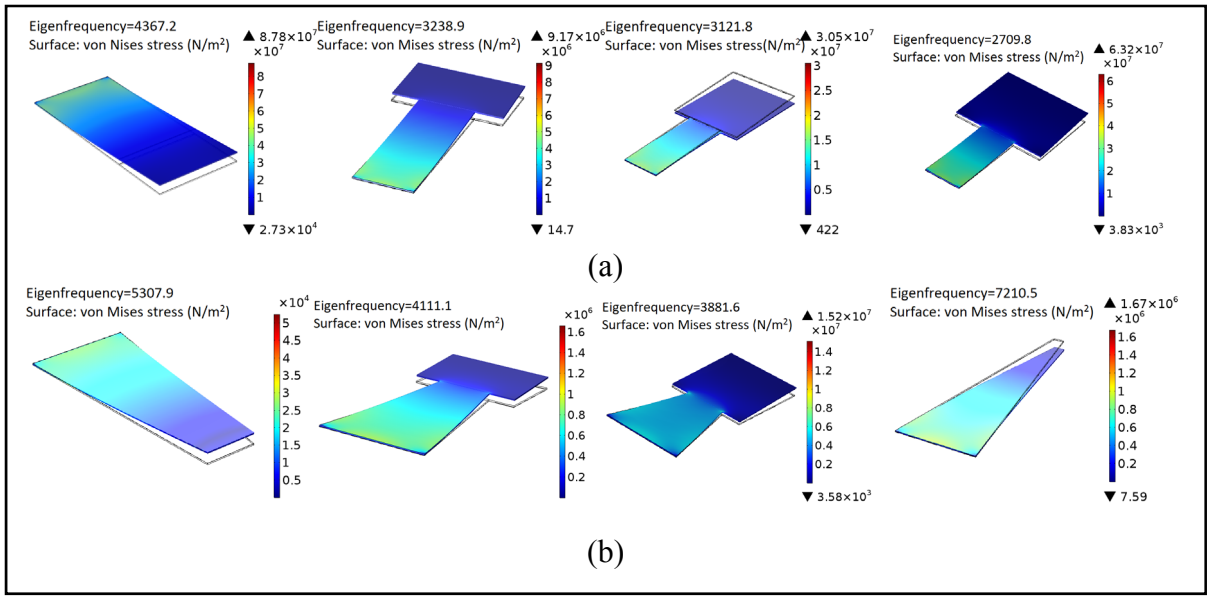

Figure 3.3 Resonant modes and stress distribution of different cantilever designs: (a) B1, (b) B2, (c) B3, (d) B4, (e) T1, (f) T2, (g) T3, and (h) T4

Moreover, COMSOL frequency domain simulations were performed to analyze the power output of the designs as a function of the vibration frequency for a given electrical load of

1 MΩ and harmonic acceleration amplitude of 7g. Figure 3.5 shows the simulation results. While the trapezoidal designs with a T-mass improve the strain distribution, as shown in Fig. 3.3, the power output of these devices can be lower than that of a cantilever or a rectangular T-shape beam. This effect occurs when a high strain zone is removed from the piezoelectric area due to the use of a trapezoidal T-shape. As a result, as it can be seen in Fig 3.5, the power output for devices T3 and T4 is lower than B1 and B2, while being higher than B3 and B4 at the cost of a higher resonant frequency. Tuning the designs to match ambient vibration frequencies is discussed in the following section.

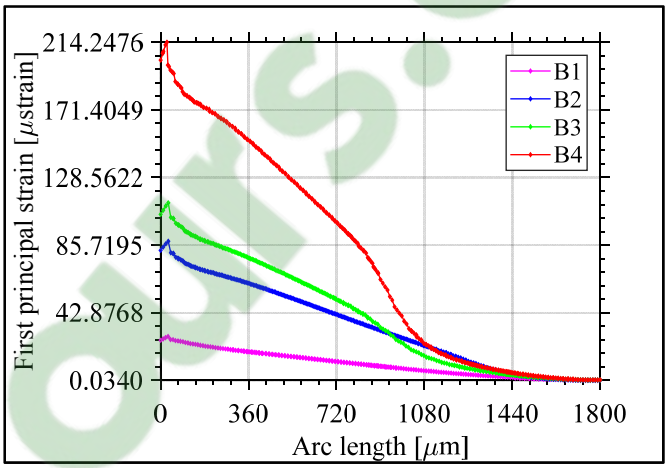

Figure 3.4 Simulated strain response over the arc length for the four B-type designs

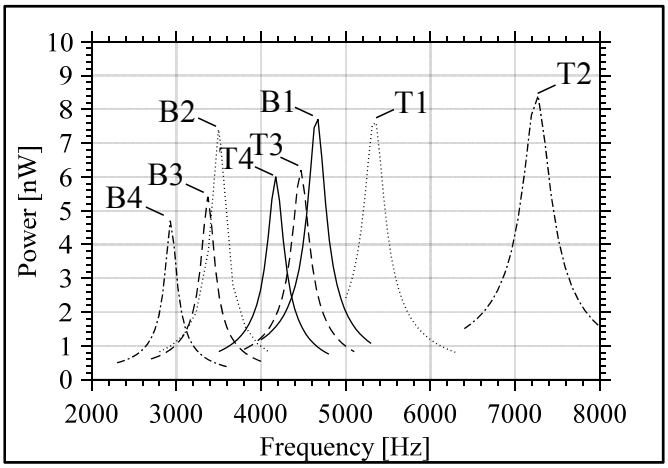

Figure 3.5 Simulation of the output power frequency response of the proposed designs

3.3.2 Resonance Frequency

Eigen frequency simulations were carried-out to assess the effect of varying the mass size on the device performance. The beam length to the mass length and beam width to mass width ratios were varied. The simulation results in Figure 3.5 show that there is a minimum resonant frequency as the mass length is varied from 10 to 1790 μm for different beam widths for a rectangular T-shape device, while keeping the overall length constant 1800 μm and mass width 800 μm. This minimum gets lower as the beam gets narrower. In T-shaped cantilever devices, two kinds of frequency behaviors can be witnessed (Narducci et al., 2008). One is dominated by the harvester's extra mass and the other is dominated by the spring constant. A minimum point is simulated to be where the mass length is equal to the beam length. This is where neither of these effects dominate on the resonant frequency. Figure 3.6 shows the trapezoidal designs simulation results for varying the beam length from 100 to 1600 μm, and adjusting the mass length accordingly to keep the overall length constant. A fixed beam anchor width, w_{B1}, of 800 μm is used, and the beam width at the mass, w_{B2}, is varied from 200 to 600 μm. Simulations show an intersection point that separates the behavior between the mass and the beam dominating the resonant frequency. For a beam with no mass, the narrower the free beam tip, the higher the resonant frequency. Conversely, if a narrow beam tip is connected to a T-shaped mass, then the narrower the tip, the lower the frequency. In the latter case, there is a limit after which the design will not be viable structurally.

To maximize the output power, the harvester's resonant frequency should be equal to the ambient driving frequency. As previously mentioned, the resonant frequency depends on the stiffness and mass. An increase in mass will require an increase in stiffness to maintain the resonant frequency constant. An increase in stiffness translates into a thicker or wider beam (Roundy et al., 2005). Thus, the choice of the geometry type and the dimensions is important and should meet the application requirements. The energy harvesters designed and simulated in this work are meant to demonstrate an understanding of the variation in frequency response of these devices rather than reporting on designs having a specific resonant frequency target.

The conclusions drawn here can be scaled to achieve a wide range of targeted resonant frequencies.

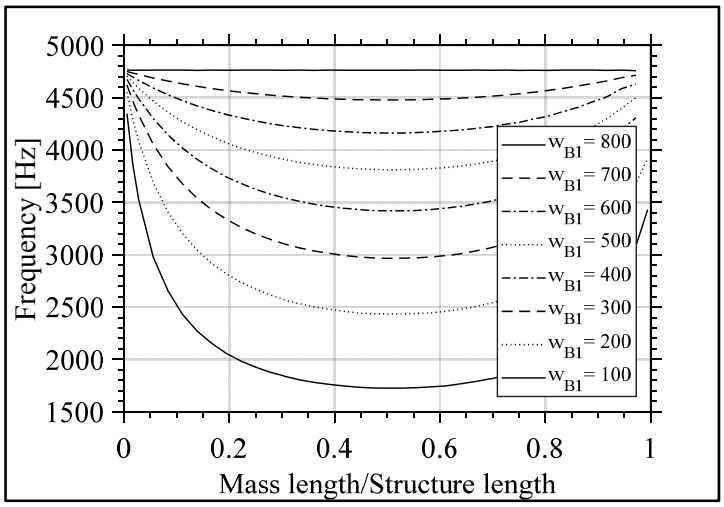

Figure 3.5 Effect of varying the mass length on the first resonant frequency for different beam widths (w_{B1}) of rectangular T-shape structures of constant length

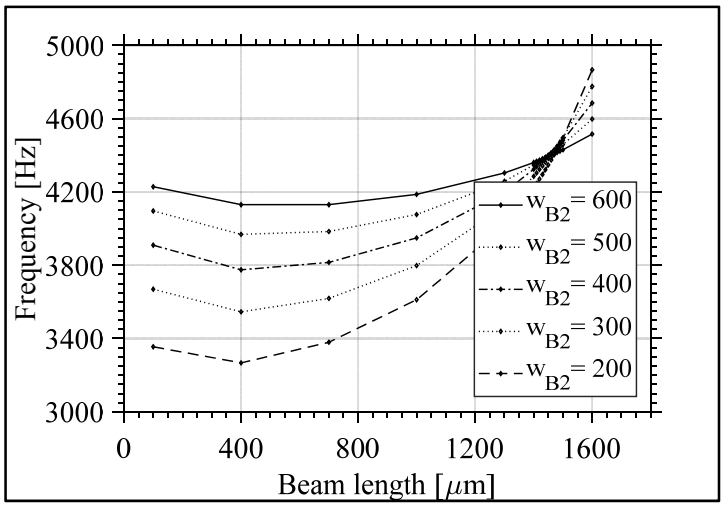

Figure 3.6 Effect on the first resonant frequency of varying beam length with fixed anchor width (w_{B1}) of 800 µm for different beam tip widths (w_{B2}) of trapezoidal T-shape structures of constant length

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3.4 Fabrication Process

The PiezoMUMPs process uses Aluminium Nitride (AlN) as the piezoelectric material. Though AlN has lower piezoelectric coefficient with respect to other piezoelectric materials, it has a good piezoelectric response, high breakdown voltage and high electrical resistivity (Giordano et al., 2009). It does not require poling after deposition and can be deposited by sputtering which makes it compatible with standard silicon IC technologies and suitable for MEMS energy harvesters.

The fabrication process requires five masks, and is fully described in (Cowen et al., 2014). Figure 3.7 briefly outlines this process. The process is carried out on a 150 mm (100) oriented silicon-on-insulator (SOI) wafer with device silicon layer thickness of 10 μm, buried oxide thickness of 1 μm and handle substrate thickness of 400 μm, as shown in Fig. 3.7(a). The top surface of the silicon layer is doped using a phosphosilicate glass (PSG) to increase its conductivity. This PSG layer is then removed via wet chemical etching. This layer constitutes the main structural layer that will be used to form the device. A 200 nm thermal oxide is then grown. The wafers are then coated with a positive photoresist and lithographically patterned. The oxide is wet-etched, as illustrated in Fig. 3.7(b). This thermal oxide serves to isolate the silicon layer from the metal stack in the areas without AlN. A 0.5 μm-thick layer of AlN is then deposited by reactive sputtering. The wafers are then coated with positive photoresist and lithographically patterned, and wet etched, as shown in Fig. 3.7(c). This piezoelectric layer is used for transduction. A metal stack consisting of 20 nm of chromium and 1 μm of aluminum is deposited and patterned through a lift-off process. This will be used to form the electrical interconnects and pads, as illustrated in Fig. 3.7(d). The device silicon is lithographically patterned, and etched using deep reactive ion etching (DRIE) to form the harvester structure, as shown in Fig. 3.7(e). Next, a polyimide coating is used on the front side as a protective material in order to maintain the wafer integrity through the subsequent trench etching. The silicon substrate is then lithographically patterned from the bottom side and etched using DRIE to form release trenches that stop at the oxide layer. A wet oxide etch process is then used to remove the now exposed buried oxide layer in the trench regions. At last, the front side

protection material is stripped by dry plasma etching. The harvester structure is completely released and free to move, as illustrated in Fig. 3.7(f). Figure 3.8 shows the SEM micrograph of the eight fabricated harvester designs that reside on a 4.3 by 4.3 mm die. Each design occupies an area of 800 by 1800 µm. A script in Skill language has been written to layout the designs in the Cadence ICFB software suite. The piezoelectric material area is split into two halves for testing purposes, requiring three pads for each design. The two pads are connected to the piezoelectric material to allow for the use of GSG coplanar probes or DC needles for testing.

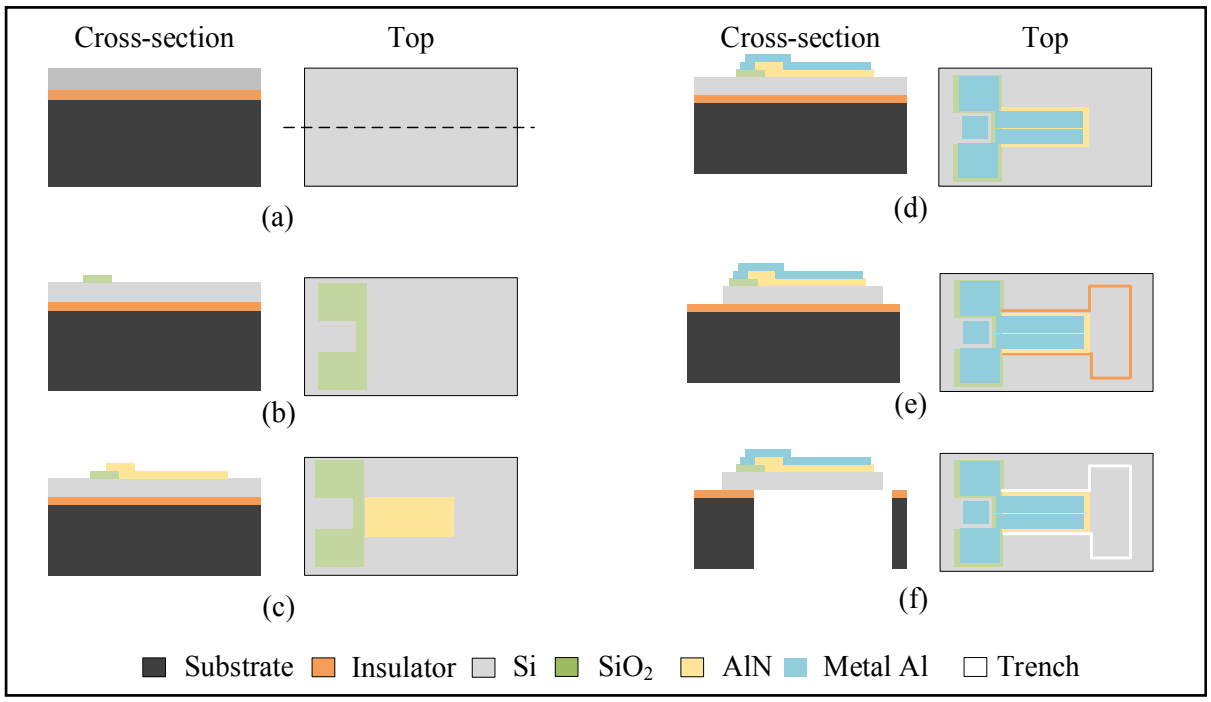

Figure 3.7 Simplified overview of the PiezoMUMPs fabrication process flow

3.5 Measurement Results

Two types of measurements have been carried out to characterize the harvesters. One by electrically driving the transducers and measuring their mechanical response, and the second using a mechanical shaker to excite the harvesters and measure their electrical response. Different samples were tested of which bare dies using probes and wire bonded dies in a package soldered to a custom PCB. Figure 3.9 shows the packaged die. The measurements

were performed with five packaged samples and five non-packaged of each design (total of 10 samples). All the designs occupy the same area, while the active piezoelectric area covers the beam area which is different from one design to another.

Figure 3.8 Micrograph of the fabricated harvesters

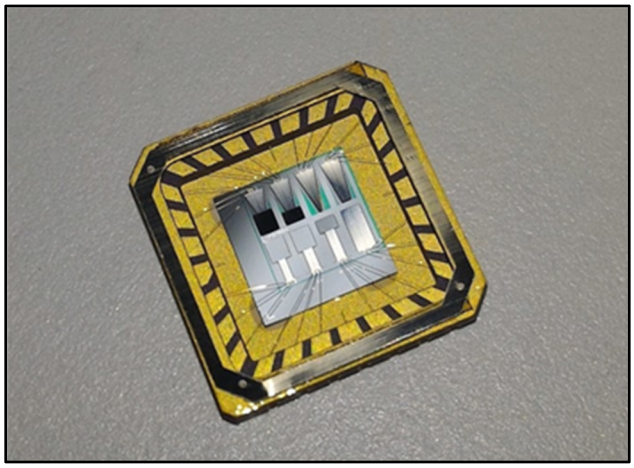

Figure 3.9 MEMS harvesters chip wire bonded in a 28-pin LCC package

A vector network analyzer VNA (E5061B from Keysight) and a probe station (EP6 from Cascade) were used as shown in Fig. 3.10 to measure the devices' S_{21} parameters (i.e.,

transmission in dB), and to verify the resonance frequency of each device. Figure 3.11 illustrates the measured resonance characteristics of harvester B2 at atmospheric pressure, which shows a resonance frequency of 3.72 kHz, bandwidth of 49.3 Hz and quality (Q) factor of 75.7. The average frequencies of all the designs are reported in Table 3.2 with an overall average standard deviation of about 125 Hz (2.9%). The resonance frequencies of the devices were slightly different because of process variation over the wafer. The influence of packaging was investigated by comparing unpackaged devices with packaged devices at atmospheric pressure. The packaged device suffered less frequency variations than unpackaged devices with an average standard deviation across the designs of 59 Hz (1.25%) and 160 Hz (3.75%), respectively. This is attributed to the varying packaging interconnect parasitics between devices affecting the electrical measurement. More precise packaging could improve the variations observed, but this is beyond the scope of this work.

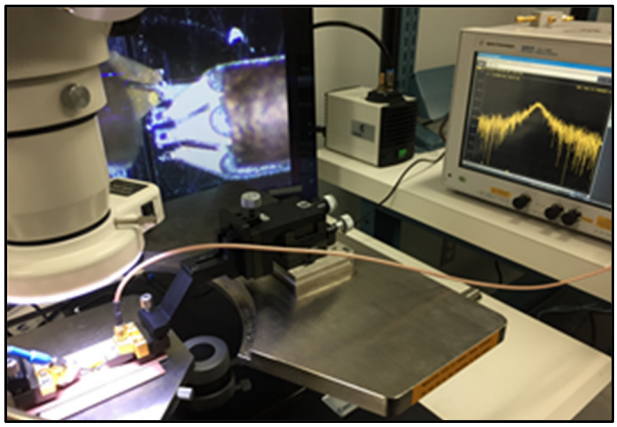

Figure 3.10 Probe test setup used to measure the resonance with a VNA

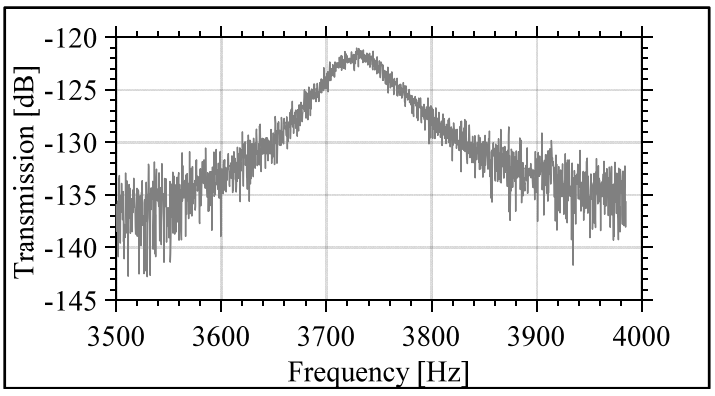

Figure 3.11 Measured resonance characteristics of design B2

Table 3.2 VNA Resonance Frequency Measurements in Hz

	B1	B2	B3	B4	T1	T2	T3	T4
Bare die	4400	3597	3450	2964	5382	7325	4512	4212
STD (Hz)	175	142	136	103	201	198	165	158
STD (%)	3.98	3.95	3.94	3.48	3.73	2.70	3.66	3.75
Packaged	4285	3485	3323	2895	5333	7326	4470	4252
STD	42	29	51	36	66	101	64	81
STD %	0.98	0.83	1.53	1.24	1.24	1.34	1.43	1.90
All	4342	3535	3379	2921	5358	7325	4491	4232
STD	139	112	117	77	152	152	127	127
STD %	3.20	3.17	3.46	2.64	2.84	2.08	2.83	3.00

Figure 3.12 illustrates the resonant frequency variation vs. the different device geometries stemming from the VNA measurements. The resonant frequency decreases as the mass length increases, as shown in Fig. 3.12(a); the resonant frequency decreases as the tip width decreases, as shown in Fig. 3.12(b); the resonant frequency decreases as beam width decreases, as shown in Fig. 3.12(c); and the resonant frequency increases as the anchor width increases, as shown in Fig. 3.12(d). This behavior confirms the results stemming from the simulations described in Section 3.3.

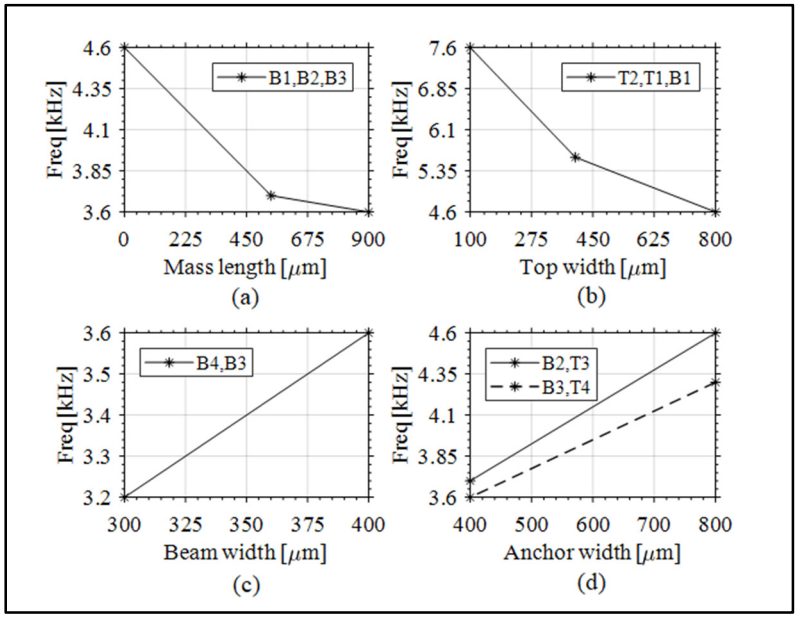

Figure 3.12 Resonance frequency comparisons

The electrical to mechanical responsiveness of the piezoelectric transducers has been further characterized using a laser dopler vibrometer (Polytec OFV-534). Figure 3.13 shows the maximum velocity of the harvesters tip to an AC driving voltage sweep of amplitude 0 to 18 V at the resonance frequency of each device. The T-designs exhibited higher velocities than the B-designs, with device T2 showing the highest velocities. A near-linear velocity to driving voltage is observed for all designs.

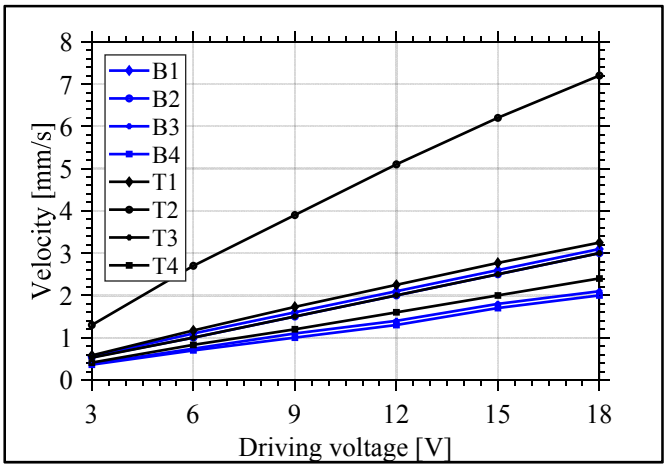

Figure 3.13 Measured harvester velocity vs driving voltage for the different harvester designs

To measure the beam responses to external mechanical vibrations, a shaker system has been used (Type 4809 from B&K). Figure 3.14 shows the experimental test setup. A computer communicates with a vibration controller to generate the signal that is fed to a power amplifier that drives the vibration stage. A miniature tear-drop accelerometer is placed on the PCB near the device under test to sense the acceleration. It provides a negative feedback to the vibration controller so that it may control the vibrations to meet the required test parameters (i.e., driving acceleration). A data acquisition system is being used to collect and analyze the results.

The devices' power output frequency responses have been investigated with this setup by using a frequency sweep from the vibration stage. A periodic chirp has been applied to sweep through a frequency range of 2000 to 8000 Hz in order to mechanically excite the devices. An acquisition system (LMS SCADAS) having an input impedance of 1 MΩ (260 pF) has been

used. Figure 3.15 reports on the output power frequency response measurements with device T2 delivering a peak of 7.1 nW. In the displayed results, the harvesters are driven at an average acceleration of about 7 g. The maximum output powers are at the resonant frequencies of each device, which are in good agreement with the previous VNA measurements presented. Note that these results are in line with the simulated results shown in Fig. 3.5, with acceptable degrees of variation, considering the simplified mechanical / electrical model used in the simulation. While the results here are used for study and comparison, this output power could be maximized by using bimorphs, a different piezo material, adding a proof mass or implementing larger designs. However, the relationship between the different designs' output powers is expected to remain the same.

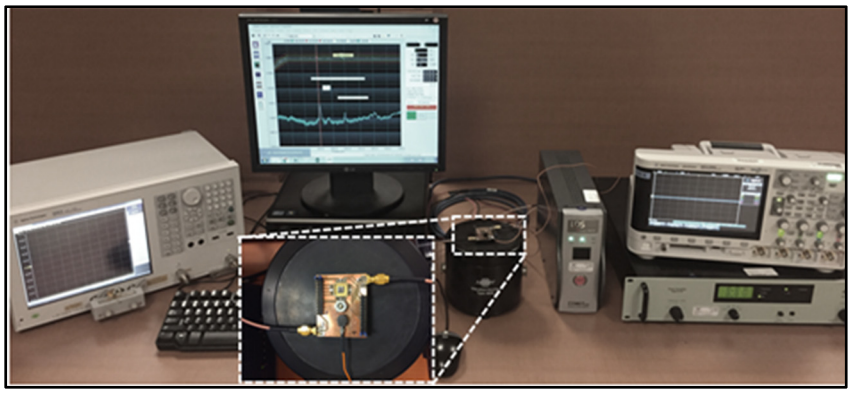

Figure 3.14 Experimental vibration test setup. Inset shows a zoomed view of the test PCB

To further validate the maximal attainable voltages, a sinusoidal signal is applied to the shaker to drive the devices at their resonant frequency and the output is measured through an oscilloscope load of 1 MΩ (13 pF). Figure 3.16 shows the measurement results. The peak harvested voltages are listed in Table 3.4. These results show good correlation with the power outputs measured earlier.

The harvested voltage depends on the vibration acceleration and the load resistance. This is illustrated for the T1 design in Fig. 3.17, where the output voltage across two different loads, the oscilloscope 1 MΩ (13 pF) load and a high impedance 10 MΩ probe (3.9 pF), is plotted vs. different accelerations. As can be seen, this variation is almost linear with acceleration at a rate

of change of about 10 mV/g. Note that the capacitances and resistances of the devices have been calculated to be in the range of 40 - 225 nF and 160 kΩ - 1.3 MΩ, respectively. These values are listed in Table 3.3.

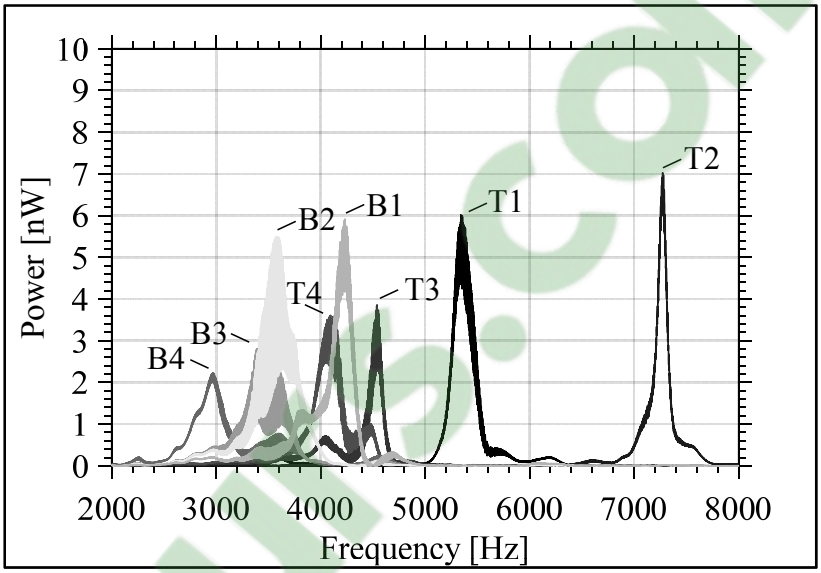

Figure 3.15 Output power variation vs excitation frequency obtained from excitation of the different harvester designs using a vibration stage

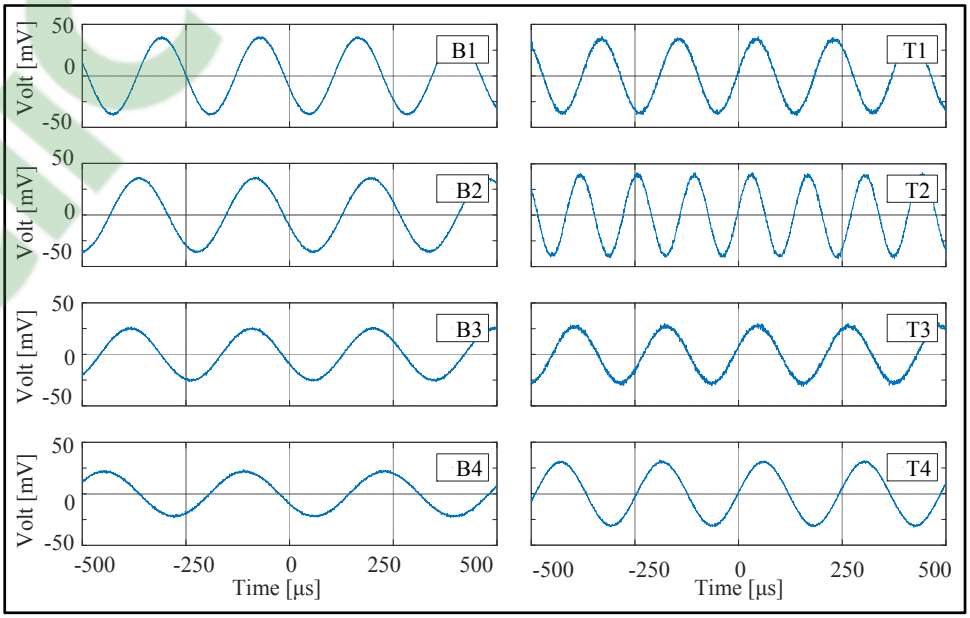

Figure 3.16 Time domain output voltage at resonance frequency and load of 1 MΩ for the different designs

Table 3.3 Capacitances and Resistances of the Designs

	B1	B2	B3	B4	T1	T2	T3	T4
Capacitance (nF)	226	78.1	55.8	41.4	169	126	118	84
Resistance (kΩ)	161	575	861	1300	176	174	300	467

In general, the narrow bandwidth of piezoelectric harvesters can present a challenge to their implementation unless it is responding to an ambient vibration near the resonant frequency. Figure 3.15 illustrates that we can form an array of cantilevers that responds to a range of resonant frequencies. Their frequency response will then overlap and will thus guarantee a voltage output over a wider range of frequencies. An array of cantilevers for multi-frequency energy harvesting can then be created (Huan, Yuantai et Qing-Ming, 2008a).

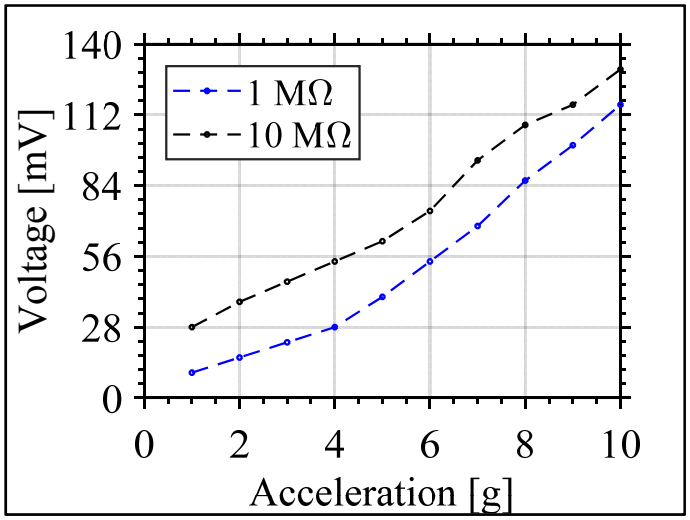

Figure 3.17 Device T1 output voltage vs acceleration
for 1 MΩ and 10 MΩ loads

3.6 Discussion

Considering the data gathered, it can be observed that for devices B1, B2, B3 and B4, the prognostic regarding the use of a T-shaped design were validated. According to the design strategy proposed, the use of a T-shape allows a reduction of up to 33% for the resonant frequency while keeping the dimensions used by the piezoelectric harvester constant. The design process includes increasing the mass length until the resonant frequency reaches a

minimum, and then decreasing the beam width to further decrease the frequency. This operation decreases the piezo area and the voltage output, however this still increases the voltage generated by unit area of piezoelectric material deposited. To increase the voltage output, trapezoidal designs have been investigated. When considering devices B1, T1 and T2, more voltage is generated as the tip is made narrower, due to a more uniform strain distribution, but this results in a higher resonant frequency.

Finally, rectangular and trapezoidal T-shaped designs such as B2 and T3, where the mass occupies 30%, and designs such as B3 and T4, where the mass occupies 50%, are compared. In comparison with the rectangular beams, the use of trapezoidal beams allows a larger reduction of the resonant frequency when the relative proportion of the mass is increased. This is achieved without compromising the power output. As shown with devices B2 and B3, the change from a 70% to 50% beam area proportion leads to a reduction of 228 Hz (6.43%) of the resonant frequency, but also a reduction of 20 mV (27%) of the voltage output. Comparatively, with devices T3 and T4, the change from a 70% to 50% beam area proportion leads to a reduction of 467 Hz (10.37%) of the resonant frequency, and a reduction of only 2 mV (3.22%) of the voltage output. Accordingly, the trapezoidal designs with mass can be a better option, as the resonant frequency can be reduced without significantly reducing the output voltage and consequently the output power.

While the trapezoidal geometries can perform better than the rectangular ones when varying the beam area proportion from 70% to 50%, there is always a trade-off between frequency and output power requiring a design to be optimized. Table 3.4 summarizes the average measured metrics, and provides an overview of the impact of the geometry on the cantilever-based piezoelectric energy harvesters' resonant frequency and output voltage in comparison to other works (Elfrink et al., 2010; Jia et Seshia, 2016b; Miller et al., 2011; Nabavi et Zhang, 2018). While this work is not aimed at structures that include proof masses, the fabricated devices are compared to other works that include proof masses and works that do not. This can highlight the advantages of the structures and help position the work and shows the potential when compared to large devices with proof masses. For this purpose, a figure of merit (FOM) that

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normalizes the power generated to the piezo area and vibration acceleration has been added to compare the performance of these devices in a more representative manner.

The proposed devices provide a good output power to piezoelectric area ratio, and relatively to their small overall size (i.e., 1800 µm × 800 µm), they compare to bigger devices such as (Elfrink et al., 2010) where a device surface area of 30 mm^2 was occupied, of which a mass surface area of 25 mm^2. Similarly, in (Miller et al., 2011) the best harvester was designed to achieve a low resonance frequency by using a large beam length of 4.5 mm and mass length of 1.5 mm. The structure uses a piezoelectric layer of PZT which has higher piezoelectric coefficient than AlN, but is not micro-fabrication friendly mainly due to the processing temperatures required for their crystallization and their use of lead. With no proof mass, a rectangular design was presented in (Jia et Seshia, 2016b). It consists of a micro cantilever with 2000 µm length and 500 µm width and comparable thicknesses. Another rectangular design with no proof mass is presented in (Nabavi et Zhang, 2018), although it was optimized for a large piezo area, the beam length is of 3154 µm and beam width is of 500 µm. Both performances fall behind the proposed structures.
Accordingly, this work proposes compact structures without proof masses that compare favorably to other similar works, as can be seen by the FOM. For larger structures with proof masses that have higher output power, the optimization strategies presented here could result in an enhanced performance.

3.7 Conclusion

In this paper, various cantilever-based piezoelectric vibrational energy harvesters designs have been investigated. Cantilever beam harvesters are still favored for their relatively high strains and simplicity of fabrication. A T-shaped cantilever structure can bring advantages over the traditional cantilever structure. It enables variations in terms of output power and resonant frequencies that have been reported here, while using the same available area. This permits a representative comparison between the fabricated devices and shows the variations that can be

obtained by changing the design geometry (i.e., beam to mass lengths and widths) for the same type of structure (i.e., T-shapes with planar mass).

This type of harvesters is relevant to a wide range of applications, and the recommendations stemming from this work can help provide better understanding of the design considerations for these devices, and pave the way towards optimal T-designs tailored for targeted applications.

Acknowledgment

The authors would like to thank the Natural Sciences and Engineering Research Council of Canada (NSERC), the Fonds de recherche du Québec – Nature et technologies (FRQ-NT) and the Microsystems Strategic Alliance of Quebec (ReSMiQ) for their financial support. The authors also thank CMC Microsystems for providing the layout design tools and enabling device fabrication.

Table 3.4 Measured Performance of the Different Designs and Comparison

Design Variant	Beam Shape	Piezoelectric Area (mm^2)	Acceleration (g)	Material	Frequency (Hz)	Output Voltage (mV)	Load	Output Power	FOM $nW.mm^{-2}.g^{-1}$
B1	Rectangular	1.42	7	AlN	4371	77	1 MΩ	5.93 nW	0.60
B2	T-shape	0.49	7	AlN	3545	74	1 MΩ	5.48 nW	1.60
B3	T-shape	0.35	7	AlN	3317	54	1 MΩ	2.92 nW	1.19
B4	T-shape	0.26	7	AlN	2946	47	1 MΩ	2.21 nW	1.21
T1	Trapezoidal	1.06	7	AlN	5365	76	1 MΩ	5.78 nW	0.78
T2	Trapezoidal	0.79	7	AlN	7269	84	1 MΩ	7.06 nW	1.28
T3	Trapezoidal	0.74	7	AlN	4503	62	1 MΩ	3.84 nW	0.74
T4	Trapezoidal	0.53	7	AlN	4036	60	1 MΩ	3.6 nW	0.97
(Jia et Seshia, 2016b)	Rectangular	1	3	AlN	3688	17.4	0.3 MΩ	1.01 nW	0.34
(Nabavi et Zhang, 2018)	Rectangular	0.25	2	AlN	1589	52	10 MΩ**	0.27 nW	0.54
(Miller et al., 2011)	Trapezoidal*	6.4125	0.29	PZT	232	4.54	12 kΩ	1.72 nW	0.92
(Elfrink et al., 2010)	Rectangular*	5	0.2	AlN	596.8	810	450 kΩ	1.46 µW	1460

* With proof mass.
** High impedance probe.

CHAPTER 4

A 0.13 µm CMOS DYNAMICALLY RECONFIGURABLE CHARGE PUMP FOR ELECTROSTATIC MEMS ACTUATION

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Abstract:

An eight stage reconfigurable charge pump for MEMS electrostatic actuation was designed and fabricated in a standard 0.13 µm CMOS technology. The purpose of the circuit is to generate sufficient on chip voltages that are continually reconfigurable for MEMS actuation. Small 1 pF pumping capacitors are used to reduce the circuit area. Digitally programmable voltage levels can be outputted by varying the number of stages and the clock drive levels dynamically. Reduced power consumption is achieved using a variable frequency clock. The circuit attains a measured maximum output voltage of 10.1 V from a 1.2 V supply. Its nominal clock is set to 50 MHz. The circuit has a compact area of 215 µm × 300 µm and consumes 864 µW at a 50 MHz clock and 252 µW at an 8 MHz clock.

Index Terms: Charge pump, reconfigurable, electrostatic actuation, microelectromechanical systems (MEMS).

4.1 Introduction

Microelectromechanical systems (MEMS) have seen significant usage growth in the past few years. This is notably due to the fast adoption of MEMS into consumer electronics, such as

smart phones, and to the growth of sensors suited to the Internet of Things (Lammel, 2015; Shaeffer, 2013). Notably, in some silicon based photonic devices, advancements in MEMS technology has helped the miniaturization and realization of complex optical components, like micro mirrors (Brière et al., 2015). Demand for large continuous DC scan angle and low-operating voltage have pushed to the development of new micro mirror systems. In most applications, electrostatic actuation is preferred because of its low power consumption and ease of implementation within MEMS fabrication processes (Hah et al., 2004). Typically, a high voltage driving circuit is necessary to the operation of electrostatically actuated capacitive MEMS devices, such as micro mirrors, where a higher actuation voltage results in larger rotational displacement. Importantly, allowing for gradual motion control translates into more design freedom and wider application breadth. The angle is controlled by the bias voltage applied on the mirror, and sufficient and precise actuation of such MEMS devices requires variable bias voltages.

As such, many electrostatic MEMS require relatively high and variable actuation voltages in order to be actuated (Nabki et al., 2011; Shirane et al., 2011). While there is a constant effort to reduce the actuation voltages of MEMS, generating these voltages remains a challenging aspect of their integration, as their magnitude goes against the trend of recent integrated circuits technologies that accommodate higher transistor densities, but offer insufficient ever-reducing voltages (e.g., 1.2 V) (Yang, Wei-Chang et Nguyen, 2013). Consequently, the variable voltages required for many MEMS are significantly higher than the supply voltage available in modern CMOS technologies.

Accordingly, a reconfigurable circuit that can generate multiple voltage levels and that can change its output voltage dynamically is desirable for MEMS actuation (Brière et al., 2015; Chu et al., 2007). Moreover, an on-chip realization of such a high voltage actuation circuit is necessary to increase the control efficiency and miniaturize the MEMS packaging footprint. Therefore, fully integrated CMOS high voltage generation circuits for MEMS have recently generated more interest, but very few works touch on voltage configurability and dynamic behavior.

Suitable for high voltage generation, charge pumps or DC-DC converters are used in a wide range of applications. Work in (Richelli et al., 2007) presents a 1.2 to 8 V non-tunable output charge pump, but for non-volatile memories. In (Vaisband, Saadat et Murmann, 2015; Yi-Chun et Otis, 2011), DC-DC converters for energy harvesting applications are presented with a focus on output regulation (e.g. 1.2 V-1.4 V) to provide supply voltages for circuits. For MEMS applications, systems with high-voltage requirements often resort to older, bulky high-voltage junction breakdown transistors or more complex technologies that limit MEMS integration into a system-on-chip (Ismail et al., 2014). For example, work in (Richard et Savaria, 2004) presents two high voltage charge pump circuits implemented in a dedicated 300 V 0.8 µm CMOS technology. One circuit produces a 20 V output from a 5 V input, while the other produces a 50 V output from the same input, below the 300 V capabilities of the technology (e.g. (Beaulieu et al., 2016)). In conventional low voltage technologies, work in (Hong et El-Gamal, 2003) describes a constant threshold voltage type charge pump with a maximum output voltage of 14.8 V from a 1.2 V input, but with a relatively large area of 0.8 mm x 0.9 mm, and no reconfigurable pumping stages. In (Innocent et al., 2003), a charge pump that can generate an output voltage of 14.8 V from a 1.8 V input is proposed, but with no detailed output voltage tunability control mechanism.

Accordingly, this paper presents a reduced size digitally reconfigurable charge pump fabricated in a 0.13 µm CMOS technology from GlobalFoundries, and that operates from a 1.2 V supply to output a tunable wide voltage range of up to 10.1 V. This work is a follow-up implementation of prior work published in (Alameh, Robichaud et Nabki, 2014), and reports on the final chip design and measurement results. The proposed circuit is tailored to the actuation of MEMS devices and is designed to leverage this specific use case. The main contributions of the proposed circuit can be listed as follows: i) the high on-chip voltage achieved from a 1.2 supply; ii) the digitally programmable output voltage; iii) the design for a small area such that it is amenable to tight integration with MEMS; iv) the fast rise and fall times in the micro seconds range to allow for sufficiently fast actuation (i.e., MEMS typically operate in the sub-millisecond or millisecond range); v) the improved power consumption

through the use of a variable frequency clock; and vi) the integrated discharge stage immune to breakdown at the output for fast discharge of the MEMS capacitive load.

The paper is organized as follows: section 4.2 gives an overview of the system, section 4.3 describes the circuitry, section 4.4 presents the simulations results, section 4.5 presents the measurement results, and section 4.6 provides a discussion.

4.2 System Overview

Figure 4.1 shows the block diagram of the proposed circuit consisting of the reconfigurable charge pump with its clock, a digital control circuit, and a discharge stage. A capacitive MEMS load is considered. The purpose of the proposed circuit is to convert the supply voltage to a higher voltage and in addition, in contrasts to typical charge pumps, provide dynamic configurability of that voltage. The charge pump circuit is designed such that a switched capacitor array can be configured dynamically using switches, as conceptually shown in Fig. 4.2. The capacitive array is composed of eight pumping capacitor pairs, C_1 and C_2 for each stage. Since the charge pump is to be integrated with MEMS in the same package, the pumping capacitor size will be limited by the available area. This is of greater importance if a multiplicity of charge pumps must be used with MEMS that require several different actuation voltages simultaneously. The top plate of each pumping capacitor is connected to the input and output terminals through switches, S_i, where $i = 1, 3, 5, ..., 31$, and switches, S_j, where $j = 2, 4, 6, ..., 32$, respectively. The bottom plate of each pumping capacitor is connected to a pair of controlled clock signals *CLK1*·*CTRLi* and *CLK2*·*CTRLi,* where *CLK1* and *CLK2* are non-overlapping clocks and *CTRLi* are control signals to enable each stage. For instance, for the rightmost stage activated in Fig. 4.2 (i.e., *CTRL1* is high), pumping capacitor C_1 is connected to the stage's input during the first phase through S_1 charging it to the stage's input voltage level when *CLK1* is low and *CLK2* is high. During the second phase, *CLK1*, in series with C_1, goes high adding the clock voltage (e.g., 1.2 V) to the stage's output through S_3. C_2 is switched in a complementary fashion, reducing output ripples and allows for an efficient (i.e., low loss) CMOS switch implementation, presented later.

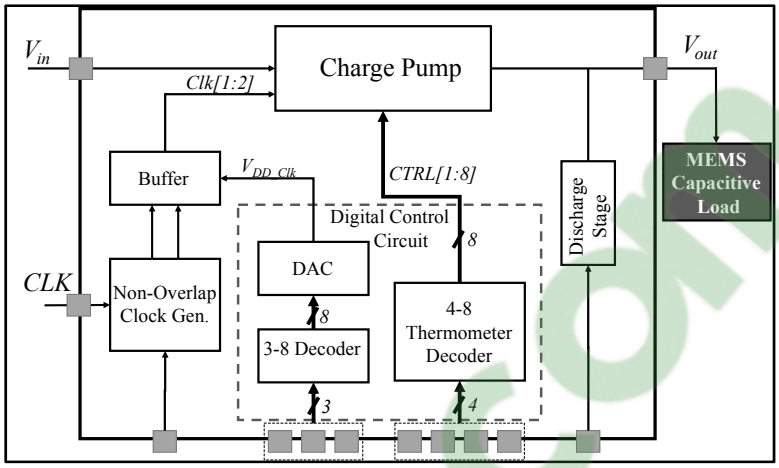

Figure 4.1 Block diagram of the proposed charge pump

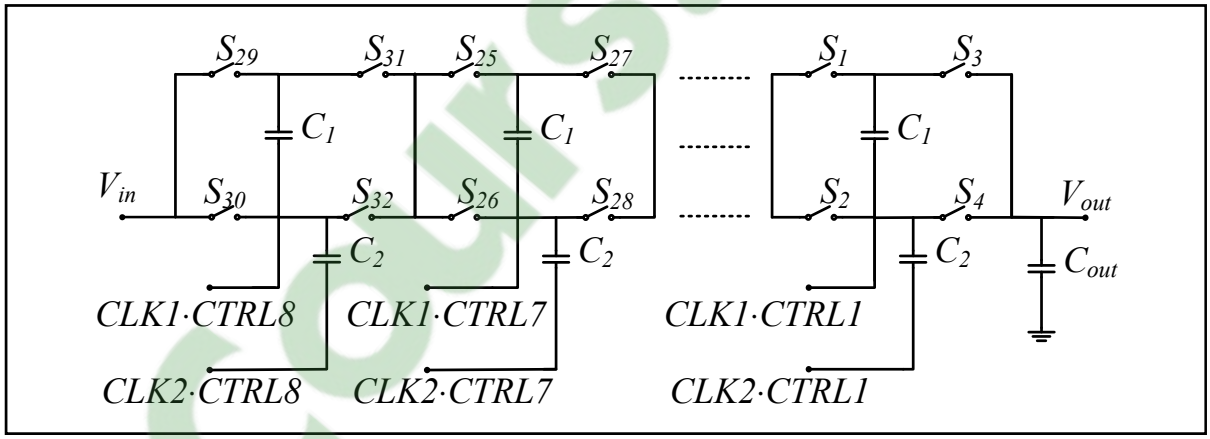

Figure 4.2 Conceptual schematic of the reconfigurable switched capacitor array

Table 4.1 Switched Capacitor Array Control Scheme

Active control signals (i.e., active clocks)	Active Switches	Output
CTRL1	S_1~S_4	$2V_{in}$
CTRL1~CTRL2	S_1~S_8	$3V_{in}$
CTRL1~CTRL3	S_1~S_{12}	$4V_{in}$
CTRL1~CTRL4	S_1~S_{16}	$5V_{in}$
CTRL1~CTRL5	S_1~S_{20}	$6V_{in}$
CTRL1~CTRL6	S_1~S_{24}	$7V_{in}$
CTRL1~CTRL7	S_1~S_{28}	$8V_{in}$
CTRL1~CTRL8	S_1~S_{32}	$9V_{in}$

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Traditional switched capacitor step-up DC-DC converters provide constant voltage gains. The pumping capacitors generate a step-up voltage in sequence (i.e., $2V_{in}$, $3V_{in}$, … $(N+1)V_{in}$, where N is the number of stages). Here, eight pumping stages are implemented to provide eight possible integer voltage gain values depending on the number of stages activated. Table 4.1 lists the switching schemes for the different gain settings.

In the practical implementation proposed here, this architecture has to satisfy application requirements. Realizing high-voltage charge pumps is limited by the breakdown of the MOS transistors used to implement the charge pump switches. As the voltage increases at every stage, and goes beyond the power supply voltage, these switches have to be biased and controlled carefully by applying suitable gate voltages that are higher than their source terminal voltages. To withstand high gate voltages, a positive voltage two-phase-clocked cross-coupled voltage doubler with threshold voltage cancellation is used in each stage (Favrat, Deval et Declercq, 1998). Triple-well NMOS transistors (Pelliconi et al., 2003), available in the selected process, are used to mitigate the limitation of the threshold voltage drop problem encountered in the Dickson design (Dickson, 1976), as the cross-coupled voltage doubler notably allows for an output that is independent of the threshold voltage of the transistors. The transistor implementation of the voltage doubler is adapted to the proposed design, and is shown in Fig. 4.3(a). Cascading this doubler enables higher output voltages, where the output voltage is ultimately limited by the breakdown voltage of the deep n-well / substrate diode. Accordingly, the proposed charge pump is implemented using a chain of eight cross-coupled voltage doublers, as shown in Fig. 4.3(b). The charge pump output voltage is given by (Pelliconi et al., 2003):

$$V_{out} = V_{in} + N\left(V_{Clk} \frac{C}{(C + C_{par})} - R_{out} \cdot I_{out} \right) \tag{4.1}$$

where V_{in} is the input voltage, N the number of stages, C_{par} the parasitic capacitance on the internal nodes of each stage, C the pumping capacitor, f_{Clk} the clock frequency, V_{Clk} the clock drive level, and I_{out} the output load current. The stage output resistance R_{out} is a nonlinear

function of the clock frequency and the on resistance of the transistors. It can be noted from (4.1) that in order to achieve variable output voltage levels in MEMS actuation applications, where the output current is very small due to the purely capacitive load, the clock drive levels or the number of stages can be varied. As such, in addition to the reconfigurable number of stages, in order to provide multiple and fractional gains, the clock amplitude voltage is varied and can be toggled for each stage.

Accordingly, two main control mechanisms are implemented (Doms et al., 2009; Ma et Bondade, 2013). Firstly, the control circuit sets the number of active stages, such that the input voltage is selectively increased depending on the number of stages that are activated. A stage is deactivated by disabling its clock. Secondly, the clock amplitude voltage, V_{dd_Clk}, is varied by the control circuit to control the output voltage as well. This allows for an area efficient design with minimized losses and versatile operation.

The timing relationship between the clock phases is important so that losses are minimized. As such, the charging and discharging clock signals are supplied by a two-phase non-overlapping clock generator carefully designed to avoid shoot-through current. The clock frequency is chosen to be of 50 MHz in order to allow for a rapid output rise time. Moreover, once the circuit reaches its voltage set point, the clock frequency can be reduced by the control circuit to lower the dynamic power consumption. This can be done because the typical load from electrostatic MEMS devices is capacitive and thus does not require a DC current.

A dynamic discharge stage is implemented to step-down the charge pump output voltage when needed as leakage current through the MEMS load is expected to be insufficient to allow for a sufficiently fast discharge. This stage is activated by the control circuit during the voltage transition and is then shut off to allow for steady-state.

To enhance the control of the switches and the tuning of the V_{dd_Clk} levels, a fully digital control is proposed.

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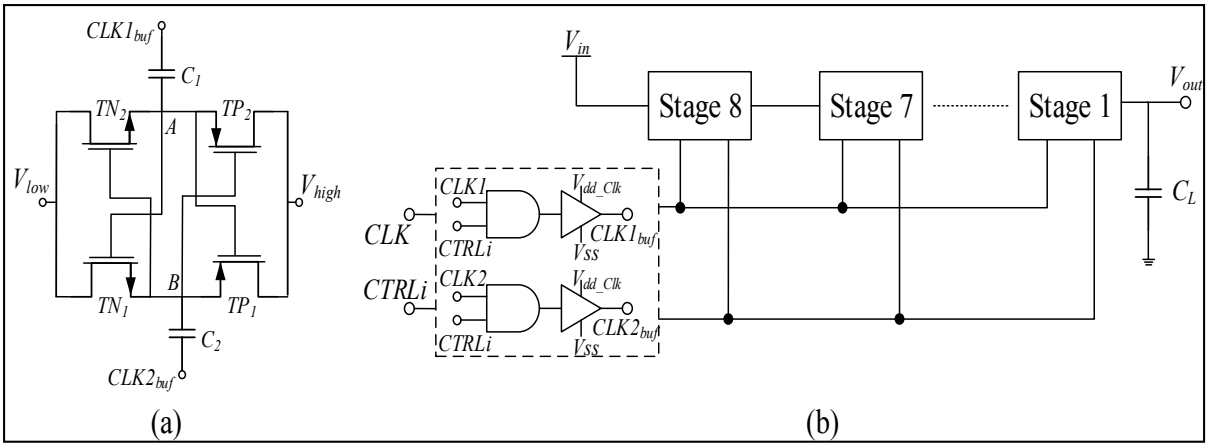

Figure 4.3 (a) Cross coupled voltage doubler stage (b) 8-stage reconfigurable charge pump block diagram (V_{in} is nominally 1.2 V)

4.3 Circuit Description

4.3.1 Voltage Doubler Cell

The cross-coupled voltage doubler cell shown in Fig. 4.3(a) has the bulk of the triple-well NMOS transistors (TN_1 and TN_2) and that of the PMOS transistors (TP_1 and TP_2) connected to their sources (Favrat, Deval et Declercq, 1998). The transistors are switched on and off by node voltages A and B, which are indirectly controlled by the clock signals through the pumping capacitors, C_1 and C_2. These internal capacitors are isolated from the output by the PMOS switches and they are implemented as metal-insulator-metal capacitors in order to minimize the chip area. The voltage doubler cell is symmetrical and is based on complementary operation. The two non-overlapping clocks, $CLK1_{buf}$ and $CLK2_{buf}$, are generated with nominally $V_{dd\_Clk} = V_{dd} = 1.2$ V and are fed to the bottom plate of the pumping capacitors. These clocks pump up the output voltage in an alternating fashion. At first, when $CLK1_{buf}$ is low and $CLK2_{buf}$ is high, node A remains at the stage's input voltage, V_{low}, while node B increases to $V_{low}+V_{dd\_Clk}$. Consequently, the gate voltage of TP_1 is sufficiently high to turn it off, while conversely the gate voltage of TP_2 turns it on such that the stage's output capacitance is charged to $V_{high} = V_{low}+V_{dd\_Clk}$. Inversely, when $CLK1_{buf}$ is high and $CLK2_{buf}$ is low, node A goes high, turning off TP_2 and charging the stage's output capacitor to V_{high} through TP_1. Accordingly, the cross-coupled structure keeps the output voltage at $V_{low}+V_{dd\_Clk}$. In addition,

nodes A and B swing between V_{low} and $V_{low}+V_{dd\_Clk}$ alternatively overcoming the threshold voltage drop problem (Tin Wai et al., 2014).

In addition to the parasitic bipolar effects, the breakdown voltage of the well / substrate diodes continues to be a limitation in designing high voltage charge pumps, it can be enhanced by using triple-wells. The use of triple-wells allows the bodies of the NMOS transistors to be biased independently at different voltages than ground. In the proposed charge pump, the deep-n-wells were biased to the output voltage (V_{high}) of the stage, the p-wells were biased to the input voltage (V_{low}) and the p-substrate was biased to ground, as depicted in Fig. 4.4. As such, the added n-well isolates the NMOS p-well from the substrate through the PN junctions. Due to the light doping of the substrate in comparison to the highly doped n+ diffusion, the breakdown voltage of the n+ / p-well junction is lower than that of the n-well / p-substrate junction (Baker, 2008). Moreover, its current leakage is higher. As such, the triple-well allows to increase the avalanche reverse breakdown voltage of the NMOS transistor junctions and reduces leakage current. In addition, connecting the bulk to the source results in a reduction in the MOSFETs on resistance. While the p-well / n-well junction limitation is mitigated by the triple-well, ultimately, the n-well / p-substrate junction remains the key voltage limitation because of its avalanche reverse breakdown voltage. This limits the maximum number of stages that can be implemented, hence some methods have been recently proposed to mitigate this limitation by biasing the NMOS bulk and deep n-well to an intermediate voltage and using polysilicon diodes over shallow trench isolation (Ismail et al., 2014). The operating gate-to-drain and gate-to-source voltages of the transistors used are specified as 1.2 V. If a yet higher input voltage was a design constraint (e.g. 3.3 V), then thick-oxide transistors would have to be used. However, the increased voltage gain per stage would require less stages to be cascaded, in order to prevent the deep n-well / substrate diode breakdown voltage of 11 V.

The transistor sizes are chosen to be relatively small in order to reduce overall area and allow for fast gate switching. Minimal channel lengths reduce on resistance leading to higher output voltage seen from (1). The W/L ratio for the NMOS transistors is 4 while the W/L ratio for the PMOS transistors is 5. The pumping capacitors are sized to 1 pF to reduce chip area.

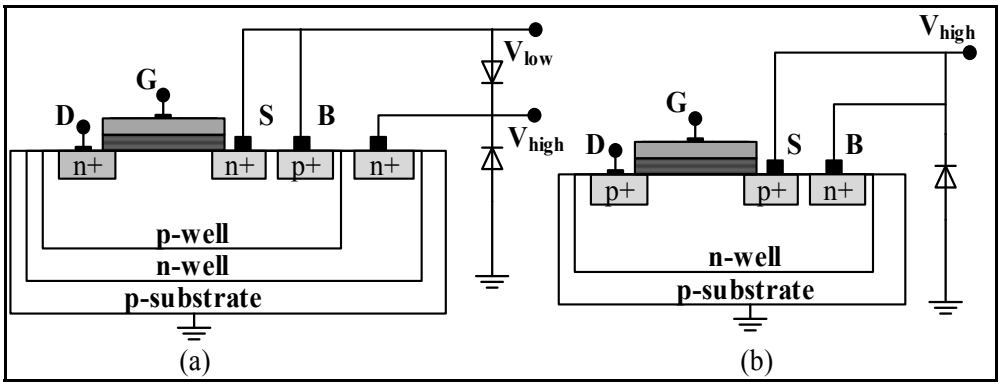

Figure 4.4 (a) Triple-well NMOS and (b) PMOS cross sections

4.3.2 Charge Pump and Control Circuit

To control the clock of each stage, a 4-to-8 thermometer decoder is implemented in the control circuit such that the number of active clocks can be varied by toggling control signals, *CTRLi*, as shown in Fig. 4.5. When *CTRL1* to *CTRL8* are high, the charge pump operates with all eight stages. For instance, the number of stages can be reduced to seven by making *CTRL8* low. This stops the switching of the capacitors of the stage by the clock, and their plate connected to the buffers goes low, while the other plate remains high. The stage is off, and the result is a charge pump with seven stages. Further reduction of the number of stages is done in the same way: one by one the stages are turned off by making more of the *CTRLi* control signals low, as indicated in Table 4.1.

To generate the two non-overlapping clocks for the charge pump, a standard NAND latch-based circuit was used (Martin et Sedra, 1981). These clocks signals have to achieve minimal delay and fast switching to preclude the charging and discharging switches from being on at the same time, i.e. prevent the reverse path that will be created from the higher voltage back to the lower voltage. The two clocks generated are connected to the voltage doubler cells through logic and a buffering inverter chain to generate $CLK1_{buf}$ and $CLK2_{buf}$, as shown in Fig. 4.5. Notably, the last inverter of the driver chain is not connected to V_{dd} but instead to a variable voltage, V_{dd_Clk}, in order to control the clock amplitude. This effectively level shifts down the

output of the driver chain into the pumping capacitors. Figure 4.6 shows the input clock, the pair of non-overlapping generated clocks, the pair of buffered non-overlapping generated clocks in an on-state with $V_{dd\_Clk} = 1$ V (as an example), and the pair of non-overlapping generated clocks in an off-state.

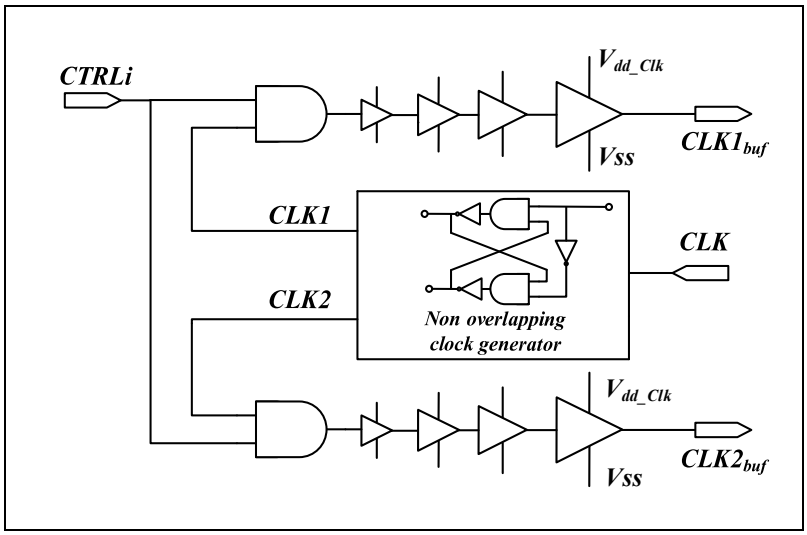

Figure 4.5 Schematic of the clock control cell with the non-overlapping clock generator

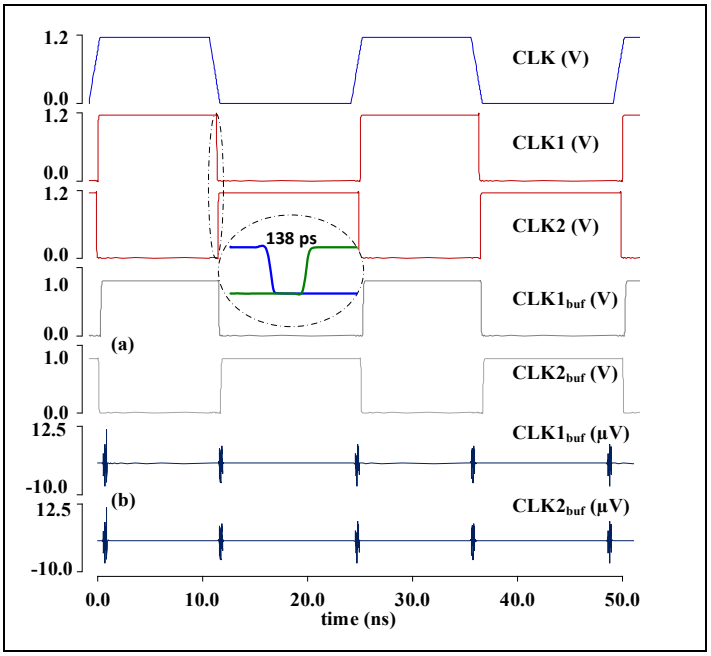

Figure 4.6 Charge pump clock waveforms for $V_{dd\_Clk} = 1$ V in (a) on-state (*CTRLi* high), and (b) off state (*CTRLi* low)

The control of the clock amplitude voltage, V_{dd_Clk}, is done using a 3-to-8 decoder along with a 3-bit resistive chain digital-to-analog converter implemented in the control circuit such that 8 values of V_{dd_Clk} can be generated between 0.5 V and 1.2 V with an increment of 0.1 V. During testing, the circuit was characterized with values of V_{dd_Clk} ranging from 0 to 1.2 V to justify the low voltage output range of the digital-to-analog converter.

Overall, a total of 7 bits of control are required to change the voltage level: 4 bits are used to set the number of active stages and 3 bits to set the clock drive level. In addition, the discharge stage (on/off) and clock frequency (high/low) are controlled with 2 additional bits. The 9 bit programming word containing the required digital control parameters is illustrated at the bottom of Fig. 4.1.

4.3.3 Discharge Stage

Figure 4.7 shows the discharge stage which is immune to voltage breakdown. It is connected to the output of the charge pump to step-down the output voltage when needed with no significant impact on power consumption. A stack of transistors is implemented to gradually decrease the high drain voltages, in order to prevent the gate oxide breakdown of the discharge transistors. The appropriate gate voltages of the discharge transistors are provided from the intermediate voltage levels of the charge pump: the output of the sixth (V_6), fourth (V_4) and the second (V_2) stages. Signal DIS is a 1.2 V pulse that controls the discharge time.

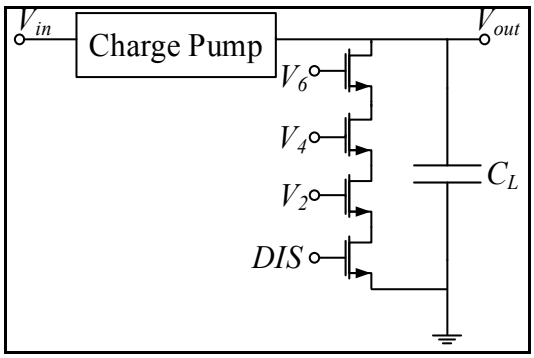

Figure 4.7 Schematic of the output discharge stage

4.4 Simulation Results

The reconfigurable charge pump is designed and fabricated in 0.13 μm CMOS technology from Global Foundries. As was previously stated, the target application is a MEMS electrostatic actuator that is capacitive in nature. The expected actuator capacitance is on the order of hundreds of femto farads and along with the pads and packaging it is modelled as 1 pF capacitor. Moreover, the packaging bond wire was modelled as a 1.5 nH inductor, and the oscilloscope probe was modeled as a capacitance (3.9 pF) and resistance (10 MΩ). This load was used in simulations and measurements. Larger capacitive loads (i.e. 1 nF) were also considered, and did not significantly affect the maximal voltage attained by the circuit or its switching noise, but resulted in a slowdown in the rise time of the output, as can be expected (Dickson, 1976; Tanzawa et Tanaka, 1997). As the proposed circuit is meant to be used as a capacitive MEMS driving circuit, the following simulation and measurements results are focused on the 1 pF capacitive load.

The dynamic behavior of the circuit when varying the number of stages and the clock drive levels can be seen in Fig. 4.8, based on simulations and assuming a purely capacitive load. Figure 4.8(a) shows the output voltage, Fig. 4.8(b) shows the intervals when the discharge stage is turned on in order to reduce the output voltage, Fig. 4.8(c) shows the high clock frequency during charging and discharging phases and the low clock frequency during steady state, and Fig. 4.8(d) shows the supply current variation and the average power consumption. Control settings are also shown in the figure. A maximum output voltage of 10.6 V is achieved. Two clock frequencies (high / low) are used. A 50 MHz clock frequency was chosen to ensure fast rise times of the output voltage for effective MEMS actuation, and the clock frequency is reduced in steady-state operation to reduce power consumption. While in simulation, a 1 MHz low-clock frequency is shown, it is to be noted that in measurements the lowest clock frequency that could be used was of 8 MHz because of the presence of output leakage due to the 10 MΩ load of the oscilloscope while testing. However, this is not a foreseen issue in a MEMS application when a purely capacitive load is present.

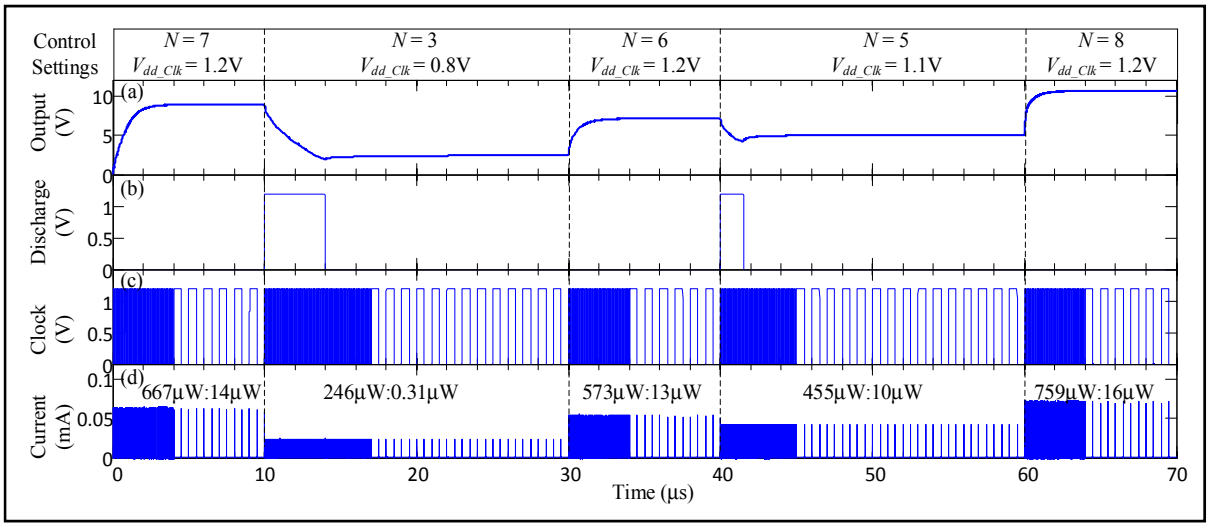

Figure 4.8 Dynamic behavior of the system: (a) output voltage (b) discharge signal (c) clock, and (d) supply current and average power consumption

The output load of this circuit is meant to be a MEMS capacitive actuator such that there is no significant output DC current delivered. In such cases, the current delivered is negligible when the switching frequency is sufficiently high while charging the capacitor or while the charge pump settles at its steady-state voltage. The charge pump efficiency is therefore not a representative metric. However, the dynamic power consumption can be significantly reduced by decreasing the frequency of the clock after steady-state, reducing the power consumption of the circuits that are ancillary to the charge pump. For instance from Fig. 4.8(d), the circuit dissipates an average of 759 µW when the eight stages are activated and the maximal output voltage is generated, and after the settling time, as the clock frequency drops down to 1 MHz, the circuit only consumes 16 µW.

Process and temperature variations are a concern in circuit design and implementation, and analysis on reliability has been discussed in works such as (Yuan et Bi, 2015). This is important in high voltage circuits such as that presented here. Accordingly, corner and Monte Carlo analyses were carried-out to validate the design. Corner analysis shows good process stability of the circuit, resulting in an output voltage variation of 30 mV and a rise time variation of 160 ns between the *slow / slow* and *fast / fast* corner conditions, while simulations over temperature showed a variation of 20 mV and a rise time variation of 100 ns between -40 and

100 ºC. Monte Carlo analysis performed via 100 simulations showed a standard deviation of 7.1 mV for the maximum output voltage 10.6 V. Note that no circuit failures or significant performance spread due to process and temperature variations were observed in measurements during the testing of the design. These measurements are presented in the next section.

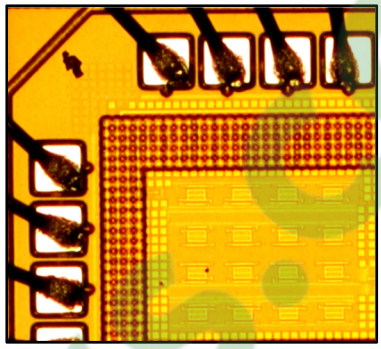

Figure 4.9 Micrograph of the 0.13 µm CMOS charge pump

4.5 Measurement Results

A micrograph of the circuit is shown in Fig. 4.9. The layout of the overall circuit occupies an area of 215 µm × 300 µm in which compactness, symmetry, and reduced parasitic capacitances are taken into consideration.

One of the key features of the design is the generation of multiple voltage levels and this is depicted in Fig. 4.10(a) and Fig. 4.10(b). In Fig. 4.10(a), a variation of the number of stages from 0 to 8 is carried out. The resulting varying output voltage is shown and matches well that attained in simulations. Figure 4.10(b) demonstrates the measured and simulated response when varying the clock voltage from 0 V to 1.2 V with 8 active stages. Simulations and measurements show similar results here as well. Reducing the clock voltage has implications on the rise time, as it reduces the driving ability of the clock inverter. Moreover, clock levels below 0.4 V reduce the output voltage significantly, as they are below the optimal operating threshold of the inverter. This warrants the use of a minimal operating voltage for V_{dd_Clk} of 0.5 V.

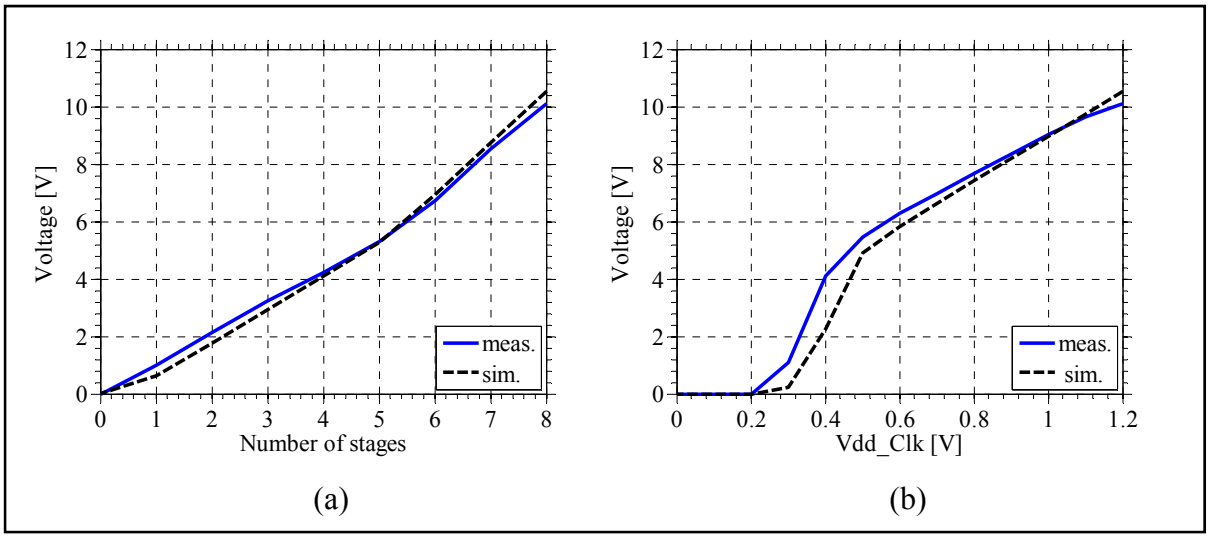

Figure 4.10 Output voltage variation for (a) different number of active stages, and (b) different clock drive voltages

To further analyze the difference between simulation and measurement and to understand the behavior of the designed circuit, a study has been performed on a wide clock frequency range limited on the higher end to 120 MHz by the clock generator used. The results of this analysis on the maximal output voltage is shown in Fig. 4.11(a). The inset of Fig. 4.11(a) shows the variation of the output voltage as a function of frequency in the below 1 MHz clock frequency range. The output voltage increases steadily until 8 MHz, as the leakage current is offset by the faster pumping of the charge. The maximal output voltage remains almost constant across the range from 8 MHz to 90 MHz. The higher clock frequencies lead to lower output voltage because of the circuitry's driving speed limitations. The lower frequency range is limited to 8 MHz because of the increased leakage current caused by the resistive part of the oscilloscope probe (3.9 pF and 10 MΩ). The current consumption for different clock frequencies is studied and shown in Fig. 4.11(b), showing that significant power saving can be achieved by reducing the clock frequency in steady state. In this figure, the eight stages are activated and the maximal output voltage is generated. This current consumption is attributed to both the supply voltage and the clock voltage, V_{dd_Clk}. Results presented in Fig. 4.11(b) also show good agreement between simulation and measurement when the oscilloscope load is considered in simulations. The slight deviations are attributed to variations in the actual leakage current from that

considered in simulations and to the potential variation in parasitics. This can also be the cause for the slightly reduced measured output voltage seen in Fig. 4.11(a).

The measured dissipated power at a clock frequency of 50 MHz, when the eight stages are activated and the maximal output voltage is generated (V_{dd} = V_{dd_Clk} = 1.2 V) is of 864 µW. At 8 MHz, this power consumption is reduced to 252 µW, in line with what is expected based on the fact that the majority of the power consumption scales linearly with the clock. This scaling is offset by the power consumption of the ancillary electronics.

With a load of 1 pF modelling the MEMS electrostatic actuator and with the oscilloscope probe, the measured output voltage reaches a maximum value of 10.1 V. In this state, a rise time of 7 µs, and a fall time of 611 µs are observed, as shown in Fig. 4.12(a) and (b), respectively. The discharge performance could be improved by increasing the size of the discharge transistors. Note that most MEMS have mechanical time constants on the order of 0.1-1 ms, and this charge pump is sufficiently fast to accommodate their actuation.

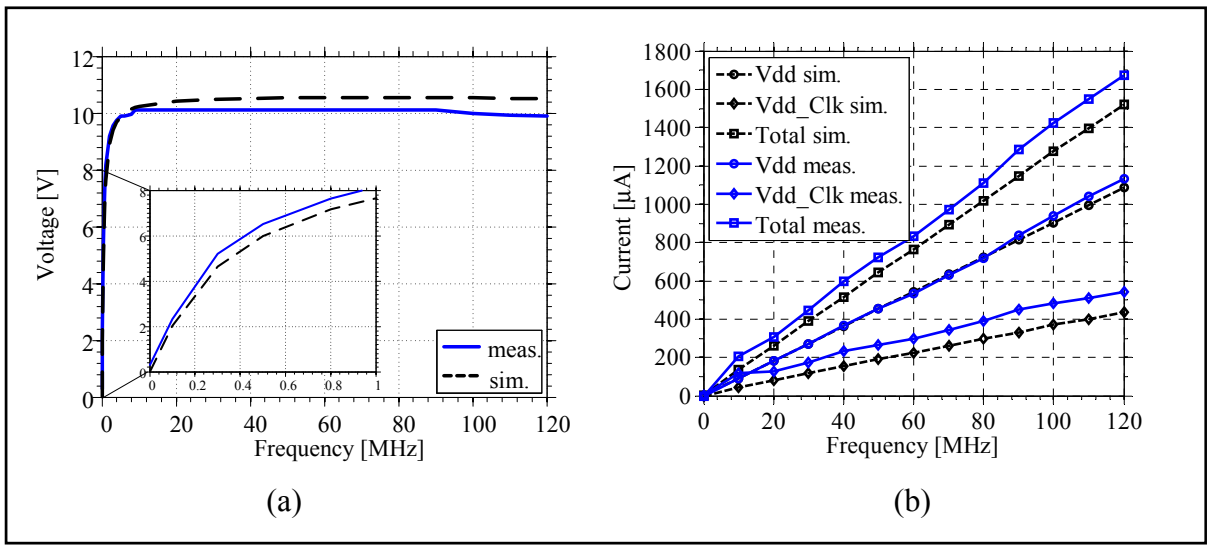

Figure 4.11 Measured impact of the clock frequency on (a) the output voltage and (b) the current consumption

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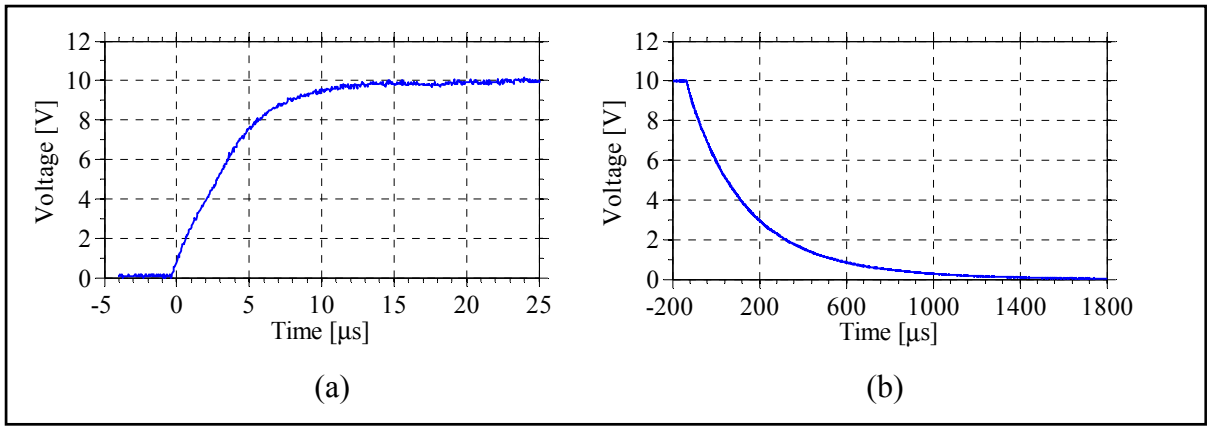

Figure 4.12 Transient measurements showing the output (a) charging and (b) discharging

Output ripple is mainly caused by switching noise. This is shown in Fig. 4.13(a), where a non-averaged DC-decoupled time measurement is plotted in steady-state for a clock frequency of 50 MHz and maximal output voltage of 10.1 V.

This output noise has an rms value of 4 mV and peak to peak value of 15 mV. To characterize the frequency content of the charge pump output, Fig. 4.13(b) plots the *averaged* output voltage spectrum when the charge pump is activated and when it is turned off. The spectrum has an integrated rms value of 2.2 mV when the charge pump is activated, and of 0.9 mV when the charge pump is turned off. The main ripple components are expectedly at the clock frequency and its harmonics, and the noise floor is not significantly increased when the charge pump is turned on. This confirms that the output ripple can be directly filtered mechanically by the MEMS or by using a low-pass filter at the charge pump output, as the ripple frequency is much higher than the resonant frequency of typical MEMS that typically lies in the 1-100 kHz range.

Figure 4.14 illustrates the different measured output voltage possibilities measured by varying the number of stages and clock drive levels, illustrating the versatility of the circuit. Fine output voltage control is achieved between zero and 10.1 V. Assigning any fixed output voltage level within this range can be done by selecting the stage number then the clock drive level or vice versa. The selection algorithm will depend on charging speed and power consumption requirements.

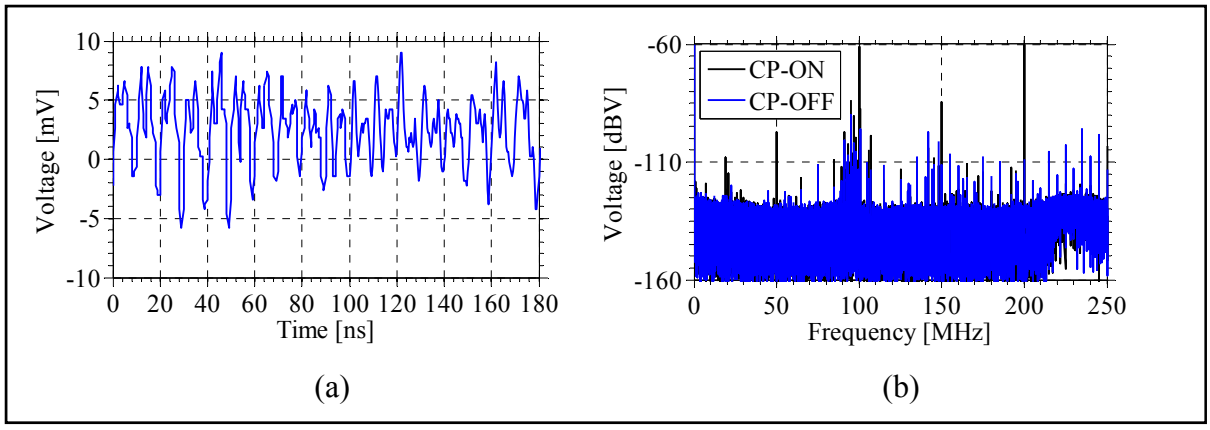

Figure 4.13 (a) DC-decoupled transient switching noise at the maximal output voltage, and (b) the averaged output noise spectrum when the charge pump is activated and turned off

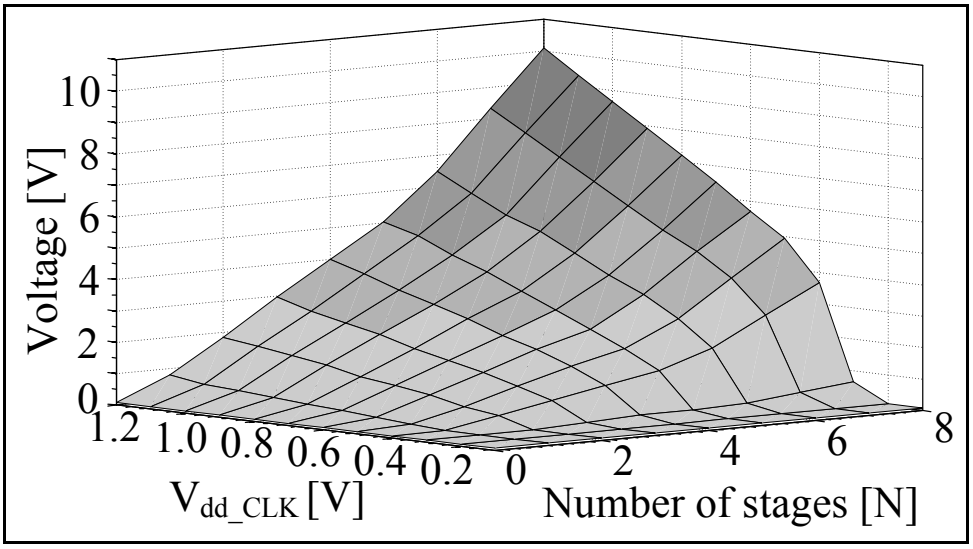

Figure 4.14 Measured output of the reconfigurable charge pump versus the clock drive level, V_{dd_Clk}, and the number of stages, *N*

4.6 Discussion

The fabricated chip behaved as designed with a slight reduction in maximal output voltage. The charges lost through stray capacitances and in the form of a leakage current through the substrate slightly reduced the output voltage gain (Innocent et al., 2003). Notably, the capacitive parasitics associated to the package and PCB are believed to have some impact, while a large portion of the layout parasitics on the internal nodes of the stages and the bottom plate parasitic capacitance of the switch capacitors are considered to have been taken into

account in simulations. Moreover, as the clock generation circuitry required a chain of progressively larger driving transistors, the associated numerous reverse biased diodes are presumed to have caused some additional leakage currents that may have been part of the slight reduction in the maximal output voltage observed in measurements (Joung-Yeal, Young-Hyun et Bai-Sun, 2009). In addition, it is to be noted that leakage current and non-modelled stray capacitance both increase the circuit's static and dynamic power consumption, respectively and can explain the variation between the measured and simulated power consumption. Table 4.2 summarizes the performance of the charge pump in comparison to other works, where different charge pumps for MEMS applications are compared to a baseline reference (Pelliconi et al., 2003). The proposed design features one of the lowest supply voltages, with a relatively high attained voltage gain per stage (i.e., (V/V)/stage). As such, the proposed design yields the most amount of voltage from a 1.2 V supply with eight stages while others used either more stages or a higher supply voltage. The low supply voltage is advantageous as it allows for finer tuning of the output voltage of the MEMS actuator by enhancing the tuning resolution achievable through the modulation of the number of stages. More bits could be used at V_{dd_Clk} to compensate for a coarser resolution, but matching the number of drive levels in V_{dd_Clk} with the numbers of stages, allows for a well spread tuning characteristic, such as seen in Fig. 4.14. In addition, the use of thin-oxide transistors made possible by the low supply voltage allows for a smaller circuit area, which is important if a multiplicity of independent charge pumps need to be placed on a single die to drive multiple MEMS actuators. This also yields lower parasitics which improves the voltage gain per stage. Finally, more and more CMOS technologies are moving to lower supply voltages and the operation at relatively low voltage makes the proposed circuit well-suited to this.

The design occupies a relatively small area of 0.0645 mm^2. Note that the area reported includes the complete system (i.e. charge pump, clocking, control etc.). Moreover, the proposed design features a digital control mechanism for the actuation of MEMS capacitive loads using a reconfigurable charge pump. While the step size voltage tuning is not uniform, as seen in Fig. 4.14, the average output tuning voltage resolution is of 0.19 V (<2% of full range). As the circuit is digitally controlled, this resolution can be further improved by increasing the DAC

resolution to provide finer values of clock drive levels, notably in the higher output voltage range. In addition to the configurable output, fast rise time, low ripple voltage achieved by the voltage doubler, minimized power consumption stemming from the controlled clock frequency, and a design leveraging the driving of a MEMS capacitive load, are other benefits of the proposed circuit that make it compare favorably to other works.

4.7 Conclusion

This paper presented a non-conventional reconfigurable charge pump tailored to electrostatic MEMS actuation. The output voltage can be digitally controlled to generate a measured tunable voltage of up to 10.1 V, with a 0.19 V average tuning resolution, and an output ripple that is below 4 mV_{rms}. This ripple that can be readily filtered by a typical MEMS device mechanically or by a standard low pass filter. A rise time of 7 µs and a fall time of 611 µs at a 50 MHz clock are achieved. By leveraging the purely capacitive load that is characteristic of MEMS electrostatic actuators, the power consumption of the circuit can be reduced in steady-state by lowering its clock frequency. The circuit has a power consumption of 864 µW for a 50 MHz clock at the maximal output voltage, and has a reduced power consumption of 252 µW for an 8 MHz clock. These specifications makes the proposed circuit a versatile biasing circuit well-suited to MEMS electrostatic actuation. The relatively small area allows for the integration of the circuit with a MEMS within the same package or the use of several such biasing circuits for MEMS that require multiple actuation voltages. Notably, an extension of this design to high voltage technology (0.8 µm HV CMOS) for 300 V operation has recently been proposed in (Beaulieu et al., 2016).

Acknowledgment

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Table 4.2 Charge Pump Performance Summary And Comparison

Reference	(Pelliconi et al., 2003)	(Richard et Savaria, 2004)	(Shirane et al., 2011)	(Innocent et al., 2003)	(Hong et El-Gamal, 2003)	This work
CMOS technology	0.18 µm	0.8 µm	0.18 µm	0.18 µm	0.18 µm	0.13 µm
Supply voltage (V)	1.8	5.0	3.3	1.8	1.2	1.2
Max output voltage (V)	10.1	20.0	16	14.8	14.8	10.1*
Number of stages	5	5	11	10+1	16	8
Voltage gain per stage ((V/V) / stage)	1.12	0.8	0.44	0.74	0.77	1.05
Output tuning resolution (V)	N/A	N/A	N/A	N/A	N/A	0.19††
Clock Frequency (MHz)	100	10	46	50	75	50
Rise time (µs)	0.5	250	N/A	N/A	65	7
Ripple voltage (mV)	400	400	N/A	N/A	150	15
Load Impedance	30pF	28pF	10MΩ	22pF	27pF	1pF**
Power Consumption (µW)	N/A	N/A	6.6mW	N/A	N/A	864 / 252†
Output current(µA)	350	25	N/A	1000	N/A	N/A**
Area (mm^2)	N/A	0.03	0.0575	0.129	0.72	0.0645

*Digitally reconfigurable. **Designed for MEMS capacitive load. †High/Low clock frequency. ††Average.

CHAPTER 5

TOWARDS AN INTEGRATED ENERGY HARVESTING SYSTEM FOR IOT SENSOR NODES

5.1 Introduction

In the previous chapters, cantilever-based piezoelectric vibration energy harvesters and circuits have been discussed. In chapter 2 the effects of the proof mass geometry has been studied, then in chapter 3 the impact of the beam geometry on the performance has been studied. In chapter 4 a dynamically reconfigurable charge pump circuit that is used for electrostatic MEMS actuation has been presented, and could be used with MEMS energy harvesters. In this chapter the results of these previous chapters are leveraged towards a complete system for IoT sensor nodes. As a result, some optimized designs and concepts have been put together towards a complete integrated system. Due to time constraints, further elaborations are to be completed in future work.

The increasing demand for autonomous sensor nodes and the search for alternative power sources to batteries have led to sustained interest in energy harvesting. Specifically, MEMS piezoelectric vibrational energy harvesters could present a solution to the power requirements. Autonomous sensor nodes have been the motive behind numerous work, with the concept shown in Fig. 5.1. An energy harvester could be used to extend the life of the energy storage unit, if not replace it, to power a sensor and a microcontroller that communicate the collected data through a wireless transceiver. This concept is a target that applies to most IoT sensor nodes.

Design, fabrication and characterization of MEMS cross-shaped piezoelectric vibration energy harvesters are presented here. Their resonance frequency has been studied as a function of their geometry. Accordingly, two cross-shaped piezoelectric energy harvesters featuring a central mass with four beams have been designed operating at resonance frequencies of about 4.3 and 5.3 kHz respectively (Alameh et al., 2018a). The proposed cross-shaped design with a center

mass, less susceptible to fracture, presents the advantage of having four cantilever harvesters. These cantilevers are rectangular in the first design and trapezoidal in the second. Moreover, increasing this center mass by adding extra masses to the corners would yield better performance. This increases the average strain, lowers the frequency, and results in multiple resonant modes in the range 4-5 kHz. Two power conditioning circuits have been fabricated in 0.35 µm CMOS technology. A cross-coupled rectifier circuit and a two-stage Cockroft-Walton circuit with DTMOS diode connected transistors has been tested to be combined with the harvester to attain an integrated microsystem.

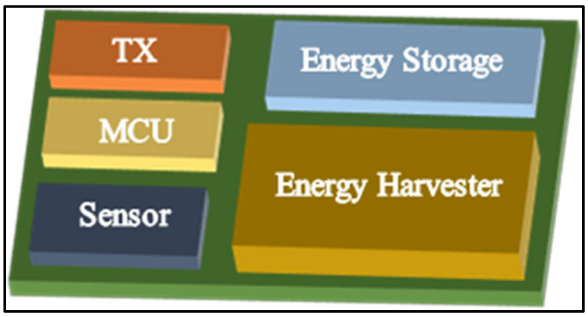

Figure 5.1 Autonomous wireless sensor node concept

5.2 MEMS Cross-Shaped Piezoelectric Vibration Energy Harvesters

Based on the recommendations of the studies performed in previous chapters, we present a novel design concept of a higher performance and wider band cross-shaped designs. In what follows, the design, simulations, fabrication process and measurement results of the MEMS vibrational energy harvester will be presented.

5.2.1 Design and Simulations

The MEMS piezoelectric energy harvesters studied here has a cross-shaped, as depicted in Fig. 5.2(a). It can be simplified to a set of rectangular cantilevers, clamped at one end and with a proof mass attached at the free ends. The piezoelectric layer covers the beams. It is sandwiched between two electrode layers and excited in the d31 mode where the induced voltage is across each beam's thickness and the strain along each beam's axis. The lumped

model, Fig. 5.2(b), shows a free to move proof mass suspended to a fixed frame with four springs. The behavior can be described as a mechanical spring-mass-damping system coupled to the electrical domain through a transformer that converts a strain to current.

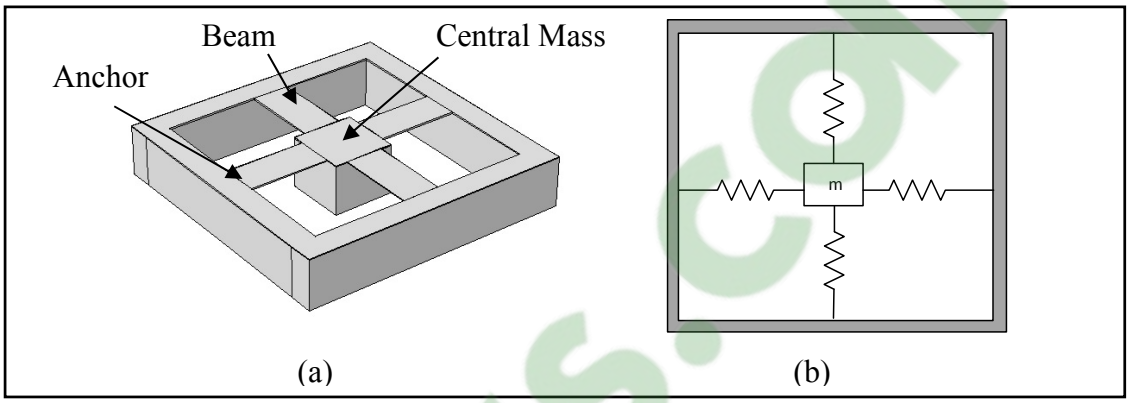

Figure 5.2 Piezoelectric harvester: (a) Cross-shaped harvester and (b) Cross-shaped lumped model

A model of a cross-shaped harvester has been created in COMSOL Multiphysics. A wide variation of frequencies can be achieved by adjusting the dimensions, within the same area. As a result, a study on the cross-shaped harvesters has been performed to help select the best dimensions possible within the available area. The design area is limited here to 1800 μm by 1800 μm. Two sets of simulations have been performed. The first one fixing the beam width to 300 μm and varying the square mass length from 300 to 800 μm (consequently beam length from 1050 to 800 μm). The second simulation varying the beam width from 100 to 500 μm while fixing mass length to 500 μm (beam length 650 μm). Figure 5.3 shows the simulation results, in line with the conclusions in chapter 2. A minimum frequency still occurs while varying the mass size, and beam width reduction will lower the resonant frequency.

Figure 5.4 shows the two proposed designs: (a) checkerboard straight (CBS) and (b) checkerboard trapezoidal (CBT) designs. The first one uses four rectangular beams connected to a central proof mass while maximizing the proof mass area by adding four extra masses to the corners of the central mass to form a "checkerboard mass". These extra masses further lower the frequency and increase the output power. The second design uses trapezoidal beams

were a more uniform strain would increase the power at a cost of slightly higher frequency. The advantage of the cross designs is having four cantilevers connected to the proof mass, instead of one, also resulting in a more robust design less susceptible to fracture (more resilient than the T- design) in the presence of a large proof mass.

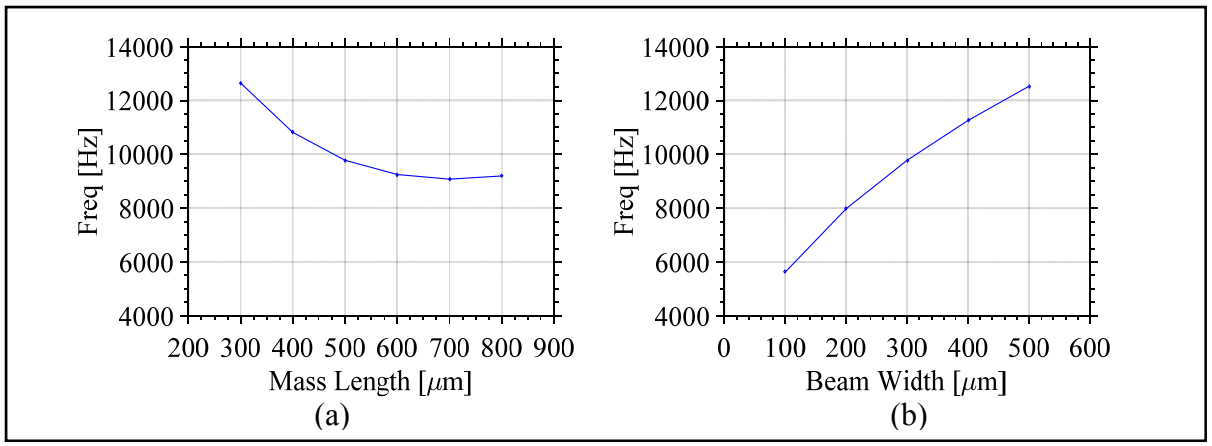

Figure 5.3 Effects of varying (a) the square mass side lengths and (b) the widths of the beam on the value of the first Eigen frequency of the structures

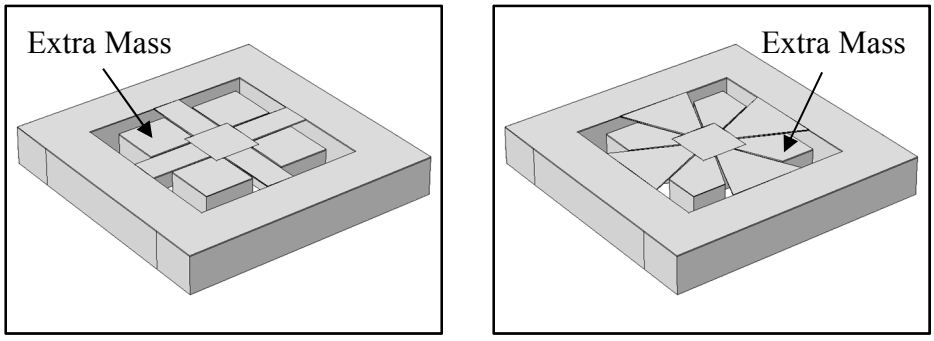

Figure 5.4 Proposed harvester: (a) Checkerboard straight (CBS) and (b) Checkerboard trapezoidal (CBT) designs

The available surface for these designs has been defined as a square of 1800 by 1800 μm^2. All the design dimensions are presented in Table 5.1. Each design is composed of a square central mass of 2.328×10^{-4}g with side lengths of 500 μm and depth of 400 μm. The four beams are 650 μm long. The straight beams are 300 μm wide while trapezoidal beams are of 800 μm anchored width and 200 μm non-anchored. The extra mass of the CBS design is of 1.25 ×

10^{-3}g. It has a total mass area 1346822.8 μm^2 (central and four petals) with each petal area 274205.7 μm^2 and the extra mass of the CBT design is 1.1×10^{-3}g with total mass area 1154154.4 μm^2 and each extra area 226038.6 μm^2.

The resonant frequency of these designs has been obtained by an Eigen frequency simulation in COMSOL Multiphysics with a vertical body load force due to an acceleration along the z-axis. The first three mode shapes for both designs are shown in Fig. 5.5. Three resonant modes are within a 500 Hz range all below 5.5 kHz. The third Eigen frequency of CBS is of 4263 Hz, and that of CBT is of 5491 Hz. This frequency range was selected as a trade-off between silicon area of the harvester designs and their resonant frequency in order to fabricate these devices in the commercial MEMS process. It is important to note that these frequencies can be scaled to other ranges depending on the size of the piezoelectric energy harvesters considered, in order to target desired applications.

To highlight the advantage of using the extra mass, Fig. 5.6 shows the first principal strain distribution of two designs, without and with extra mass, along a cut line straight through the middle across the total structure length. In Figure 5.6(a), about 325 μstrain is at the anchor then this starts decreasing along the first beam length till it reaches its minimum at 350 μm of the beam length after which the mass raises this strain to 120 μstrain at 650 μm, the end of the beam. On the mass, there is no strain for 500 μm then the same strain distribution is observed on the second beam. Most of the strain is concentrated near the clamped end of the beams and by increasing the mass this strain increases, hence lowering the frequency and increasing the output power. The advantage of the extra masses can be seen in Fig. 5.6(b) where the strain reaches 2400 μstrain at the mass and 1200 μstrain at the anchor.

Table 5.1 Fabricated Design Parameters

Design	Beam(μm) $L_b \times W_{b1} \times W_{b2} \times H_b$	Central Mass(μm) $L_m \times W_m \times H_m$	Extra Mass Volume (μm^3)
CBS	650×300×300×10	500×500×400	4×274205.7×400
CBT	650×800×200×10	500×500×400	4×226038.6 ×400

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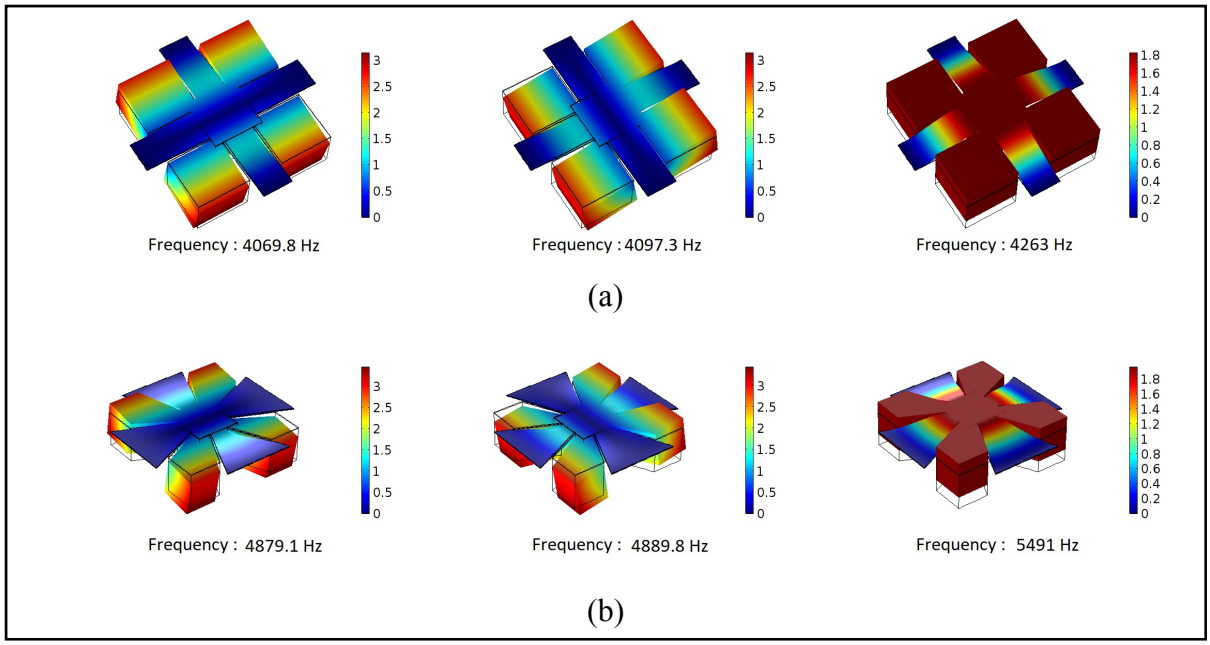

Figure 5.5 First three resonant modes of (a) CBS and (b) CBT designs

Figures 5.7(a) and (b) shows the corresponding simulation voltages of CBS and CBT, respectively. The maximum output voltages of 775 mV for CBS and 2.4 V for CBT are obtained across a 1MΩ load, and is computed for a harmonic excitation acceleration of 8g on the harvester generating a maximum power of 0.6 µW and 5.76 µW respectively. The higher voltage levels due to the extra mass helps the power conditioning circuit as will be discussed later.

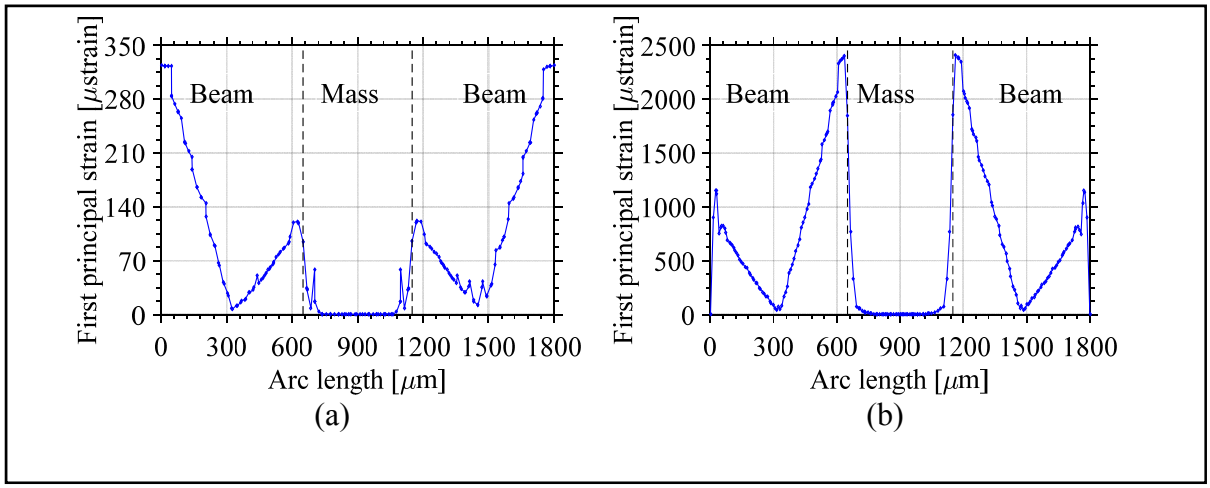

Figure 5.6 First principal strain distribution of (a) Design 1 and (b) Design 2

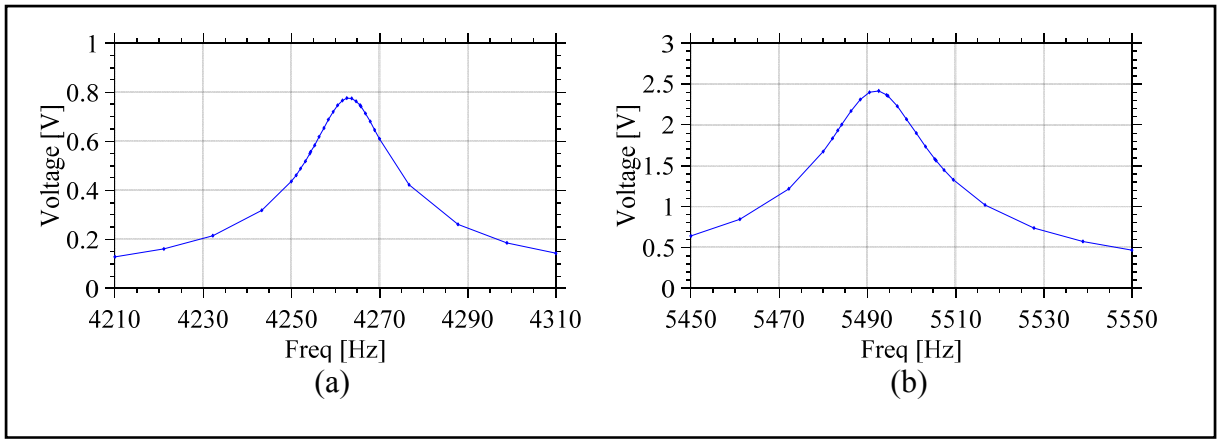

Figure 5.7 Simulation output voltages (a) CBS and (b) CBT designs

5.2.2 Fabrication Process

The devices were fabricated using PiezoMUMPs process. A commercial technology provided by MEMSCAP. It is a five mask process that uses AlN as the piezoelectric material. Figure 5.8 shows a cross sectional and top view of the CBS design using the above process. The beams are mainly comprised of a 0.5 µm AlN piezoelectric thin film deposited by reactive sputtering onto a 10 µm doped silicon device layer. A top metal layer comprised of 20 nm Cr and 1 µm Al deposited by beam evaporation to cover the top piezoelectric active region. The proof mass is constructed from an unetched suspended silicon substrate 400 µm thick. Fig 5.9 shows a micrograph of the two fabricated designs CBS and CBT.

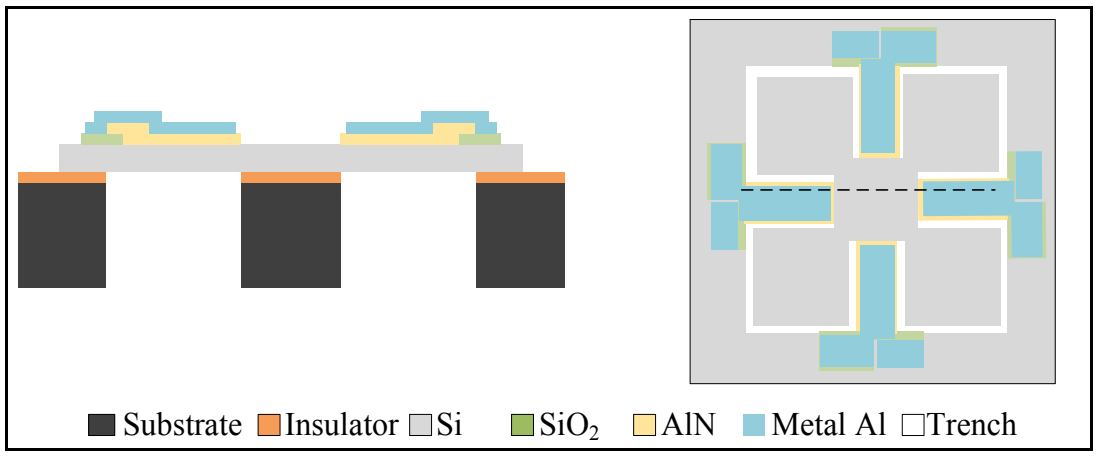

Figure 5.8 Cross-sectional and top view of the fabrication process

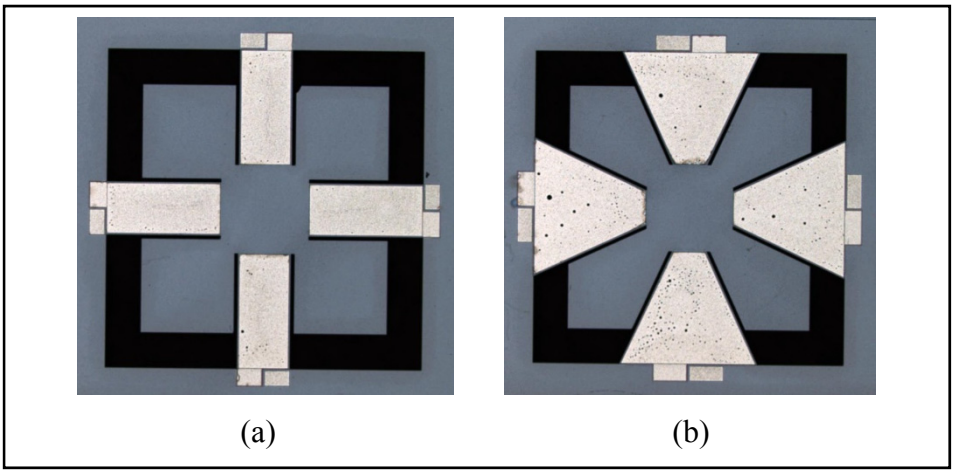

Figure 5.9 Micrograph of the fabricated (a) CBS and (b) CBT designs

5.2.3 Measurement Results

A vector network analyzer VNA has been used to characterize the harvesters. This permits the measurement of the resonance frequency of the structures using a probe station and DC needles as seen in Fig. 5.10(a). By using two DC needles, connecting port 1 of the VNA to the signal pad and port 2 to the ground pad, the measurement of the transmission coefficient S_{12} or S_{21} allows us to measure the resonance frequency of the structure. The measured resonance frequencies of CBS and CBT seen in Fig. 5.11, show good agreement with what have been simulated.

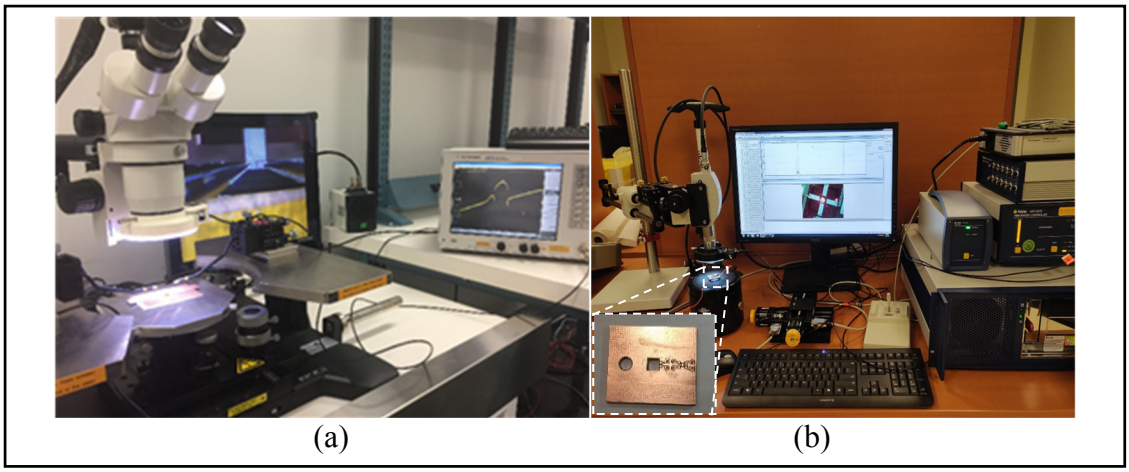

Figure 5.10 Measurement setup (a) Probe station and (b) Vibrometer. Inset shows custom PCB used for testing

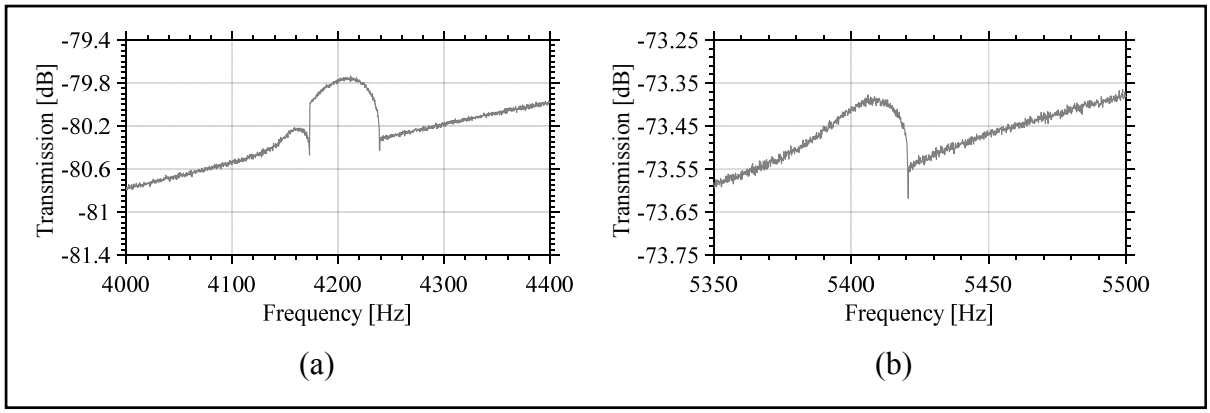

Figure 5.11 Resonance frequency of the fabricated (a) CBS and (b) CBT designs

The use of a vibrometer allows the measurement of the frequency response in terms of velocity at any point on the fabricated design. The test setup is shown in Fig. 5.10(b). Performing these measurements requires the placement of the structure under the laser beam used. This structure must then be excited. This excitation can be electrical or mechanical. If an electrical type excitation is chosen, then we could use a function generator. We can perform a frequency sweep at a voltage of defined amplitude (or acceleration if mechanical excitation is used) to measure the speed. This measurement can be performed using the temporal acquisition mode of the vibrometer and then implement a Fourier transformation on the signal in order to obtain the frequency response. The temporal acquisition mode does not allow the direct visualization of the frequency response of the system and a signal processing step is necessary, this method makes it possible to acquire a maximum of $2^{26} = 67$ million points as opposed to 12800 points in frequency acquisition mode. The maximum frequency resolution is therefore much higher by using this measurement mode. The result of these measurements is presented in Figure 5.12.

Using a "stage" under the vibrometer, allows us to automate these measurements and thus measure the response of the structure at several points when subjected to the same excitation. The signal processing of all of these points allows us to perform the scan of these structures and thus to visualize the resonance mode of the structure at a given frequency. We did visualize the mode shape of the fabricated devices by scanning $50 \times 50 = 2500$ points linearly spaced in a grid. Figure 5.13 shows the scan performed at the first resonance mode frequency of CBS and the third resonance mode of CBT.

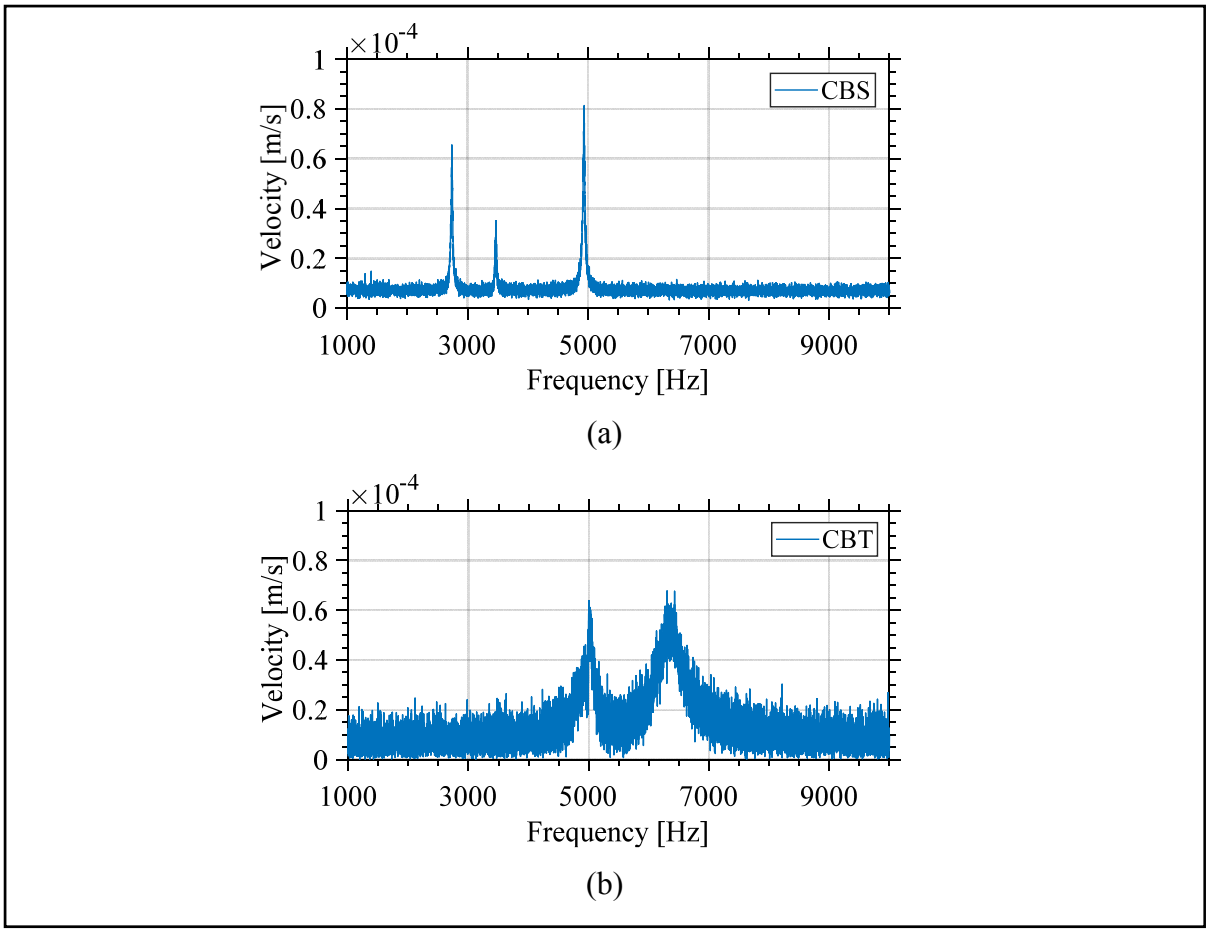

Figure 5.12 Measured harvester velocity vs frequency for (a) CBS and (b) CBT designs

The use of a vibration shaker makes it possible to measure the output voltage of a system. The realization of these measurements requires the connection of the DUT structure to the control unit of the shaker. An accelerometer is used so that the shaker is controlled in both power and frequency. When the structure is excited at its resonant frequency at a defined acceleration we can then measure the voltage and thus calculate the power supplied by the system using an oscilloscope or the acquisition system of the shaker. The result of these measurements is shown in Figure 5.14. The figure shows an output voltage of 173 mV and 583 mV measured across one beam at an acceleration of 8g and a load of 1 MΩ. With four beams, the voltages will be 692 mV and 2.33 V generating about 0.48 µW and 5.4 µW of peak output power in the CBS and CBT devices, respectively.

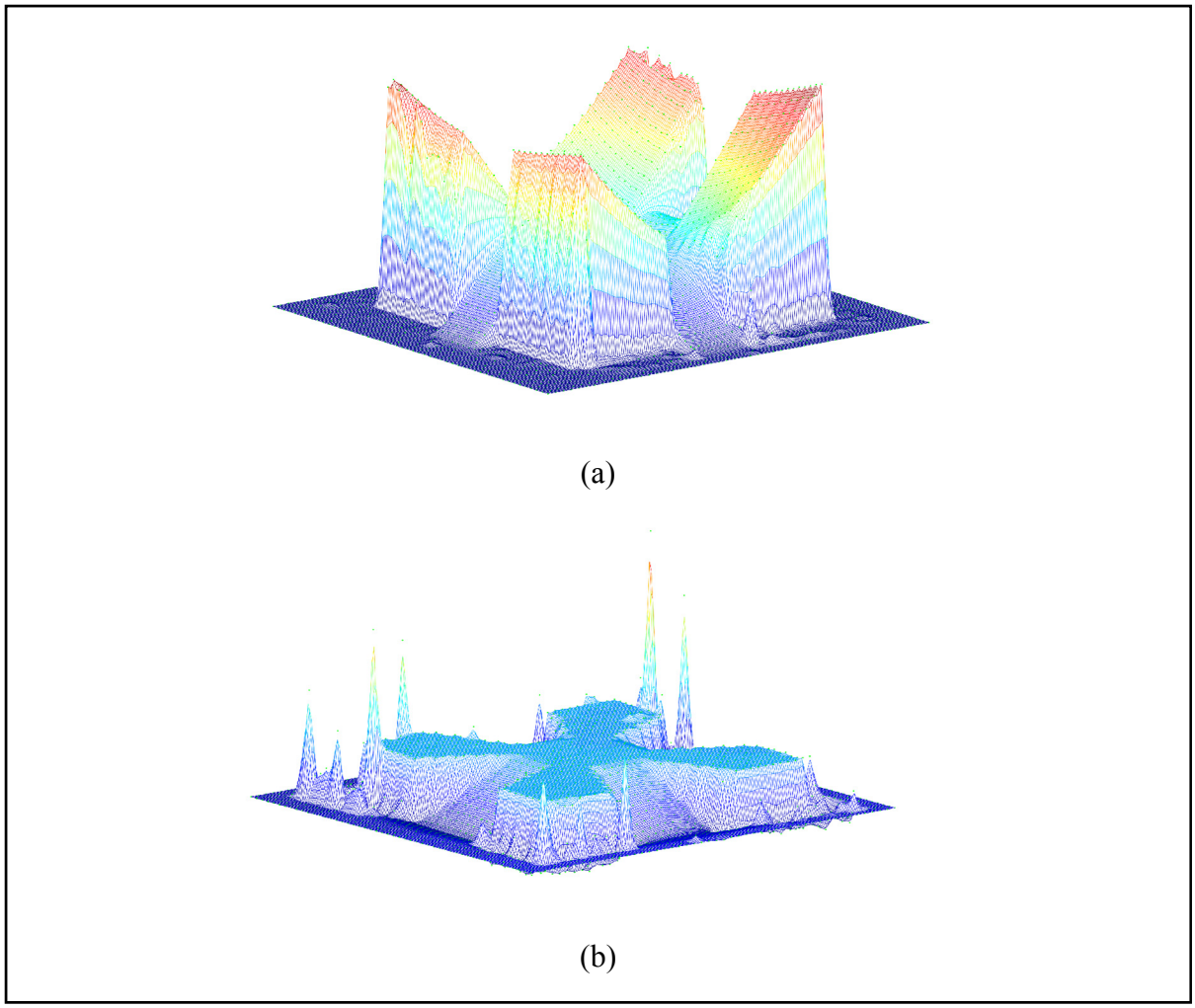

Figure 5.13 (a) CBS first resonant mode, and (b) CBT third resonant modes

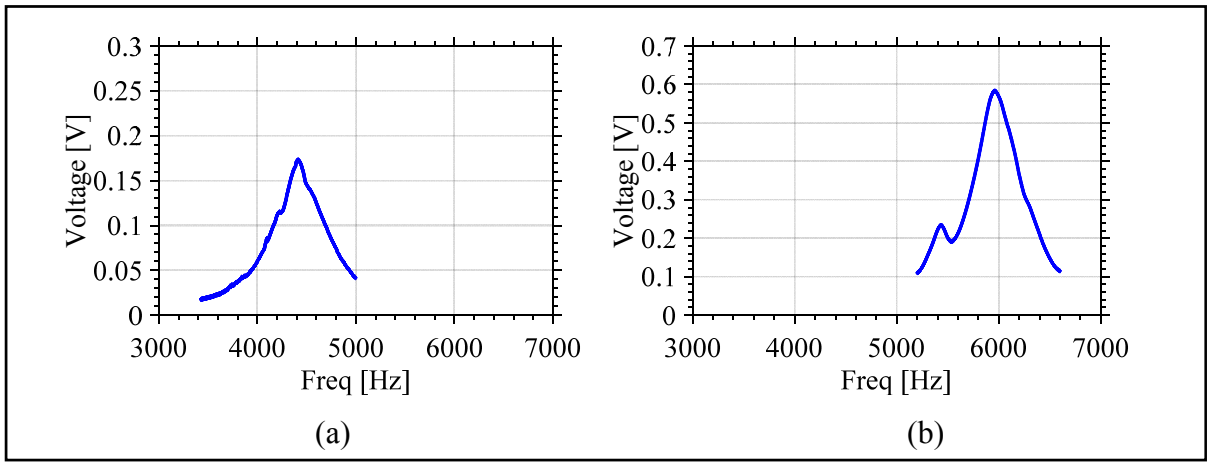

Figure 5.14 Measured output voltage (a) CBS and (b) CBT designs

5.3 Power Management Circuit

The output of an energy harvester is not directly suited as a power supply for circuits because of variations in its power and voltage over time. The output power that is generated varies with the ambient conditions. Power conditioning for MEMS vibrational transducers is an essential aspect of an energy harvesting system to ensure that the output of the harvester is suitable to power electronics that require a stable DC supply (e.g., 1.2 V). Notably, very high efficiency and low voltage operation of the conditioning circuits are of interest for highly integrated systems, as they potentially enable their operation in a wide range of environments. Energy efficient conditioning is important to capture low level vibrations and provide sufficient energy to a given system. Figure 5.15 shows the block diagram of an energy harvesting system.

The circuit has to be of small size, low power and provide both rectification and DC-DC conversion. These were the main criteria behind the topology selection. Accordingly, two power conditioning circuits have been investigated: a Cockroft-Walton multiplier and a CMOS low power cross-coupled rectifier. Both circuits can be cascaded to provide multiple output levels from a regulated input, or can be controlled to generate a regulated output from a variable input. This gives a more versatile, agile, and reconfigurable input output circuit. Figure 5.16 shows the layout and the micrograph of the two fabricated circuits. A 0.35 µm CMOS technology from AMS has been used for fabrication.

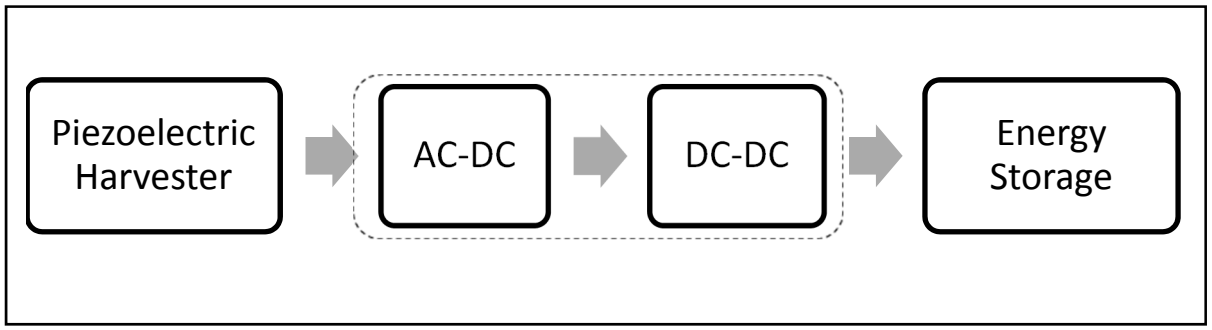

Figure 5.15 Energy harvesting block diagram

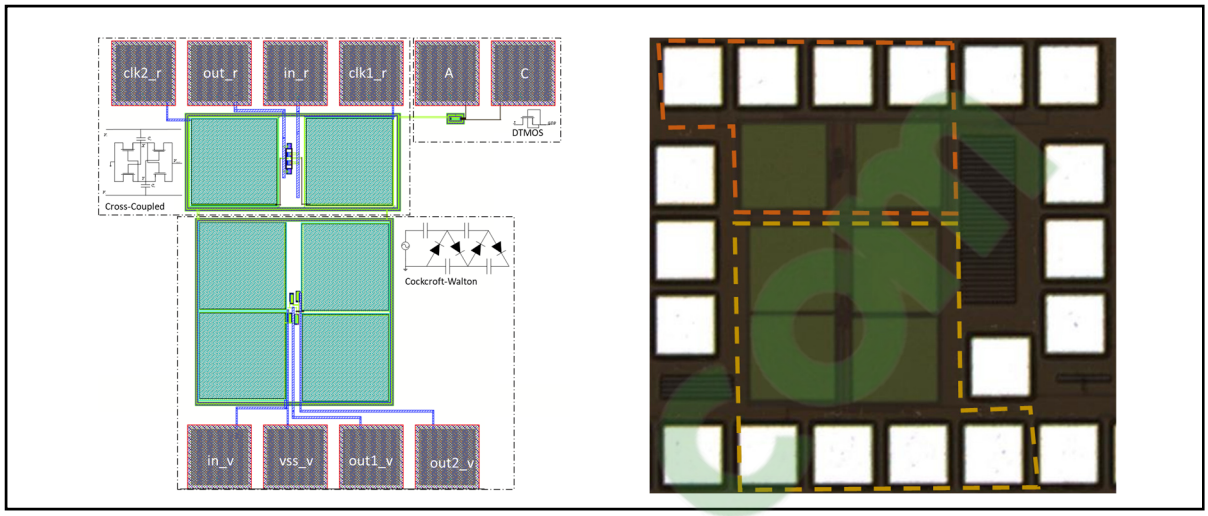

Figure 5.16 Chip layout and micrograph

5.3.1 Cockroft-Walton Multiplier

A Cockroft-Walton (CW) multiplier, or also called Villard multiplier, has been adapted to generate the regulated DC voltages from the low AC voltages provided by the harvester. Figure 5.17 shows a one and two-stage CW circuit. The operation of the one stage circuit starts with a negative half cycle of an input AC signal of amplitude V_p. D_1 is ON and C_1 is charged to a peak voltage V_p. During the positive cycle, input V_p is added to the capacitor's voltage charging C_2 to $2V_p$ through D_2.

This topology uses diodes and capacitors. For an all integrated solution diode connected transistors are implemented. While these suffer threshold voltage drop limitation, the use of DTMOS transistors has been adapted. This can lower the threshold voltage according to equation 5.1:

$$V_t = V_{t0} + \gamma\left(\sqrt{\left|2\phi_f\right| + V_{SB}} - \sqrt{\left|2\phi_f\right|}\right) \qquad (5.1)$$

where V_t is the transistor's threshold voltage, V_{t0} is the threshold voltage for zero substrate bias, γ is the body effect parameter, V_{SB} is the source to body substrate and φ_f is the surface potential.

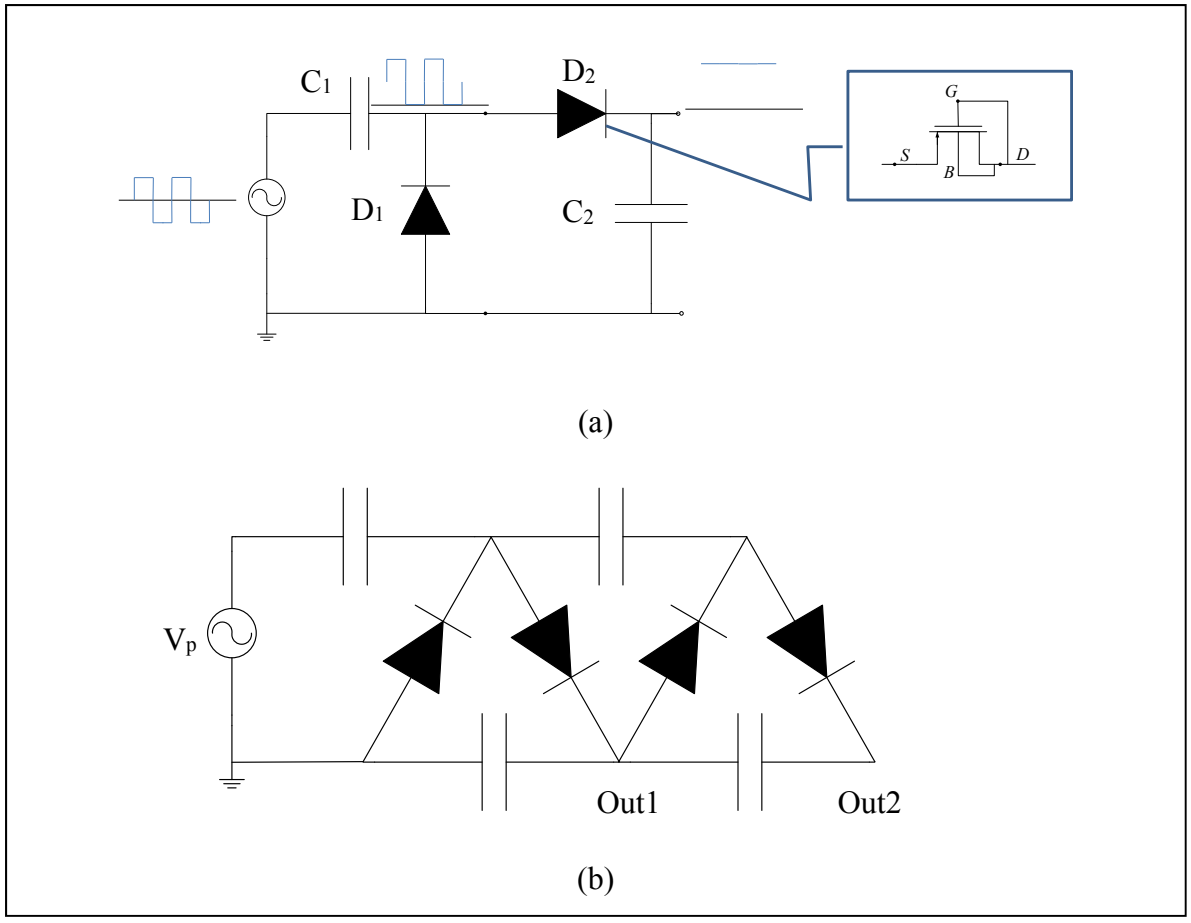

Figure 5.17 (a) One stage and (b) two-stage Cockroft-Walton multiplier

DTMOS concept where the body terminal is connected to the gate terminal in diode-connected transistor is shown in the inset of Fig. 5.17(a). This implementation permits a dynamic control over threshold voltage in the rectifier design. During forward conduction, the threshold voltage will be lower which enables the rectifier to operate at low voltage amplitude. Similarly, rise in the threshold voltage during reverse conduction reduces the reverse conduction loss in the rectifier. However, this threshold is always their and could present a limitation in terms of the implementation of this topology.

5.3.2 Cross-coupled Rectifier

The diode losses witnessed with the Cockroft-Walton configuration present a limitation and therefore a cross-coupled configuration has been investigated (Alameh et al, 2017). To

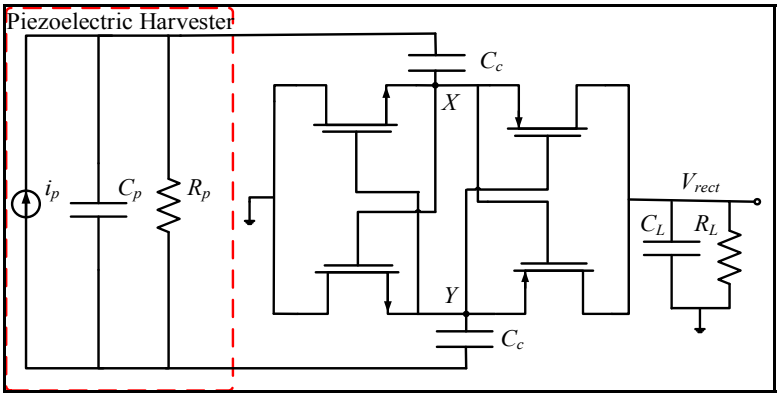

Figure 5.18 Cross-coupled rectifier

improve the power conversion efficiency and mitigate the diode forward voltage drop in diode based rectifiers, cross-coupled rectifiers are proposed. Figure 5.18 shows a single stage of the CMOS rectifier circuit connected to the equivalent electrical model of the piezoelectric harvester. To achieve the best efficiency, there are rigorous design trade-offs among optimal transistor widths, lengths and capacitor sizes. Simulations have showed minimal transistor sizes yield an optimal design choice. Rectifier design has been optimized to achieve best power conversion efficiency (PCE) which has been calculated as:

$$PCE = \frac{P_{DC}}{P_{av}} \cdot 100 \tag{5.2}$$

with P_{DC} being the DC power at the output of the rectifier and P_{av} is the power provided by the harvester. Optimizations had to be made to work at low input voltages thus low threshold voltage transistors have been used. The coupling capacitors C_c allows for DC decoupling and have a high pass filter response while C_L has a low pass response and helps the output ripple attenuation. The PCE of the cross-coupled rectifier as a function of the input voltage is shown in Fig. 5.19.

Table 5.2 Specifications of the Designed Rectifier

W_n	W_p	Freq	V_{in}	C_L	C_c	R_L
10 µm	10 µm	5 kHz	720 mV	1 µF	10 pF	10 MΩ

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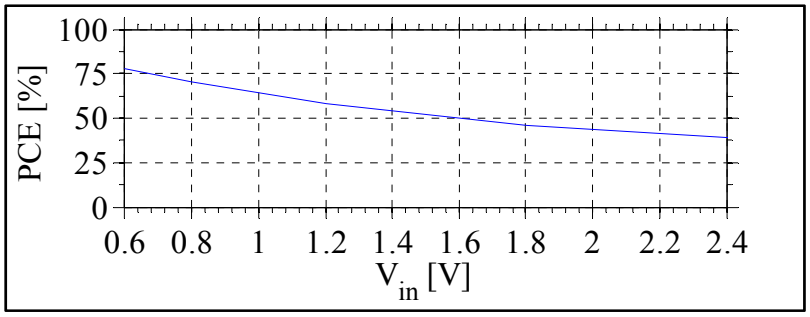

Figure 5.19 Rectifier efficiency versus input voltage

Circuit simulations have been performed using the SpectreRF simulator. The equivalent electrical model of the harvester has been represented by a current source in parallel with a capacitor and parasitic resistance feeding a rectifier circuit. A current source of 6.1 µA, piezo capacitance of 164 pF and parasitic resistance of 10 MΩ models the harvester. An energy storage capacitive load of 1 µF has been used to collect the generated power. Transistor sizing was designed to reduce ON resistances, and has been confirmed by simulation. Table 5.2 lists the specifications of the designed rectifier. A sinusoidal signal of amplitude 720 mV is generated and rectified. The rectifier is designed to account for variations in the input voltage of the harvester. Figure 5.20 shows the output of the rectifier in which a ~0.25s charging time is required to charge the 1 µF energy storage load capacitor through the 640 mV output of the rectifier. This energy storage capacitor can be used as a buffer to smoothen out the intermittent power, before a DC-DC converter, in order to regulate the voltage feeding the targeted load circuits (Alameh et Nabki, 2017b).

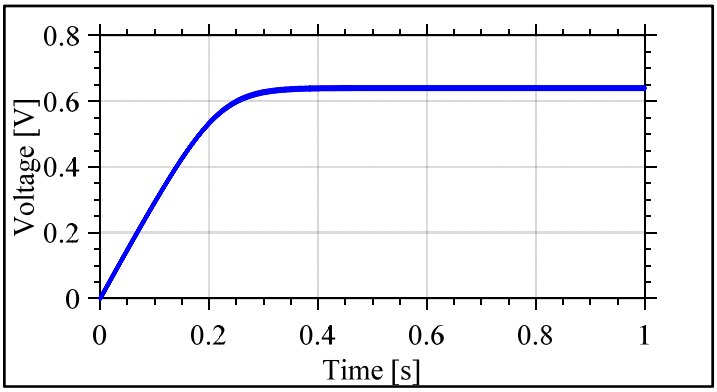

Figure 5.20 Output voltage with 1 µF capacitive load

5.3.3 Measurement Results

Fig. 5.21 shows the test setup used to test the two fabricated circuits. Each of the two circuits has 4 pads thus 4 DC needles have been used to access the pads directly. A frequency generator to generate the input signals and an oscilloscope to monitor the output have been used.

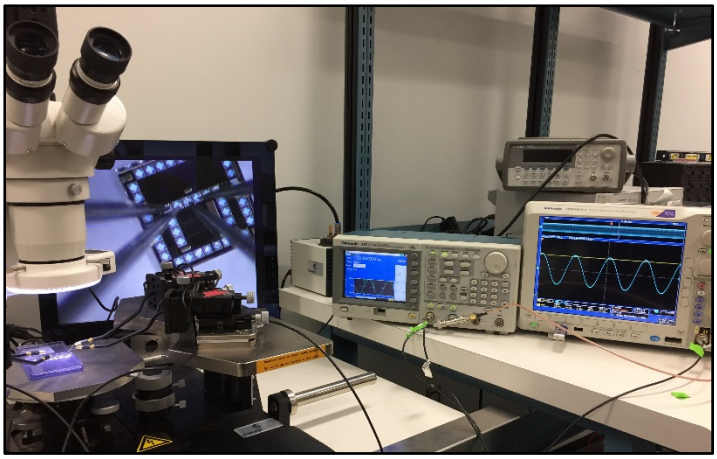

Figure 5.21 Rectifier circuit test setup

The Cockroft-Walton structure was tested first. One of the advantages of this circuit is to have two outputs from a single input and this is what has been verified in Fig. 5.22(a). With an input vibration of amplitude 1 V at a 1 MHz frequency, the outputs measured across the 1 MΩ load oscilloscope are: output 1 440 mV and output 2 860 mV. However, this output scales with the frequency and this is illustrated in Fig. 5.22(b). The lower the frequency, the lower is the efficiency. For this rectifier to work with the energy harvester, the frequency should be lower and the regulated voltage should be stored in a larger capacitor. For this design, a frequency of 5 kHz and a storage capacitor of 100 µF has been used and as can be seen in Fig. 5.22(c) the circuit behaves as intended, with a regulated output voltage of 328 mV. The losses due to the use of the diodes affected this output.

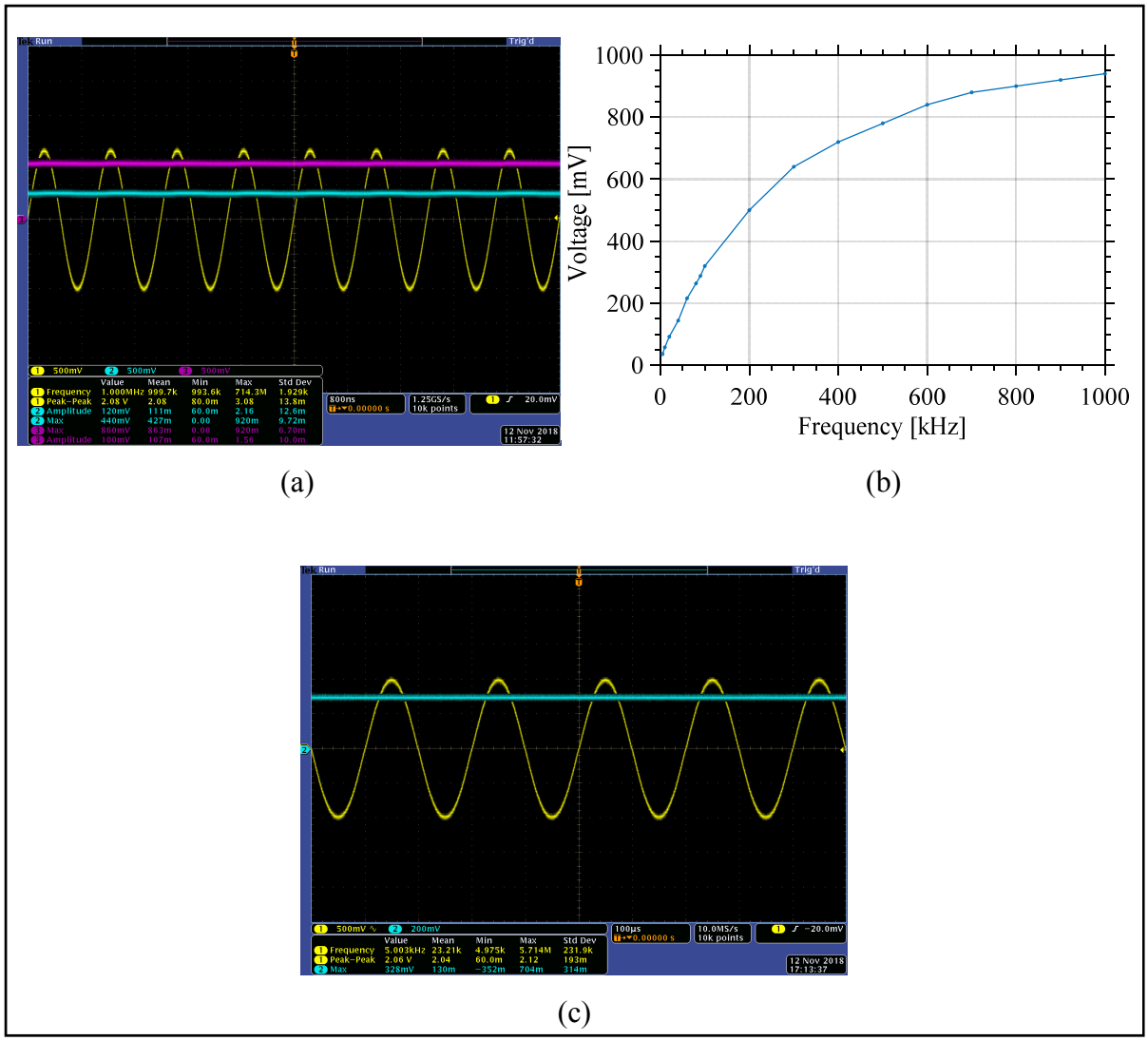

Figure 5.22 (a) Measurement results of Cockroft-Walton structure with 1 MΩ load
(b) Voltage variation as a function of frequency and
(c) Measurement results with 100 µF capacitive load

The cross-coupled structure was tested next. Figure 5.23(a) shows the output with 1 MΩ load at 10 kHz. With the same logic in mind for this circuit to work with the energy harvester the frequency was set to 5 kHz, signal amplitude 1 V and storage capacitors of 4.7 µF and 100 µF have been used. Measured results are shown in Fig. 5.23 (b) and (c). From a 1 V input voltage, a regulated output voltage of 750 mV has been achieved.

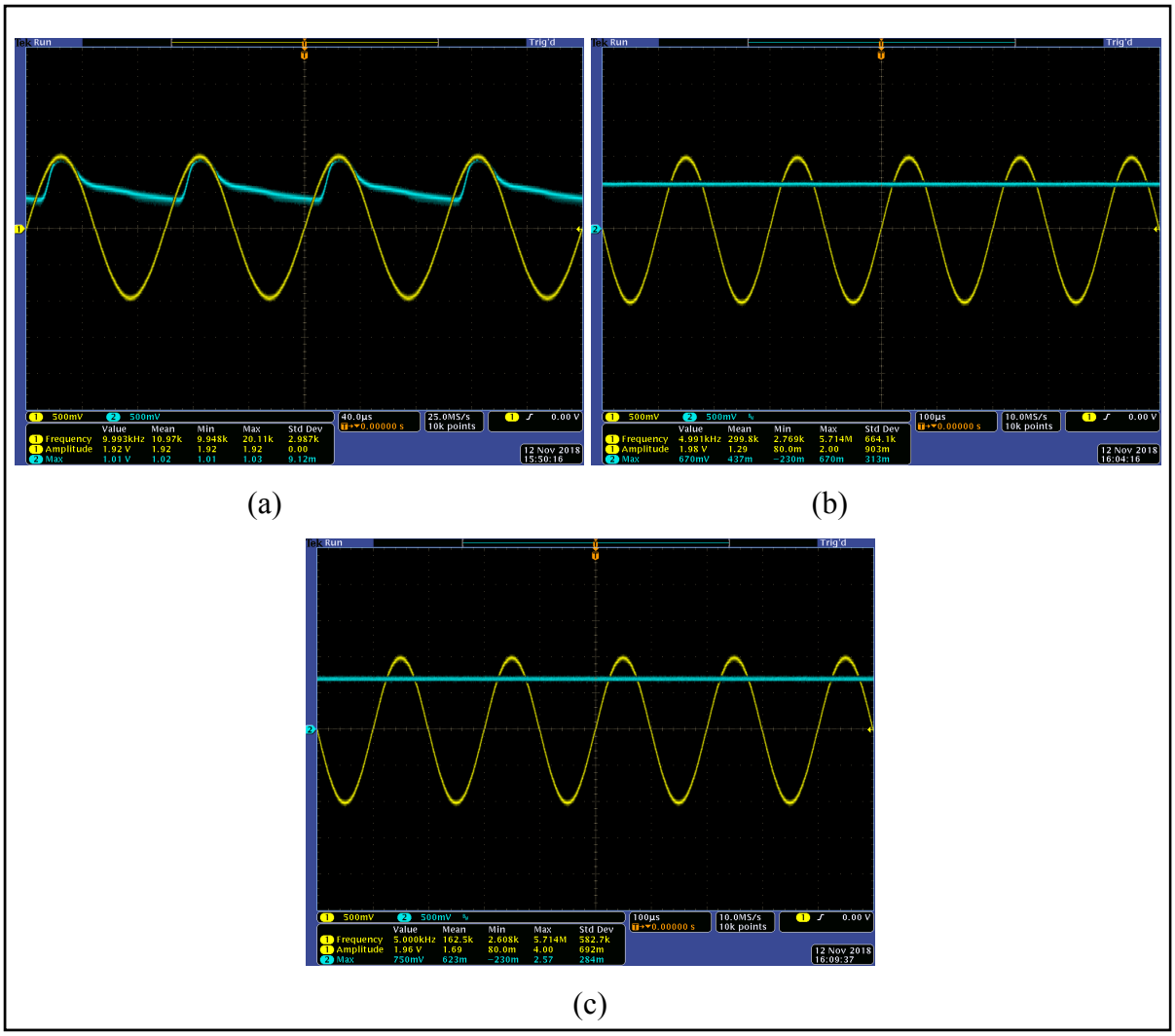

Figure 5.23 Cross-coupled measured results at (a) 1 MΩ (b) 4.7 µF and (c) 100 µF

An important feature of this circuit is that it could be used to respond to an input voltage to generate multiple regulated output voltages. Chapter 4 presented a reconfigurable circuit to meet this criteria and step up the voltages. Another feature of this circuit, is its capability to step down the voltages. It can be used for negative voltage generation. The negative charge pump operation has been tested and Fig. 5.24 shows the measurement result. With a 500 mV input signal at 1 MHz frequency, an output voltage of -396 mV was recorded on the oscilloscope.

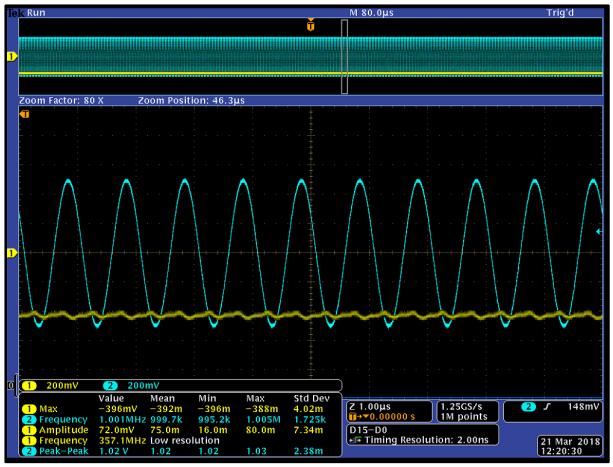

Figure 5.24 Negative charge pump measured voltage

5.4 Concept of an Integrated Energy Harvester for Wireless Sensor Node

The block diagram of an autonomous wireless sensor node can be seen in Fig. 5.25. The power consumption of a wireless sensor node containing a microcontroller, a wireless transmitter and a temperature sensor has been analysed. According to the previous measurements, the CBT design plus a cross-coupled rectifier have been selected to be integrated towards a System-in-Package (SiP).

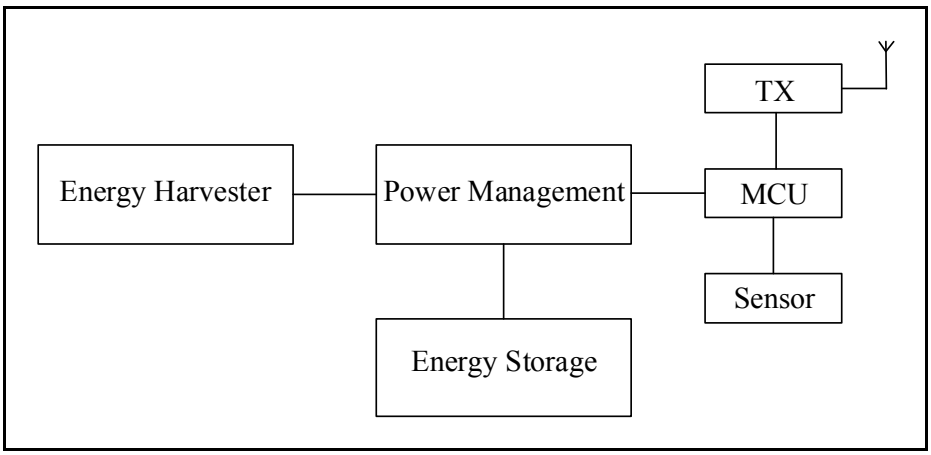

Figure 5.25 Autonomous wireless sensor node block diagram

In conventional technology, a wireless IC consumes power whether it was or was not in data transmission operation. However, using a technology were the wireless IC transmits very short

pulses instead of a continuous wave, as shown in Fig. 5.26, means that when the pulse signal stops, the wireless IC also stops thereby consuming minimum power. As a result, it is possible to develop a prototype node using nW energy. Accordingly the consumed average power ($P_{consumed}$) can be approximated as follows:

$$P_{consumed} = P_{sleep} + D.P_{active} \quad (5.3)$$

Where power consumed in idle or sleep mode P_{sleep}, power consumed in active mode P_{active} and duty cycle D. With this kind of operation you can bring down the power to the nW range.

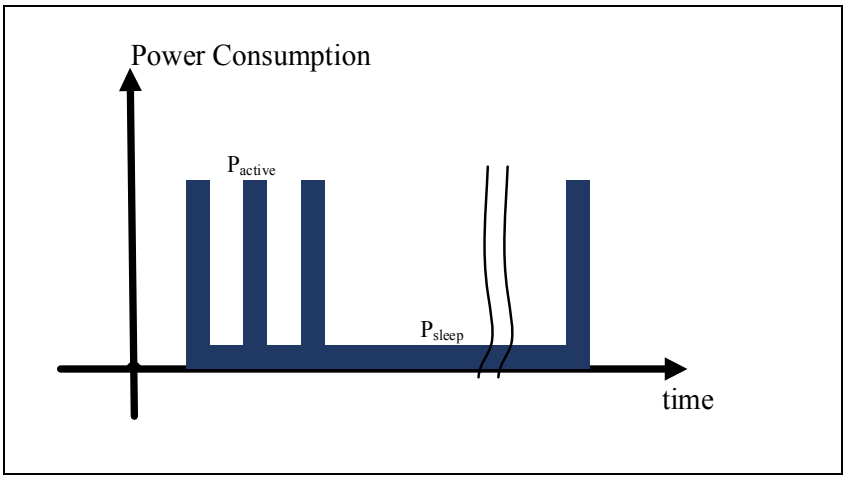

Figure 5.26 Power consumption profile of a sensor node

Two examples of wireless sensor node conceptions have been considered:

The first example is a 4-bit RISC microcontroller (EM6607), a wireless transmitter (nRF24L01) as well as temperature (AD7814) and acceleration sensors (LIS3LV02DQ). With low duty cycle (one action each 10 minutes), the average power needed is 150 nW (Ammar, 2007).

A second more recent and practical example has been analysed. It consists of a CC1310 wireless microcontroller from Texas Instruments (SoC microcontroller and transmitter), a

rechargeable battery (3.7 V battery 150 mAh lithium ion) and Sensor BME280 from Bosch Sensortec (temperature, pressure and humidity sensors all in the same package). The average power needed by the whole node is about 70 µW at a sampling period of 2 min, data rate 500 kbps, transmit power - 10 dBm, without oversampling of the data from the sensor and frequency of the MCU is 48 MHz (Brini, Deslandes et Nabki, 2018).

An array of harvesters can be connected to generate higher power levels when required. In that case, based on simulations and measurements, another advantage of the proposed designs is that it can generate much more power than a traditional cantilever when used in the same area. This proves that with an energy harvesting system as the one proposed an autonomous wireless sensor node can be achieved, and this will be the target of our next work.

5.5 Conclusion

In this chapter, two cross-shaped piezoelectric energy harvesters were presented. The geometry of the harvester has an impact on the performance, such that dimension ratios have to be chosen carefully to attain optimal performance. The extra mass added presents noticeable advantages in terms of compact size, relatively high strain distribution and ease of fabrication. This could be a step towards more efficient designs for wireless sensor nodes, especially if paired with custom rectifier designs as the one proposed. Cockroft-Walton and cross-coupled rectifiers have been designed and fabricated in a 0.35 µm CMOS technology. A cross-coupled design brings the advantages of higher efficiency and agility required to power a sensor node system like the one analyzed, based on a wireless microcontroller from TI, by deploying an array of these harvesters.

CONCLUSION

Summary

In this thesis, piezoelectric vibrational energy harvesters were discussed with power shaping circuitry (e.g. rectifying, DC/DC conversion) to condition the power output of the transducers for use in the sensing systems. This research project is studied with multi-faceted work touching MEMS and ICs. The ultimate research objective has been identified to work towards autonomous wireless senor nodes, and a research plan was set based on a proposed methodology to achieve the desired goal. Designs were studied and implemented to quantify the operation of energy harvesters and DC-DC converters.

The driving force for energy harvesting in this work is to power wireless sensor networks for IoT applications. In chapter 2, the effects of proof mass geometry on piezoelectric energy harvesters are studied. The impact of different geometrical dimension ratios, beam to mass lengths and beam to mass widths, have been analyzed. A T-shape piezoelectric energy harvester has been fabricated and tested operating at a frequency of about 4 kHz and generating about 62 nW. Chapter 3 investigates the power output of several geometric variations of cantilever beams, and examines the advantages of balancing the strain distribution throughout the beam. Eight rectangular and trapezoidal T-shaped designs are fabricated for the same area. Resonant frequencies ranging from 2.9 to 7.2 kHz and power outputs ranging from 2.2 to 7.1 nW are reported. In chapter 4 a reconfigurable charge pump for MEMS electrostatic actuation was designed and fabricated in a standard 0.13 μm CMOS technology. The purpose of the circuit is to generate sufficient on chip voltages that are continually reconfigurable for MEMS actuation. Voltage levels can be outputted by varying the number of stages and the clock drive levels dynamically. Reduced power consumption is achieved using a variable frequency clock. The circuit attains a measured maximum output voltage of 10.1 V from a 1.2 V supply. This circuit can be applied to energy harvesting applications as well. In chapter 5, a novel cross-shaped piezoelectric vibration energy harvester is proposed featuring four beams and a central with extra corner masses resulting in an improved performance. A cross-coupled

rectifier circuit has been designed and fabricated to be combined with the harvester towards an integrated microsystem.

In general, the energy harvester specifications depend heavily on the desired application that dictates these specifications. Among the most important specifications for the power system are the total size and average power required. This thesis will pave the way towards novel fully contained energy harvesting microsystems that will be usable in a wide range of applications including autonomous sensors.

The main outcomes of this thesis are:
1. Design and fabrication of a reconfigurable DC/DC converter chip to support wide input/output voltage ranges, low power, energy efficient and compact system.
2. Design and fabrication strategies and implementation of rectangular and trapezoidal T-shaped MEMS energy harvesters.
3. Cross-shaped MEMS harvesters to be integrated with power management circuitry towards an integrated energy harvesting system.

Contributions

The contributions of this thesis are:
1. A design tuning of the frequency for T-shaped energy harvester structures by varying the proof mass geometry in order to achieve the lowest frequency possible.
2. A method for increasing the power output of the energy harvester without significantly sacrificing the resonant frequency by considering trapezoidal T-shaped cantilevers.
3. A novel reconfigurable DC-DC converter charge pump architecture.
4. Novel checkerboard piezoelectric vibrational energy harvesting structures for maximal output power and lower resonant frequency.

The wireless sensors market will experience significant growth in the coming years and the impact of the MEMS and integrated circuit design methodologies and designs stemming from

this research is expected to contribute to this market that requires heightened levels of MEMS energy harvesters and power conditioning circuit performance and agility.

List of Authored Publications

Journal Articles

[J3] A. H. Alameh, M. Gratuze, and F. Nabki, "Impact of Geometry on the Performance of Cantilever-based Piezoelectric Vibration Energy Harvesters," submitted IEEE Sensors Journal, 2019.

[J2] A. H. Alameh, M. Gratuze, M. Elsayed, and F. Nabki, "Effects of Proof Mass Geometry on Piezoelectric Vibration Energy Harvesters," Sensors, vol. 18, no. 5, p. 1584, 2018.

[J1] A. H. Alameh and F. Nabki, "A 0.13-µm CMOS Dynamically Reconfigurable Charge Pump for Electrostatic MEMS Actuation," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 4, pp. 1261-1270, 2017.

Conference Proceedings

[C7] A. H. Alameh, M. Gratuze, A. Robichaud, and F. Nabki, "Study and Design of MEMS Cross-Shaped Piezoelectric Vibration Energy Harvesters," in IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2018.

[C6] A. H. Alameh and F. Nabki, "A 0.13 µm CMOS power conditioning circuit for piezoelectric vibration energy harvesters," in IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2017.

[C5] A. H. Alameh, A. Bouchami, and F. Nabki, "A Wide Voltage Range Charge Pump in 0.13 µm CMOS for Biasing of MEMS Resonators," in IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2016.

[C4] A. Aghighi, A. H. Alameh, M. Taherzadeh-Sani and F. Nabki, “A 10-Gb/S Low-Power Low-Voltage CTLE Using Gate and Bulk Driven Transistors,” in IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2016.

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[C3] P. O. Beaulieu, A. H. Alameh, M. Menard, and F. Nabki, "A 360 V high voltage reconfigurable charge pump in 0.8 μm CMOS for optical MEMS applications," in IEEE International Symposium on Circuits and Systems (ISCAS), 2016.

[C2] A. H. Alameh, A. Robichaud, and F. Nabki, "A reconfigurable charge pump in 0.13 μm CMOS for agile MEMS actuation," in IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2014.

[C1] A. Robichaud, A. H. Alameh, F. Nabki and D. Deslandes, " An agile matching network using phase detection for antenna tuning," in IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2013.

RECOMMENDATIONS

The work presented in this thesis can be continued along different avenues. The integration of the harvester, rectifier circuit and the storage capacitor will be completed. A complete wireless sensor node is to be built including the microcontroller, sensor, transceiver, battery and energy harvester. In-house fabrication of the harvesters is to be implemented. Further work includes improving the efficiency of DC-DC circuit and investigating different sensor node applications including automotive industry and agriculture. However the main focus will be on underwater sensor nodes.

To allow practical implementation of MEMS energy harvesters, the focus needs to be on designs with a low resonant frequency and with a large bandwidth. To improve their performances, future work should be directed towards tunable energy harvesters. According to the work presented in this thesis, the CBT design has shown to be a design of great potential. Thus a larger design is to be fabricated to generate higher output voltages at lower frequencies. Other geometries are to be considered. A chip has been sent to fabrication that aims at tuning the frequency of the CBT design through the use of electrostatic actuation, in addition to different designs that are based on the idea of tapering the beams, and/or electrostatic actuation.

On the harvester side, as mentioned, in house fabrication of the harvester is to be implemented. This is now possible with the acquisition of a sputtering machine that permits the deposition of the piezoelectric material. Recipes for the deposition of AlN need to be developed. This will give more flexibility in terms of design considerations, in addition to reducing the lead time compared to the use of commercial technology.

With the reduction of the resonant frequencies, and the increase of power output of the MEMS energy harvesters, the design of a monolithic more efficient power conditioning circuit is to be implemented. Different topologies are to be investigated that aim at enhancing the conversion efficiency. The integration of the harvester and conditioning circuit in a single package or even chip scale package using multi-technology interposer platform is to be realized.

The second charge pump circuit that has been put on hold due to the discontinuation of the GlobalFoundries 0.13 μm CMOS technology is to be replaced by the TSMC technology and the circuit will be fabricated in this technology. Once proven to be successful, the work will shift towards the reconfigurability part of the circuit by varying the number of stages and other control mechanisms. This will allow the use of this design with a wide range of inputs and the reusability of the design in different environments.

To allow the design of a complete wireless sensor node, the harvester would need to be integrated with both a sensor and some communication device. This wireless sensor node is to be built based on a modelling approach for the design of ultra low power wireless sensor nodes. The environment in which this sensor will be placed, leads to lots of different design choices, including the design of the MEMS energy harvester, the rectifier circuit, the DC-DC converter, the type of sensor implemented, and the communication protocol.

In terms of applications for the wireless sensor node, about 70% of the earth's surface is covered with water in which there is huge amount of unexploited resources. There is a need for underwater observation. Underwater wireless sensor nodes are used to monitor and sense aquatic environments and to transfer information. Today's sensor networks consist of battery-powered sensor nodes with a limited energy budget. Underwater sensor nodes cannot survive on battery power for a long time. The challenges of replacing the battery frequently dictates the need for alternative solutions such as the use of energy harvesting technology. During a future work, the proposal is to investigate this issue by enhancing the node's power consumption through considering optical wireless communications and looking at energy harvesting as a power source to extend the battery life.

APPENDIX I

A WIDE VOLTAGE RANGE CHARGE PUMP IN 0.13 µm CMOS FOR BIASING OF MEMS RESONATORS

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Abstract:

A wide voltage range charge pump is designed in 0.13 µm CMOS technology to provide biasing voltages for MEMS resonators. The pump provides an output range of 32.6 V, from - 16.1 V up to 16.5 V, by using four different charge pump cells based on cross-coupled voltage doublers. Two cascaded negative charge pumps and two cascaded positive charge pumps with enhancements to breakdown and high voltage tolerance are implemented.

Keywords: DC-DC converters, charge pump, MEMS resonators, reconfigurable.

INTRODUCTION

Oscillators are used heavily in RF circuits. In recent years, microelectromechanical systems (MEMS) based oscillators have seen advances that resulted in their proliferation in timing applications that are dominated by the use of quartz crystals. MEMS resonators, which are at the core of MEMS-based oscillators, are much smaller than a quartz crystal and can be incorporated with integrated circuits (ICs). In addition to allowing for higher levels of integration, MEMS resonators allow for the benefits of batch processing, smaller form factor and lower cost (Nabki et al., 2009). Among the resonator characteristics that most affect oscillator design and performance are its resonance frequency, series motional resistance, quality factor Q, and power-handling ability. These parameters strongly depend on the bias

and excitation signals applied to the resonator and on its geometry (Yu-Wei et al., 2004). For example, electrostatic MEMS resonators require a DC bias voltage, VP, in which an increase reduces the resonance frequency and reduces the insertion loss of the resonator. Lower cost electrostatic resonators also typically require higher DC bias voltages as they feature critical dimensions for their electrostatic transducers that are relaxed. Moreover, for applications requiring low phase noise, biasing the MEMS resonator at a higher DC voltage will reduce its insertion loss and increase the signal power (Haechang, Partridge et Assaderaghi, 2012; Ismail et al., 2014).

The generation of these biasing voltages is often carried out off-chip using external DC supplies, due to the limitations on the voltages that can be generated on-chip (e.g. 1.2 V). This goes against the integration advantage of MEMS oscillators, as MEMS resonators require voltages which are much higher than typical CMOS supply voltages. Therefore, in this work, a charge pump designed in a standard 0.13 µm CMOS technology is proposed to provide variable high voltages for MEMS electrostatic resonators biasing. While there is a constant effort to reduce MEMS resonators actuation voltages, we present a low-power and highly efficient charge pump with an output range of 32.6 V, from -16.1 V up to 16.5 V. The circuit operates from a 1.2 V supply, allowing for a fully-integrated MEMS based oscillator system.
The paper is organized as follows: section II presents an overview of MEMS oscillators. Section III describes each of the circuit blocks of the proposed charge pump. Section IV presents simulation results, and is followed by a conclusion.

APPLICATION OVERVIEW

A MEMS-based oscillator has been presented in (Bouchami et Nabki, 2014), in which a non-linear resonator model is implemented and then integrated with a transimpedance amplifier (TIA). The oscillator consists of a TIA capable of sustaining oscillation with an electrostatic clamped-clamped (C-C) beam resonator, as shown in Fig. AI.1, so that high phase-noise performance can be attained. The TIA is comprised of a regulated cascode (RGC), variable gain amplifier (VGA), an output buffer and an automatic gain control (AGC). It can provide a

high gain-bandwidth product to offset the resonator losses and to ensure a small phase shift such that high oscillation frequencies can be attained. Furthermore, the TIA is characterized by low input and output impedances to avoid loading the quality factor of the resonator.

While in operation, the charge pump will generate the desired resonator actuation voltage, V_P, so that high phase-noise performance and required start-up response can be attained by reducing resonator insertion loss. For this purpose, a DC- DC converter (i.e., charge pump) with wide voltage range that is reconfigurable is required. Figure AI.2 shows the block diagram of the proposed system. It includes the block diagram showing the four sub pumps along with their clock generation, and the MEMS resonator which is biased on each side by the charge pump. Note that the MEMS resonator is biased through biasing tees that can be inductive or resistive. The first of the sub pumps is the positive charge pump (PCP 1) that can generate a maximum output voltage of 10.6 V from a 1.2 V input, followed by a second positive charge pump (PCP 2) that takes the output from the first pump as its input to generate a 16.5 V maximum output voltage. Moreover, a negative charge pump (NCP 1) with 0 V input generates a 9.4 V output is also followed by a second negative charge pump (NCP 2) to reach 16.1 V. Consequently, a range from -16.1 V to 16.5 V can be covered with this charge pump. The four sub pumps have been designed based on a cross coupled voltage doubler cell with enhancements to the transistors breakdown limitations (Pelliconi et al., 2003). The different sub pump biasing techniques are later described.

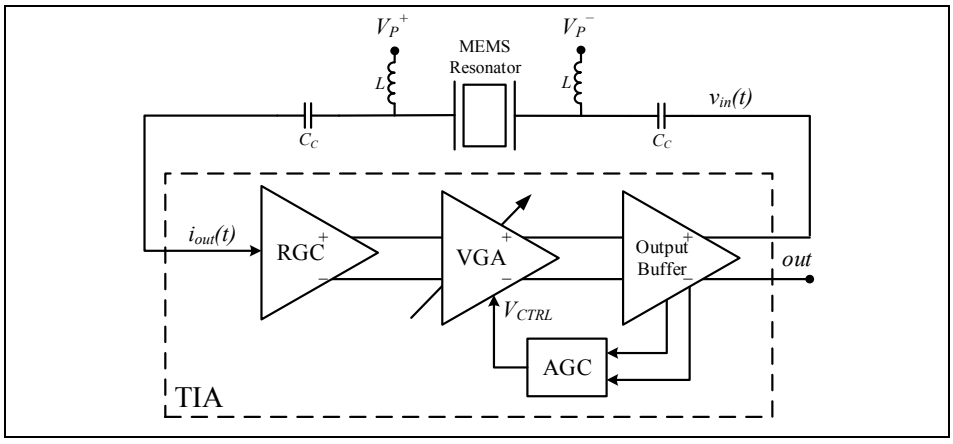

Figure AI.1 MEMS-based oscillator with expanded TIA block diagram

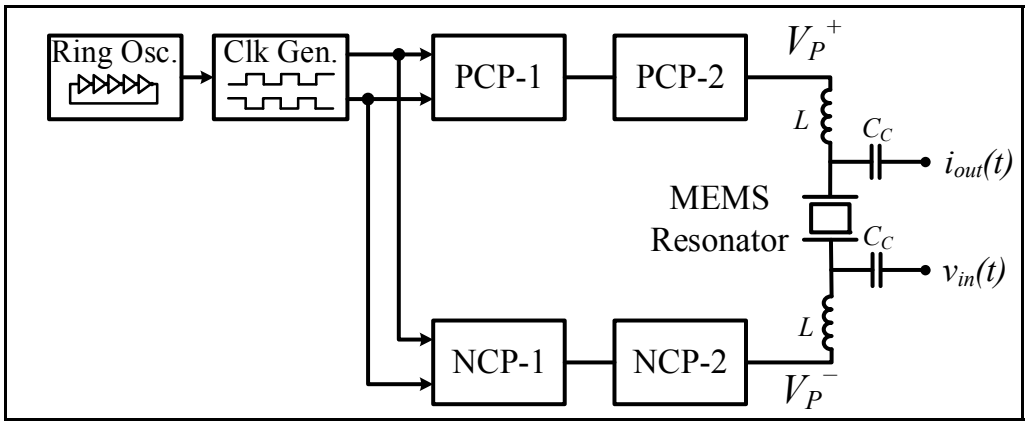

Figure AI.2 Block diagram of the proposed circuit

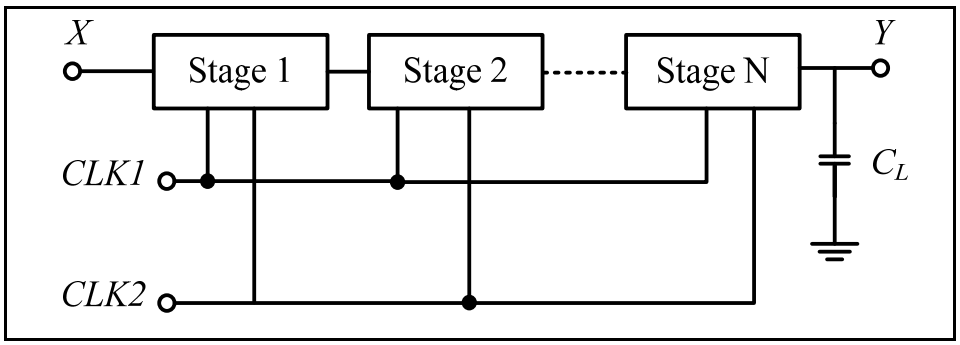

Figure AI.3 Sub pump block diagram

Table AI.1 Sub Pumps Parameters

	PCP-1	PCP-2	NCP-1	NCP-2
X	V_{in}	V_{P1}^+	GND	V_{P1}^-
Y	V_{P1}^+	V_{P2}^+	V_{P1}^-	V_{P2}^-
N	8	12	8	12

CIRCUIT DESCRIPTION

Figure AI.3 shows the sub-pump general block diagram, and Table AI.1 shows the inputs, outputs and the number of stages of each of the four sub pumps, which relates to the block diagram of the proposed circuit in Fig. AI.2.

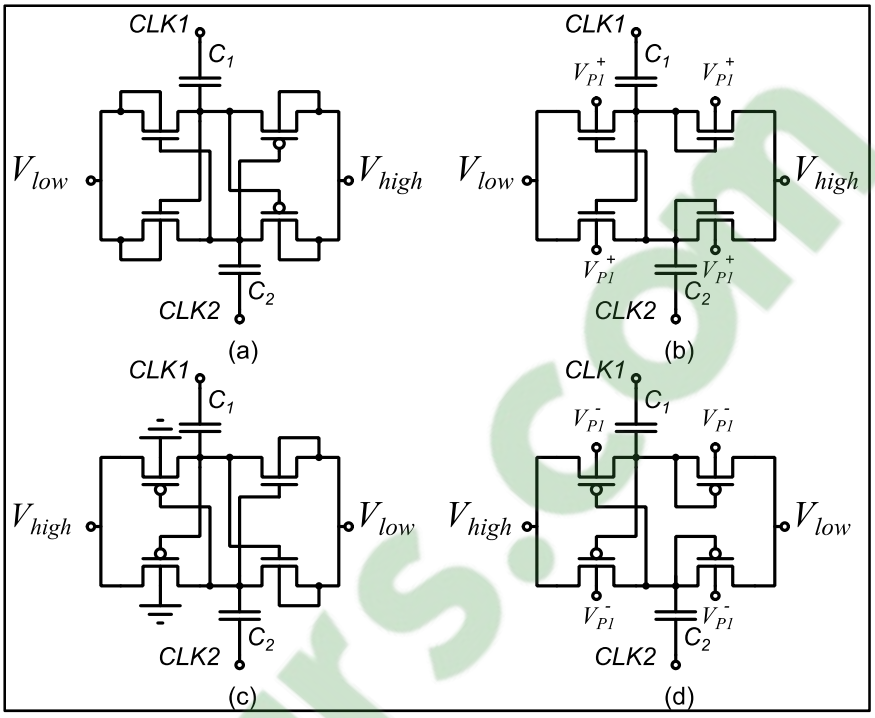

Figure AI.4 Voltage doubler cell schematic of (a) PCP-1, (b) PCP-2, (c) NCP-1, and (d) NCP-2

A. Positive Charge Pump 1 (PCP-1)

The first positive charge pump is based on the design presented in (Alameh, Robichaud et Nabki, 2014). The cell of an eight stage reconfigurable charge pump that adapts the cross coupled structure with a triple well (Pelliconi et al., 2003) is shown in Fig. AI.4(a). This structure provides the required high gate voltages of the switch NMOS transistors. The use of triple wells allows the bodies of the NMOS transistors to be biased independently at different voltages than ground. Two non-overlapping clocks pump up the output of each cell in an alternating fashion through two PMOS switches to $2V_{in}$. The main advantage of such a structure is that it eliminates the impact of the threshold voltage found in the Dickson design (Dickson, 1976) without affecting the charge transfer function. Cascading these doublers enables higher output voltages, where the output voltage is only limited by the MOS transistor breakdown voltages, specifically the substrate to n well breakdown voltage. The n-well / p-substrate junction remains the key voltage limitation because of its avalanche reverse breakdown voltage. The deep n-wells are biased to the output voltage (V_{high}) of the stage, the

body is connected to the source and to the input voltage (V_{low}), and the p-substrate is biased to ground. The bulk of the PMOS transistors is connected to the sources, as shown in Fig. AI.5(a). The W/L ratio for the NMOS transistors is 4 (480 nm / 120 nm) while the W/L ratio for the PMOS transistors is 5 (600 nm / 120 nm). With an input voltage V_{in} = 1.2 V and clock coupling capacitors sized to 1 pF, the maximum output is 10.6 V. Note that all transistor and coupling capacitor sizes are kept the same in the other sub pumps later described.

B. Positive Charge Pump 2 (PCP-2)

The first charge pump is limited by the breakdown voltage of the deep n-well / substrate diode. To overcome this limitation in the second positive charge pump, the NMOS bulk and deep n-well terminals are connected together and held at a fixed potential, the output of the first pump as shown in Fig. AI.5(b). In this case, with the p-substrate connected to ground, the deep n-well / substrate diode breakdown problem can be overcome. However, the breakdown limitation will be the n+ / p-well diode breakdown voltage (Ismail et al., 2014). The output voltage is outputted through NMOS diode-connected transistors, shown in FigI. A.4(b), with the same preceding biasing to replace the PMOS switches that will suffer breakdown in this case. However, using diode-connected switches at the output reduces the gain due to the threshold voltage loss and consequently lowers the efficiency of this sub pump. With PCP 2 composed of twelve stages, the maximum output voltage is raised to 16.5 V, including the preceding eight stages of PCP 1.

C. Negative Charge Pump 1 (NCP-1)

Given the fact that what is important for the MEMS resonator is the difference between its ports biasing voltages, the negative maximum output voltage will increase the output voltage that the resonator can be biased at. Among the advantages behind the choice of the cross coupled based charge pump, is that it is symmetrical; hence it can be used for negative voltage generation as well. A negative voltage can be generated by interchanging the PMOS and NMOS transistors (Richard et Savaria, 2004). However, it has been shown in (Ethier et al.,

2009) that by simply switching the input and output, a latch-up is triggered during the first charge pumping cycles if the sources of the PMOS transistors are connected to their bulk (i.e. to the deep n-wells), and thus the deep n-wells of the negative charge pump are all tied to ground, as shown in Fig. AI.4(c). For the NMOS transistors, the bulk is connected to the sources to the more negative potential and the deep n-well and the substrate are connected ground, as shown in Fig. AI.5(c). Using the ground as an input, and with eight stages, a value of -9.4 V is achieved.

D. Negative Charge Pump 2 (NCP-2)

To reach larger magnitude negative voltages, the same technique as with PCP-2 is carried out. Taking the advantage of the triple well T3 isolation, PMOS transistors can be isolated from the substrate. The body of the PMOS is in a separate well such that it can be biased separately and kept at a fixed potential, the output of NCP-1, as shown in Fig. AI.5(d). PMOS diode connected switches have been used at the output with their bodies again connected to the output of NCP-1, as illustrated in Fig. AI.4(d). A maximum of -16.1 V is attained using a total of twenty stages. This can lead to the wide output range that is desired for MEMS resonator biasing.

E. Clock Generation and Voltage Control

A current-starved voltage-controlled ring oscillator is designed to generate the clock, followed by a two phase non overlapping clock generator. The NAND latch-based circuit was used to generate the two 50 MHz clocks with careful attention to avoid shoot-through current and to preclude the charging and discharging switches from being on at the same time, preventing the reverse path that will be created from the higher voltage back to the lower voltage. The generated clocks feed all four sub pumps. Nominally, the clock supply voltage is 1.2 V.

The clocks driving voltages along with the input voltage V_{in} and the number of stages N define the conversion gains of a charge pump. To vary the gain of the charge pump depending on the load requirements, the number of stages can be varied, i.e. by shutting the clock of the stages

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that are not used. As such, a reconfigurable charge pump with multiple gains can be achieved as described in (Alameh, Robichaud et Nabki, 2014).

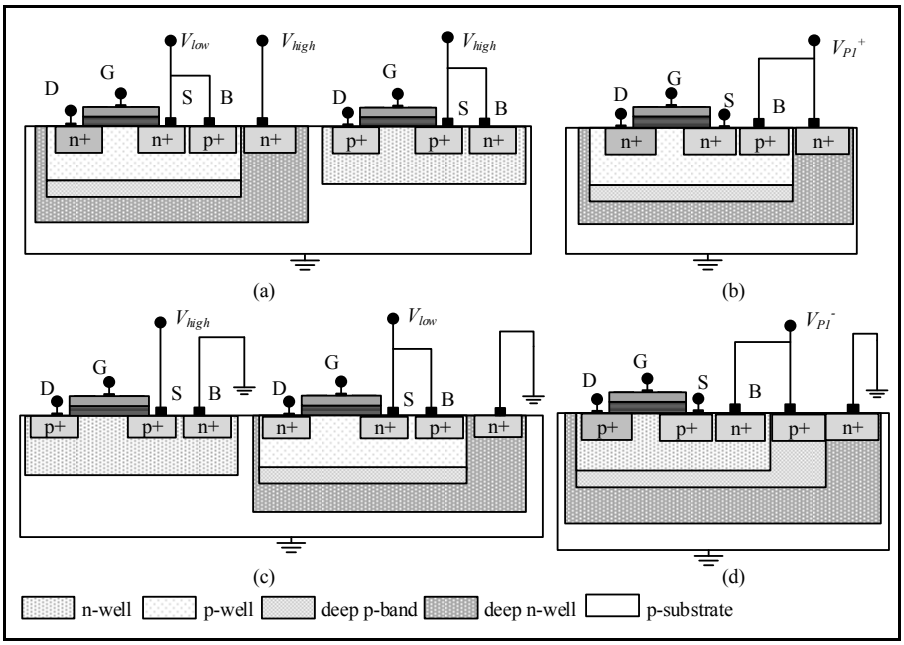

Figure AI.5 Simplified transistor cross-sections for (a) PCP-1 (b) PCP-2 (c) NCP-1 and (d) NCP-2

SIMULATION RESULTS

The circuit was simulated using the SpectreRF simulator in a CMOS 0.13 µm technology. Clocks CLK1 and CLK2 are generated with a switching frequency of 50 MHz and clock driving voltage of 1.2 V. Figure AI.6 presents the simulated output voltages of the four sub pumps: VP1+, VP2+, VP1- and VP2-. The positive charge pump operates with a supply voltage of 1.2 V, while the input of the negative charge pump is connected to ground. A maximum positive output voltage of 16.5 V can be achieved with both PCP-1 and PCP-2 being activated, with a rise time of 14.7 µs and a low ripple voltage of 12 mV. A largest magnitude negative voltage of -16.1 V with a fall time of 24.4 µs and a ripple voltage of 18 mV can be achieved. Both positive and negative outputs provide a voltage range of 32.6 V.

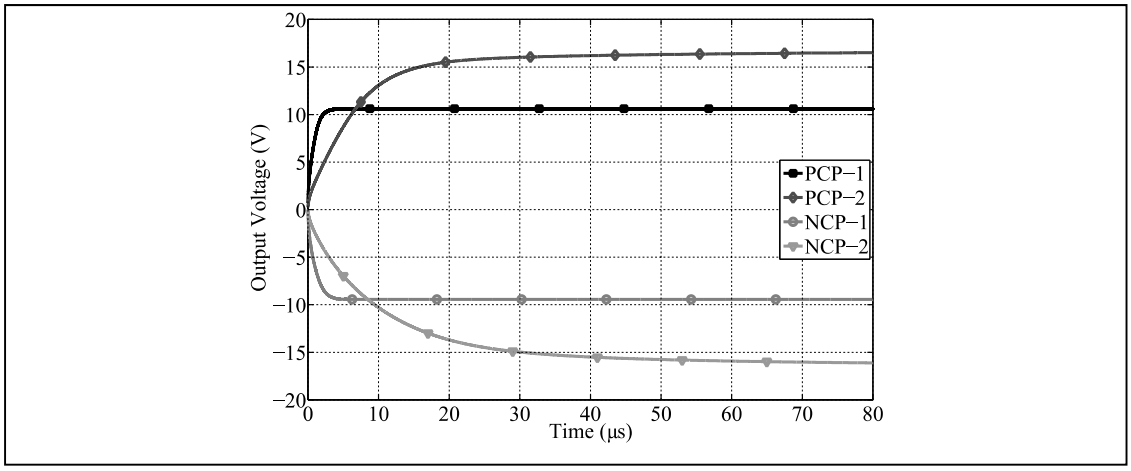

Figure AI.6 Simulated output voltage transient of the four sub pumps with a 1 pF load

The circuit is designed to bias MEMS resonators, hence the 1 pF capacitive load used at the outputs of the circuit in simulations to model the resonator and interconnect parasitics (i.e., pads, pins, etc.). As such, there is no static current delivered to the output. Power consumption is calculated for each circuit separately. The circuit dissipates 74 μW of power when the maximal positive output voltage is generated including the power dissipated in the clock generator, and of 31 μW when the maximal negative voltage is generated and the input connected to ground.

A current source has been added at the output to study the I / V characteristics of the proposed charge pump, with simulation results shown in Fig. AI.7. It can be seen that below a 10 μA output current, the voltage remains within 80% of its maximal value for all four sub pumps. Figure AI.8 shows how the simulated charge pump efficiency varies by changing the output current from 0 to 50 μA. Efficiency is calculated for each sub pump separately. Although the desired application is for capacitive MEMS biasing requiring no DC output current, the circuit exhibits good performance with relatively high efficiencies even with non-zero DC output currents.

The charge pump occupies a total area of about 0.24 mm^2. The areas of the first, second, third and fourth sub pumps are 0.05 mm^2, 0.07 mm^2, 0.05 mm^2 and 0.07 mm^2, respectively.

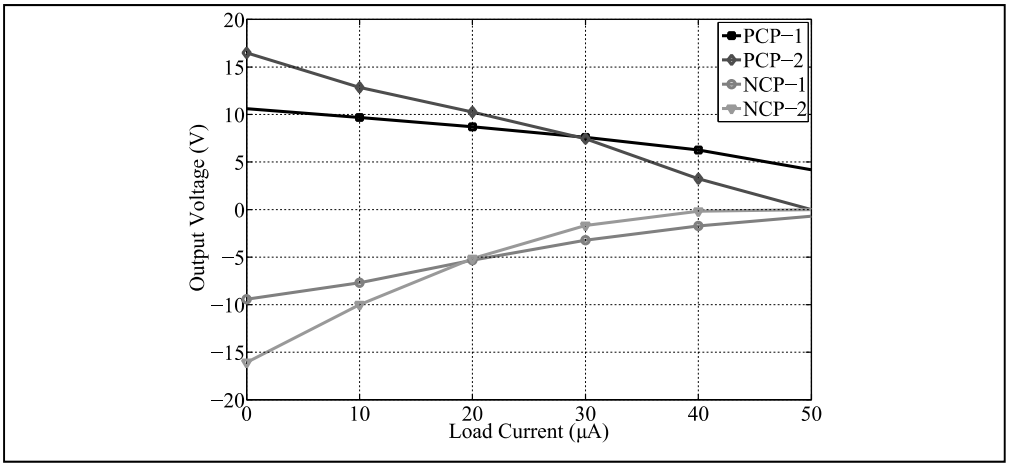

Figure AI.7 Simulated output voltage vs load current of the four sub pumps

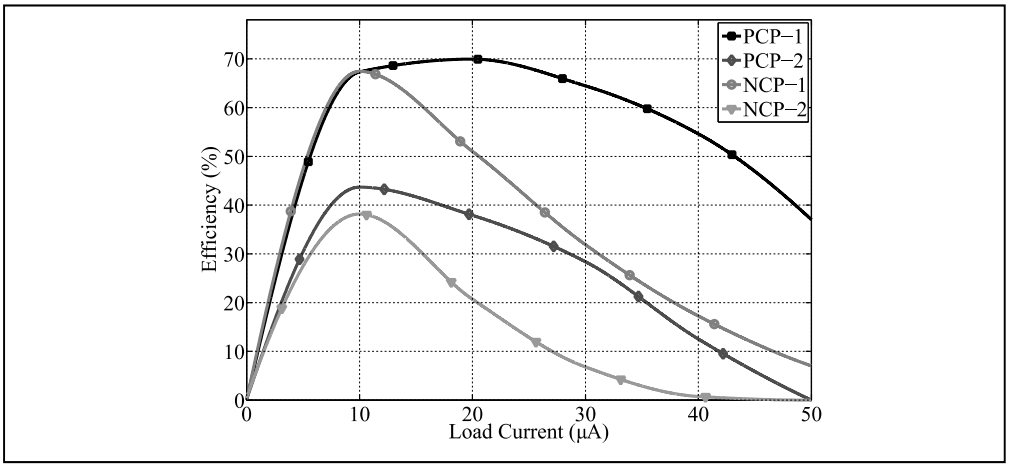

Figure AI.8 Simulated efficiency vs load current of the four sub pumps

Table AI.2 Performance Summary

	PCP-1	PCP-2	NCP-1	NCP-2
Output voltage (V)	10.6	16.5	-9.4	-16.1
Ripple voltage (mV)	30.68	11.87	22.2	18
Rise time (μs)	1.76	14.73	2.21	24.35
Power consumption (μW)	39.17	74.11	24.52	30.88
Efficiency (%)	69.94	43.69	67.43	38.17
Area (mm^2)	0.05	0.07	0.05	0.07

CONCLUSION

This paper presented a low-power wide-range charge pump for MEMS resonators. Table AI.2 summarizes the charge pump characteristics. A range of 32.6 V from a 1.2 V supply is achieved in a standard 0.13 µm technology without the need to go to high-voltage technologies or other complex technologies that can limit the integration with MEMS (Beaulieu et al., 2016). Accordingly, the enabled voltage range is suitable for use in a fully integrated MEMS oscillator such that the proposed circuit generates the DC biasing of the resonator.

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