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## LIST OF ABBREVIATIONS AND ACRONYMS

3D	Three Dimensional
5G	5 <sup>th</sup> Generation
ASIC	Application Specific Integrated Circuit
BEOL	Back End Of Line
BER	Bit Error Rate
BGA	Ball Grid Array
CMP	Chemical Mechanical Polishing
CPU	Central Processing Unit
CPW	Co-Planar Waveguide
CPWG	Co-Planar Waveguide with Ground
DC	Direct Current
EM	Electromagnetic
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
GCPW	Grounded Co-Planar Waveguide
GPU	Graphics Processing Unit
GSG	Ground Signal Ground
HFSS	High Frequency Structure Simulator
IoT	Internet of Things
ISM	Industrial, Scientific, Medical
LACIME	Telecommunications and Microelectronics Integration Laboratory
LCP	Liquid Crystal Polymer
LTCC	Low Temperature Co-fired Ceramic
MaCE	Metal-assisted Chemical Etching
MEMS	Micro Electro-Mechanical Systems
MCM	Multi-Chip Module
PNA	Power Network Analyzer

## XVIII

RF	Radio Frequency
RLCG	Resistance, Inductance, Capacitance and Conductance
SEM	Scanning Electron Microscope
SET	Single Electron Transistor
SiP	System in Package
SIW	Substrate Integrated Waveguides
TCV	Through Ceramic Via
TSV	Through Silicon Via



## LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

Ag	Silver
Au	Gold
°C	Centigrade
Cu	Copper
Gbps	Giga bits per second
mΩ/sq	Milli-Ohm per square
Pa.S	Pascal Second
Ppm/°C	Parts per million per centigrade
Sq	Square
W	Tungsten
W/mK	Watts per meter-Kelvin
Ω	Ohm
Ω/sq	Ohm per square



# INTRODUCTION

## **Motivation and context**

The worldwide growth in data usage is continuing and accelerating even more with the emerging of new technologies such as 5<sup>th</sup> generation (5G) of mobile networks, ultra-high-speed fiber for internet, TV broadcasting of 4K contents and sensor networks. Therefore, the demand for more data and more bandwidth will continue to rise. In addition, the development of communication systems and the number of accessible services on the devices operating at millimeter-wave frequencies, make it necessary to develop low-cost and high-density integrated circuits and packages while retaining their performance. To accommodate this trend, cost-effective multi-layer packaging technologies that offer high reliability with very good performance to maintain signal integrity are needed. These technologies must facilitate the size reduction for high-density packages. One of the main challenges in multi-layer structures is connecting different layers vertically through vias and enabling multi-chip assemblies with interconnections that are as short as and as dense as possible.

## **Problem statement**

Traditionally, the use of vertical interposers on silicon-based substrates and Through Silicon Vias (TSVs) to interconnect different layers has been one of the enabling technologies to allow high-density multi-chip integration, albeit with limited functionality and relatively high cost of fabrication. TSVs are filled by conductors such as copper, tungsten or polycrystalline silicon and they must have an isolation layer enclosing the conductive material to electrically isolate the silicon substrate and the TSV. This thin isolation layer does not work appropriately at high frequencies (Jonghyun Cho, 2010) and will also increase the DC loss of the system. In fact, despite the promising performance of TSVs and silicon interposers at low frequencies, the low resistivity of the silicon substrate leads to an excessive attenuation of transmitted signal at higher frequencies and particularly at millimeter-wave frequencies. This high substrate loss

will become a significant barrier to having an acceptable RF performance and to the development of 3D System in Package (SiP) application based on silicon. Moreover, the high loss of signals in TSVs produces a high noise coupling coefficient among different signals of the system and therefore it could increase jitter, phase noise of clock signals and the bit-error-rate in the data transmission of RF systems (Helmy & Ismail, 2006). In addition, the integration of RF passive components in the inner layer of silicon multi-layer structure is challenging. This challenge makes the design more complex and increases the number of fabrication steps, which consequently increases the cost of manufacturing. Finally, one should also note that the costly part in the silicon interposer manufacturing is via fabrication, isolation and filling. Therefore, finding a technological solution that can provide similar integration capabilities of silicon interposers with TSVs while addressing its limitations is the key problem to be addressed in this thesis.

A LTCC technology-based interposer is one possible alternative to silicon interposers. Indeed, LTCC technology provides the possibility of having an arbitrary number of dielectric layers using very low loss materials with high conductivity metals such as silver (Ag) and gold (Au). It is a promising technology for the realization of 3D integrated circuits and is well suited for packaging. However, the achievable pitch, size of vias, line width and line-to-line spacing with conventional LTCC fabrication methods are not comparable to those that can be achieved with silicon interposers with TSVs. Therefore, for LTCC-based interposers to be viable, the problems related to the standard LTCC fabrication process must be addressed and solutions must be proposed and developed.

### **Thesis objectives**

The main objective of this research project is to bring the necessary improvements to the LTCC fabrication process that will enable it to offer a viable and cost-effective alternative to silicon interposers with TSVs. The second objective is to apply the enhanced LTCC process to the design and realization of a small package for high-density SiP integration of an optoelectronic multi-chip module in collaboration with Ciena Corporation and McGill University. To reach

these objectives, we will seek to realize the smallest micro-via dimension that is possible to fabricate on the thin ceramic sheets along with narrowest transmission lines with the smallest possible pitch between vias as well as the lines.

### **Thesis organization**

This thesis organized in four different chapters. The first chapter discusses the literature review regarding the vertical interposer on silicon substrate, TSV, micro-via, vertical interconnection on multilayer ceramic substrate and LTCC fabrication process. An experimental investigation of micro-vias in LTCC is presented in the second chapter. This chapter also presents a fabricated transmission line designed using the proposed micro-vias on a multilayer ceramic substrate. The third chapter introduces the design and fabrication of a first prototype for an opto-electronic SiP module using wire-bonds to connect the chips to the package. Afterward, a second prototype of this package, employing micro-vias and flip-chipped devices is presented in the fourth chapter. Finally, the last chapter provides a brief conclusion of the work accomplished.

### **Thesis contributions**

The work presented here has led to the development of an enhanced LTCC process with demonstrated feasibility of through ceramic micro vias and small lines widths and pitches. The process makes the realization of ceramic interposers with through ceramic micro-vias feasible thereby offering a viable alternative to silicon interposers with TSVs. This process was utilized to realize a SiP package that was delivered to Ciena and McGill for the integration of a multichip optoelectronic module. The main results of this work were the subject of IEEE international 20<sup>th</sup> Electronics Packaging Technology Conference (EPTC) publication. In addition, I was participated on other paper which is under review to published on the journal of Transactions on Components, Packaging and Manufacturing Technology. Following are the details of these publications:

Adibi, A., et al., "Ceramic Interposer for Ultra-High Density Packaging and 3D Circuit Integration," IEEE 20th Electronics Packaging Technology Conference, pp. 13-16, Dec 2018.

Pourzadi, A., Adibi, A., Kouki, A., "A Fast Technique for Realization of Lumped-Element Values Into 3D Physical Layout on LTCC," IEEE Journal of Transaction on Components, Packaging and Manufacturing Technology.

## CHAPTER 1

### LITERATURE REVIEW

In current telecommunication systems, due in part to the arrival of 5G technology and the Internet of Things (IoT), higher data speeds and greater bandwidth are required. The peak data rate for a whole system was around 100 Mbps in the late 1990s. By 2017 it had increased to more than 200 Gbps (C. Doerr, 2017). This need for higher speed of data transmission accelerates the need for new technologies and methods of data transfer to reach the desired rates and beyond. Therefore, this has served as a motivation for designers to move towards higher frequency bands such as millimeter-wave or optical frequencies (M. A. Jezzini, 2016).

This increasing of the speed of transmission will increase the losses in microwave circuits and systems. On one hand, in millimeter-wave and optical frequencies, the physical length of components and circuits are much smaller compared to the wavelength. On the other hand, demand for low cost and high reliable technology maintain performance of the system, makes it inevitable to move towards a new technology of fabrication and 3D packaging. In this project, a cost-effective technical method for this purpose based on Low Temperature Co-fired Ceramic (LTCC) technology is proposed and demonstrated.

The first chapter of this thesis presents a literature review concerning the related subjects such as TSV, interposer, micro-via, multilayer SiP, LTCC presentation and its fabrication process.

#### 1.1 Through Silicon Via (TSV)

In multi-layer circuits or packages based on silicon substrates, TSVs (Through Silicon Vias) are used to create a vertical transition path for the signals between different layers. This technique is an alternative to connection through bonding wires in order to increase the number of I/O, decrease signal delay and therefore increasing the speed of data transmission. Figure 1.1 presents the structure of a TSV (left) with reference to the active device and back-end

interconnect stacking in a wafer (Ravi Mahajan, 2017), and a SEM (Scanning Electron Microscope) photograph of a typical fabricated TSV (right). These via-holes are isolated from the silicon substrate by a dielectric layer and then filled by conductor such as polycrystalline silicon, W (Tungsten) or Cu (Copper). It is important that these vias have the return and radiation losses as low as possible.

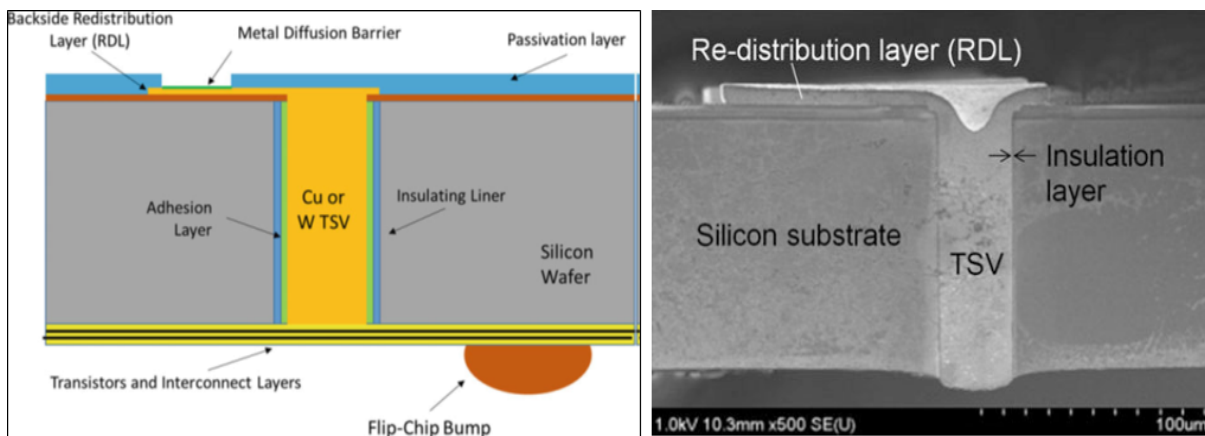


Figure 1.1 Left: Structure of TSV in the silicon back-end interconnect stack. Right: SEM of fabricated TSV: electrical design of through silicon via<sup>1</sup>

The silicon interposer has complicated fabrication process that increases the cost of manufacturing. In general, the costliest part is creating the hole via on the silicon substrate, isolation and filling. Fabricating this vertical electrical connection in a silicon substrate can be carried out by different techniques that require several steps. In one of these techniques, the first step is deep silicon etching where the holes are created on the silicon substrate. The next step is via oxide deposition to insulate the conductor from substrate to degrade the DC (Direct Current) loss of the substrate. After that, conductor plating is performed where a liquid conductor is injected into the hole. The processes of BEOL (Back End Of Line) Chemical Mechanical Polishing (CMP) or polishing the surface of wafer is the last step (Gong, 2014).

<sup>1</sup> 3D Microelectronic Packaging. Cham: Springer Nature; 2017. p. 31



The silicon technology has some drawbacks at high frequency such as low resistivity for the TSV, ineffective isolation layer and high noise coupling coefficient among different signals due to the high value of signal loss. The resistivity of silicon substrate attenuates the signal passing vertically through TSV, and consequently this lossy signal degrades the RF performance at high frequencies (Soon Wee Ho, 2008). When current flows in the fine TSV, it can generate ohmic heat and accordingly hot spots in high-power chips, that negatively effect on the performance of the package (Heng Yun Zhang, 2014).

Additionally, the thin isolation layer surrounding the conductive material filled inside the TSV cannot prevent sufficiently the electrical parasitic coupling and critical substrate noise in the vicinity of active devices and/or adjacent TSVs. The effect of this noise is increasing the jitter and phase noise of clock signals as well as increasing the Bit-Error-Rate (BER) of the RF signals (Jonghyun Cho, 2010). In (Nauman H. Khan, 2011), coaxial TSVs with a diameter of 35.4  $\mu\text{m}$  were used in order to overcome the noise issues of regular TSVs. In (Heng Yun Zhang, 2014), the TSVs with 10  $\mu\text{m}$  diameter were used in high power circuits where two dummy dies and a thermal die were added to the circuit to improve the thermal performance of the structure.

## 1.2 Interposers

The word Interposer comes from a Latin origin “interpōnere” which means, “to put up between”<sup>1</sup>. An interposer electrically connects different parts of an electronic circuit through multiple layers and vias. In modern packaging technology, vertical interposers with flip chip attachments are used as an alternative to wire-bond connections. Generally, the performance of wire-bonds at frequencies above 30 GHz is not practical because it will have some impact on the performance of the device (C. Doerr, 2017). Due to the high characteristic impedance of wire-bonds, it would have an inductor behavior at high frequencies or behave as an antenna or a resonator (Rida, 2013). Therefore, wire bonding decreases the quality of the RF signals at

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<sup>1</sup> Collins Dictionary

high frequencies. The interposers are employed as a good alternative for wire-bonds in 3D packages; and most interposers in use today are made with silicon substrates and TSVs.

The use of silicon interposers is principally in the integration of Micro Electro Mechanical Systems (MEMS), Field Programmable Gate Array (FPGA) technologies, ASICs (Application Specific Integrated Circuits), server CPUs (Central Processing Unit), GPU (Graphics Processing Unit) and wireless devices (Timothy G. Lenihan, 2013).

In (Yan Yang, 2019), a CPW (Co-Planar Waveguide) transmission line on a silicon substrate in multilayer structure is presented where the Ground-Signal-Ground (GSG) TSV used for vertical interconnection. This structure operates in the frequency up to 40 GHz. The designed parameters of this transmission line such as via diameter, depth of via and center-to-center pitch of the lines are 20  $\mu\text{m}$ , 100  $\mu\text{m}$  and 100  $\mu\text{m}$ , respectively. The (Kuili Ren, 2016) presents a development process of thick silicon interposer for integrated inductor, micro-strip and CPW transmission lines. In their paper, a TSV with the diameter of 80  $\mu\text{m}$  and the thickness of 300  $\mu\text{m}$  for vertical interposer is reported. In other work presented on (J-R. Tenailleau, 2013), a TSV developed for the RF interposer applications with the nominal diameter of 75  $\mu\text{m}$  and pitch of 125  $\mu\text{m}$ , which is scalable for industrial production. They tested this via on a structure of dual via chain including CPW transmission line access, which is operates in the frequency range of DC to 20 GHz. In (Liyi Li, 2015) a via with a diameter of 28  $\mu\text{m}$ , a pitch size of 80  $\mu\text{m}$  and a depth of 162  $\mu\text{m}$  was fabricated on silicon substrate by using Metal-assisted Chemical Etching (MaCE).

At high frequencies, the ceramic interposer is a good alternative for the silicon interposer because of its lower resistivity and its easier fabrication process. In (Li & Zhou, 2015), a seven-stage cascaded coaxial impedance based on ceramic sheets of Ferro A6S designed to use as a vertical transition for low-pass structure in 20 layers. The reason of using these seven stepped coaxial impedances is increasing the bandwidth and decreasing the second order resonant frequency. This via transition works from DC up to 30 GHz and the diameter of via in this structure varies from 120  $\mu\text{m}$  to 220  $\mu\text{m}$ . The measurement results for the microstrip to

microstrip transition through the coaxial via from DC to 30 GHz were better than -12 dB and -0.5 dB for  $S_{11}$  and  $S_{21}$ , respectively. Another work of vertical transition from microstrip to microstrip was reported in (Chih-Chun Tsai, 2011) where the via has a diameter of 135  $\mu\text{m}$  and they achieved a return loss better than -20 dB and an insertion loss below than -0.48 dB for the whole ISM (Industrial, Scientific, Medical) band (DC to 67 GHz). In addition, the (T. Kangasvieril, 2006) reported three different transitions from GCPW (Grounded Co-Planar Waveguide) to GCPW, GCPW to microstrip and GCPW to stripline by employing the vias 150  $\mu\text{m}$  in diameter in a 8-layer structure. The result of this work present good transmission characteristic up to V-band (50 GHz). The insertion loss and return loss measured -0.4 dB and -18 dB, respectively.

Table 1.1 summarizes the different research where the vias with varying diameter were used for different interposer applications.

Table 1.1 different application of vertical interposer

	<b>Via diameter</b>	<b>Thickness</b>	<b>Frequency</b>	<b>Application</b>	<b>Substrate</b>
Yan Yang, 2019	20 $\mu\text{m}$	100 $\mu\text{m}$	DC to 40 GHz	CPW transmission line	Silicon
Kuili Ren, 2016	40 $\mu\text{m}$ 80 $\mu\text{m}$	70 $\mu\text{m}$ 230 $\mu\text{m}$	N/A	Integrated inductor, micro-strip and CPW transmission lines	Silicon
J-R. Tenailleau, 2013	75 $\mu\text{m}$	200 $\mu\text{m}$	Up to 20 GHz	2.5D Interposer applications	Silicon
Liyi Li, 2015	28 $\mu\text{m}$	162 $\mu\text{m}$	N/A	Silicon interposer in wafer level	Silicon
Li & Zhou, 2015	120 – 220 $\mu\text{m}$	2000 $\mu\text{m}$	DC to 30 GHz	Microstrip to microstrip transition through Coaxial via	Ceramic
Chih-Chun Tsai, 2011	135 $\mu\text{m}$	740 $\mu\text{m}$	DC to 67 GHz	Microstrip to microstrip	Ceramic
T. Kangasvieril, 2006	150 $\mu\text{m}$	800 $\mu\text{m}$	DC to 50 GHz	GCPW to GCPW GCPW to microstrip GCPW to stripline	Ceramic

Clearly, as Table 1.1 shows, the main challenge for making ceramic interposers is the fabrication of smaller micro-via that can be comparable with the range of via diameter in silicon substrate.

### 1.3 Micro-vias in ceramic substrate

Micro-via is a crucial part of high-density interconnection in multi-layer SiP structures at high frequency, because it should support the small pitch between the pads of devices and between the adjacent lines. By increasing the frequency, the wavelength will be decreased. Consequently, the width of transmission line, the dimension of ICs and RF components that used in this range of frequency will also decreased. Therefore, creating the micro-via in order to make interconnection between different layers of package is crucial. In fact, fabricating the smallest possible via is the biggest challenge of multi-layer packaging. The value of via diameter and the small pitch between two adjacent vias can determine the miniaturization ability of the multi-layer packaging.

In conventional RF structures and circuits, the long interconnections and vias act as an undesirable transmission lines in high-speed data transmission, which causes an extra delay into the system. This transmission line behavior in interconnection happens when the electrical length of interconnection or via is longer than half of the signal rise time. Therefore, by increasing the frequency and the speed of signals, it will be important to keep these internal connections as short as possible. In addition, the short interconnections prevent having the high inductance in the system and thinner vias can reduce radiation loss; and consequently, the insertion loss is improved.

Furthermore, in order to achieve proper filling of micro-vias, the aspect ratio of the vias should be considered. The aspect ratio is the ratio between the depth (thickness of ceramic sheet) and width (diameter of hole) of vias as given by equation 1.1 and illustrated in figure 1.3. A via that has a smaller diameter than its length can be unrealizable for fabrication.

$$Aspect\ Ratio = \frac{Depth\ (\mu m)}{Width\ (\mu m)} \quad (1.1)$$

Indeed, the smaller the aspect ratio of vias is, the easier it is to fill it. The aspect ratio of via fabrication for mass production in industrial project is 0.64:1, which means that via diameter should be 64 percent of substrate height (IMST, 2011).

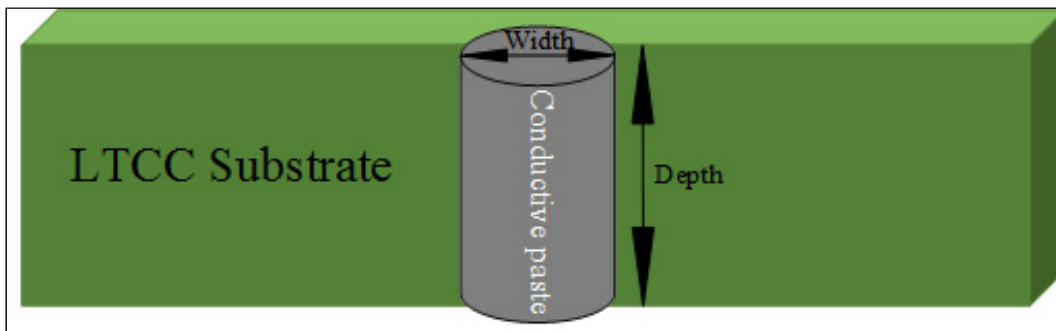


Figure 1.2 Via aspect of ratio (Depth to Width)

In (Gangqiang Wang, 2006), they achieved to drill and use the vias with the diameter between 50-100  $\mu\text{m}$  in a six-layer high interconnect density design with a decent alignment. In (M. A. Jezzini, 2016), they used the vias with 150- $\mu\text{m}$  diameter for multi-layer packaging on LTCC on the layers with the thickness of 127  $\mu\text{m}$  and 254  $\mu\text{m}$ . This design is working at the frequency of 37 GHz with 3 dB bandwidth. In paper (J. Vanek, 2008), an experimental test has been done to figure out the smallest via diameter realizable on different ceramic type of sheets. Hence, the smallest via diameter that built experimentally was 115  $\mu\text{m}$  on the Ferro A6M tape with the thickness of 100  $\mu\text{m}$ . In other works, a micro-via with 75  $\mu\text{m}$  diameter on a 254  $\mu\text{m}$  thick ceramic sheets was fabricated (Shafique, 2009) by using the 25  $\mu\text{m}$  focal diameter laser for use in the fabrication of a Substrate Integrated Waveguides (SIW) operating at the frequency of 25 - 40 GHz. These resolutions were applied for substrate-integrated waveguide fabrication but remain far from the typical TSV resolution of 25  $\mu\text{m}$  or better via diameter and a pitch of 50  $\mu\text{m}$  or better.

In the SiP and multilayer package, the signal transition between different transmission lines has a key role in the structure. One of them is CPW to stripline signal transition and in (A. Bhutani, 2017) a fabricated via-based CPW to stripline signal transition is presented. This structure fabricates on the LTCC substrate tape of DuPont<sup>TM</sup> GreenTape<sup>TM</sup> and operate from

DC to 150 GHz. In this broadband signal transition, they used signal via with the diameter of 80  $\mu\text{m}$  for vertical transition. The shortest pitch of these vias was 200  $\mu\text{m}$  and the thickness of layers was 106.7  $\mu\text{m}$  after firing. In this design, an air cavity between signal via catch-pads and stripline, and circular apertures in lower ground of stripline employs in order to reduce the parasitic capacitance effect of structure. In (Zhipeng Li, Aug. 2017), a microstrip-to-microstrip signal transition is designed to operate from 5 GHz up to 60 GHz. In this structure two type of vias for signal and ground transition with different diameter are used. The diameter of signal via and ground via are 450  $\mu\text{m}$  and 150  $\mu\text{m}$ , respectively. In addition, in several project for millimeter-wave applications the researcher used the rectangular via for the vertical transition in multilayer structure. In (Isapour Aria, 2019), a vertical LTCC integrated waveguide for multilayer structure is presented, which is operates at the frequency around 60 GHz. The proposed structure facilitates the integration of passive component such as filters, couplers and power dividers perpendicular to the surface of structure. For this design, the rectangular vias were required to make the vertical waveguide.

Table 1.2 used circular via diameter in different projects

	<b>Via diameter</b>	<b>Frequency</b>
Gangqiang Wang, 2006	50-100 $\mu\text{m}$	N/A
M. A. Jezzini, 2016	150 $\mu\text{m}$	37 GHz
J. Vanek, 2008	115 $\mu\text{m}$	N/A
Shafique, 2009	75 $\mu\text{m}$	25 – 40 GHz
A. Bhutani, 2017	80 $\mu\text{m}$	DC to 150 GHz
Zhipeng Li, Aug. 2017	150 $\mu\text{m}$	5 – 60 GHz

The size of micro-via is constrained between two boundaries. First diameter limit of micro-vias fabrication determined by the laser beams or punching machine, which limit the physical size during via drilling. Second, the viscosity of grain paste. This can limit the size of micro-

via where the viscosity decreases, the via diameter should increase and vice versa; otherwise, the conductive paste cannot fill the micro-vias properly. Based on the bibliography of previously published work regarding vias in ceramic substrate, which is summarized in table 1.2, the standard vias used currently on LTCC technology has the diameter varies from 50  $\mu\text{m}$  to 150  $\mu\text{m}$  with a pitch ranging from 150  $\mu\text{m}$  to 300  $\mu\text{m}$ . Via filling for these sizes is well established and is achieved with standard metal pastes.

#### 1.4 3D SiP

The use of appropriate material and technology for millimeter wave and optical frequency packaging is important to have the optimum package size, impedance, and low loss. The 3D or multi-layer System in Package (SiP) technology is an advanced packaging method, which enables the designer to interconnect the integrated components and circuits in different layers together while also connecting them with the active devices located on the surface of the package. This is useful in applications such as: Single Electron Transistor (SET), FinFet Transistor, Integrated Circuit (IC) and etc. Current 3D technology for multi-layer low loss packaging is based on the silicon substrate and Liquid Crystal Polymers (LCP), (M. A. Jezzini, 2016). Due to their inconvenience for operating at the higher frequency, RF engineers have been motivated to use the ceramic substrate as an alternative to these technologies.

The development of this technology to operates at millimeter wave and optical frequencies with different functionalities requires that the devices be as small as possible, in addition to short and dense interconnections, smaller micro-vias and finer physical substrate. The reduction of the length of interconnections makes the propagation time shorter and decreases the parasitic effects. Additionally, the consumption and fabrication cost of the system decreases due to the reduction in the size of components, and the use of 3D packaging, (Rida, 2013). In the other hand, these dense multi-layer packages and their interconnections can increase the crosstalk between the channels.



In addition, substrate loss is a critical property in improving the functionality of 3D SiP. LTCC technology can provide the distinct opportunity for 3D packaging. It is one of the pioneer technologies that provide the possibility to integrate the passive components in the inner layers of structure and interconnect the integrated components to the other elements or transmission line on different layers or connect them to the active components where mounted on the surface of structure through the vertical interposer. While, the vertical interposers of silicon substrate and LCP substrate have their own constraint in optical frequency. The isolation layer of TSV works inappropriately at high frequency and LCP does not provide the necessary mechanical rigidity for vertical interposer (M. A. Jezzini, 2016). Furthermore, the cavity formation is another LTCC advantage in order to use for high-density package at high frequencies. LTCC technology facilitates the open or close cavity fabrication in any desired shape and depth. The main use of these cavities can be putting the component inside them in order to decrease their connection length.

The ability to integrate passive components inside of the LTCC substrate provides a package with high reliability by decreasing the number of interconnections and also reducing the length of them. The electrical elements that can be integrated in the inner layer of LTCC packaging technology including resistors, capacitors, inductors, LC shunts and series, the components such as filters and resonators, etc. Additionally, in this technology the value of capacitor and inductors can be easily increased by using respectively the conductive and magnetic tapes (Rida, 2013).

## **1.5 LTCC Technology**

Low Temperature Co-fired Ceramic (LTCC) is a multi-layer technology used to design and fabricate passive components on 3D structure, which facilitates the size reduction of high-density and multi-functional RF package in millimeter-wave and optical frequencies. In this technology, the circuits and components designed with ceramic sheets use dielectric, resistive and conductive paste which are co-fired concurrently in an oven at the temperature below than 1000 °C (around 850 °C) for more than 12 hours. This sintering temperature enables the

designer to use the low resistance and high conductive conductors such as silver (Ag) and gold (Au) (Aria Isapour, 2017).

A conventional LTCC structure can include dielectric tapes, buried and surface-mounted conductors, transmission lines, passive components, resistors, interconnecting vias, surface-mounted electrical and optical devices. This technology has the possibility to design and fabricate the passive components in inner layers as buried components or on top layer as surface-mounted components. Therefore, LTCC is an assuring technology for 3D integrated structure and package that offer high reliability with very good performance. Generally, this technology is used in different applications such as passive components, integrated circuit, functional MCM (Multi-Chip Module) and System in Package (SiP).

### 1.5.1 Advantages of LTCC

LTCC technology has attracted the attention of RF designer because of its numerous advantages to operate at high frequency (up to 100 GHz). These advantages allow this technology to be a considerable alternative for current technology for 3D integration and fabrication of miniaturized package. In addition, it facilitates the integration of passive components in the inner layer of structure. LTCC has the following characteristics:

- Low loss conductor and tangent loss,
- Low dielectric loss at millimeter wave and optical frequencies,
- Allow to use noble conductors such as silver (Ag) and gold (Au),
- Offers multilayer structure (up to 40 layers) with high accuracy of device alignment,
- Possibility to integrate electrical passive component in inner layers,
- Better thermal resistance and thermal expansion coefficient than silicon substrate,
- Better product reliability than silicon technology at millimeter wave,
- Compatibility with hermetic sealing,
- Cost efficiency.

In this project, the A6M ceramic sheets provided by Ferro Corporation was used as a substrate with different thickness of 1-mil, 2-mil, 5-mil and 10-mil. The thinnest ceramic sheet (1-mil) has not yet be commercialized and is used only for research purpose. In addition, we used a customized gold-based conductive paste (CN30-078M) provided by Ferro for this tiny sheet. Table 2.1 present the typical properties of A6M ceramic tape.

Table 1.3 Characteristics of Ferro A6M ceramic tape and conductor paste<sup>1</sup>

<b>Thermal Coefficient Expansion</b>	7.0	Ppm/°C
<b>Thermal conductivity</b>	2	W/mK
<b>Dielectric Constant</b>	5.7 ± 0.2	@ 10 GHz
	6 ± 0.2	@ 50 GHz
<b>Loss Tangent</b>	< 0.1	@ 10 GHz
	< 0.15	@ 50 GHz
<b>Conductor Thickness</b>	8	µm
<b>Tape Shrinkage</b>	15.8 ± 0.3	% X, Y
	26.0	%Z
<b>Viscosity of Conductor Paste</b>	28000	Poise
<b>Resistivity of Conductor Paste</b>	< 12	mΩ/sq
<b>Thermal conductivity of CN30-078</b>	>50	W/mK

### 1.5.2 LTCC Fabrication process

The LTCC manufacturing process has various steps as shown briefly in figure 2.1 provided by LACIME (Telecommunications and Microelectronics Integration Laboratory), laboratory at

<sup>1</sup> Technical Data Sheet of Ferro A6M/A6M-E High Frequency LTCC Tape System and A6M/A6ME LTCC Au Conductor System

ETS (École de Technologie Supérieure). The fabrication process is simplified and demonstrated different phase of LTCC manufacturing procedure as an infographic.

The LTCC fabrication process begins with cutting green tapes with the dimension of 12x12 cm. This dimension is the acceptable dimension of fabrication devices that used in LACIME laboratory. Then, the sheets are punched by laser machine or punching machine in order to make the vias. The difference between these machines is that laser machine offer drilling the vias in different shapes and diameter size, whereas the punch machine has some predefined vias with different size. In the laboratory of LACIME, we have the opportunity to use the punching machine and the LPKF U3 laser machine with a minimum diameter of 15  $\mu\text{m}$  to make micro-vias. Generally, the punching machine is used for making the vias with regular diameter sizes in the ceramic sheets; and similarly, to create the alignment via in the corners of the tape. The alignment via is several standard vias in two different sizes of 3 mm and 150  $\mu\text{m}$  that located in the four corners of the sheet in order to facilitate the precise alignment during the fabrication process. On the other side, the laser machine has the ability to use for making any circular or rectangular via with different diameter sizes (LTCC Process Design Rules, 2018). Although milling with a laser beam diameter of 15  $\mu\text{m}$  allows to drill vias smaller than 50  $\mu\text{m}$  in LTCC, the coarse metal grain in standard metallic pastes makes via filling of such micro-vias impossible.

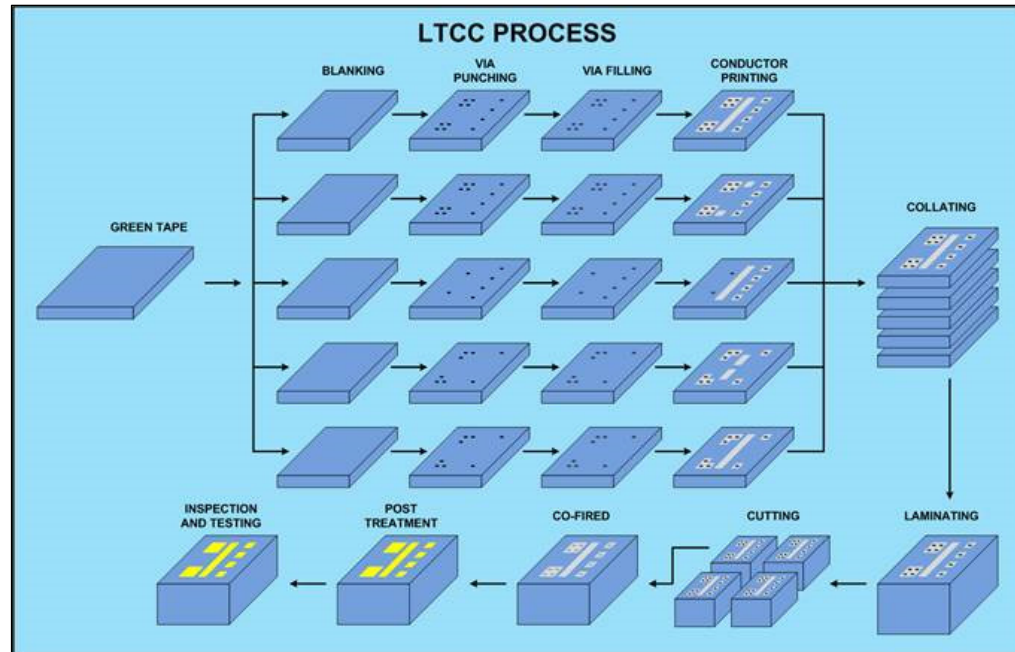


Figure 1.3 LTCC fabrication process provided by LACIME<sup>1</sup>

Afterward, the drilled vias will be verified by microscope to investigate if their shapes are correct and drilled properly. Then, the vias are fill by appropriate conductive paste manually or by printing machine. The next step is conductor printing where the conductor lines are print on the surface of every needed sheets. As an additional process of this step, the ablation will be done on the conductor lines in order to trim them or create the necessary dimension and shapes on them. Subsequently, these individual sheets are collated and stacked by a stack machine; after that the structure is put in the isostatic press machine in order to completely remove any undesired tiny space of air between the layers. After the laminating steps, the LTCC structure with the dimension of 12x12 cm is cuts to one or several structures with suitable dimensions. Finally, these structures are co-fire on the oven at the temperature of around 850 °C for more than 12 hours. Post treatments on the structure can be done if the conductors must be trimmed. The last step is mounting the surface-mount devices and wire-bond them to the ceramic structure.

<sup>1</sup> Photo courtesy of LACIME (Telecommunications and Microelectronics Integration Laboratory), ETS

One of the benefits of this kind of multi-layer fabrication process is that each layer is fabricated separately, and it could be replaced or re-fabricated before stacking if any damages or defects is found on the sheets. This advantage of fabrication process compared with the silicon technology will save the time because it prevents re-manufacturing the whole structure, and therefore keeps the cost efficiency of fabrication.

## CHAPTER 2

### LTCC FABRICATION PROCESS IMPROVEMENT FOR CERAMIC INTERPOSER REALIZATION

To offer a viable option to silicon interposers, TSV's diameter, pitch to pitch of vias and width of lines in silicon substrate, we must be able to achieve very small vias (micro-via) with the diameter in the range of below 50  $\mu\text{m}$  (the current minimum via diameter in LTCC technology) and as close as possible to the range of 20  $\mu\text{m}$ , single ended and differential transmission lines with line widths and pitch of 100  $\mu\text{m}$  and 125  $\mu\text{m}$ , respectively. In this chapter, we investigate the feasibility of ceramic interposers and propose the necessary LTCC process improvements that will help meet the goal.

Following the LTCC technology and fabrication presentation, an experimental investigation regarding the realizable small micro-via diameter and small center-to-center via pitch will be introduced. This investigation was carried out on a thinnest Ferro's A6M ceramic sheet with the thickness of 1-mil which is available currently for the research purpose. Afterwards, in order to demonstrate the functionality of the proposed technique of micro-via fabrication for high frequency circuitry, these thin ceramic sheets and fabricated micro-vias were experimentally used to build the 50  $\Omega$  CPW (Co-Planar Waveguide) transmission lines. These transmission lines have been designed as a multilayer structure using Trough Ceramic Via (TCV) to connect the surface printed lines with the buried lines located in inner layer.

#### 2.1 LTCC Micro-Via Fabrication

This section is focused on the realization of micro-vias in LTCC technology as an alternative to TSVs.

### 2.1.1 Micro-via Fabrication Steps

Realizing a micro-via in LTCC fabrication process consists of two important steps: first steps is punching or drilling the via holes in the ceramic sheets and the second ones is filling them with an appropriate conductive paste. In this process, every step has its limit in order to manufacture vias and decreasing their diameter size. In general, there are two issues that limit the diameter size of micro-via; the first one is laser beam diameter, and the second one is the viscosity and particle size of the conductive paste for filling the vias. While the laser process determines the minimum feasible via pitch before the two adjacent vias mechanically collapse, the viscosity and grain size of the conductive paste limits the size of the minimum via diameter that can be filled properly.

In this project, an LPKF U3 laser machine with a laser beam of 15  $\mu\text{m}$  diameter is used to drill the micro-vias. Then, the via filling is carried out on a thick film screen-printing machine with adjustable vacuum under tapes for proper filling. This vacuum facilitates the leaking of conductive paste into the hole. In fact, the viscosity of the paste, using for via filling has the reverse relation to the vacuum using in this process. Similarly, with the same conductive paste, if the diameter of vias are small, then the vacuum should be more intense than using the via with larger diameter size. Furthermore, the grain size of conductive paste is also an important factor of manufacturing; since the pastes with the bigger grain size are unable to enter and fill the holes that has smaller outer diameter size. Therefore, to be able to realize smaller micro-vias, a paste with small grain size along with a thin LTCC green tape are needed. To this end, a customized custom gold-base conductive paste (Au8886-A) provided by Ferro Corporation was used.

In order to overcome the second limit of micro-via fabrication and filling the holes properly by this customized conductive paste, which has low viscosity, the aspect ratio of micro-via should be as small as possible. Therefore, a custom 1-mil thick Ferro green tape was used in this project. It is worthwhile to mention that the 1-mil thick Ferro's ceramic sheet was not available for commercial purposes yet.



### 2.1.2 Experimental Investigation of LTCC Micro-Via

To determine the best realizable micro-via diameter and minimum possible pitch, an experimental investigation was performed by using the thinnest Ferro's A6M ceramic sheet and special conductive gold-based paste fabricated by Ferro Corporation. First, an array of vias with varying diameter size and different pitches was created. In this investigation, the micro-via diameters ranged from 16 to 36  $\mu\text{m}$  in the steps of 2  $\mu\text{m}$ . The reason of choosing the size of 16  $\mu\text{m}$  as the smallest via diameter is the limit of LPFK U3 laser machine, which has a laser beam of 15  $\mu\text{m}$ . In addition, the center-to-center pitch of vias was varied from 26  $\mu\text{m}$  for the smallest diameter (16  $\mu\text{m}$ ) to more than 100  $\mu\text{m}$  for the larger micro-vias in the steps of 5  $\mu\text{m}$ .

The figure 2.1 in below presents a diagram of the designed micro-via's array in different diameter and pitch combinations to be fabricated. In general, the minimum pitch of micro-vias for every diameter have been chosen to start from via diameter size plus 10  $\mu\text{m}$ ; for example, the minimum pitch of 18  $\mu\text{m}$  via diameter is 28  $\mu\text{m}$  and the minimum pitch for the diameter of 36  $\mu\text{m}$  is 46  $\mu\text{m}$ . The designed array of micro-via was fabricated on a 1-mil thick LTCC green tape and the figure 2.2 shows a photograph of seven most interesting columns of these filled micro-vias. In this picture, each column represents vias of the same diameter with increasing spacing between them going down.

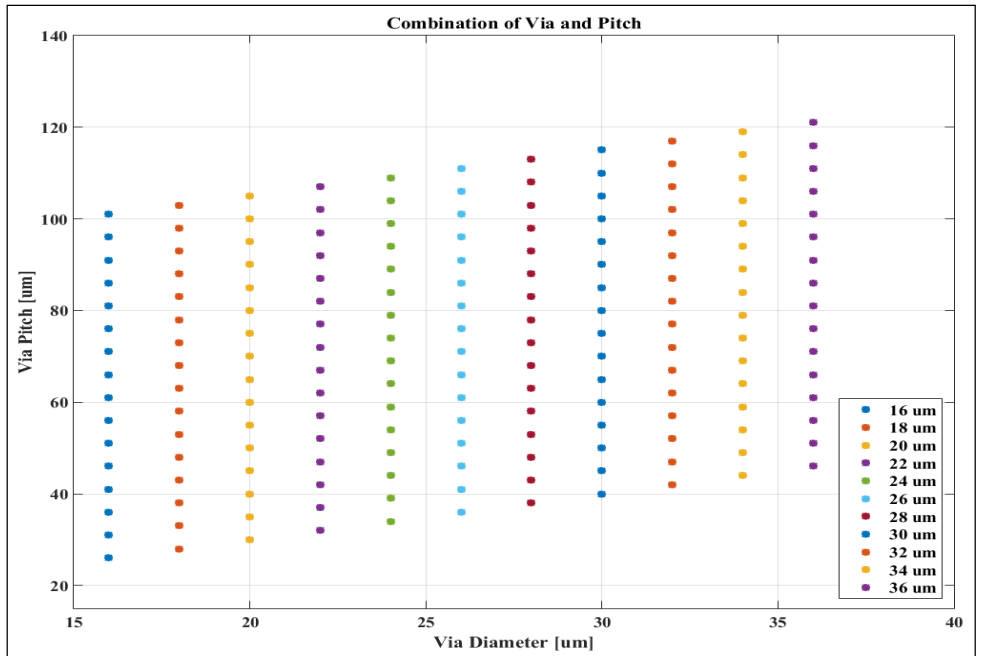


Figure 2.1 Via diameter vs Via pitch

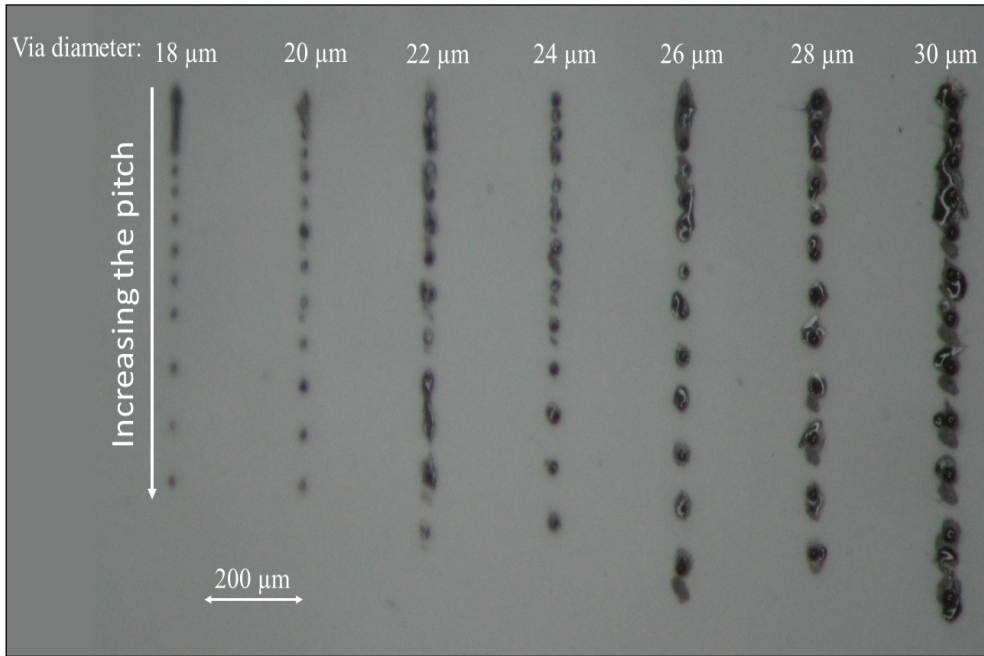


Figure 2.2 Fabricated micro-via with varying via diameter and via pitch on 1-mil thick ceramic sheet

The result of this experimental investigation was examined by a 3D confocal laser microscope, Olympus LEXT OLS 4000, available at LACIME laboratory. In order to determine the smallest realizable via diameter, we consider the last row of micro-vias where the spacing between adjacent vias is largest.

Based on this examination, the vias with the diameter of 16  $\mu\text{m}$  and 18  $\mu\text{m}$  had unacceptable circular shape. Because the laser machine with the laser beam of 15  $\mu\text{m}$  was unable to properly drill this range of diameter size; and accordingly, the filling of these series of micro-vias were impractical. On the other side, for the micro-vias with the diameter of 30  $\mu\text{m}$  and beyond, there were lack of metallization. The reason is that this conductive paste was incapable to fill appropriately these ranges of micro-vias with big aspect ratio. In fact, this gold-based paste has the small grain size and low viscosity (15-25 Pa.s<sup>1</sup> at 25.5 °C  $\pm$  0.5 °C) comparing to the regular conductive past. Therefore, during filling the micro-via even without using the vacuum option from bottom of the ceramic sheet, the conductive paste spread out from the other side of the holes with large size of via diameter.

Unlike these two ranges of via diameters on the corners of the designed array, the micro-vias with the diameter between 20 – 28  $\mu\text{m}$  were drilled correctly in a circular shape with accurate diameter size. In addition, they filled properly by the customized conductive gold-based paste. Consequently, to take advantage of this 1-mil thick ceramic sheet, we were limited to use the micro-vias with the diameter between 20 – 28  $\mu\text{m}$ .

In addition to the smallest via diameter, the minimum possible center-to-center pitch of micro-via should be determined. Thus, in order to determine the smallest pitch, the column of the via with the diameter of 20  $\mu\text{m}$  considered as the smallest filled micro-vias and again a visual inspection with the 3D confocal microscope has been done. Therefore, the 40  $\mu\text{m}$  of center-to-center pitch was detected as a smallest pitch of two adjacent filled micro-vias. In general, based

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<sup>1</sup> Pascal Second

on our experimental investigation and validated with fabrication, the pitch of micro-via should be at least twice of the diameter of the micro-vias.

Figure 2.3 demonstrates a picture of two adjacent micro-vias with the diameter of  $20\ \mu\text{m}$  and the center-to-center pitch of  $40\ \mu\text{m}$ . This picture was taken by 3D confocal microscope where a pair of micro-vias was drilled correctly and filled appropriately.

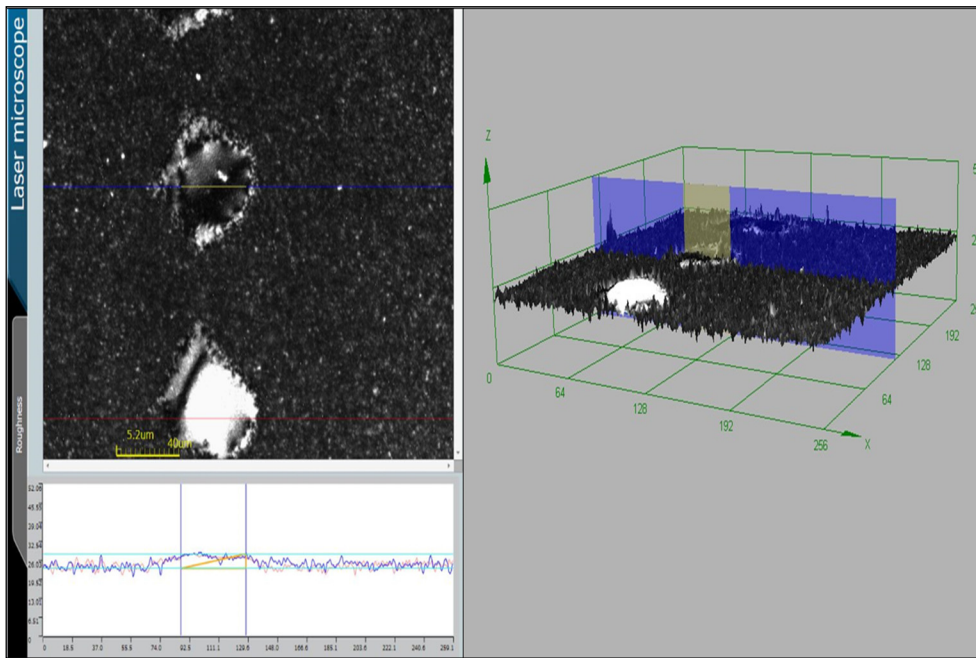


Figure 2.3 3D image by confocal microscope. Left: surface of the sheet and filled with  $20\ \mu\text{m}$  via. Right: 3D view of the same micro-via

As the consequences of this experimental investigation, the  $20\ \mu\text{m}$  micro-via is considered as a smallest realizable diameter size for manufacturing the micro-vias on this thin ceramic sheet and the  $40\ \mu\text{m}$  treated as a minimum center-to-center pitch of via that is feasible to fabricate in this range of micro-via.

This experimental investigation was verified by visual inspection through 3D microscope in order to verify the conductive paste filling inside the micro-via, alongside the verifying short connection between adjacent vias. Furthermore, we used an ohmmeter to check the electrical

connection the micro-vias. At the end, we wrote a design rules for the micro-via fabrication including the dimension of the via, convenient conductive paste, how to inject the conductive paste to the via, required vacuum below the ceramic sheets during filling the micro-via, etc.

## **2.2 Transmission Line Interconnects**

In general, transmission line is a conductor trace that conduct the signal of radio frequency from a source or emitter to the receiver or load. It consists of two conductors for the signal and its return path. LTCC technology can support all kind of transmission line, but we focused on the single ended and differential transmission line in the form of CPW (Co-Planar Waveguide).

### **2.2.1 Co-Planar Waveguide**

In this project, we use the CPW transmission line to connect the electrical and optical components of the package. CPW is a planar transmission line that consists of three conductors, which support signal transition on the same plane. It includes one single conducting track in the center, and two return path conductors located at the two sides of the conducting track with an equal gap. The CPWG (Co-Planar Waveguide with Ground) is a common variant of the CPW line, whereas a ground plane located on the other side of the dielectric substrate as a third return conductors. This ground plane is connected to two other return paths on top of the dielectric through the vias in order to reduce losses.

In printed circuit board technologies, CPW transmission lines are made on top of the dielectric substrate, in this case ceramic substrate. Furthermore, the CPW line is vertical symmetrical from the middle of central line. The characteristic impedance ( $Z_0$ ) of this transmission line is determined by the physical gap between the central line and two sides return path, along with the width of the conducting line, while the thickness of dielectric has no impact on the impedance of CPW. This advantage of CPW and CPWG line comparing to the microstrip and stripline facilitate the signal transitions from narrow transmission line to wider ones and vice versa without requiring any changes on the thickness of dielectric substrate. This possibility

will be useful to connect the devices with different pad sizes and pitch of pads in a package. In addition, CPW transmission line can be used as a surface printed line and buried line in multilayer structures. All the transmission lines used in this work were CPWG. Figure 2.4 shows a CPWG transmission line with its electric fields.

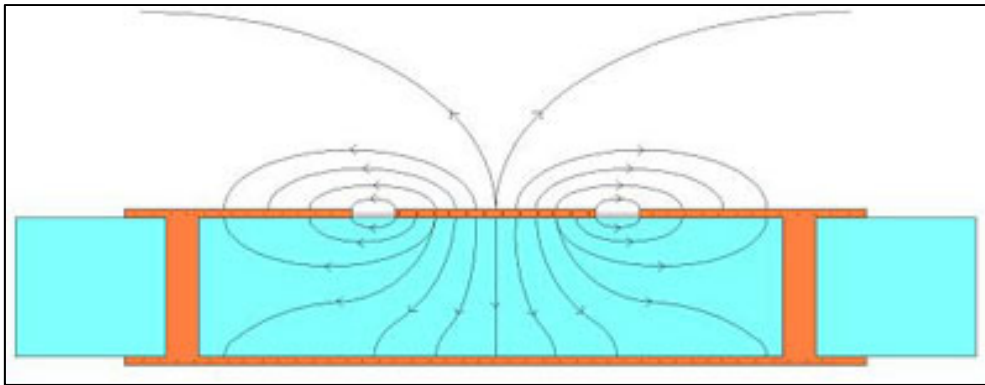


Figure 2.4 Cross-sectional view of a CPWG transmission line with electric field lines<sup>1</sup>

The CPW line have some advantage comparing to the other type of transmission lines such as high isolation between signal traces, because there is a ground line between them. In addition, the CPW transmission line has less loss comparing to the microstrip line specially at higher impedance, which make it a better choice for compact layout. Also, it has less dispersion than microstrip for the millimeter wave frequencies. Contrariwise, CPW transmission line has two more track than microstrip, so it takes more space and it has lower heat transfer possibility comparing to microstrip.

Based on the symmetrical characteristic of the CPW, it can support four mode of excitation. These modes are including coplanar mode, slot-line mode, parallel plate mode and microstrip mode. The coplanar mode of excitation in CPW is not purely TEM, it is more quasi-TEM because the conductors are in contact with two different material which is substrate and air. Also, the parallel plate mode excited while the top and bottom ground of CPW are connected through the vias by the distance inferior than  $\lambda_g/10$ .

<sup>1</sup> © Microwave Journal, March 14, 2011

## 2.2.2 Differential Coplanar Transmission Line

The differential transmission line is a structure of information transmitting consist of two symmetric conductive signal paths for the inverting and non-inverting signal in addition to a single ground path, whereas these two balanced signals flow in opposite-phase currents but with equal amplitude. Normally, the total impedance of differential transmission line is twice of the impedance of each line when they conduct individually. As the advantage of differential transmission lines, it can reduce emitted electromagnetic radiation, minimizes electronic crosstalk, less EMI (Electromagnetic Interference) and better noise protection. The higher resistance to the interference source facilitates using the differential signaling for longer distance between the transmitter and receiver of the system. Contrariwise, the disadvantage of this technique is that the differential signals are always accompanied by a some common-mode signal due to the unbalanced amplitude. Figure 2.5 shows a differential CPW transmission line in the form of GSGSG (G and S stands for Ground and signal respectively).

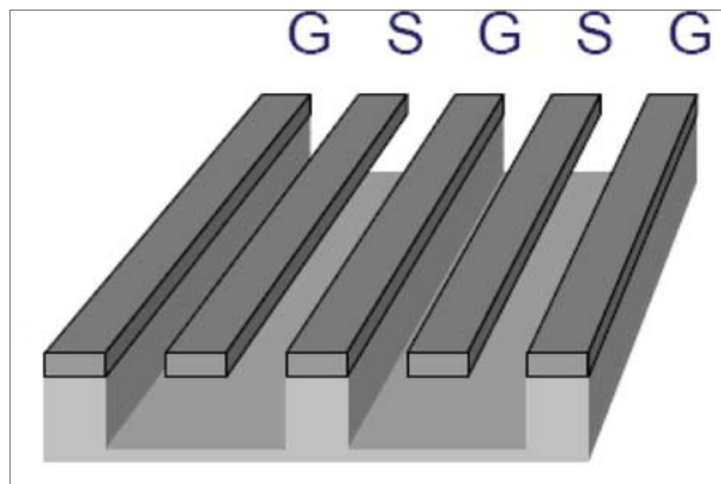


Figure 2.5 Differential coplanar transmission line in the form of GSGSG.  
Taken from Yikun Yu, (2010)

Due to the advantages of differential transmission line in high-speed digital circuits and high data rate transmitting systems, it is more commonly used in modern designs. Comparing to the single-ended transmission line, the differential transmission line is more immune to keep the difference voltage between the driver and receiver, and it is also protected against having the

common noise couples into the both terminations. Also, differential transmission line has the possibility to transit the signals twice faster than single-ended transmission line, while it consumes lower voltage.

Regarding the noise effect on differential transmission line, the noise affects equally on the positive and negative sides of the signals; in the other hand these two sides of differential transmission lines are separated by a physical gap into different paths. In addition, the differential signaling considered the potential difference between the two lines of differential transmission line and therefore the effect of noise on these two paths of system canceled each other. Consequently, the transmitting system with differential transmission line is more robust to the noise comparing to the single-ended transmission line.

In order to have a good differential transmission line, it should have uniform cross section, symmetry in the width and spacing of the lines. Moreover, the lines length must be equal to have the same time delay in both transmitting lines.

### **2.3 Ceramic Interposer Integration – Simulation**

In this part, the designed transmission lines for one channel and then for two channels in multi-layer structures are presented and showed in the figures 2.6 and figure 2.8, respectively. In each design, a single micro-via was used for every line to connect the top layer to the below layer. These simulated structures that are presented below has three layers consist of two 1-mil sheets and one 5-mil sheet below them. This structure with only three layers is so fragile, therefore, we added some extra sheets under these layers in order to support the structure physically without any electrical effect on the transmission lines behavior. In this work, the transmission lines designed with different pitch of lines from 125  $\mu\text{m}$  to 252  $\mu\text{m}$ . In these two designs, the minimum spacing between the lines was 60.5  $\mu\text{m}$  and 160  $\mu\text{m}$  respectively for the pitch of 125  $\mu\text{m}$  and 252  $\mu\text{m}$ . In order to achieve these small spacing, we used the ablation technique during post processing of fabrication process.



At the first simulation with the pitch of  $125\ \mu\text{m}$ , the single channel CPW transmission line designed to be a  $50\ \Omega$ , both at top layer and inner layer. This transmission line, figure 2.6, has the characteristic such as center conductor width of  $68\ \mu\text{m}$ , a ground lines of  $61\ \mu\text{m}$  and micro-via diameter of  $24\ \mu\text{m}$ .

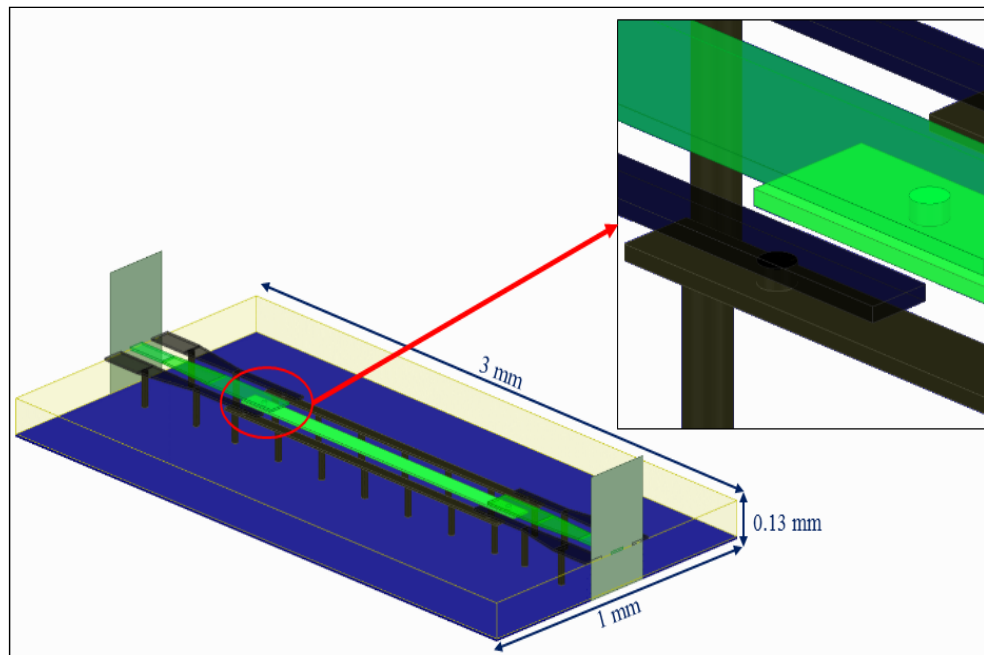


Figure 2.6 A transmission line and a zoom to the designed micro-via in this structure

The results of this simulation confirm that the insertion loss of the designed single transmission line is above  $-0.6\ \text{dB}$  and the return loss is inferior than  $-20\ \text{dB}$  for the entire simulated frequency band from 1 to 50 GHz. The S-parameter results of this one-channel  $50\ \Omega$  CPW transmission line presented in the figure 2.7.

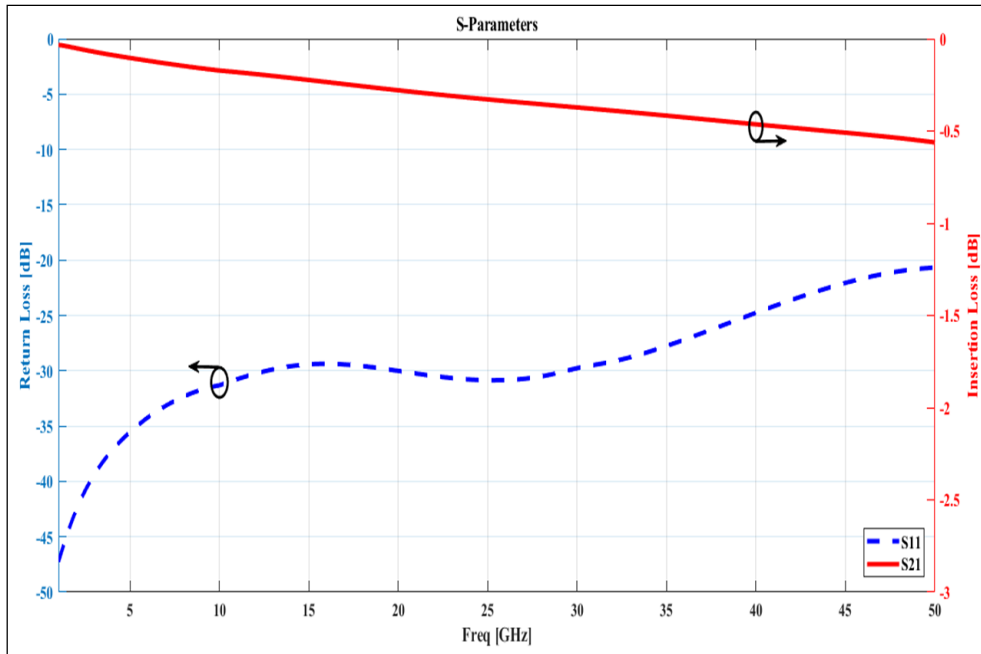


Figure 2.7 Simulation result of S-parameters of one-channel transmission line

In a similar project based on silicon substrate which was presented in state of the art, (Yan Yang, 2019), they have obtained the simulation results of  $> -0.35$  dB and  $< -15$  dB for insertion loss and return loss, respectively. Table 2.1 compare the CPW transmission line on silicon substrate presented on (Yan Yang, 2019) and the CPW transmission line on ceramic substrate presented in this work. This comparison confirms the similar results for the simulation of the CPW transmission lines on the silicon substrate and on the ceramic substrate.

Table 2.1 Comparing two CPW transmission line and vertical interposer in silicon and ceramic substrate

	<b>Yan Yang, 2019</b>	<b>This work</b>
<b>Substrate</b>	Silicon	Ceramic
<b>Via Diameter</b>	20 $\mu\text{m}$	24 $\mu\text{m}$
<b>Substrate Thickness</b>	100 $\mu\text{m}$	130 $\mu\text{m}$
<b>Center to Center Pitch</b>	100 $\mu\text{m}$	125 $\mu\text{m}$
<b>Insertion Loss</b>	> -0.35 dB	> -0.6 dB
<b>Return Loss</b>	< -15 dB	< -20 dB
<b>Frequency</b>	Up to 40 GHz	Up to 50 GHz

After that, we added another channel alongside the first conducting line with the common ground line between these two channels in order to have a transmission line in the form of GSGSG. This two-channel interconnection presented in figure 2.8, was designed to have two adjacent 50  $\Omega$  CPW lines with a pitch of 250  $\mu\text{m}$  between the centers conductors of two channels while the line width, the gap between the lines and micro-via diameter are the same as the one-channel transmission line designed.

Figure 2.9 shows the simulated results of near-end and far-end cross talk for this two-channels structure in blue and red, respectively. The presented figure demonstrates that the value of the two crosstalk was below than -30 dB for the entire frequency band from 1 to 50 GHz.

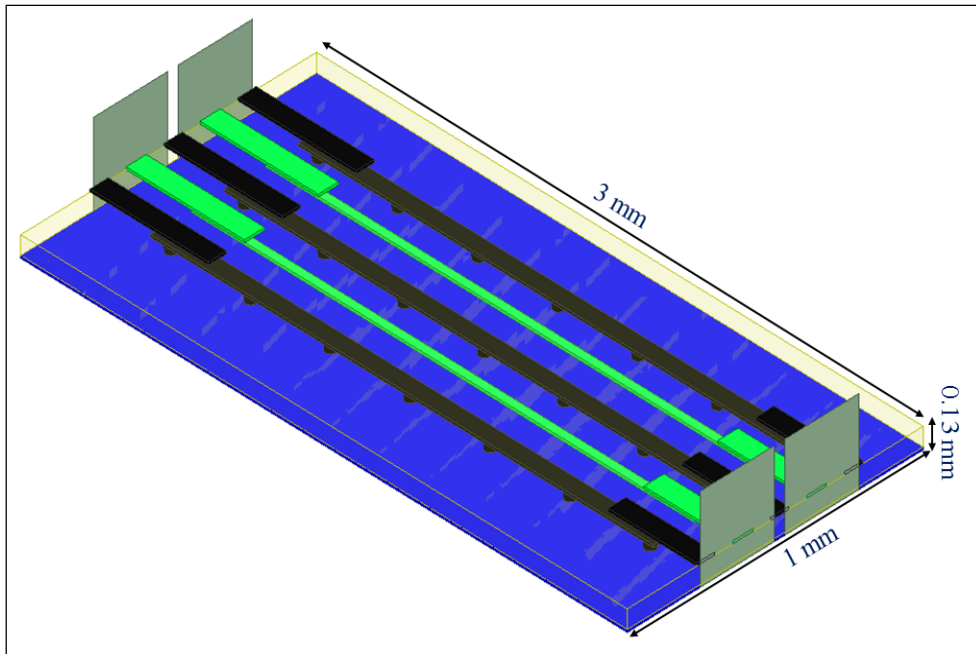


Figure 2.8 Schematic of designed differential transmission line in form of GSGSG with the pitch of 125  $\mu\text{m}$  between the lines

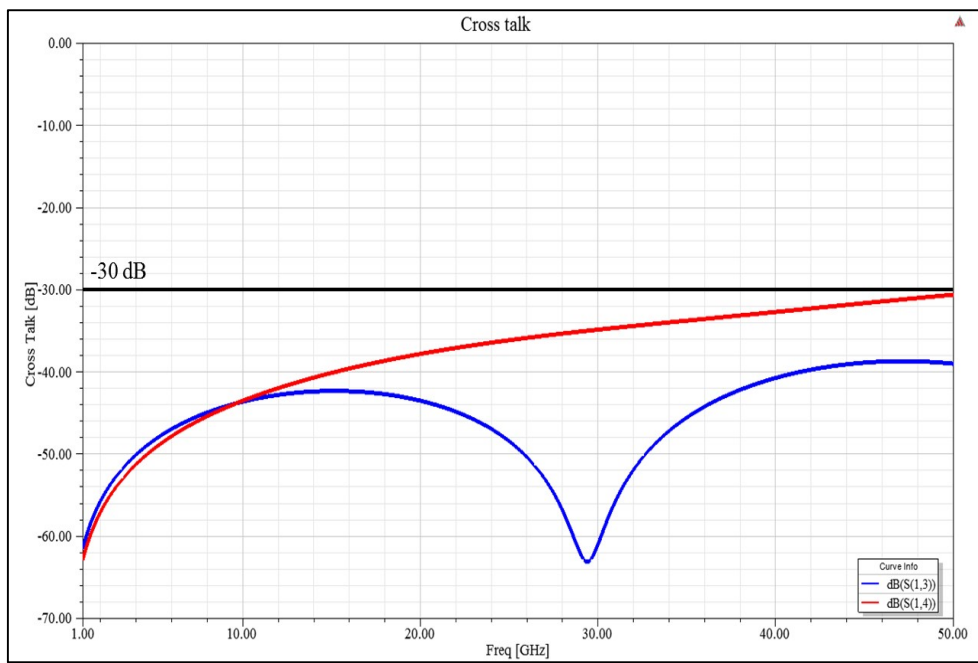


Figure 2.9 The near-end (blue) and far-end (red) Crosstalk simulation result of designed two-channel transmission line

One of the important applications of the proposed interposer structure is in a package design consist of different components by different pitch size of the output pads. Therefore, in order to connect these components with different pitch size, a transition with different width of lines and different pitches is required. This micro-via method will facilitates the fabrication of transmission lines with narrower width of line and smaller pitch of chip's I/O pads. Then, to achieve this transition, a two-channel transmission line with different pitch size of lines in both ends was designed. Figure 2.10 shows the design of such transition for two-channel going from a pitch of  $125\ \mu\text{m}$  to  $252\ \mu\text{m}$ . In this design, the dimension of the lines and spacing on the side with the shortest pitch is the same as one-channel designed transmission line with the same pitch of  $125\ \mu\text{m}$ . But for the pitch of  $252\ \mu\text{m}$ , the width of signal line, ground lines and the space between the lines are  $76\ \mu\text{m}$ ,  $108\ \mu\text{m}$  and  $160\ \mu\text{m}$ , respectively. This structure was simulated from 1 to 50 GHz and their result of insertion loss and return loss are demonstrated in figure 2.11, respectively in blue and red. Also, figure 2.12 present the near-field and far-field crosstalk of this designed transmission line in red and blue, respectively. Based on this result, the insertion loss of this structure is better than  $-1\ \text{dB}$ , the return loss result is inferior than  $-16\ \text{dB}$  and both crosstalk has the value inferior than  $-54\ \text{dB}$  in all the frequency band.

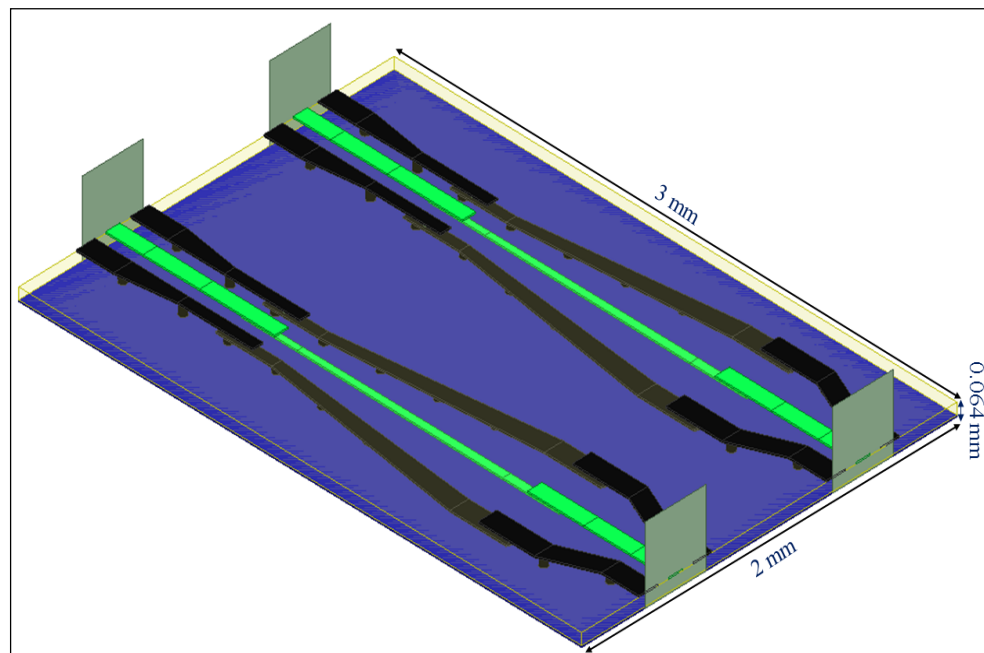


Figure 2.10 Schematic of designed transition for two channels

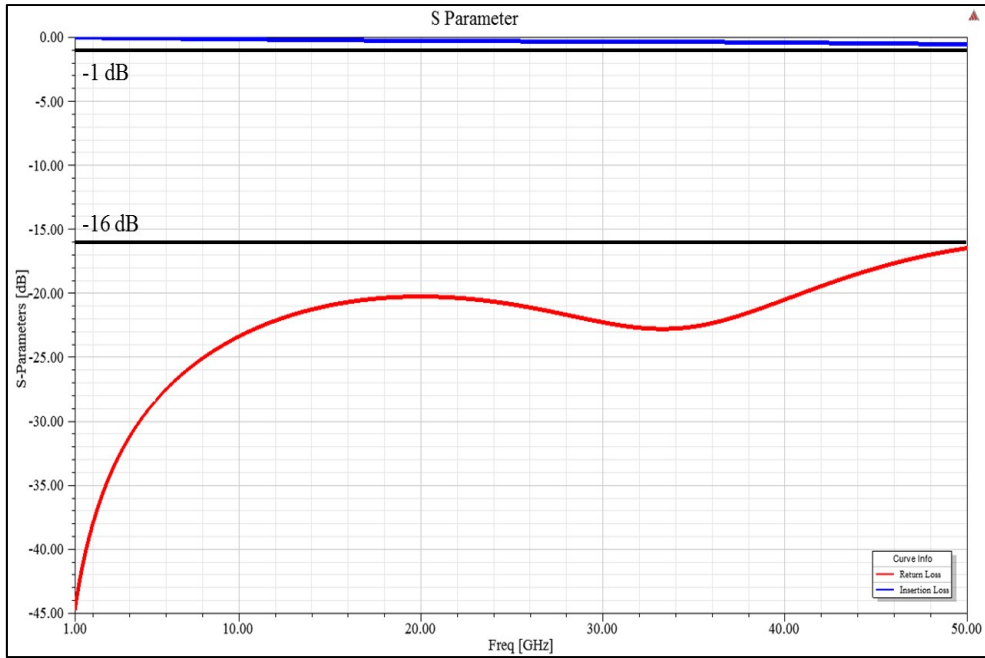


Figure 2.11 The insertion loss (blue) and the return loss (red) of simulated two-channel transmission line in Fig. 2.10

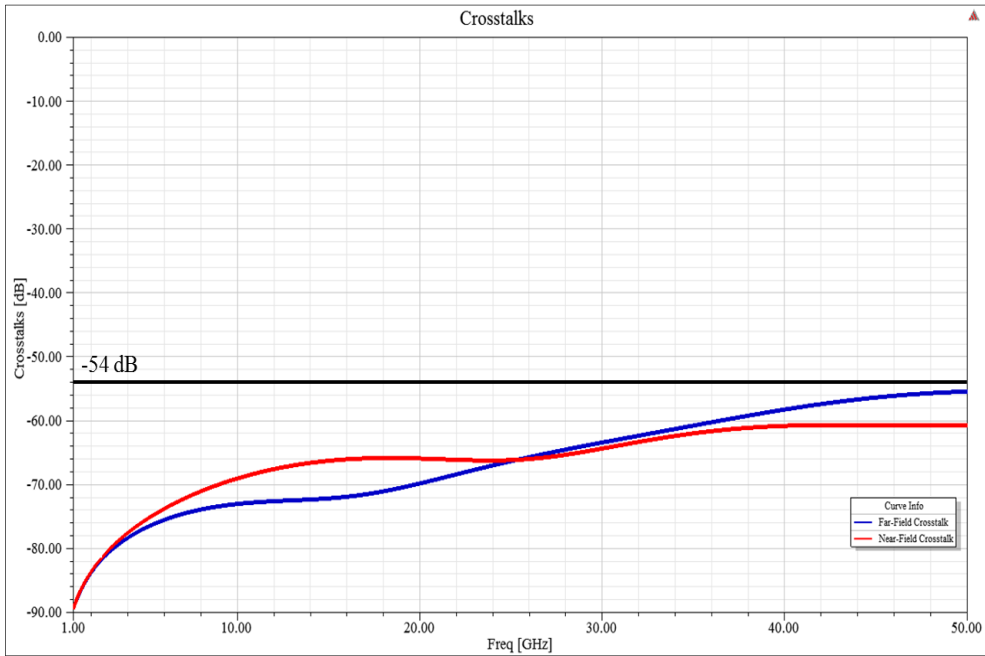


Figure 2.12 The Near-Field and Far-Field Crosstalk results of simulated transmission line in red and blue respectively

## 2.4 Ceramic Interposer Integration – Fabrication

The designed and simulated transmission lines in above was fabricated by using the proposed TCV processes on several Ferro A6M ceramic sheet with different thickness of 1-mil and 5-mil by means of our LTCC facilities at LACIME. Figure 2.13 shows a photograph of the fabricated structure with the various dimensions of pitch, where the dimension of D1 and D2 are 252  $\mu\text{m}$  and 125  $\mu\text{m}$ , respectively.

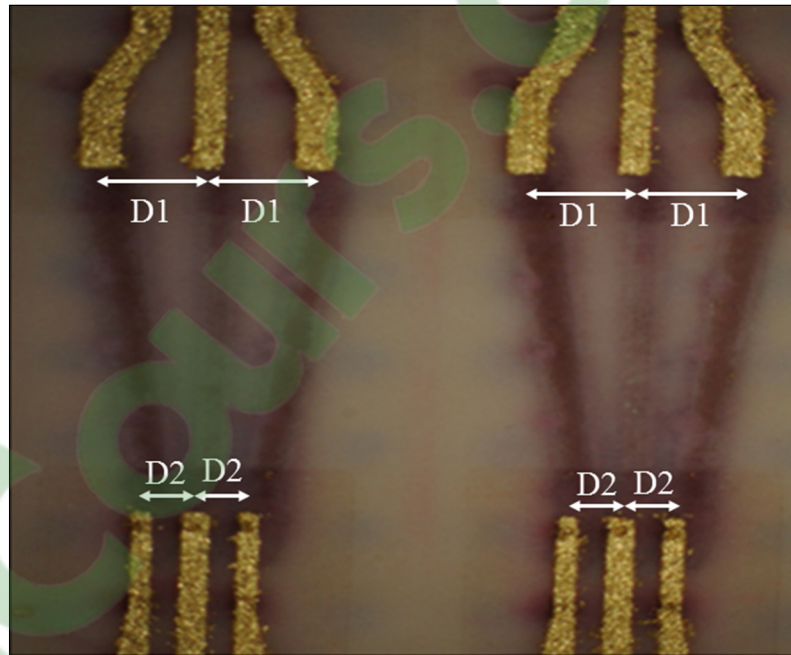


Figure 2.13 Fabrication of the transmission line using micro-via

In this multilayer structure, the thinnest ceramic sheet with the thickness of 1-mil was used for the top layer and its underlay layer; and the 5-mil ceramic sheet was used below of them. This three-layer simulated circuit has not enough thickness in order to be a stable and solid structure, so it would have high risk of cracking and curving during co-firing in the oven, which degrade the quality of the signals. Therefore, we added some extra layer below than the three-layer structure under the ground plan. Since these extra layers located under the ground plane without any electrical connection to the other part of circuit, they are ineffective on the functionality of the transmission line. The only role of these extra layers is physical support

for the main structure in order to prevent breaking during or after fabrication and avert the curve that could be create during co-firing in the oven. In the other hand, by using the thin LTCC layer for this transition with TCVs, the buried lines that are connected the two ends of surface line are visible in the figure 2.13.

The fabricated circuit was measured using a four-port PNA-X network analyzer N5247A, and a probe station, MPI-T67A-GSG100. Based on this measurement, the obtained results show that the value of insertion loss is better than -1.3 dB and the measured value of return loss is below than -13 dB. A comparison between the simulation and measurement results for the designed and fabricated structure is shown in figure 2.14 and table 2.2 summarized the value of this comparison. As a consequent, a good agreement is seen between simulation results and measurement results. In addition, the discrepancy at higher frequency may be attributed to an observed slight curving of fabricated circuit. Unfortunately, because of some technical issue during measurement, the measurement of crosstalk was impossible.

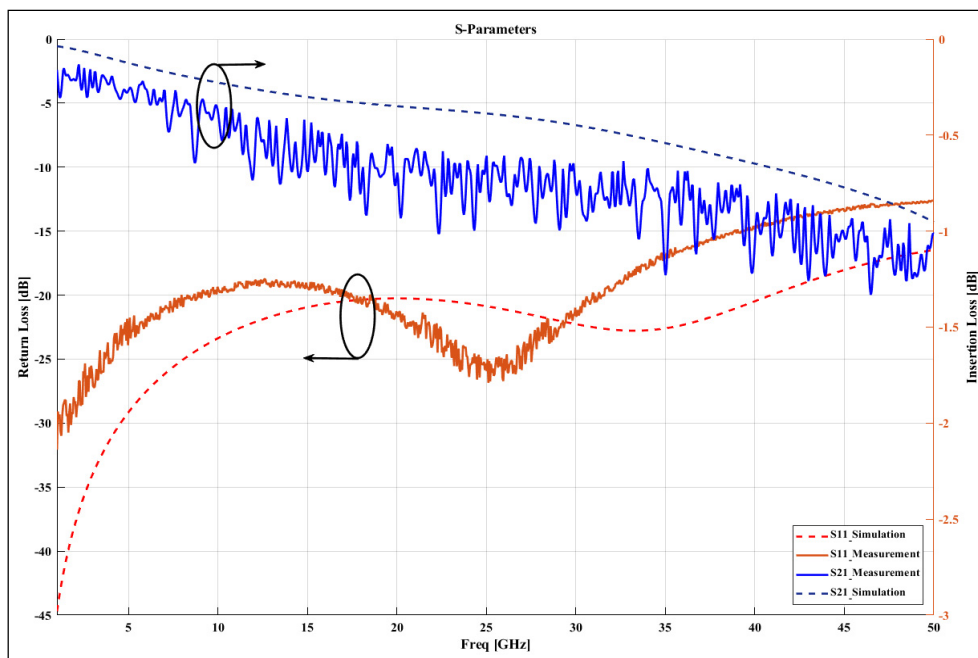


Figure 2.14 Comparing simulation results and measurement results



Table 2.2 Comparison between the simulation and measurement results from DC to 50 GHz

	<b>Simulation</b>	<b>Measurement</b>
<b>Insertion Loss</b>	> -1 dB	> -1.3 dB
<b>Return Loss</b>	< -16 dB	< -13 dB

## 2.5 Conclusion

In this chapter, a new process of micro-via fabrication housing by LTCC was proposed. We achieved to realize a micro-via with the diameter of 20  $\mu\text{m}$  and center-to-center pitch of 40  $\mu\text{m}$ . This technology of micro-via fabrication in ceramic substrate or TCVC offers a comparative substitute for TSV with less complexity and cost of fabrication in vertical interconnection of microwave and opto-electronic structures. This fine pitch and tiny diameter of via facilitate using various interconnections and transmission line suitable for high-speed connections in high-frequency packaging.

In addition, these micro-vias used for the short interconnection between different layers of multi-layer structure which makes the smaller interposer. The obtained simulation results of CPW transmission line on ceramic substrate is comparable to the results of CPW transmission line on silicon substrate. Then, we used this proposed method in order to design an advanced SiP opto-electronic package as an alternative for the conventional package that presented on chapter 2.

Based on this project, LTCC technology has less complexity of fabrication comparing to silicon-based technology in millimeter-wave frequencies and therefore it could be a good alternative for the photonic packaging in the area of millimeter-wave and light-wave.



## **CHAPTER 3**

### **OPTO-ELECTRONIC PACKAG DESIGN USING WIRE-BOND**

The previous chapters presented an overview of the LTCC technology, its characteristics, its fabrication process, design and fabrication of micro-via for vertical interposers on ceramic substrate. This chapter introduces a 3D integration and conventional packaging design at microwave and millimeter-wave frequency based on thin ceramic sheets of LTCC technology for the high-dense RF and opto-electronic package.

In this chapter, we propose the first iteration of SiP opto-electronic package design on millimeter-wave frequency. In this iteration the micro-vias were used in order to achieve the short pitch between the optical modulator and RF driver of package. Also, the wire-bonds were employed for the interconnections between the driver, modulator and substrate.

#### **3.1 Opto-electronic package on LTCC**

A typical opto-electronic package consists of the transmitter side and the receiver side with their essential optical elements such as laser, modulator and photodetector in addition to the electronic component like driver, transistor, filters, etc. is presented in figure 3.1.

Designing a prototype for opto-electronic SiP will be presented in this section. In this iteration, the wire bonding was used as a conventional fabrication method for the interconnection between the devices, the devices to the substrate, etc. This project of SiP design is in collaboration with two industrial and academic partners that designed and fabricated the driver and modulator of the package. Ciena Corporation as the industrial partner and McGill University as the academic partner, collaborated in designing the driver and modulator. In these prototypes, the main goal is to design a miniaturized SiP hosted by LTCC technology with the interconnection as short as possible. Also, developing the micro-via fabrication for vertical interposers used in different layers of package to decrease the length of interconnections. In

addition, the DC tracks, which are required for connecting the DC sources to the components were placed in inner layers to decrease the size of package and keep the surface as free as possible for surface mounting the active devices, the connections of RF probes and optical fiber to the driver and modulator, respectively.

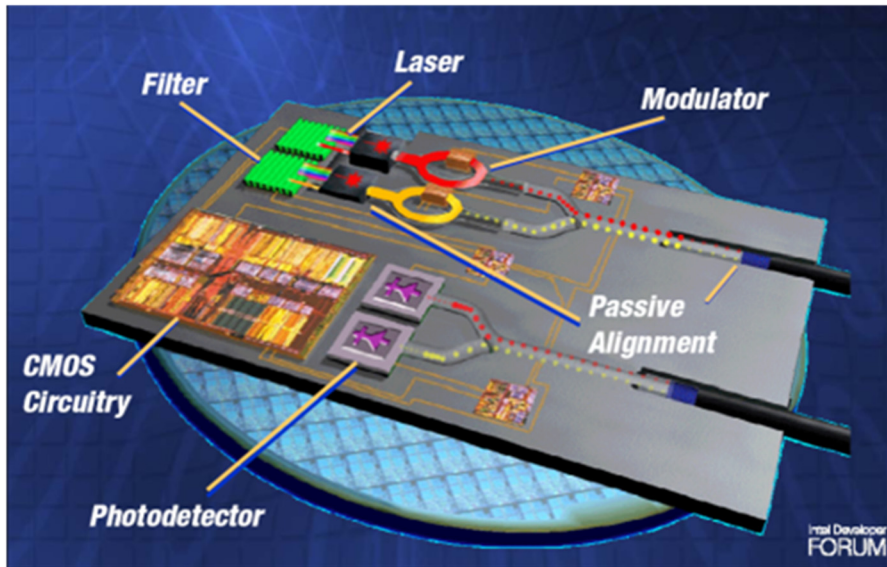


Figure 3.1 Opto-electronic Package<sup>1</sup>

The modulator and electronic driver operate at the frequency range between 38 – 48 GHz. The final package has the dimension size of 30x30 mm and the height of LTCC substrate is 1.52 mm. By considering the 6mm height of header for DC power suppliers, the whole package has the 7.52 mm of height. Figure 3.2 presents the 3D view of this designed opto-electronic package, while figure 3.3 offered a zoom view to the interconnections of the package through wire-bonds and micro-vias. Also, figure 3.4 shows the circuit schematic of the package.

<sup>1</sup> © Photo courtesy of Intel

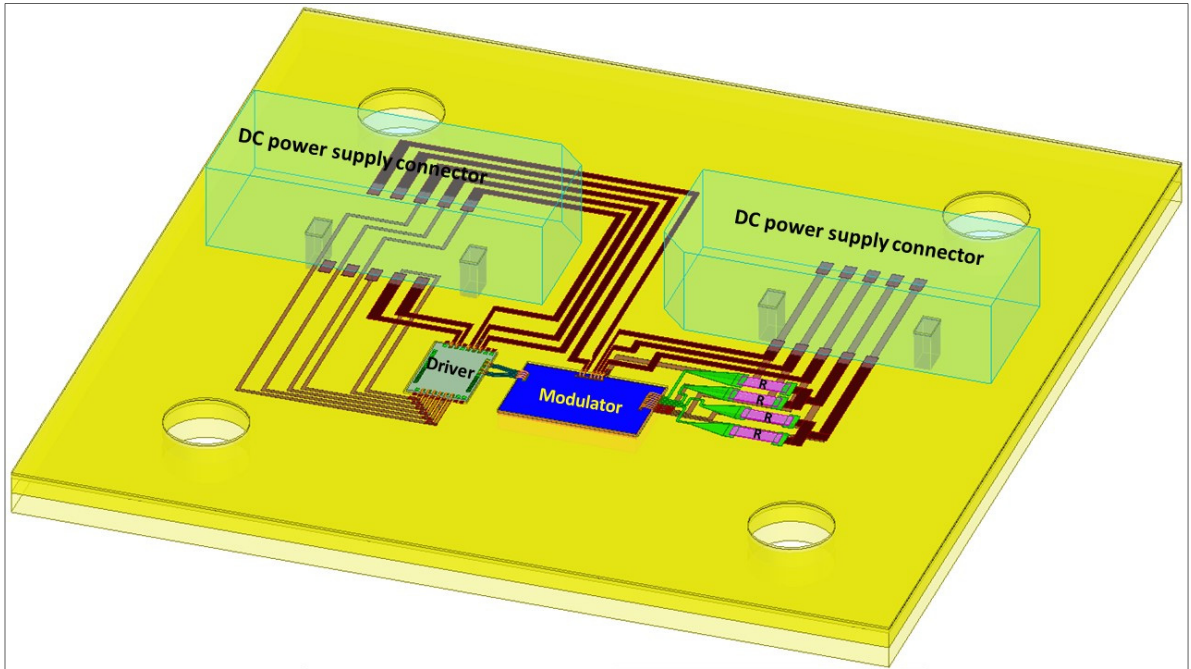


Figure 3.2 A trimetric view of the opto-electronic designed package

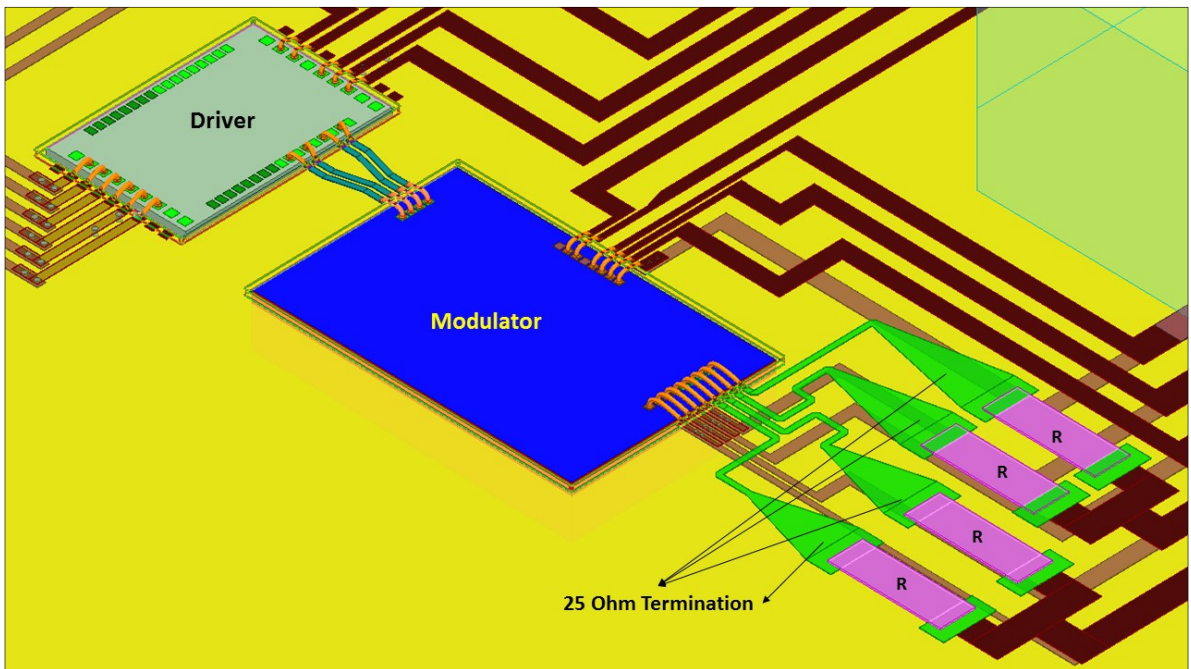


Figure 3.3 Close view to the interconnections of package through wire-bond and micro-via

One of the main issues of the package design is the length of interconnections through wire-bond that degrades the quality of the electrical signal. The initial length of needed wire-bond for connecting the modulator and driver to the substrate was approximately 1550  $\mu\text{m}$  and 800  $\mu\text{m}$ , respectively. To reduce the length of interconnections through wire-bond and decrease its negative effects on the package functionality, two open cavities were made to put the modulator and driver inside the LTCC substrate. This technique allows reaching the minimum height level difference between the surface of components and the surface of substrate. By this method, the length of wire-bond decreased up to 552  $\mu\text{m}$  in the longest wire-bond that was for modulator and 260  $\mu\text{m}$  for the shortest ones, which was for driver. These short lengths of wire-bonds can decrease the parasitic inductance and in general will improve the performance of the interconnections and consequently the quality of signal transmission.

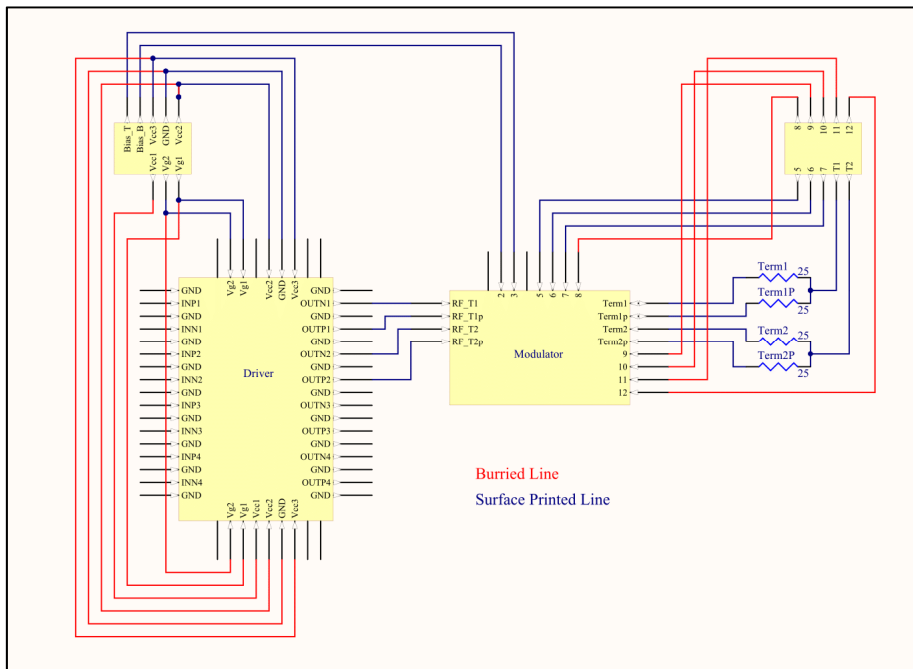


Figure 3.4 The circuit schematic of the opto-electronics package

Furthermore, the multilayer structure facilitates the integration of some transition and passive components in the inner layer in order to keep its surface as free as possible for mounting other devices (chips and active components) and/or other usage. In this case, we used the inner layer for the DC tracks to make the connections between components and DC power supplies

through CPW buried lines. In this iteration, the surface area is dedicated for the differential two-channel CPW transmission lines to carry the RF signals from driver to modulator, four resistors used for the termination of these two channels with the value of  $25 \Omega$  for each line of channels and two headers of socket for connecting the package to DC suppliers. In addition, there is free space on the surface for placing the fiber optics on top of the modulator with required high accuracy for alignment of fiber and modulator. Furthermore, there is free space for the direct connection between the RF probes and the input pads of driver. To make this direct connection, the surface of driver placed a few micrometers above than the LTCC structure.

In this work, a simulation has been done by using HFSS (High Frequency Structure Simulator) in order to obtain the scattering parameters. The S-parameters describe the electrical behavior and performance parameters of the system where  $S_{11}$  or return loss is the reflected voltage to the input port,  $S_{21}$  or insertion loss is the reverse voltage gain,  $S_{31}$  and  $S_{41}$  are near-end and far-end crosstalk respectively, which present the isolation level of these two ports regarding to the input port.

In this simulation, the S-parameters show the result of  $100 \Omega$  differential CPW line. Based on Ciena design regulation the differential transmission line should be  $100 \Omega$ . The importance of this transmission line is making a good impedance match between the I/O pads of driver and RF pads of modulator. Figure 3.5 presents the results of transmission lines such as insertion loss, return loss, near-field crosstalk and far-field crosstalk in red, blue, green and brown, respectively. Based on the results presented in this figure, the insertion loss is better than -1 dB, the return loss is below than -14 dB and the value of near-field and far-field crosstalk are inferior than -23 dB.

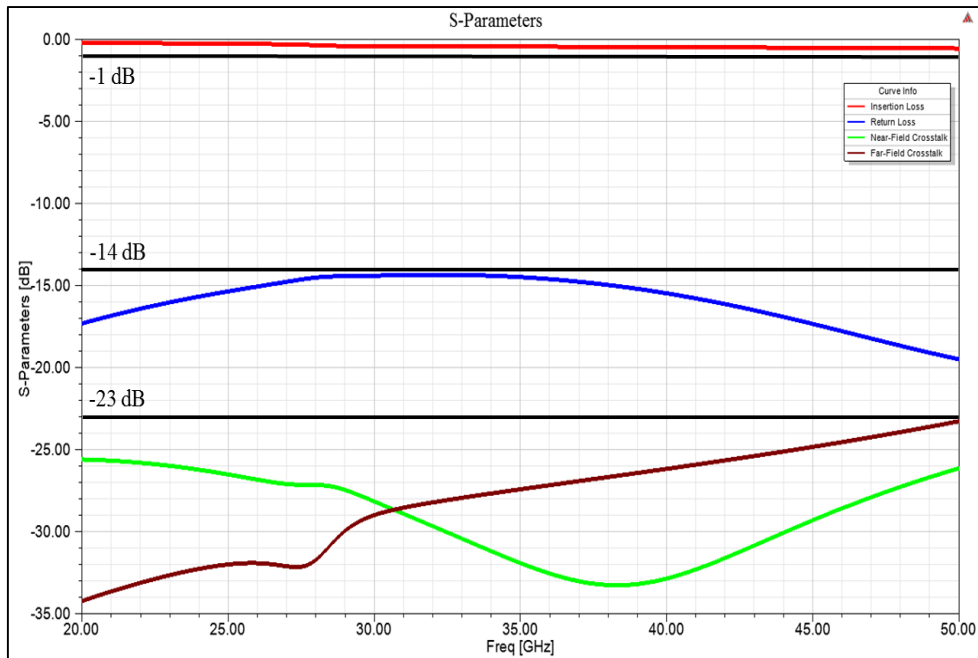


Figure 3.5 The S-parameter results of the CPW transmission line used in the package

### 3.2 Fabrication of Opto-electronic Package

This multi-layer designed package consists of eleven layers, which is two 2-mil and nine 10-mil A6M ceramic sheets. The RE87-011 thick film resistor paste was used for making the 25  $\Omega$  termination of every line of channels. Ferro Corporation provides this buried resistor and it is specifically designed to use in the LTCC structures based on Ferro A6M ceramic sheet. Based on its datasheet, the resistivity of this paste is 10  $\Omega/\text{sq} \pm 30\%$  and its operational frequency is up to 110 GHz<sup>1</sup>. Figure 3.6 shows the fabricated package using conventional LTCC manufacturing method.

<sup>1</sup> Technical Data sheet of RE87 Resistor Series, Ferro Corporation.



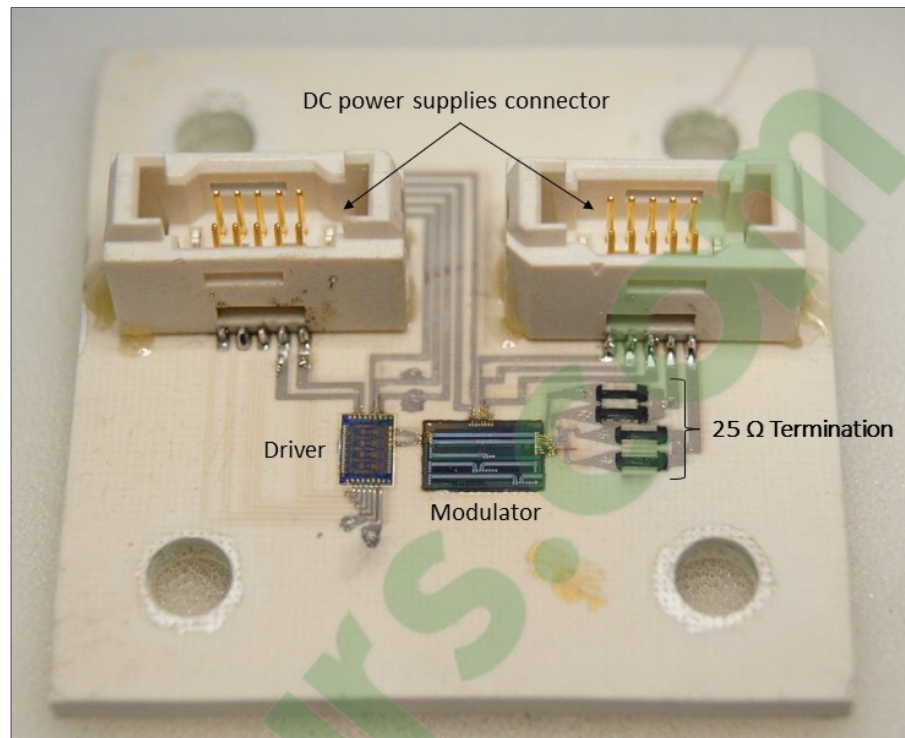


Figure 3.6 Fabricated package using the micro-via and small line-to-line pitch

The advantage of this designed package by using micro-via with small line-to-line pitch is that the DC and RF tracks printed on LTCC substrate could follow the  $125\ \mu\text{m}$  center-to-center pitch of pads on modulator and driver; whereas with regular via diameter and pitch of standard LTCC design rules these tracks should have more distance between them which increase the length of required wire-bond to connect the modulator and driver to substrate. This issues of longer wire-bond with unequal length would have the effect on the equality of the lines of channels, therefore this negative effect would make the phase difference between the two lines of a channels. Figure 2.7 demonstrates an X-ray view capturing by 3D microscope inside the fabricated prototype of ceramic interposer where the micro-vias with the pitch of  $125\ \mu\text{m}$  (P) used to make this vertical electrical interconnection between different layers of package.

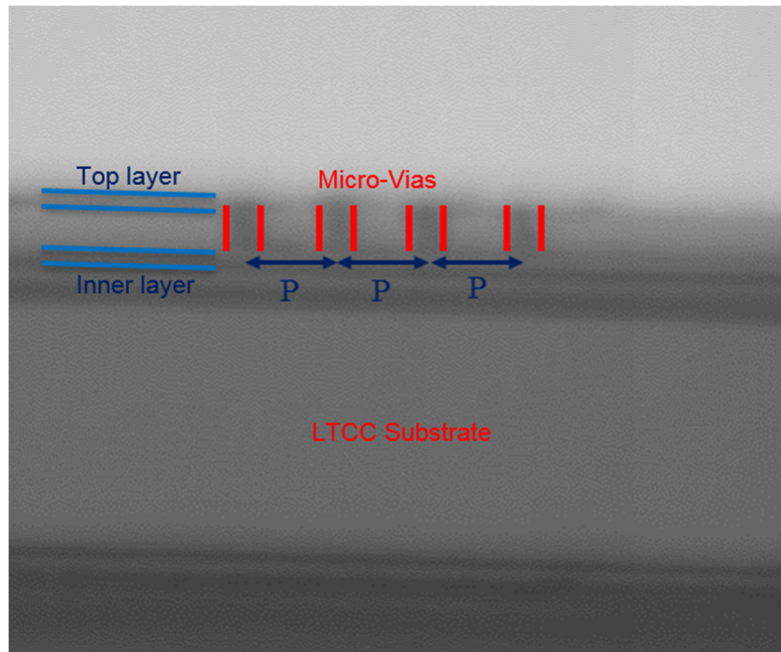


Figure 3.7 X-ray image of fabricated micro-via inside the Opto-electronic SiP

The biggest challenge of this fabrication was wire bonding in the narrow line and printing the resistive pastes with the value as close as possible to  $25 \Omega$ . The final value of impedances after firing the structure was around  $32 \Omega$ . Therefore, they required several trims such as increasing the thickness with re-printing the resistive paste and ablation the edges of resistive paste in order to reduce their value and achieved  $25 \pm 1 \Omega$ . This accuracy of resistance value comes from the design specification provided by Ciena.

The fabricated package was sent to McGill University to use their facility of optical laboratory for testing the whole package. We asked several times for the results but unfortunately, we never received any test results of the package from them. The reason is still unknown for us.

### 3.3 Conclusion

The multilayer package housing by LTCC is a cost-effective packaging technology that offers a viable alternative to silicon interposers for the integration of multi-chip high-speed electronic

and opto-electronic systems in a single package with high reliability and very good performance to maintain signal integrity.

The low tolerance of this technology normally offers a  $\pm 5 \mu\text{m}$  accuracy of device alignment, which is a critical issue for the photonic integration. The Alignment of between the optical fiber and optical receiver or transmitter is very important in order to transmit correctly the light beam and prevent losing the data through this transmission among optical devices. In addition, the possibility of integrating passive components and creating different open and close cavities inside the structures, besides the low transmission loss and low dielectric loss of ceramics substrate are the other benefits of LTCC technology to be used in millimeter wave frequencies and opto-electronic package.



## CHAPTER 4

### OPTO-ELECTRONIC PACKAGE USING FLIP CHIP

In this chapter, a second prototype for opto-electronic SiP is presented. In this prototype, we removed the wire bonding connection and replaced it with the new method of micro-via, vertical ceramic interposer presented in chapter two and the flip chip method.

#### 4.1 Package Design with Flip-Chip Method

In the conventional package presented in chapter 2, the most important part that degrades the reliability and performance of the package was the interconnections between the components and the substrate through the wire-bonds. As mentioned before, the wire-bond increases noise coupling and decreased the quality of electrical signals in high frequencies. Therefore, in order to overcome this issue of conventional package and improve its performances in optical frequency, the flip-chip method with micro-via vertical interposer was used. In flip-chip technique, the devices are connected to the substrate through the solder ball, which has better functionality than wire-bond. The Ball-Grid Array (BGA) also increases the bandwidth comparing to the wire-bond connections, especially by using the material such as gold and copper. In addition, the vertical interposer below the solder balls was used for the interconnection between two components and DC sockets through the inner layer and buried transmission lines.

#### 4.2 SiP Prototype Design and Fabrication

This prototype is based on the first iteration of package design which was presented in the chapter 3. The difference of second design comparing to the first ones is that, in this package, the modulator and driver are placed inside the structure through two cavities created on the backside of package. They connected to transmission lines printed on the ceramic substrate by using solder balls. In addition, there are two open cavities on the top side of package where the

right cavity considered for the optical fiber that required direct connection with high accuracy to the modulator from top side of it. The left cavity is intended to be the place for the RF probes in order to connect it directly to the RF pads of driver. The DC connections of this prototype is the same as previous one on the first iteration with little modification in order to use solder ball instead of wire bonding. Furthermore, the transmission lines between modulator and driver are printed on the back side of an inner layer and buried in the structure. The figure 4.1 presents this second prototype and figure 4.2 shows a closer view to the designed interconnections in this package.

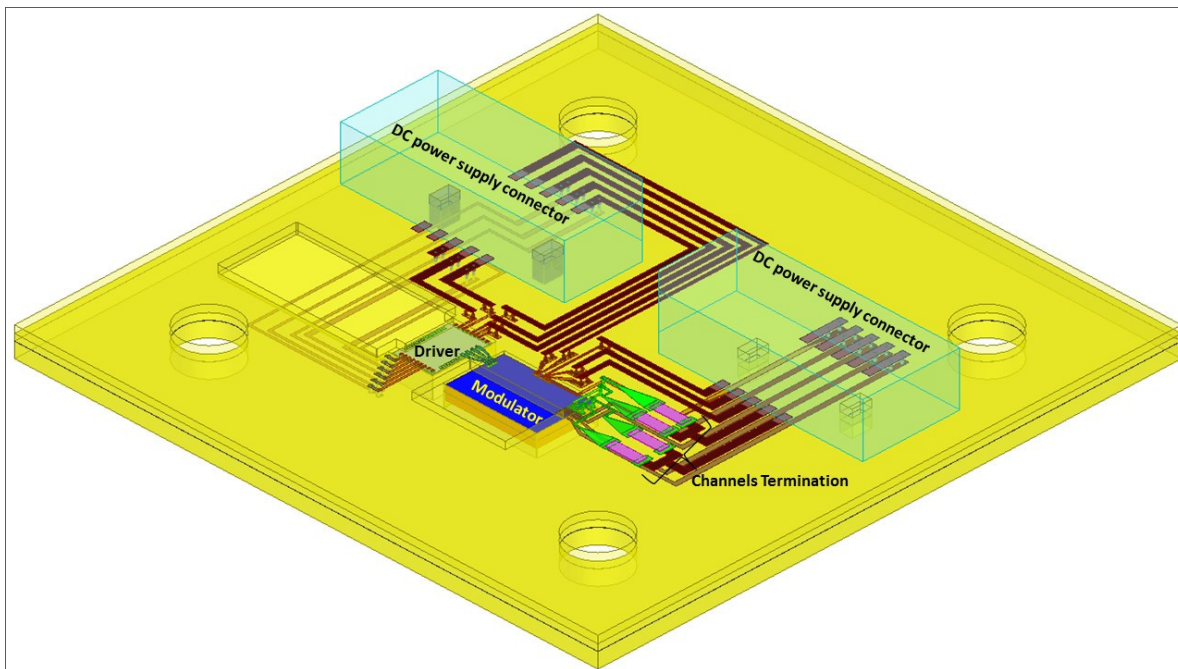


Figure 4.1 An isometric view of the advanced opto-electronic designed package

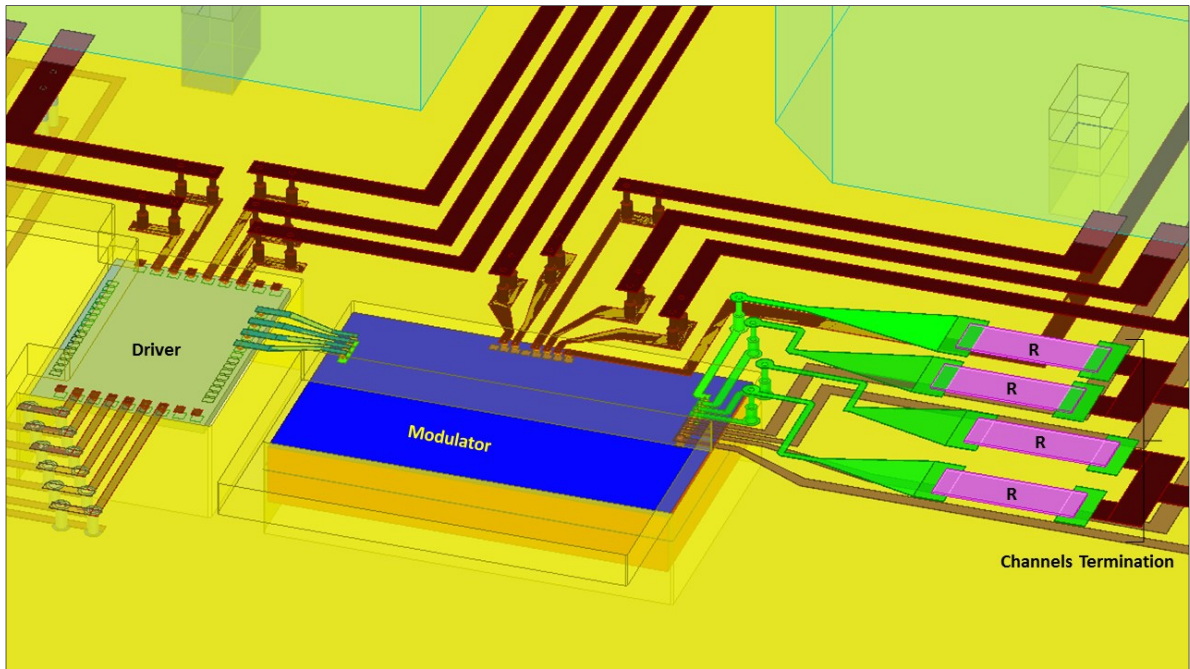


Figure 4.2 A close view to the designed interconnection through micro-via

The advantage of this designed micro-via with small line-to-line pitch comparing to the regular pitch in LTCC technology is that the DC and RF tracks printed on LTCC substrate could follow the 125  $\mu\text{m}$  pitch of DC pads and RF pads on modulator and driver; whereas with regular via diameter and pitch of standard LTCC these components could not mounted as a flip-chip device on the ceramic substrate. This technique also overcome the issues of several wire bonding with unequal length that make the negative effect on the performance of the RF signals.

Figure 4.3 shows the simulation results of the transmission line between the driver and modulator in this iteration. Based on this result, the value of insertion loss is above than -0.6 dB, the return loss was inferior than -19 dB and the near-field and far-field crosstalk were below than -30 dB. Comparing to the obtained results of previous prototype, in this iteration of designed SiP we achieved to have the better functionality of the transmission line.



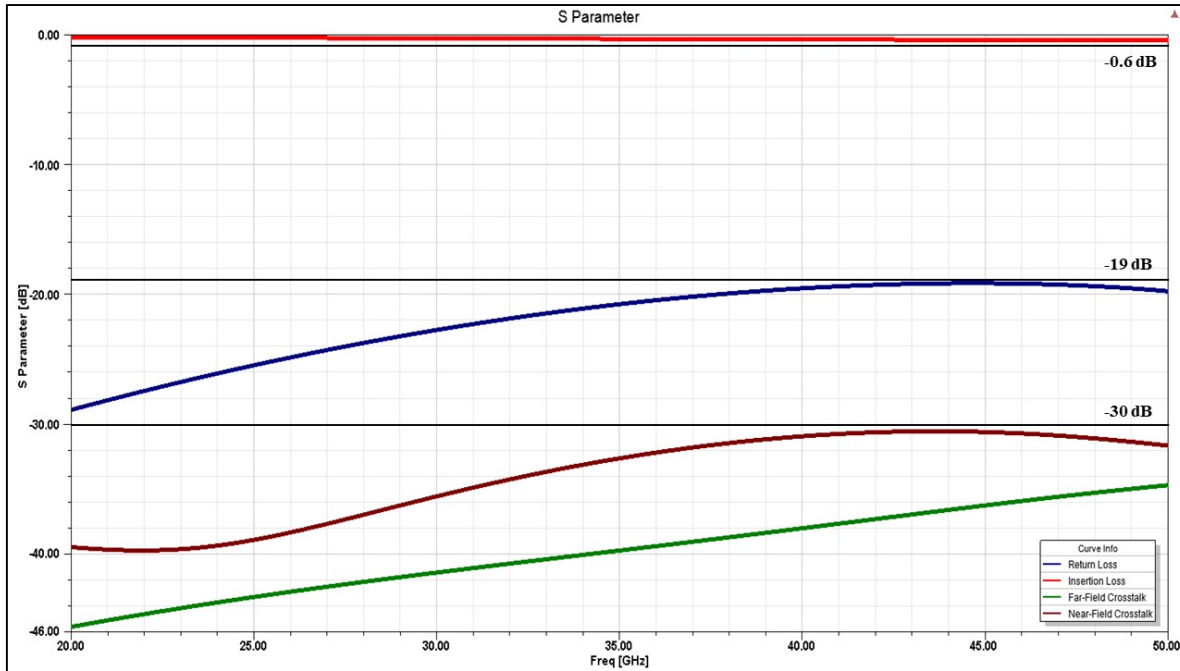


Figure 4.3 The S-parameter results of the CPW transmission line used in 2<sup>nd</sup> iteration

For the fabrication of this prototype, twelve ceramic sheets of Ferro A6M were employed. The other components and material that are used in the fabrication of this prototype are the same as the fabrication of first iteration. The firing process of this structure was very challenging, three prepared samples were broken during firing but the 4<sup>th</sup> ones was successfully fired. In the 1<sup>st</sup> try, we used the standard profile of co-firing for the ceramic sheets of A6M for the structure with cavity. We put the structure in the oven, without any lid on top of the structure. After firing, the circuit have broken in two area; between two cavities and at the bottom of left cavity till the screw hole. Also, the circuit was curvy. For the 2<sup>nd</sup> try, we used the same profile as the 1<sup>st</sup> try by putting a lid on top of the structure. The fired circuit had the same two cracks as the first ones, but the it has less curve comparing to the previous try. During the 3<sup>rd</sup> try, we placed the structure in an uncooked LTCC mold. The result of this try was a circuit with a negligible curve and a crack between two cavities. Figure 4.4 shows the circuit and its mold after firing (left) and the fired circuit which has a crack between two cavities (right).



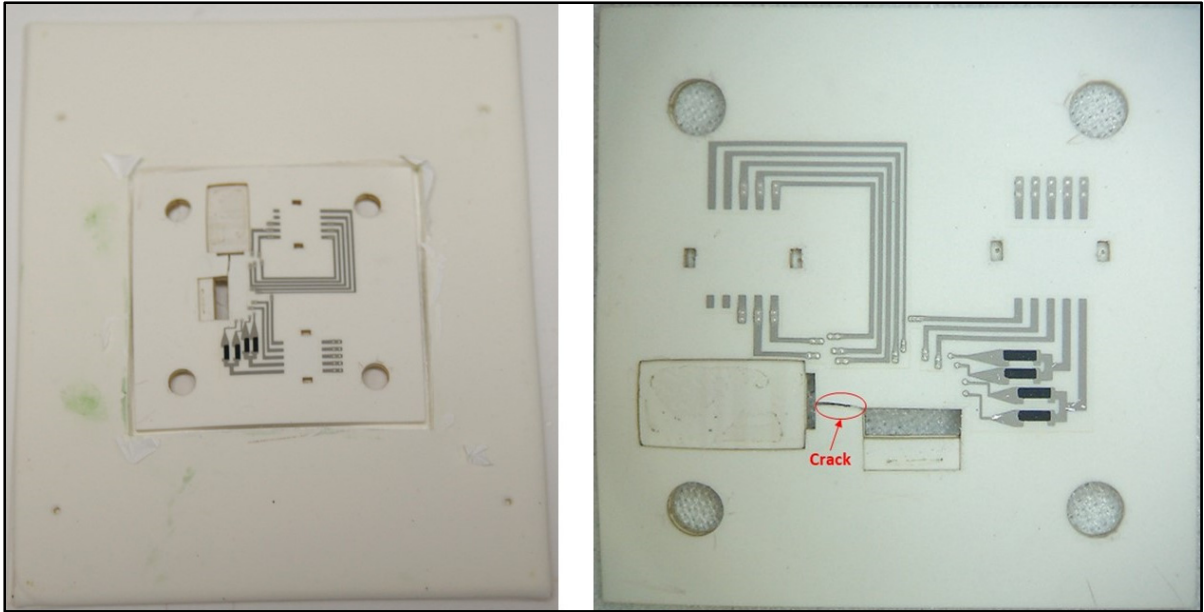


Figure 4.4 Left: The 3<sup>rd</sup> sample of designed package and its mold after firing. Right: A close view to the same fabricated package and the crack between cavities.

At the 4<sup>th</sup> try, we achieved to fire the last sample successfully without cracks or curve. For this firing, we follow the suggestion profile of firing by Ferro which was inspired by 9K7 ceramic sheets profile with cover. In this profile of firing, the temperature increases 1 °C per minute ramp to 450 °C with two hours hold at this temperature. Then, it increases 7 °C per minute ramp to 850 °C with a 15 minutes hold at this temperature. The firing process finished by a residual cool down of approximately 3 °C per minutes. The total profile was approximately 15 hours which is 3 hours more than standard profile for A6M ceramic sheets.

The last firing was done after submitting this thesis for defence. Unfortunately, we can not find a good place for mounting the driver and modulator on the package by flip-chip technic before the thesis defence and covid-19 pandemic. In addition, because of this situation we do not have opportunity to take a photo of this fired package.

### **4.3 Conclusion**

Based on this new prototype, the length of interconnections between components and substrate was decreased by using solder ball and micro-vias instead of wire-bond. Due to the simulation results, the solder ball will increase the performance of this package comparing to the previous prototype. The value of S-parameters such as insertion loss, return loss and crosstalk in this iteration was 0.4 dB, 5 dB and 7 dB respectively better than 1<sup>st</sup> iteration. In addition, there is more space on the surface of the package for other applications. However, the fabrication process of this prototype is more challenging and more difficult than expected, because we must do out-source for mounting the driver and modulator.

## CONCLUSION

A new process for micro-via fabrication and filling in LTCC technology (TCVs) was proposed and demonstrated that 20  $\mu\text{m}$  diameter with 40  $\mu\text{m}$  pitch vias are realizable. This small diameter of micro-via and fine pitch of micro-vias enable us to propose various interconnections and transitions suitable for high-speed interconnections and for high-density packaging in System in Package (SiP) and high frequency electronic chips. In addition to the standalone interposers, the developed fabrication process has been used to design a high-density package for the integration of opto-electronic SiP and electronic chips with operational bandwidth up to 48 GHz. This novel cost-effective packaging technology offers a viable alternative to silicon interposers for the integration of multi-chip high-speed electronic systems in a single package with high reliability and very good performance to maintain signal integrity.

Based on the obtained results, LTCC technology with less fabrication complexity could be considered as a good technology for the integration of passive components, multi-layer package for RF, opto-electronic application, etc. Moreover, practical TCV for vertical transitions have been demonstrated to be feasible and offer a viable alternative to TSV with better performance at millimeter wave and optical frequency, with less complication and lower-cost fabrication process. In this work, we achieved to fabricate and used a micro-via in a CPW transmission line with the diameter of 24  $\mu\text{m}$  and the pitch of 125  $\mu\text{m}$ ; while the regular via diameter and pitch in LTCC technology is 50  $\mu\text{m}$  and 200  $\mu\text{m}$ , respectively.

In addition, the main results of this work regarding the micro-via fabrication on a thin ceramic sheet were the subject of a publication on IEEE 20<sup>th</sup> EPTC international conference which held on Singapore on December 2018. The title of this paper was: "Ceramic Interposer for Ultra-High Density Packaging and 3D Circuit Integration". Also, during my master project I was participated in writing another paper which is in under review in order to published on the journal of Transactions on Components, Packaging and Manufacturing Technology. Its title is:

“A Fast Technique for Realization of Lumped-Element Values Into 3D Physical Layout on LTCC”.

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