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LIST OF ABREVIATIONS

PAE	Power add efficiency
HEMT	High electron mobility transistor
CMOS	Complementary metal–oxide–semiconductor
RF	Radio frequency
LNA	Low noise amplifier
DC	Direct current
PA	Power amplifier
TWTA	Travelling wave tube amplifier
GaN	Gallium nitride
SiC	Silicon carbide
GaAs	Gallium arsenide
WiMAX	Worldwide Interoperability for Microwave Access
Pout	Output power
Pin	Input power
Pdc	Direct current power
AM	Amplitude modulation
PM	Phase modulation
HD	Harmonic distortion
CCA	Current conduction angle
ZVS	Zero voltage switching
DB	Power ratio in decibels
ADS	Advanced design system
VGS	Voltage between gate and source
VDS	Voltage between drain and source
LTCC	Low temperature co-fired ceramic
HFSS	High frequency structure simulator
AuSn	Gold Tin
CuDi	Copper diamond

NA	Network analyzer
IMD	Intermodulation Distortion
PEP	Peak Envelope Power
ACPR	Adjacent Channel Power Rejection
QPSK	Quadrature phase shift keying

INTRODUCTION

Today's globally-interrelated telecommunication technology is at the forefront of optimization research. The arrival of smart phones and related mobile equipment on the consumer scene marked a major turning point in the evolution of advanced technology; it also radically altered how users engage with their devices. Instead of having to use multiple pieces of equipment for activities such as texting, internet browsing, and online gaming, consumers now had the means, through their Internet-connected phones, to do everything they wanted to do on just one mobile device.

There is a catch, though – along with a growing need for faster and faster Internet speeds, there was also an equally urgent need for longer battery life. The exponential increases in data transfer rates meant that exponential amounts of energy were being used to power cellular network infrastructure, and batteries were reflecting the usage by draining at faster rates. The focal point of this present research is boosting the efficacy of power-added efficiency (PAE). The entrance of digital circuits onto the telecommunications stage, along with low-power CMOS, meant that digital signals could be delivered faster and with less energy use. Unfortunately, the front-end RF equipment in the devices (e.g., low-noise amplifiers [LNA] as well as power amplifiers) is known as an energy hog that consumes immense quantities of available power in the system.

Given this situation and considering the increasing consumer demand for more effective energy use, taming the PAE of power amplifiers is offered as a solution. Furthermore, Class F and inverse Class F PAs show the most promise in our quest due to their ability to provide extreme levels of energy while at the same time providing outstanding power efficiency (i.e., higher than 80%), which is accomplished by managing the amplifiers' harmonic content.

Microwave power amplifiers (PAs) change DC power from lower/moderate to high microwave power through the generation of current waveforms, large voltages and high frequency. In fact, microwave PAs serve as essential components in high-frequency systems such as radars,(Skolnik,2002) and wireless communications devices e.g., microwave heaters

and cellular phones,(Osepchuk,2002). Since its introduction in the early 20th century, microwave power first used magnetrons, followed by travelling wave tube amplifiers (TWTAs) and klystrons, which function by moving electrons within a low-pressure area, (Pozar,1998). The adoption of silicon bipolar 3-terminal transistors mid-century positioned solid-state equipment at the forefront of amplifier development mainly because it was easy to implement and was also more reliable. Further advances led to the adoption of solid state in semiconductor materials such as GaN, SiC, InP and GaAs for high frequency signal spectrum areas, (Frederick et al,2003), while cost-efficiency, sizing and ease of use of the technology also gradually improved across the semiconductor industry.

Today, high-power kW- to MW-range amplifiers still mainly use TWTAs, but they are slowly being replaced by semiconductors that provide high power density. So, for instance, while GaAs equipment (in use over the past 30 years) provides around 1 W/mm at 10 GHz, GaN transistors provide >5 W/mm power density at 10 GHz. The insignificant increase in power density offered by semiconductor equipment points to the possibility of solid-state transistors likely replacing TWTAs for applications in the high microwave power sector.

Compared to traditional Si devices or GsAs, Gan-field effect transistors (FETs) have achieved a ten-fold increase in output power density in high-power amplifiers for use in surveillance radar and wireless base stations (Wu et al., 2001). However, higher power density comes at the cost of increased channel temperatures, which can then lead to a decrease in the long-term reliability of FETs. To deal with this situation, appropriate thermal resistance in the amplifier needs to be developed via the application of a heat sink. Such a heat sink must also take into account both the mechanical and the thermal needs of the equipment.

The most suitable conductive material for decreasing thermal resistance in high-power amplifiers is Cu, but Cu can also raise the thermal stress levels. This is due to Cu having a relatively large Young's modulus and also because of the significant differences between the semiconductor material's and Cu's thermal expansion coefficient. In order to align Cu's

linear thermal expansion coefficient with the semiconductor's coefficient, alloy materials that are Cu-based (e.g., CuMo, CuW, CuDi) can be utilized. However, such alloys might also introduce varying degrees of loss in thermal conductivity (Radivojevic et al., 2005).

Numerous tools for thermal simulation currently exist. For instance, ANSYS and Flotherm can be applied in thermal analysis at the system level (Canonsburg, 2014), while APDT and TCAD are commonly applied in thermal analysis at the transistor level. In using APDT or TCAD, detailed information on the transistor must be provided by the user (Sohrmann et al., 2013). This process can be extremely time- and resource-consuming. So, as a means to gauge the thermal properties, including thermal simulation, in PAs in a relatively straight-forward way, a novel approach is suggested. In this approach, we use ANSYS, which is a thermal analysis tool that is part of CFD's ANASYS suite (Canonsburg, 2014) and features a highly adaptable graphic user interface (GUI), along with an extensive collection of models. From this collection, an appropriate PA model for analyzing thermal reliability can be sourced and used for our purposes.

Thesis Problems

Two of the most critical elements in power amplifiers which are used for modern applications are good linearity and high efficiency. However, these two elements also have conflicting needs that require power amplifier design approaches which are unique to them. Two other important needs are to attain a high level of output power, and to maintain the preferred high efficiency across a broad operational range. Other issues challenging power amplifiers are problems related to heat dissipation, as the energy becomes mostly unwanted heat if the power remains unconverted into a useable signal. Low-efficiency PAs demonstrate the highest amounts of heat dissipation, and this factor has become a major problem in some designs.

Thesis objectives

The main objective in this thesis study is to develop a high-efficiency class F power amplifier which is operational at 5.7 GHz. For our purposes, a 'high-efficiency' device is defined as equipment and components which have the lowest possible power dissipation. A second objective is to develop a thermal design for a class F amplifier through the combination of established thermal design and heatsink technology.

Outline of this thesis:

GaN semiconductor material is well suited for use in high-frequency and high-RF systems. The present study develops a class F power amplifier by employing a discrete GaN transistor. The nonlinear characteristics and electrical performance will then be tested in the newly developed PA.

The thesis is arranged as follows. Chapter 1 discusses the terms used to gauge the PA's electrical performance. It also discusses the nonlinear behavior of PAs, along with operational conditions. Chapter 2 presents the design outcome of a class F power amplifier using a nonlinear transistor model approach explained in the previous chapter. Chapter 3 we will evaluate the thermal characteristics of the designed power amplifier. Finally, Chapter 4 compares a range of measurements results in order to test the performance of the newly-developed PA. The outcomes of these tests give a clear indication of the benefits and disadvantages of using GaN semiconductors for power amplifiers.

Thesis contribution:

Class F power amplifiers are utilized in almost all high frequency wireless communication systems and have great impact on overall system performance. Since power amplifiers mostly operate in deeply nonlinear operation conditions, consume relatively large amount of

system power budget, generate significantly large amount of heat they must be carefully designed and fabricated to have a reliable and cost-effective system.

GaN as a semiconductor material having large energy band gap, high electron mobility and high thermal conductivity offers high power density devices, which are ideal candidates for development of high power microwave power amplifiers. The purpose of this thesis work is performance evaluation of a class F power amplifier, designed and fabricated using GaN technology, for future wireless systems, including but not limited to radar, 5G, medical imaging and microwave heating, which are the typical high frequency applications that need high power amplifier devices

CHAPTER 1

POWER AMPLIFIER FUNDAMENTALS

1.1 Introduction

Power amplifiers (PAs) are critical parts of wireless communication systems such as satellite communications, radar, and mobile communications. However, because the power requirements of applications can be very different, the performance parameters must be made suitable for each type of usage.

A power amplifier (PA) can be defined as equipment utilizing DC power in order to boost the power from incoming signals. So, for instance, microwave power amplifiers function in the so-called microwave frequency portion of the radio frequency spectrum, meaning that they are meant to be used in high frequency situations.

In general, because the main purpose of PAs is to boost power to the level specified by the application, they are mostly employed under large-signal usage. However, large-signal usage tends to distort the signal as well as cause instability and biasing, all of which much be taken into consideration in the development of PAs for specified applications. Therefore, in this chapter, we present definitions for the various types of operating parameters and also introduce and discuss amplifier classes, operational modes, and problems around stability

1.2 Basic Parameters

The simplified energy flow depicted in Figure 1.1 illustrates some fundamental parameters of power amplifier functioning. As shown, we can formulate an amplifier's output and input power as follows:

$$Pout(t) = G(t) * Pin(t) \tag{1.1}$$

where:

Pout(t) : output power in watts

Pin(t) : input power in watts

G(t) : Power gain in watts/watts

Moreover, because different power level requirements can be anything from micro-Watts all the way up to Mega-Watts, we represent power as a dB scale in relation to 1 mW. So, the formulation shown above (i.e., input / output power and power gain) is able to be written on the dB scale as:

$$P_{out,dBm} = G_{dB} + P_{in,dBm} \quad (1.2)$$

Where:

Pout,dBm : output power in dBm as a function of frequency.

Pin,dBm : input power in dBm as a function of frequency.

G,dBm : power gain in dB as a function of frequency.

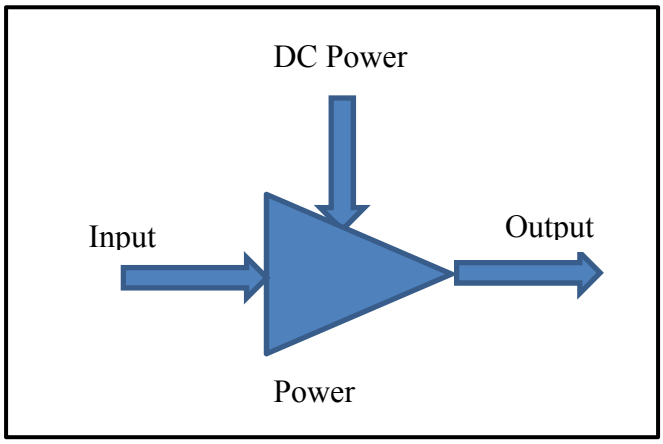

Figure 1. 1 Basic operation of a power amplifier

As shown in Equation (1.2), when the input power rises, the output power will constantly rise as a result. However, in realty, high input power causes the amplifier to saturate from nonlinear behaviour, resulting in gain compression, as depicted in Figure 1.2.

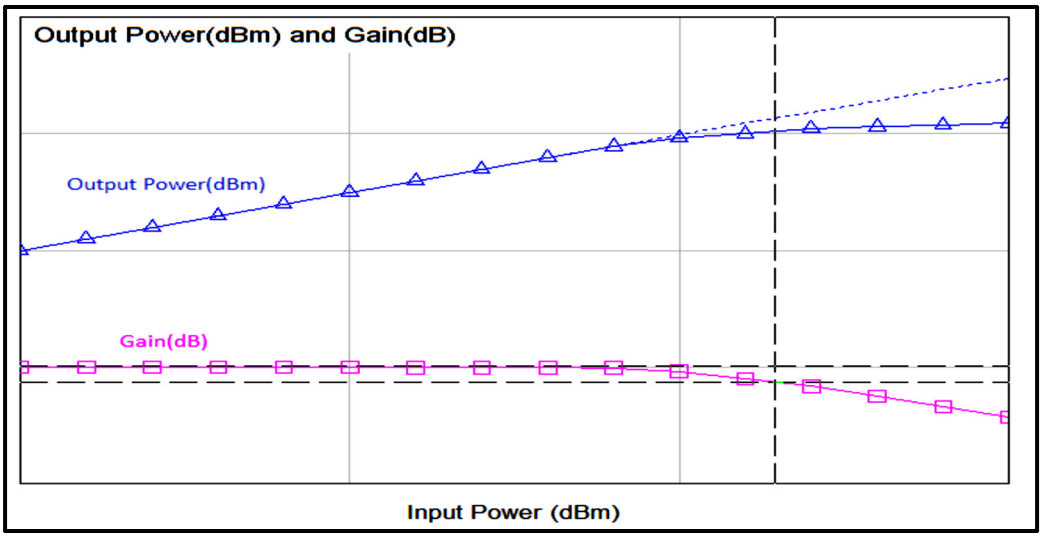

Figure 1. 2 Input power, output power and power gain relation of a typical amplifier

The compression behaviour of a typical amplifier is represented by the two figures of merit Pout, -1 dB, which is the output power level that has deviated 1 dB from ideal linear behaviour, and Pin,-1dB, which is the corresponding input power level. Figure 2-3 illustrates these parameters, indicating that input power and output power measured at precisely 1 dB of compression can be formulated as:

$$\text{Pout,dBm} = (\text{GdB}) + \text{Pin,dBm} \tag{1.3}$$

As mentioned above, saturation output power level is yet another parameter in a typical power amplifier. It indicates the maximum output power which may be removed. Figure 2.3 illustrates that rises in input power result in output power achieving the 1 dB compression point, after which further rises lead to output power saturation (i.e., maximum value).

We discussed previously how microwave PAs change DC power to microwave signal power, suffering loss from the process. A PA figure-of-merit, drain/collector efficiency, can be formulated as:

$$\eta = Pout/P\text{dc} \tag{1.4}$$

Where

η is power efficiency.

Pout is output power.

Pdc is DC power.

To remove the majority of available power out of a PA, it must operate at high input power levels such that the levels of the DC power and output power are the same as the input power. This is accomplished through a power-added efficiency parameter, which considers the contribution of input power, as shown in Equation (1.5). Figure 1.3 depicts efficiency parameter, gain and output power all to be a function of input power.

$$\eta add=(Pout-Pin)/P\mathrm{dc} \tag{1.5}$$

Where

ηadd is power add efficiency.

Pout is the output power.

Pin is the input power.

Pdc is the DC power

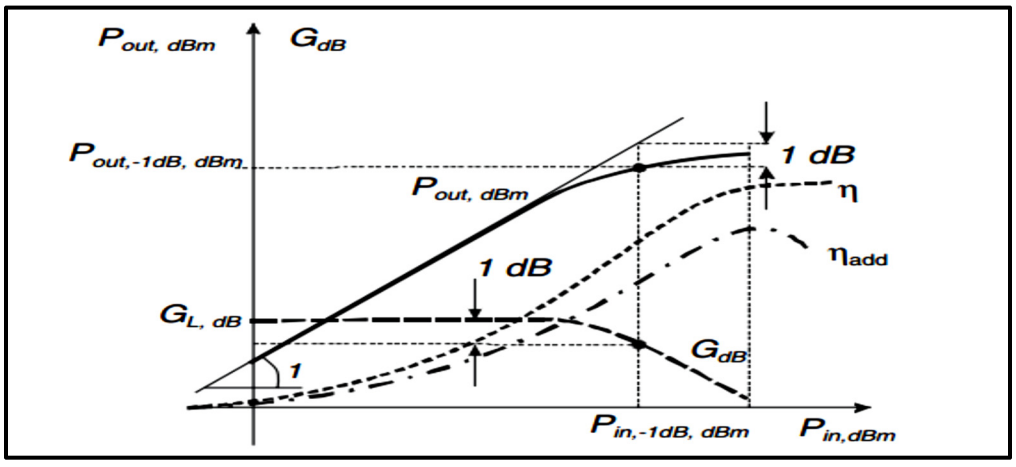

Figure 1. 3 Power amplifier parameters
Taken from Colantonin et al (2009)

1.2.1 Distortion Parameters

Because power amplifiers function in large signal sectors, the output signal from a PA becomes a changed version (i.e., distortion) of the input signal. This happens as a result of restrictions caused by the semiconductor. However, when a PA employs a 3rd order power series approximation, the PA's output voltage is formulated as a function of input voltage:

$$V_O = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 \tag{1.6}$$

Where:

V_O is power amplifier output voltage

V_{in} is the input voltage.

a_1, a_2, a_3 is amplifications factors.

Hence, if input signal presents as a single-tone excitation

$$V_{in}=A\times\cos(2\pi ft) \tag{1.7}$$

The output voltage is

$$\mathrm{V_0} = \mathrm{a_2}\,\frac{\mathrm{A^2}}{2} + \mathrm{A}\times\left(\mathrm{a_1} + \frac{3}{4}\mathrm{a_3A^2}\right)\times \mathrm{COS}(2\pi\mathrm{ft}) + \mathrm{a_2}\,\frac{\mathrm{A^2}}{2}\cos(2*2\pi\mathrm{ft}) + \mathrm{a_3}\,\frac{\mathrm{A^3}}{4}\mathrm{COS}(3\times 2\pi\mathrm{ft}) \tag{1.8}$$

Equation (1.8) clearly indicates that when a single-tone signal affects a PA, the result at the output is the generation of DC, fundamental, 2nd and 3rd harmonic components. Therefore, by applying Equation (1.8), input and harmonic power components are formulated as:

$$Pin=\frac{\mathrm{A^2}}{2} \tag{1.9}$$

$$\mathrm{P_{out.f}}=\frac{\mathrm{A^2}}{2}\times\left(\mathrm{a_1} + \frac{3}{4}\mathrm{a_3A^2}\right)^2 \tag{1.10}$$

$$P_{out.2f} = a_2^2 \times \frac{A^4}{8} \tag{1.11}$$

$$P_{out.3f} = a_3^2 \times \frac{A^6}{32} \tag{1.12}$$

From these formulations, we can see that the power of fundamental component becomes a function of the constants $a1$ / $a3$, along with input signal amplitude.

1.2.2 Harmonic Distortion

Equation (1.8) shows how PAs can create harmonic components as a result of single-tone excitation. Harmonic distortion can be defined as the amount of power in harmonic frequencies related to fundamental component power (Colantonio et all,2009). Given this definition, the nth harmonic distortion of HDnf can be formulated as:

$$HD_{nf} \triangleq \frac{Pout_{nf}}{Pout_f} \tag{1.13}$$

Thus, in a 3rd power series approximation, the harmonic distortion in 2nd / 3rd harmonic components is formulated by applying the harmonic powers from Equations (1.10) to (1.12):

$$HD_{2f} \triangleq \frac{Pout_{2f}}{Pout_f} = \frac{\left(a_2^2 \times \frac{A^4}{8}\right)}{\frac{A^2}{2} \times \left(a_1 + \frac{3}{4}a_3A^2\right)^2} = \frac{\left(a_2^2 \times \frac{A^4}{8}\right)}{\left(a_1 + \frac{3}{4}a_3A^2\right)^2} \tag{1.14}$$

$$HD_{3f} \triangleq \frac{Pout_{3f}}{Pout_f} = \frac{\left(a_3^2 \times \frac{A^6}{32}\right)}{\frac{A^2}{2} \times \left(a_1 + \frac{3}{4}a_3A^2\right)^2} = \frac{\left(a_3^2 \times \frac{A^6}{32}\right)}{\left(a_1 + \frac{3}{4}a_3A^2\right)^2} \tag{1.15}$$

Along with harmonic distortion in every harmonic component, we also obtain the Total Harmonic Distortion (THD):

$$THD = \frac{\sum_{n=2}^{\infty} P_{out,nf}}{P_{out,nf}} \tag{1.16}$$

1.2.3 Gain offset (AM/AM) and Phase Distortion (AM/PM)

Because the 3rd-order power series approximation from Equation (1.6) is a memoryless operation, a few of the nonlinear effects are not visible. A PA's input / output signals can be formulated as:

$$V_{in}(t) = \mathrm{A}(t) \times \cos(2\pi f t + \Phi(t)) \tag{1.17}$$

$$Vout\ (t) = \mathrm{G}[\mathrm{A}(t)] \times \cos(2\pi f t + \Phi(t) + \theta[A(t)]) \tag{1.18}$$

where:

G[A(t)] is Gain, nonlinear function of input signal amplitude.

[A(t)] is Phase change inserted by PA, nonlinear function of input amplitude

Nonlinear behaviour in gain is AM/AM, while nonlinear behaviour in phase change is AM/PM conversions. Moreover, amplitude's nonlinear behaviour comes primarily from nonlinear transconductance, whereas phase's nonlinear behaviour comes from nonlinear behaviour in internal capacitors and inductors from transistor models. Figure 1.4 depicts curves in AM/AM as well as AM/PM (Colantonio et all,2009).

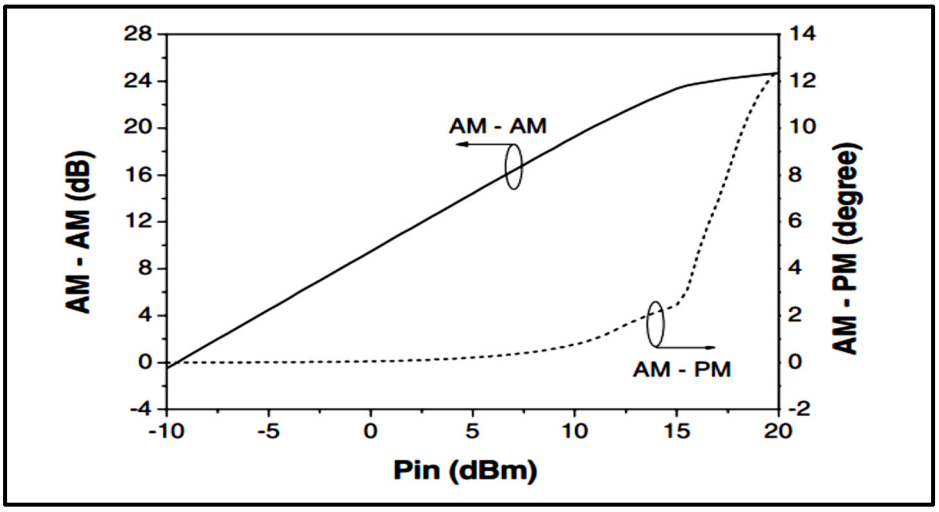

Figure 1. 4 AM/AM and AM/PM characteristics of a typical PA
Taken from Colantonin et al (2009)

However, it is well known that nonlinear input drive-dependent AM/AM and/or AM/PM behaviours are problematic in communications devices because they have a negative impact on the system's constellation diagram. As well, AM/PM conversions occurring in phased array systems could negatively affect the antenna's beam-forming capacity, leading to reduced performance.

1.2.4 Power Amplifier Classes

Power amplifiers (PAs) are classified as either linear or non-linear. In general, linear PAs can create output power that is directly proportional power being input without creating excessive harmonic power, whereas in non-linear PAs, input and output are not proportional, as the PAs function close to cut-off regions and create sizeable harmonics along with the main signal. Similarly, amplifiers can also fall into one of two classifications (classes), namely biasing or switching classes, (Colantonio et al, 2009). Biasing amplifiers (e.g., class A,B, AB and C amplifiers) are categorized as such due to their inherent quiescent point (bias point) and/or output Current Conduction Angle (CCA) θ. In this case, θ can be defined as: "the fraction of RF input drive signal where non-zero current is flowing through the device", (Colantonio et al, 2009). In contrast, switching class amplifiers (e.g., Class E and Class F amplifiers) have a network configuration attached to an active element, though not at the bias level. Hence, switching transistors are switches that turn off and on in accordance with input drive signal , (Colantonio et al, 2009). It is worth noting that because Class E / F amplifiers can offer high power-added efficiency, they are attracting increasing interest from researchers and engineers alike. However, in our current study, we will deal almost exclusively with classes A, B, AB, E, inverse F (F^{-1}) and F (the latter in greater detail).

1.2.4.1 Class A Power Amplifier

Class A amplifiers are linear and have a conduction angle of 360°, which indicates the transistor is turned on and able to conduct across a whole sinusoidal cycle. The majority of small-signal amplifiers fall into this designation due to their relative simplicity of design and

optimal linearity. However, the 360° conduction angle of Class A amplifiers gives them ultra-low efficiency, thus rendering them applicable mainly to low-power applications. Class A amplifier transfer characteristics, along with corresponding voltage / current waveforms, are illustrated in Figure 1.5.

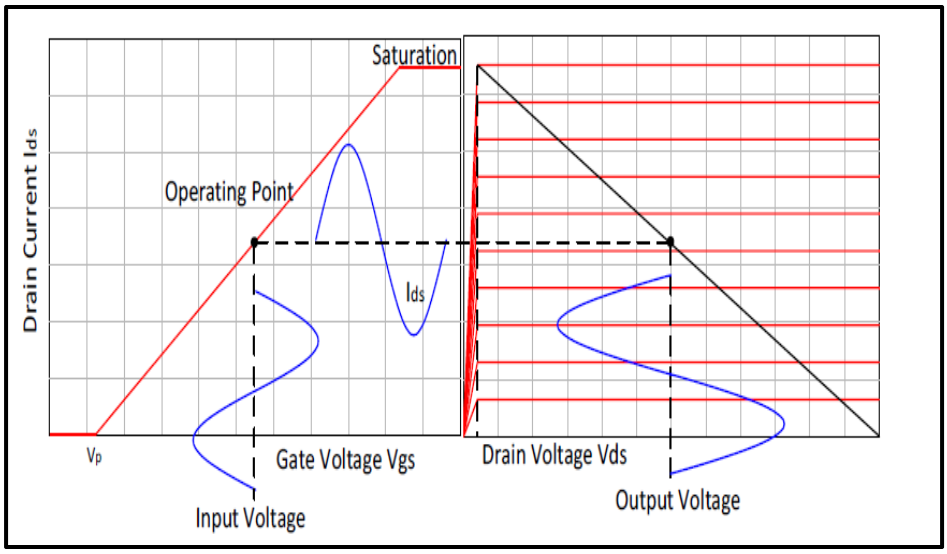

Figure 1. 5 Input and output waveforms of class A power amplifiers

1.2.4.2 Class B Power Amplifier

Class B amplifiers' bias level is lower than Class A's and near the cut-off region. Unlike Class A, the transistor in Class B completes only half an input drive signal cycle, giving these amplifiers a CCA measuring approximately 180° and improved efficiency over Class A , (Colantonio et al, 2009). Class B amps typically show low-grade performance for linearity (due to excessive higher order harmonics), but this can be mitigated by employing dual transistors in a so-called push-pull setup. However, in this 2-transistor setup, both transistors can be OFF simultaneously, resulting in crossover distortion. Figure 1.6 illustrates Class B amplifiers' transfer characteristics as well as corresponding voltage / current waveforms.

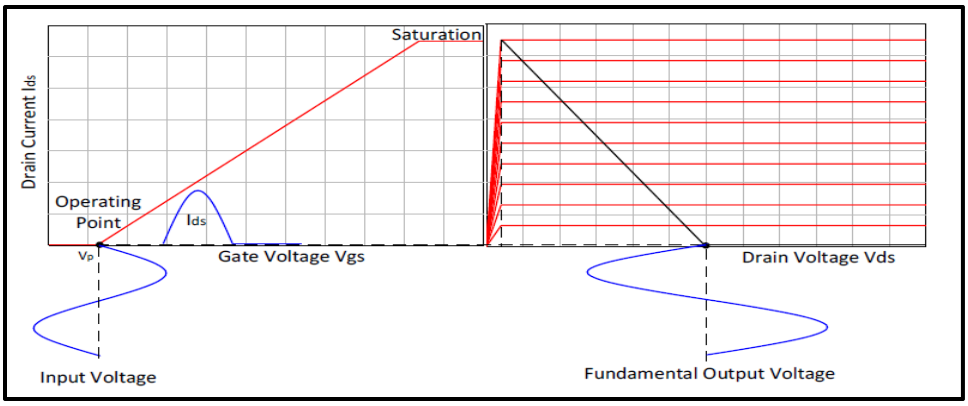

Figure 1. 6 Input and output waveforms of class B power amplifiers

1.2.4.3 Class AB Power Amplifier

As their name implies, Class AB amplifiers function as a combined version of classes A and B amplifiers with regard to efficiency and linearity. Hence, the efficiency and bias point of Class AB amps is situated somewhere between classes A and B amps, as illustrated by Figure1.8. Furthermore, the crossover distortion of Class B is significantly less in Class AB push-pull amplifiers , (Colantonio et al, 2009), giving better linearity. Class AB's transfer characteristics along with corresponding voltage/current waveforms are shown in Figure 1.7.

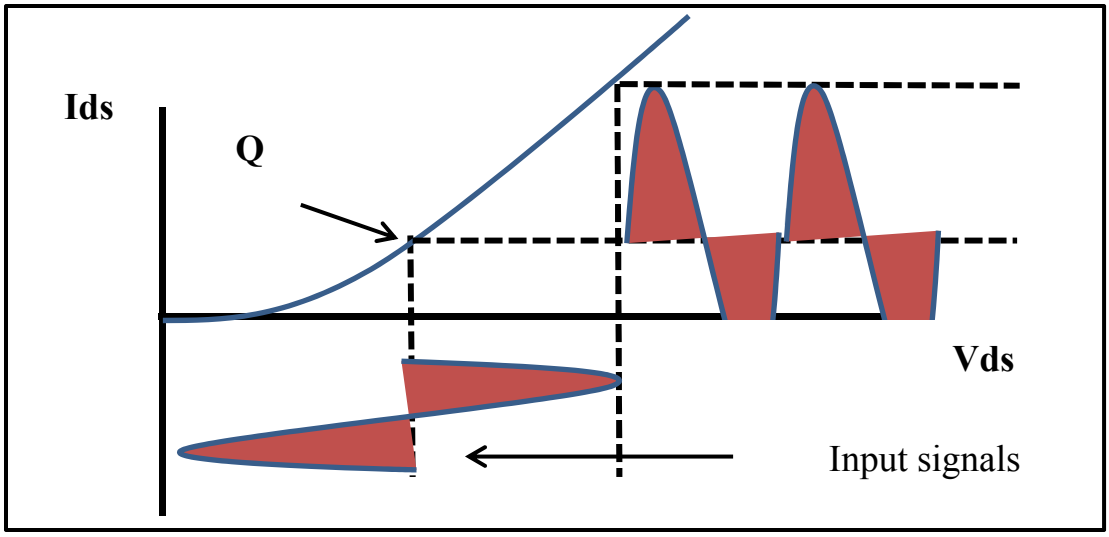

Figure 1. 7 Transfer characteristics, voltage and current waveforms of Class AB PAS

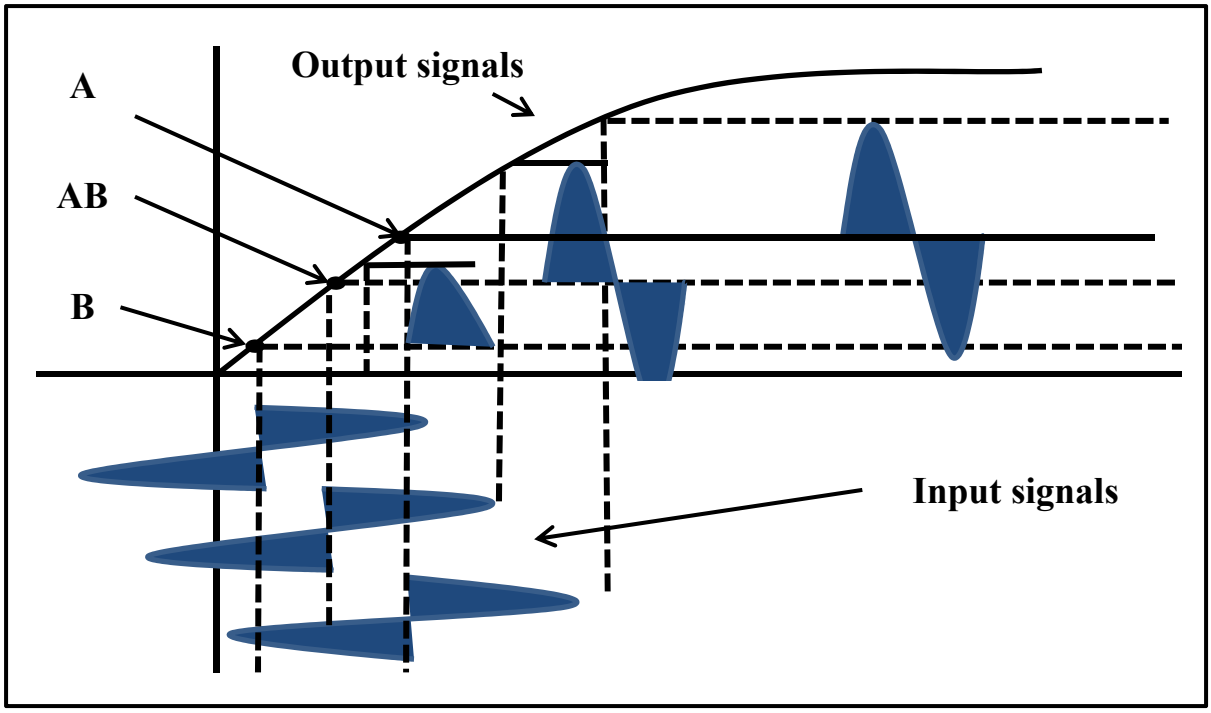

Figure 1. 8 Bias points and voltage / current waveforms for classes A, B and AB

A comparison between the three classes is shown in Figure1.8. As can be seen, the Class A bias point can be found half-way between the saturation and cut-off region, and the channel shows as constantly ON. Furthermore, the input signal is followed by the output signal. Also shown in the figure is that the bias point for Class B is situated close to the deep cut-off region and provides a half-sine wave near the output, with even harmonics only , (Colantonio et al, 2009). Finally, the bias point for Class AB can be found situated midway between classes A and B, with the output signal following 50% the given input signal.

1.2.4.4 Class E Power Amplifier

Also labeled as the 'switching class', Class E amplifiers are easily identifiable by their network configuration to the input and output. Equipment in this class acts like a switch, going ON or OFF for duty cycles of approximately 50%. Class E's employ reactive elements for their output network in order to increase efficiency through zero voltage switching (ZVS) as well as zero voltage derivative switching (ZVDS), the latter which is zero voltage with the

switch ON. In ZVDS, no overlap exists between voltage / current waveforms, meaning there is zero loss from the switching , (Colantonio et al, 2009).

Figure 1.9 shows a transistor (depicted here as a switch symbol), with the Cp indicating a shunt capacitor that models the transistor intrinsic parasitic capacitance as well as the circuit capacitance. The aim is to ensure the amp's appropriate proper switching behavior. The Ls and Cs create a series resonator that operates near the fundamental frequency and only passes this signal to the load. The capacitor Cp charges if the switch is ON. However, if the switch is OFF, Cs and Ls function in series together with R, forming a damped oscillating circuit. This enables the Cp to discharge at the resistive load R , (Colantonio et al, 2009).

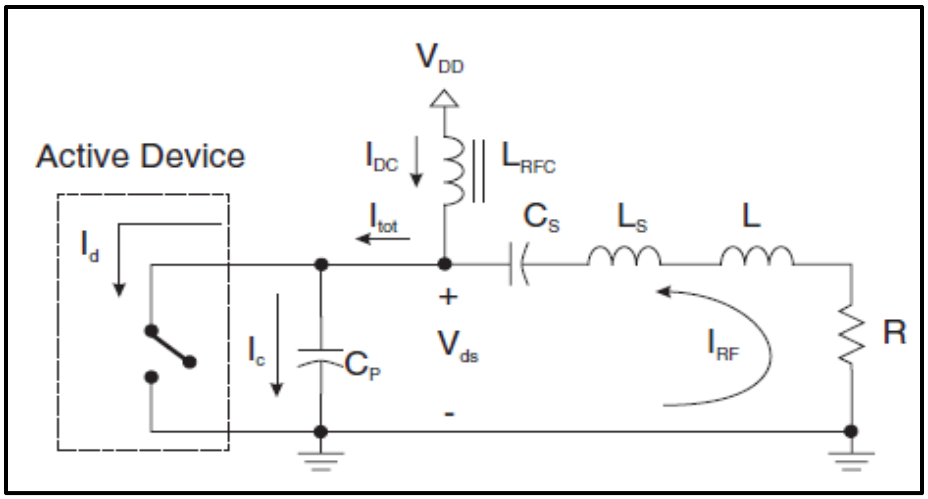

Figure 1. 9 Circuit diagram for Class E amplifiers
Taken from Rosu(2011)

In Figure 1.10, we can see a depiction of the drain current waveform during ON (T1) and the capacitor current waveform during OFF (T2), as well as the drain voltage waveform during period T2. In Figure 1.11, we can see the voltage waveform during OFF and the current waveform during ON. It is worth noting that because there is zero overlap between the voltage and current waveforms, there is zero power consumption under RF functioning.

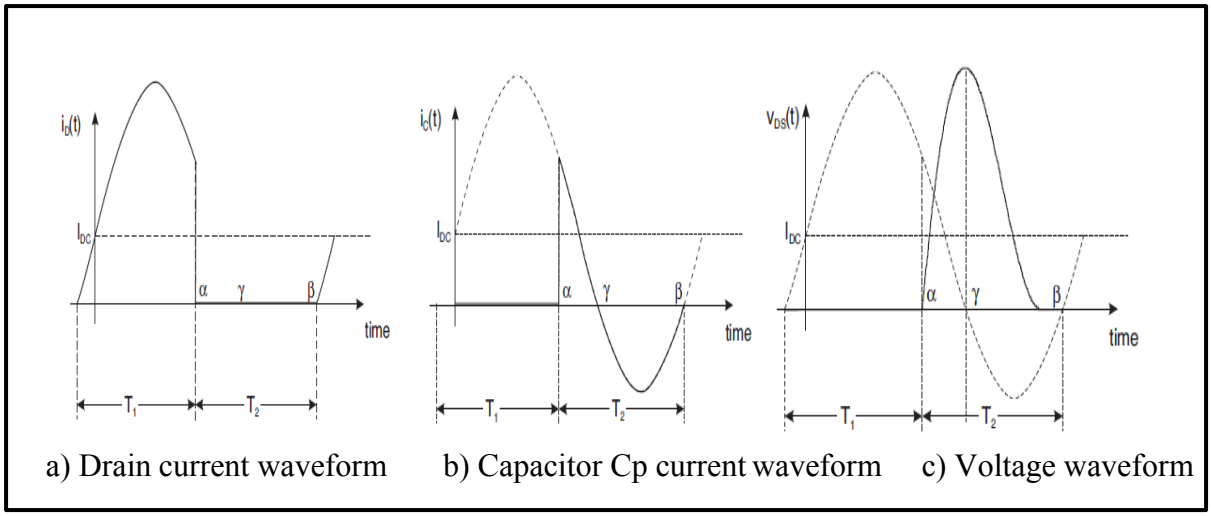

Figure 1. 10 Drain current, capacitor current, and drain voltage waveforms of Class E
Taken from Colantonio et al (2009)

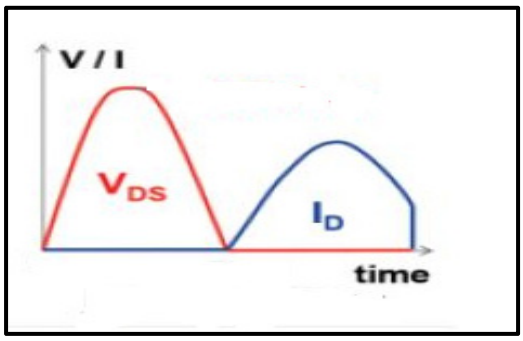

Figure 1. 11 drain voltage and current waveforms of Class E
Taken from Colantonio et al (2009)

1.2.4.5 Class F Power Amplifier

Class F amplifiers represent the successful 'marriage' of the best of classes B and E. To attain Class E ZVS and ZDVS, the efficiency and fundamental signal power are increased through the control of harmonic content and waveforms near the Class F drain , (Colantonio et al, 2009). Class F amps are biased with a quiescent point similar to Class B's (a CCA of 180°). As mentioned previously, switching in the active equipment causes harmonics in the transistor. A negative feature in biasing-class amplifiers, harmonics are actually generated intentionally to increase Class F's PAE. While, theoretically, Class F amplifiers can attain

perfect efficiency with no power consumption or harmonics power sent to the load, nearly an infinite number of harmonics have to be controlled, making this “perfection” unrealistic, (Schmelzer, 2007).

We would see the voltage waveform near the drain as a perfect square wave and the corresponding drain current waveform as a 180° out-of-phase half-sine wave, (Colantonio et al, 2009). Under such theoretically attainable situations, there would be complete elimination of the overlapping area between voltage and current waveforms, with zero power being consumed at the switching. Figure 1.12 illustrates this ideal (but currently unrealistic) Class F voltage and current waveforms giving 100% operational efficiency. Further underlying the theoretical base of this assumption, Equations (1.19) and (1.20) provide formulations for Class F current and voltage waveforms. In the formulations, Ø represents the phase differences in fundamental signal and harmonics, (Colantonio et al, 2009).

Although past research into Class F amplifiers has mostly looked into the output network, more recent inquiries point to the input network’s importance for efficiency improvement, especially the second harmonic input termination’s shaping of waveforms at the input and subsequent PA level. Experiments were conducted both with and without input wave-shaping network, showing that PA without it gave a maximum PAE of 60.31%, whereas PA with it (to control $2f_o$ and $3f_o$) gave PAE of 88.97%. This represents nearly a 30% boost in PAE.

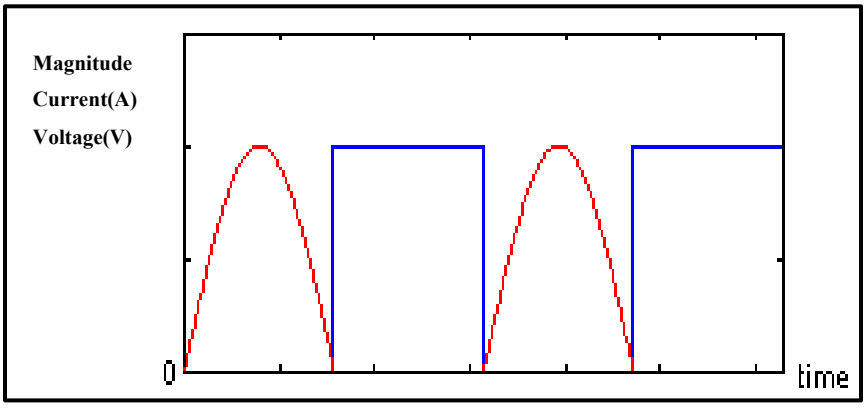

Figure 1. 12 Voltage waveform (blue) and current waveform (red)

$$V(t) = Vdd + V_1 \cos(wt + Ø_1) + V_2 \cos(2wt + Ø_2) + V_3 \cos(3wt + Ø_3) + \ldots \quad (1.19)$$

$$I(t) = Idd + I_1 \cos(wt + Ø_1) + I_2 \cos(2wt + Ø_2) + I_3 \cos(3wt + Ø_3) + \ldots \quad (1.20)$$

To achieve a truncated half-sine current waveform giving a perfect (theoretically idealized) efficiency rate, we applied a normalized Fourier Series Expansion closed-form equation for the coefficients, as shown in Equations (1.23) and (1.24) , (Colantonio et al, 2009). In the equations, n indicates harmonic order.

$$A_0 = \frac{1}{\pi} \quad (1.21)$$

$$A_1 = \frac{1}{2} \quad (1.22)$$

$$A_{n,even} = \frac{2}{\pi} \frac{(-1)^{\frac{n}{2}+1}}{n^2-1} \quad (1.23)$$

$$A_{n,odd} = 0 \quad (1.24)$$

Next, to achieve perfect square voltage waveform for perfect (theoretically idealized) operational efficiency, we applied normalized Fourier Series Expansion closed-form coefficient equations, as shown in Equations (1.27) and (1.28) , (Colantonio et al, 2009). In these equations, n indicates harmonic order.

$$B_0 = \frac{1}{\pi} \quad (1.25)$$

$$B_1 = \frac{1}{2} \quad (1.26)$$

$$B_{n,even} = 0 \quad (1.27)$$

$$B_{n,odd} = \frac{2}{\pi} \frac{(-1)^{\frac{n}{2}+1}}{n^2-1} \tag{1.28}$$

As we can see from Equations (1.23) and (1.24), we first have to get rid of the odd harmonics in the current waveform near the drain if we are to form a truncated half-sine waveform featuring even harmonics only. Next, and as illustrated in Equations (1.27) and (1.28), we also have to get rid of the odd harmonics in the voltage waveform near the drain if we are to create a perfect square waveform that features even harmonics only , (Colantonio et al, 2009). Both of these steps have to be taken if we are to get rid of any overlapping area between voltage and current waveforms that have zero power consumption on active equipment.

In Figure1.13, we can see how the presence of harmonics impacts the shaping of voltage and current waveforms. On the right side, the voltage waveform's top and bottom are flattened, while the transition slope steepens when additional even harmonics are included. On the left side, the current waveform's negative swing is flattened, while transition time speeds up when additional odd harmonics are included. In reducing voltage and current signal transition time, the size of the signals' overlapping area is decreased, and efficiency gets a boostTo

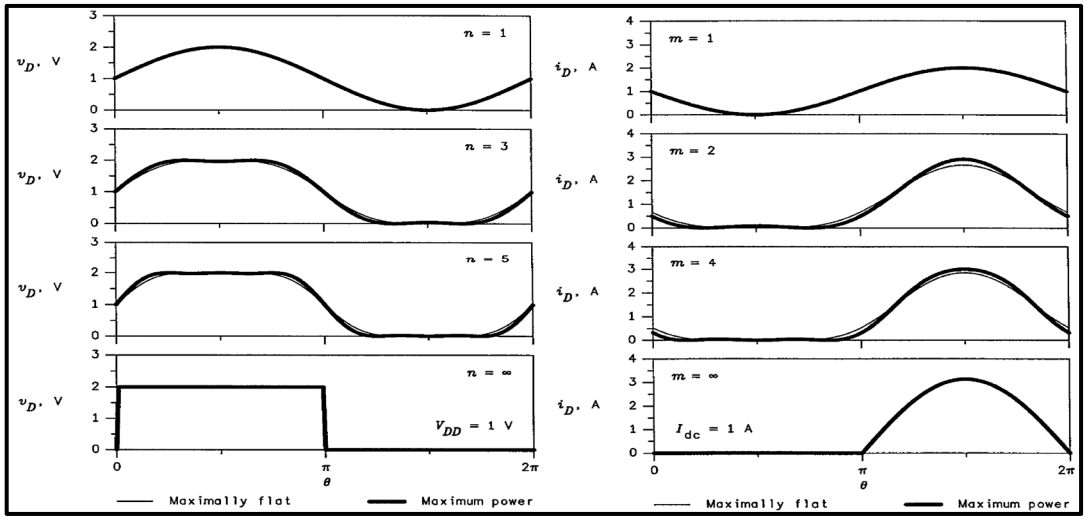

Figure 1. 13 Drain voltage (left) and current (right) waveforms
at different numbers of harmonics
Taken from Raab (2001)

achieve a desired drain waveform, amplifier output networks need to have certain termination impedances for various harmonics. More specifically, for the harmonics needed to shape voltage waveforms, output networks have to present either an open or a high impedance near the transistor drain in order to prevent harmonic power from escaping. Unwanted harmonics can be dealt with by short / low impedance at the transistor drain to decrease harmonic power.

As can be seen in the figures below, inverse Class F (F^{-1}) amplifier waveforms present as the inverse of Class F amplifiers, such that a Class F^{-1} amplifier shows a half-sine voltage waveform and square current waveform near the drain, as illustrated in Figure 1.14 "Maximum efficiency and output of Class-F power amplifiers. Furthermore, Equations (2.29) and (2.30) calculate the output impedance for classes F and F^{-1} amplifiers.

Output impedances for Class F: $Z_{2n} = 0 , Z_{2n+1} = \infty \ldots$ (1.29)

Output impedances for Class F^{-1}: $Z_{2n} = \infty , Z_{2n+1} = 0 \ldots.$ (1.30)

where n = harmonic order

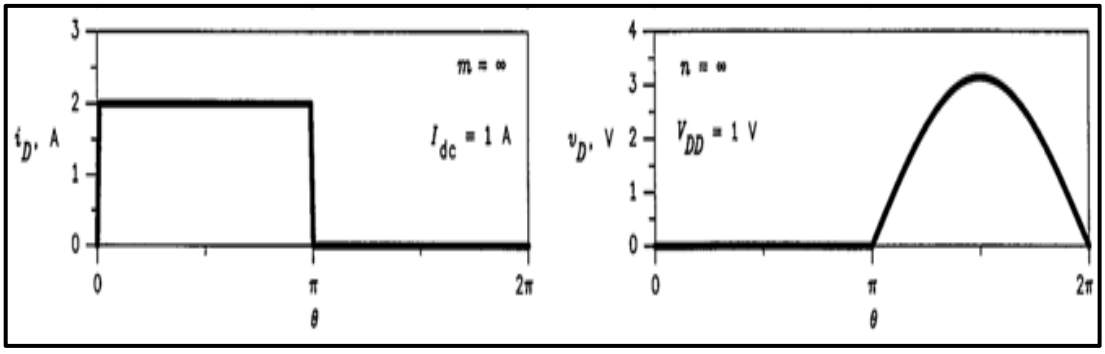

Figure 1. 14 Invers Class F voltage and current waveforms
at infinite number of harmonics
Taken from Raab (2001)

As mentioned above, perfect efficiency can be attained theoretically, but at the expense of simplicity (i.e., the matching networks will grow impossibly complex with the need to control a near-infinitive number of harmonics). This situation is neither practical nor

desirable. In simplified format, Figure 1.15 illustrates a schematic of the classes F and inverse Class F amplifiers' output network. Also of note is that the high frequency signal has the tendency to flow into the drain-source channel and short to the ground due to drain-source parasitic capacitance Cp of the transistor. This is shown in Figure 1.15, (Colantonio et al, 2009). The indication here is that higher order harmonics make reduced contributions either to waveform shapes or PAE. In fact, the transistor parasitic capacitance represents one of the key characteristics restricting the upper bound operating frequencies of transistors such that a small number (rather than an infinite number) of harmonics can be controlled. The filter block essentially operates like a harmonic trap whose purpose is to stop the delivery of harmonic power to the load. This makes it part of the fundamental signal's impedance-matching network which can be utilized for form a desired waveform near the drain.

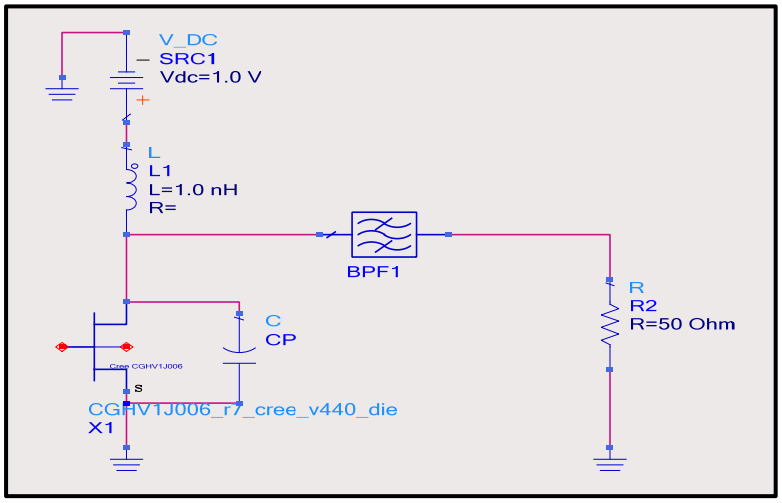

Figure 1. 15 The classes F and inverse Class F amplifiers

Class F topology can be categorized according to the highest order of harmonic that is under control, (Colantonio et al, 2009). So, for instance, a topology is referred to as a third harmonic peaking or third harmonic injection only if there is control present up to the third harmonic. Similarly, a topology is referred to as fifth harmonic peaking/injection only if there is control present up to the fifth harmonic.

Figure 1.16 illustrates a third harmonic peaking configuration in Class F amplifiers. As can be seen, the L3||C3 parallel resonator operates at the third harmonic frequency. This means that it is open to third harmonic signals but rejects any other frequency as a short circuit. Furthermore, the shunt parallel L1||C1 resonator functions at the fundamental frequency such that it shifts the fundamental frequency signal onto the load but shorts harmonics to the ground, resulting in zero harmonic power in the load. It is worth mentioning that output voltage and current waveforms show as being entirely sinusoidal as well as in phase due to the application of a 50Ω resistive load.

In most published research papers (Schmelzer,2007) (Raab,2001), the third harmonic peaking topology is practically applied in order to keep the network from being too complex while providing a robust performance. Normalized harmonic content up to third harmonic and the composition of voltage/current waveforms for third harmonic peaking is shown in

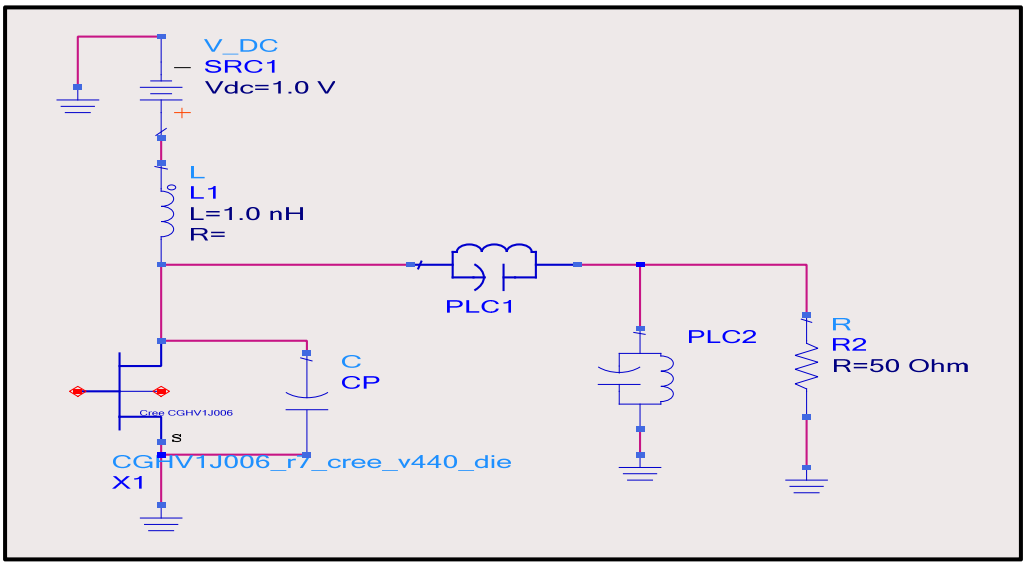

Figure 1. 16 3rd Harmonic peaking configuration using lumped elements

Figure 1.17. With proper magnitude of third harmonic voltage signal, a flattened top and bottom of the voltage waveform can be created

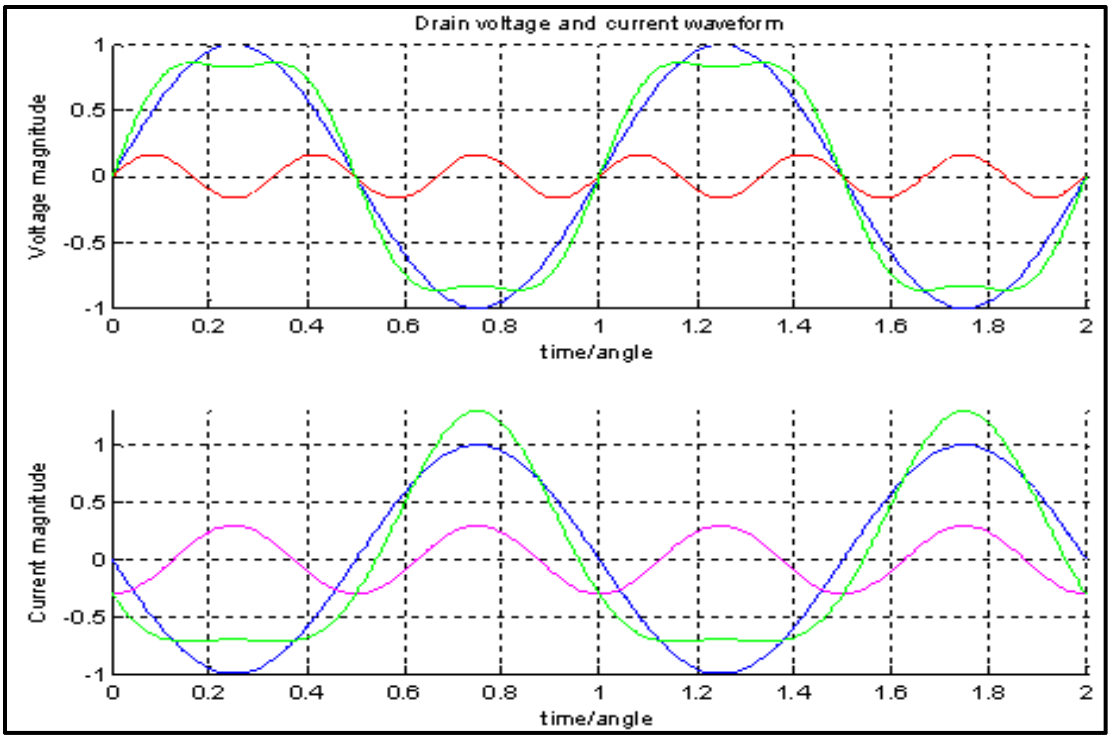

Figure 1. 17 Class F drain voltage and current waveform of 3rd harmonic peaking configuration blue – 1st harmonic / red – 3rd harmonic cyan – 2nd harmonic/green

Figure 1.18 below shows a more advanced Class F configuration, controlling all harmonics using lumped and distributed elements. As described before, L1||C1 parallel resonator provides a short to all harmonics at point B. With a quarter-wavelength transmission line (λ/4 transformer) at f_0 placed between the shunt resonator and the drain, all odd harmonics will have 180° phase shift and all even harmonics phase will stay unchanged at point A. However, this would only be true in theory. In practice, a fixed λ/4 transformer at the fundamental frequency cannot be used for an infinite number of harmonics. As the frequency increases, the line becomes more inductive to the signal and causes imperfect transformation between an open and a short. Moreover, L1||C1 resonator in parallel with the load is assumed to have an infinitely high-quality factor, which is hard to achieve in real implementation. Quality factor for parallel resonators can be calculated according to kind of transistor. It requires a large capacitance C to inductance L ratio or large value of R in order for a high Q factor.

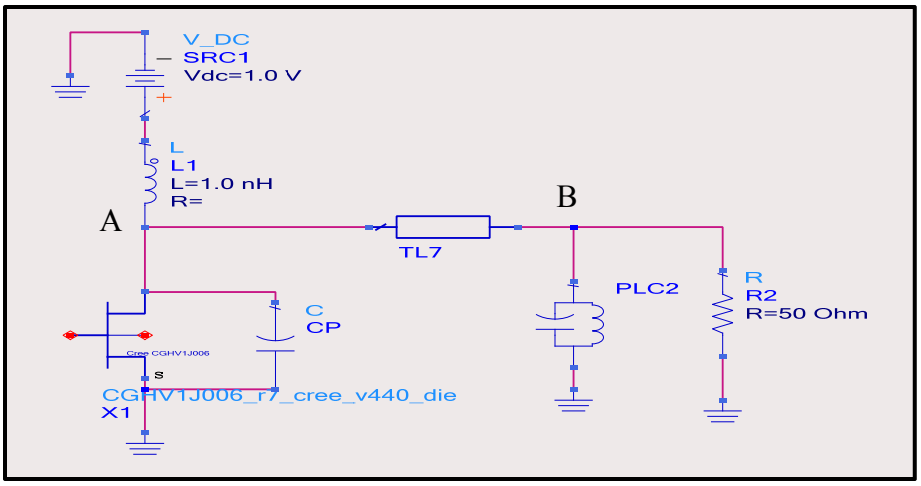

Figure 1. 18 Example of 3rd Harmonic peaking configuration

1.2.5 Quality Factor For RCL

There are 2 ways to implement a Class F PA. One way is to use lumped elements and the other way is to use distributed elements. This project will use distributed elements. Lumped elements are more suitable than distributed elements for low frequency applications because devices using lumped elements are smaller in size for such applications. However, lumped-element PAs are hard to design as the operating frequency gets higher because of the difficulty in finding small inductors in pH range value. Because of the tiny inductance required by the high Q resonator at high frequency, it makes the lump-element design impractical. Moreover, it is difficult to find ideal components without knowing the uncontrolled parasitic model of elements as the frequency increases. Therefore, lumped elements with low percentage tolerance such as 2% must be chosen and experimentally characterized before the usage. A few percent of variation in lumped element values will have a great impact on the system performance. Moreover, it is difficult to obtain inductors.

$$Q_P = R\sqrt{\frac{L}{C}} \tag{1.31}$$

1.3 Power Amplifier Circuit Blocks

To get a deeper understanding of a class F power amplifier's internal dynamics, designers can break down a device into relevant circuit blocks. Figure 1.19 illustrates how a PA can be divided into blocks. Such a breakdown can also be applied as the topology in high-frequency designs. The present thesis work employs this specific topology for its PA design.

In a typical power amplifier, an output matching network changes the load impedance to optimal impedance given in the transistor and drain bias network in order to use drain bias voltage. The output matching network is then integrated with the drain bias network.

However, in the present study, the two networks are viewed as separate circuit blocks in order to better relay how each one works.

Along with an input matching network and a gate bias network, the input side in a power amplifier features a stability network. The design of the stability network must be such that it can handle the PA's stability issues. As well, DC block capacitors are positioned on all sides of the amplifier. The purpose of these capacitors is to block any DC component in the incoming and outgoing signals, and thus to permit the propagation of RF signals only.

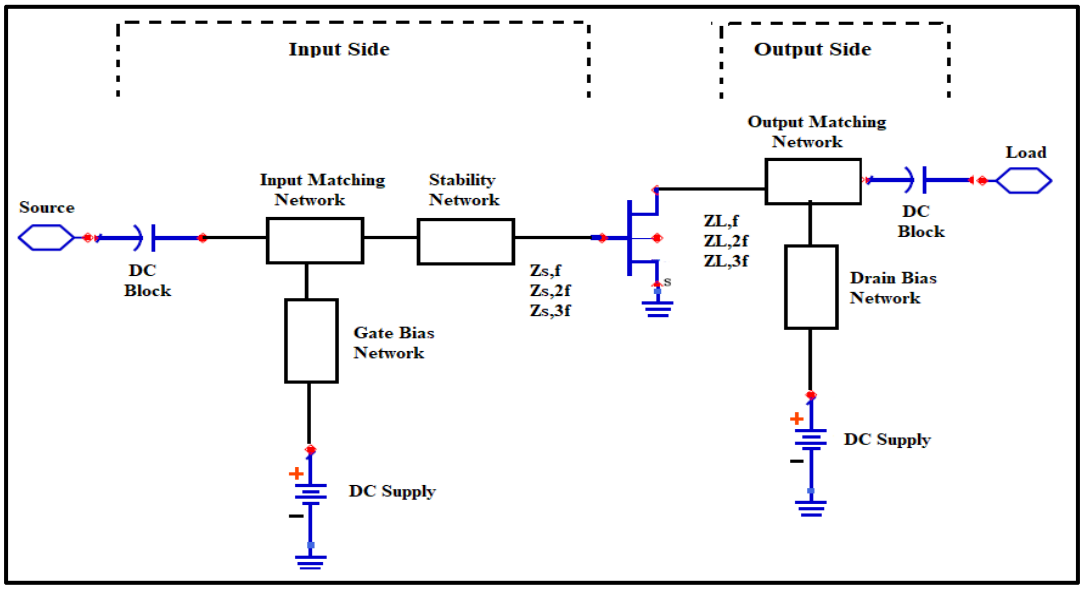

Figure 1. 19 Class F power amplifier block diagram

1.3.1 Stability Network

A very crucial aspect of power amplifiers is that they not oscillate. However, because of feedback mechanisms in transistors, output signals could potentially be rerouted at the input side; if this occurs, and the input and feedback signals share some of the same phases, this could lead to oscillations. While the process may be done on purpose for oscillator circuits, it is undesirable in amplifiers because it negatively impacts their performance and also can be dangerous. So, following the decision regarding operational class, the next step is performing a stability analysis for the transistor, as well as designing a stability network, if one is required.

If circuits lack the necessary stability for the application, there is the potential for unlimited increase in signal. This situation puts the active devices into the mode of large signal operation and/or saturation. To avoid this unwanted scenario, power amplifiers need to be stable across all frequencies as well as all source-load impedances. Oscillations could cause any one or more of the following problems (Gilmore et all,2003):

- Unusually noisy circuits,
- Damage to the device being used, caused by undesirable large signal operation,
- Saturation of the active device, resulting in the circuit design becoming invalid.

We can use a few different approaches to find out whether or not a transistor is potentially unstable. One of the simplest approaches is the μ-factor, in which the designer only has to consider a single parameter to see if the device is stable. This parameter is:

$$\boldsymbol{\mu} = \frac{1-|S22|^2}{|S11-\Delta S22^*|+|S21*S12|} \tag{1.32}$$

where $\Delta = S11 * S22 - S21 * S21$

The designer needs to take the μ-factor into consideration for the zero frequency up to the high frequencies for the applicable band, adding to the design a stability network if one is required. In the present work, the μ-factor has been applied to the design process in order to

assess any stability issues occurring at circuit level. As the μ increases, there is also a reduction in maximum available gain (MAG) from the applicable active devices. So, for the band of interest, the μ-factor should be sufficiently big to give a stable operation while at the same time being sufficiently small to get high gain. Chapter 4 discusses a few simulations involving the μ-factor relation to MAG.

Stability networks are a prerequisite for circuits, if the aim is to have unconditional stability across all frequencies and impedances involving the transistor. Figure 1.20 illustrates two stability network topologies. In this study, the topology in Figure 1.20.a is used mainly because it is easy to implement with microstrip circuits. The RC network's equivalent series impedance is expressed as:

$$Z_{eq} = \frac{R}{1+w^2*R^2*C^2} - j\frac{w*R*C}{1+w^2*R^2*C^2} \tag{1.33}$$

The resistance from the equivalent impedance boosts the loss amount at the power amplifier's input side. Therefore, because transistors generally exhibit higher gain in low frequencies, and also because the available gain goes down when the frequency goes up, the transistor requires high resistance for low frequencies but lower resistance when the frequency goes up to ensure stability. Equation (1.33) shows how resistance goes down when frequency goes up, indicating that the capacitor's reactance is becoming short. Power amplifiers benefit from this scenario because of the available gain-frequency relationship, so choosing the right R and C results in a network that has unconditional stability.

However, in actual applications, higher frequencies means that circuit elements have to be comparable to wavelength and that the circuit elements as act as distributed elements. In this work, the R-C network is being designed with distributed resistance and capacitance that feature parasitic components (e.g., additional shunt capacitances and inductances) on the actual elements. These inductances and actual capacitance C could potentially resonate and create open circuits on a frequency band, leading to only the series resistance being effective. As a result, there could be undesirable high loss. To prevent this situation, designers should

take the time to model the circuit elements in order to gauge the impacts of the parasitic components as well as the actual high frequency

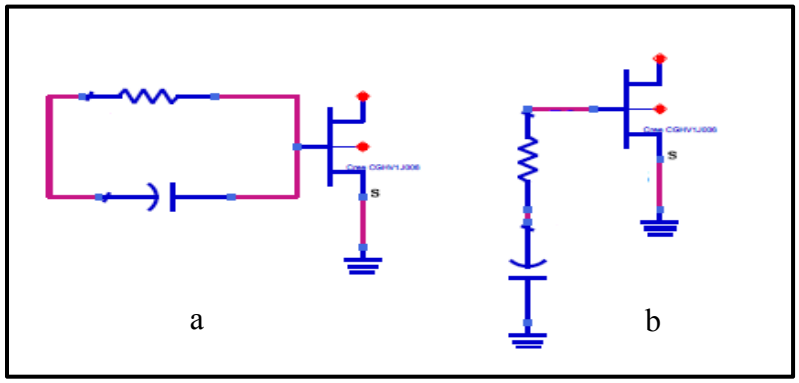

Figure 1. 20 Stability network topologies

1.3.2 Matching Networks

Input and output matching networks work together to create optimal impedances. These are derived from the active devices load pull data at the gate and drain. Another important feature in these networks is low loss matching elements, which prevent power loss during output/input stages. However, because the large size of lumped elements makes them impractical for microwave frequencies, distributed elements like short or open stubs and series transmission lines can be employed instead for matching elements.

Complex impedances can be matched by employing single or double stub lossless matching networks. These are then realized by employing microstrip series lines or stubs. Because one part of a single stub matching network is unable to accomplish wideband matching, multi-section networks have to be utilized for impedance matching in wide bandwidths. Figure 1.21 illustrates an open single stub matching network, while Equation (1.34) expresses the input impedance.

$$Z_{in} = -j * Z_2 cot\theta_2 + Z_1 * \frac{Z_L + j * Z_1 * tan\theta_2}{Z_1 + j * Z_L * tan\theta_2} \quad (1.34)$$

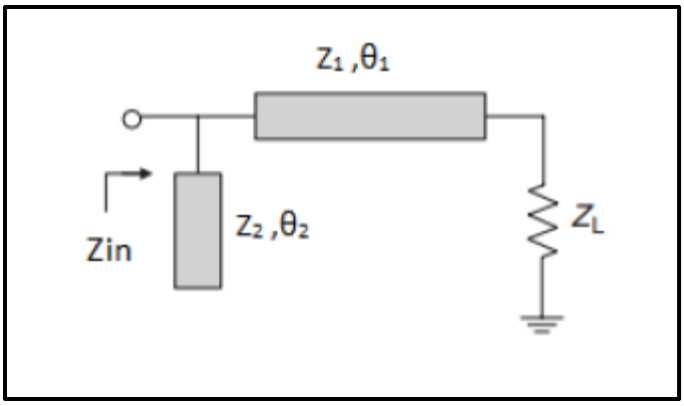

Figure 1. 21 Single, open stub matching network

An additional issue in the matching strategies mentioned above is how the approaches are based on having continual input / output impedances across frequencies, but a power amplifier's optimal impedance gets altered in the interested frequency band. So, for wideband matching, the impedance transformation has to be monitored in the matching network and for the entire frequency band. One typical method involves using quarter wavelength transformers as well as low pass matching networks simultaneously in order to realize the necessary impedance matching for interested frequency bands.

On the other hand, if the requirement is for high RF output power, wide gate periphery devices are preferable as they significantly reduce the transistor's load and source impedances. This effect will be demonstrated later in Chapter 4 of the present work. The transistor employed as this thesis study's active device displays an optimal load impedance (real part) of 2 ohms. So, in matching 2 ohms and 50 ohms, the output matching network has 1:25 as an impedance transformation ratio but matching this in wide bandwidths is difficult.

1.3.3 Bias Network

When bias network elements cannot be applied in matching elements, this means that the bias network input impedance is extremely high and open circuit. In low-frequency

amplifiers, we can use bias networks with RF chokes. Bias networks can be developed with λ/4 transmission lines for microwave frequencies.

Figure 1.22 shows drain bias and lumped element gate networks. As can be seen, the electrical length separating the RF choke from the decoupling capacitor has to be relatively short so as not to alter the RF short impedance. For this reason, PA designers can use the Smith chart for their RF bias network design in order to locate the Z_bias impedance.

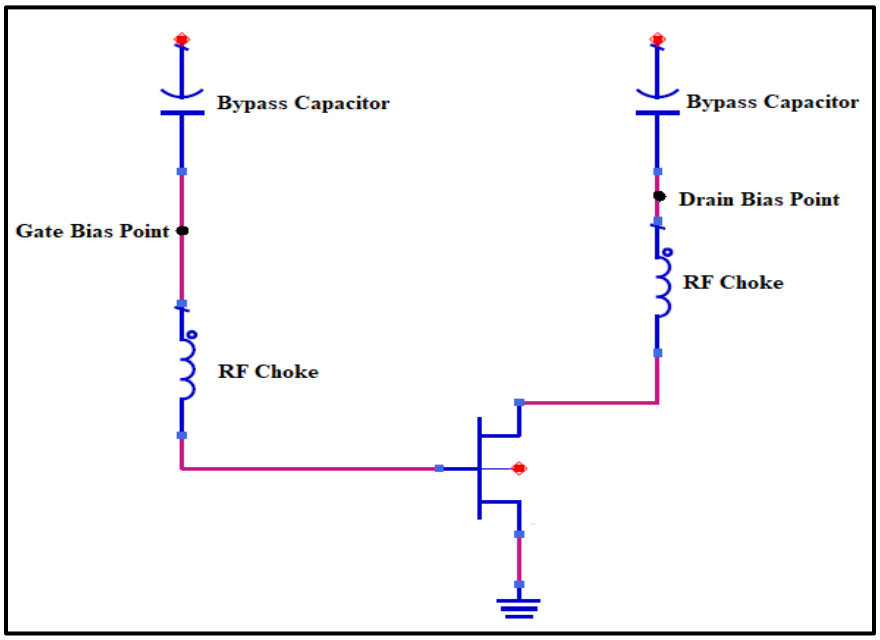

Figure 1. 22 A typical lumped element gate and drain bias networks

Figure 1.23 depicts a bias network which has been synthesized utilizing λ/4 transmission lines along with decoupling capacitors for gate/drain bias point short circuiting (ultra-low impedance). Theoretically, as reduced impedance behaviour in a capacitor comes from increasing the frequency, we assume that the capacitor's bias points have quite low impedance values (that is, near short-circuit status on the Smith chart). But theory is not practice, so in reality, capacitors tend to exhibit complex electrical modeling, meaning that they exhibit resonance frequencies that lower the frequency spectrum's usable range.

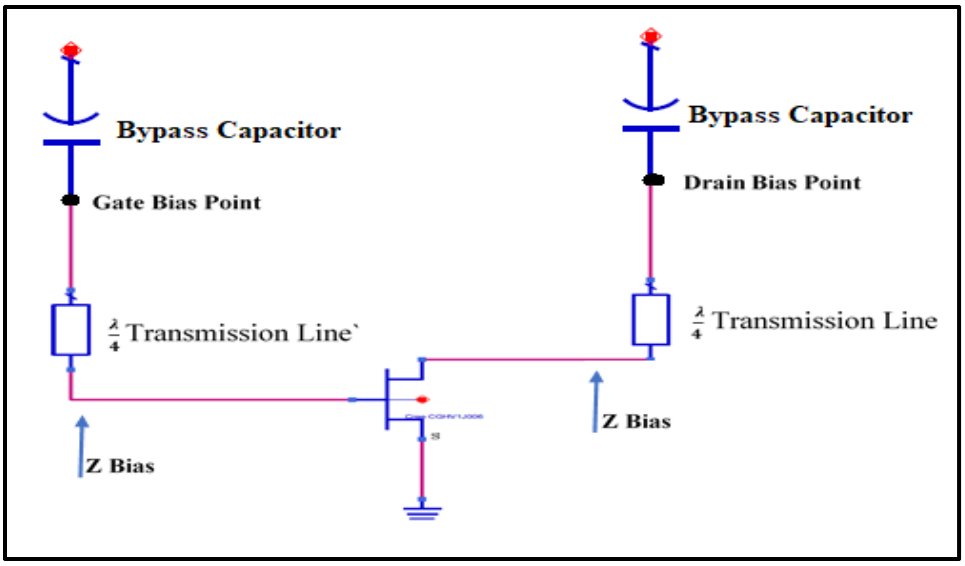

Figure 1. 23 A typical distributed bias network with short circuit capacitor

Figure 1.24 illustrates a wideband distributed element bias network. As can be seen from the figure, the λ/4 microstrip butterfly stub serves as the wideband short circuit for the biasing point, while the λ/4 transmission line changes the short circuit into an open circuit. Moreover, because the microstrip butterfly stub is a short circuit, we no longer require a close bypass capacitor. To deal with any abrupt alterations that negatively impact performance, we can use a decoupling capacitor in order to decouple circuit and supply.

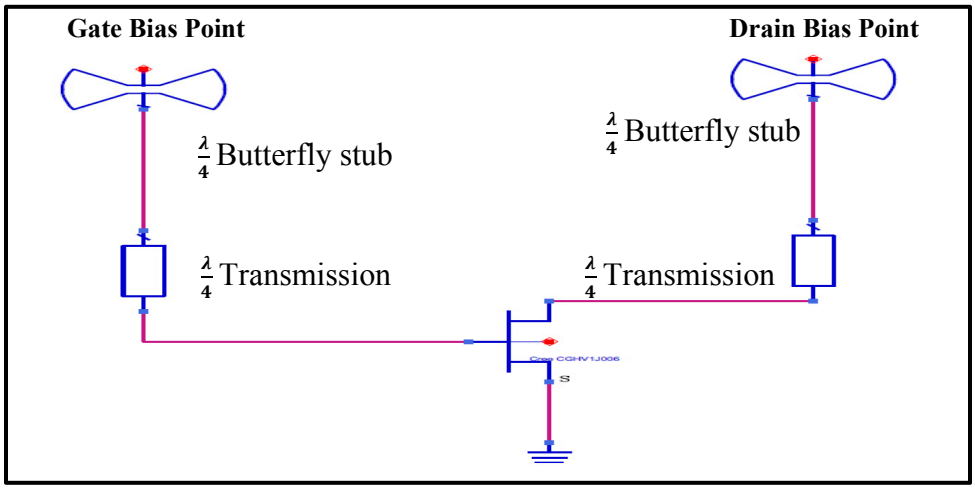

Figure 1. 24 A typical distributed bias network with butterfly stub

1.4 Literature review:

Within wireless communications systems, power amplifier blocks typically use up the majority of the available power. This situation will only get worse, as the latest versions of technology require more and more data transmission capability at the same time as they demand as little spectrum usage as possible. The key to this dilemma of creating high data transmission abilities with low spectrum usage is to optimize power efficiency through reductions in off-chip components used in the radio frequency transmission systems. This would be particularly relevant in mobile wireless applications, which demand the smallest possible sizing. Extensive research has been performed on these issues thus far. Below is a summary of the most relevant and promising results in the literature.

Kuroda et al. (2012) looked at designing and fabricating a class F amplifier by employing AlGaN/GaN HEMT at 5.7 GHz. However, when operating at 5.7 GHz, the parasitic effects (e.g., output capacitance in bounding wires) need to be eliminated, which is accomplished through adjusting the load circuit. The researchers applied nonlinear analysis and exact large-signal model parameters from computer simulations to design their class F amplifier and used harmonic impedance tuning to improve their efficiency rates. Kuroda et al.'s (2012) amplifier, which incorporated a low-loss resin microstrip substrate into the design, maximized drain efficiency up to 77.1% and power-added efficiency up to 68.7% when operating in the 5.69 GHz range. It was critical to reduce losses in the parasitic resistances, as these can lower efficiency levels (Kuroda et al., 2012).

Ahmed (2016) pursued a class F PA design strategy that used Gigahertz frequencies. Class F can be applied in wire application PAs of any frequency that require high output power, good gain, and high efficiency. Several different harmonic terminations using design approaches like load network with lumped LC elements are potential contributors to enhancing efficiency in class F PAs. Thus far, the best PAE recorded in the literature is 82.9%, which falls far short of the potential and ideal 100% efficiency rate. Ahmed (2016) suggested adopting a novel method that incorporates wireless RF applications in order to attain higher efficiency in class F PAs.

In Hayati (2015), a novel structure was in fact realized for high-efficiency and high-frequency class F Pas. The researcher employed ATF-34143 pHEMT transistors which were loaded optimally for harmonic and fundamental frequencies. Hayati's (2015) results show that a highly efficiency class F PA mode was attainable for 2.4 GHz, with a PAE at 80% and 23.6 dBm output power. In this design, the size reduction was achieved by paring back the sizes of the output matching circuit and harmonic control circuit (Hayati, 2015).

Gaw et al. (2005) developed a class F amplifier which featured high PAE, using pHEMT technology. The design method was simulation-based and employed a load-pull/source-pull strategy. Results for 2 GHz showed excellent agreement with the simulation and underscored the importance of the second harmonic input tuning. Also in Gaw et al. (2005), there was a comparison of cases both experimentally and theoretically, showing worst and best and case terminations measuring, respectively, 42% and 76% saturated PAE. This design strategy could be applied for optimizing the intermodulation distortion and additional output power of a range of Pas (Gaw et al., 2005).

Shang et al. (2016) explored the development of a novel high-efficiency K-band MMIC medium-power PA. The design incorporated multi-harmonic matching through the application of GaAs pHEMT process technology and functioned at 26GHz frequency using 2GHz bandwidth. The researchers attained an output power of 20 dBm 1 dB compression-point with an efficiency of 40%. For evaluating thermal characteristics, the researchers also proposed the design of a novel thermal reliability analysis strategy which could be based on ICEPAK (Shang et al., 2016).

As shown above, few techniques are implemented at 5.7 GHz. Furthermore, few of these have been fabricated using the LTCC. The proposed research is focused on a class F power amplifier design at 5.7 GHz using GaN technology. In addition, a novel thermal reliability analysis method is proposed also to evaluate PA thermal characteristic

CHAPTER 2

ELECTRICAL DESIGN OF CLASS F POWER AMPLIFIER

2.1 Introduction

Chapters 1 presented the main ideas and parameters to consider when designing a power amplifier. Chapter 2 will present the basic requirements for designing and building a power amplifier prototype. As will be seen, designing a PA requires several steps, each one of which can have an impact – for good or for bad – on the PA's performance capabilities. After the PA is constructed, small- and large-signal simulations will be carried out to compare the performance of this PA with those in the literature. As well, circuit topology and a drain voltage pulsing method is presented.

In PA design, the process begins by defining the requirements and specifications. The process is completed when the newly designed PA has been validated, meaning that it has met all or most of the stated requirements and specifications. The next sections provide a detailed outline of the design process.

2.2 Requirements

Performance requirements for PA design usually include factors like bandwidth, efficiency, output power and gain, as well as specifications on linearity parameters, electrical performance, and mechanical dimensions. Additional factors and specifications could involve temperature range, which would mean that thermal precautions would have to be included in the design.

The PA should include the following features. In fact, these requirements lay the groundwork for subsequent design decisions.

Table 2.1 PA Requirements

Parameter	Requirement
Operating Frequency	5.7 Ghz
Input Power	25 dBm
Output Power	36 dBm
PAE	As high as we can
Small Signal Gain	17 dB

2.3 Device selection

The design process has several steps. As a first step, deciding which active device (here, the transistor) to use is very important. The transistor must not only have suitable efficiency and output power, but also the right gain, linearity requirements, and reliability. Table 2.2 compares a few semiconductor materials and their parameters, (Runton et al, 2013). So, for instance, if we need high power density, the best option might be GaN devices, but they are quite expensive. On the other hand, if cost is more important than power, a GaAs device would be ideal. Another consideration is the transistor's upper limits for operation frequency. These need to be checked to see if the operation band suits the project center frequency and bandwidth.

Table 2.2 Some properties of semiconductor materials

Property	Si	GaAs	GaN	SiC	InP
Electron Mobility ($cm^2V^{-1}S^{-1}$)	1500	8500	1000	900	5400
Hole Mobility ($cm^2V^{-1}S^{-1}$)	450	400	350	120	200
Saturated Drift Velocity ($10^7 cm/s$)	1	2	1,8	0,80	2
Thermal Conductivity (W/cm.C)	1,40	0,45	1,7	4,90	0,68
Dielectric Constant	11,90	12,90	14	10	8
Substrate Resistance (Ohm)		>1000	>1000	<20	>1000

In accordance with the requirements defined in table 2.1, Cree's CGHV1J006D GaN discrete transistor die is chosen as the active device in this project. Total gate length of the CGHV1J025D is 0.25 um and the overall size of the die is 0.8 mm x 0.84 mm with a thickness of 100 um. A photo of the transistor is shown in Figure 2.1.a. The CGHV1J006D non-linear model is obtained from the manufacturer Cree and applied in simulation. The ADS model of the transistor is shown in Figure 3.1.b. The parameters case temperature (tcase) and junction-to-case thermal resistance (crth) need to be adjusted according to the datasheet and instructions.

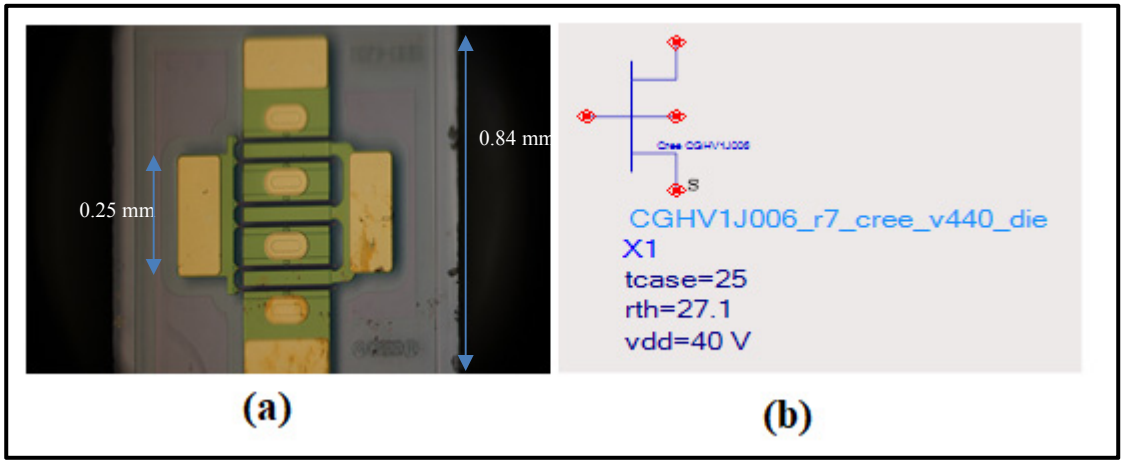

Figure 2.1 The CGHV1J006D GaN Transistor (a) physical photo (b) ADS model

2.4 LTCC Technology and Material Selection

Along with choosing an active device, the designer must also choose a specific substrate material that will be used to construct the matching circuits. Low loss tangent material is ideal for maintaining the gain and power provided by the active device. Thermal conductivity should also be a priority, as certain substrate materials experience heating which results from circuit losses and/or high RF power levels.

Another consideration is that high dielectric constant materials provide the opportunity for designing circuits that are relatively small, giving an overall smaller PA. In this case, a large

dielectric constant material that features high thermal conductivity and low loss tangent is preferable. We chose Rogers A6M as a substrate material. Table 3.2 lists its main properties.

Table 2.3 Rogers A6M Material Properties

Parameter	**Value**
Dielectric Constant	5.9
Loss Tangent	0.0008 @ 5GHz
Thermal Conductivity (Watts/m°K)	1.5
Thickness	39.5 mil

In this study, microstrip transmission lines and stubs are constructed on a Rogers A6M substrate material. The width and length of the microstrip lines have been measured using the LineCalc tool found in ADS design. Figure 2.2 illustrates the substrate layers.

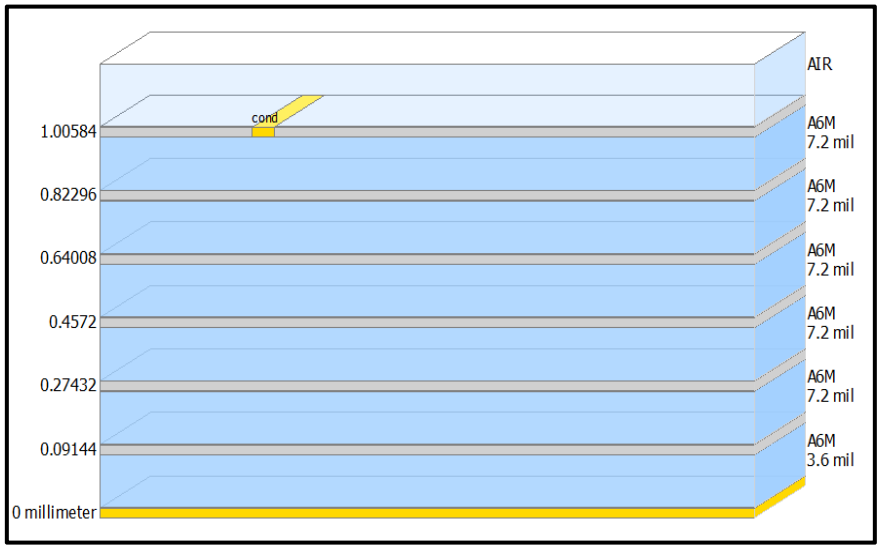

Figure 2.2 Substrate layers

2.5 Bias Network

Bias networks are mainly used to move the current and voltage across an amplifier. Bias lines need high impedance to prevent loading down main lines. In a bias network, power is sent to an RF choke that prevents the RF from coming into contact with the DC supply. This is because there is high impedance in fundamental frequencies (e.g., 5.7 GHz). Biasing can still be realized through the use of microstrip components like λ /4 lines and stubs. To recap: the primary purpose of biasing networks is to hinder RF's ability to stop DC when power is being supplied. The PA in the present work is broadband, so we will use a microstrip butterfly stub because it has a large bandwidth for stop-band in the adjustable wings (Joshi et al, 2006). Figure 2.3 shows a bias network with a quarter wave length.

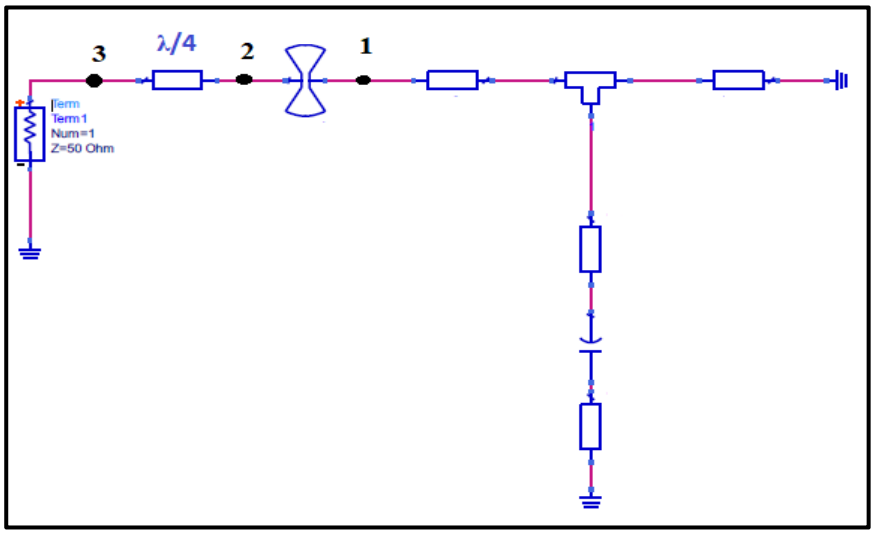

Figure 2.3 Design of bias network with a quarter wave and stub

In f_0, the RF open circuit (node1) is changed by MBSTUB to the RF short circuit (node2), just as node2 is changed to RF open circuit (node3). The progression across these nodes provides a full Smith chart rotation (360) as well as open circuit on node3 in quarter-wave line MLIN. Figure 2. 4 indicates impedance equal to 12.4 kΩ.

In $2f_0$, RF open is changed by MBSTUB into RF open, because lambda on this frequency is twice the value, such that changes to the stub become equivalent to full rotation of the Smith

chart. Hence, the RF open can then change into RF short in quarter-wave line. In much the same way, $3f_0$ MBSTUB changes RF open circuit into RF short at the left node, a change which is equivalent to a Smith chart rotation of 540 degrees. Consequently, MLIN can rotate the RF short quarter wave on the chart, giving RF open at the left node.

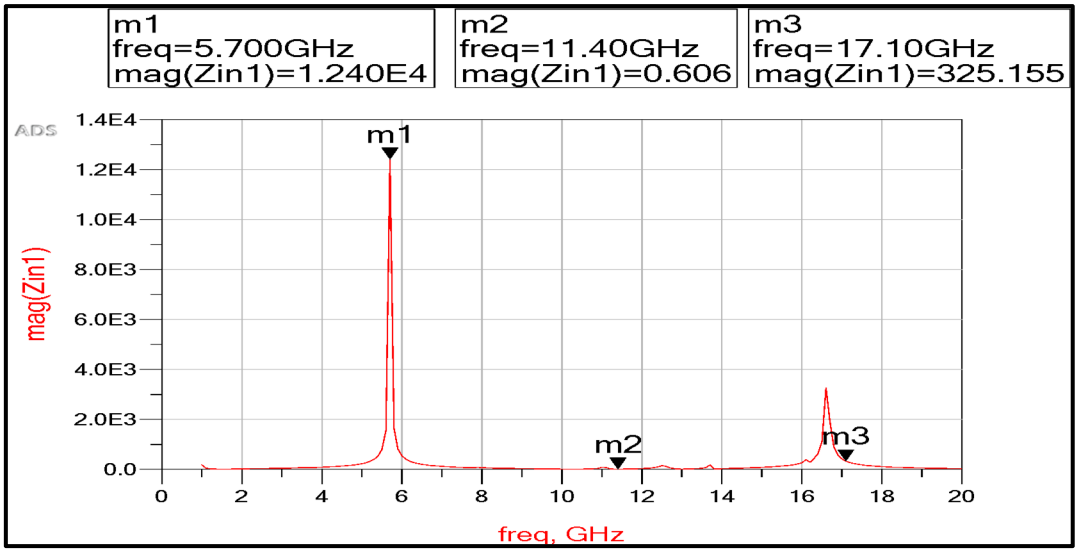

Figure 2.4 Resulting high impedance value for center frequency from simulation

Additionally, in $2f_0$ as well as $3f_0$, the quarter-wave line left node shows, respectively, a short circuit and an open circuit. Simulation results indicate that impedance goes to zero (or short circuit), as shown as m2 in Figure 2.13. Hence, while an open circuit in $3f_0$ gives impedance for this frequency, it is valued at 325Ω or significantly low compared to high impedance.

2.6 Transistor Analysis Using Nonlinear Model

Having the transistor nonlinear model available has made the design procedure much easier. This is because the main analyses (stability and DC) and the load pull simulations are performed with ADS on Agilent.

2.6.1 DC Analysis

According to the instructions for the CGHV1J006D ADS model, the valid range of gate voltage Vg is from -10 V to +2V . The valid range of drain voltage Vdd is from 0V to 140 V. Figure 2.5 below shows the simulated circuit for determining the bias point of the amplifier. Figure 2.6 shows a DC simulation based on transistor drain IV curves. The transistor's knee voltage measures approximately 20 V while the breakdown voltage measures around 140 V. In order to create a voltage swing from 20 V to 140 V, the drain voltage quiescent point needs to fall more or less in the middle of the two voltages. So, 40 V has been chosen as the quiescent point, having taken thermal issues into consideration and also wanting to maintain a certain distance from the breakdown region.

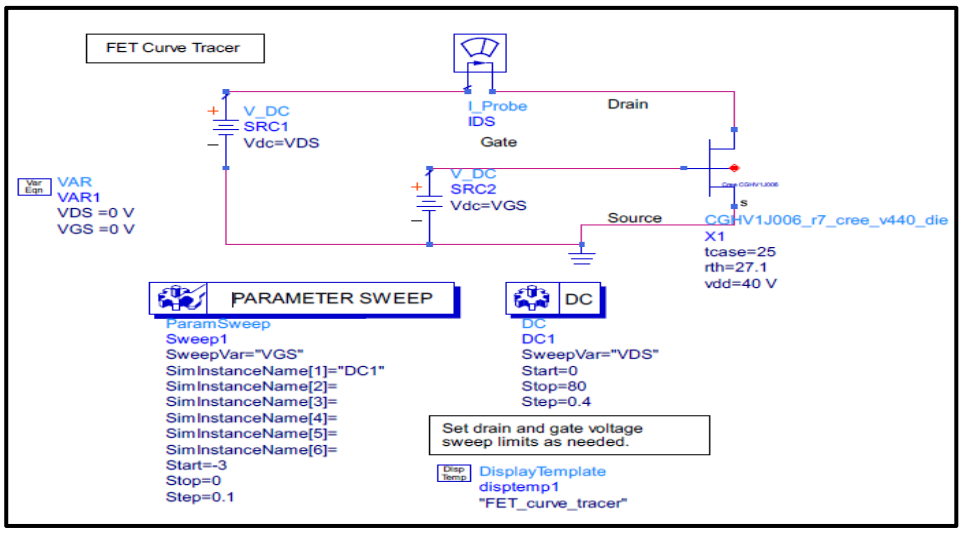

Figure 2.5 ADS schematic for determining DC bias condition of PA

As a Class F amplifier, The gate bias voltage of -2.6 V is picked as indicated by the marker m3. This bias point is chosen because of the small quiescent current of 45 mA through the transistor drain showing that the transistor is biased close to the cut-off region.

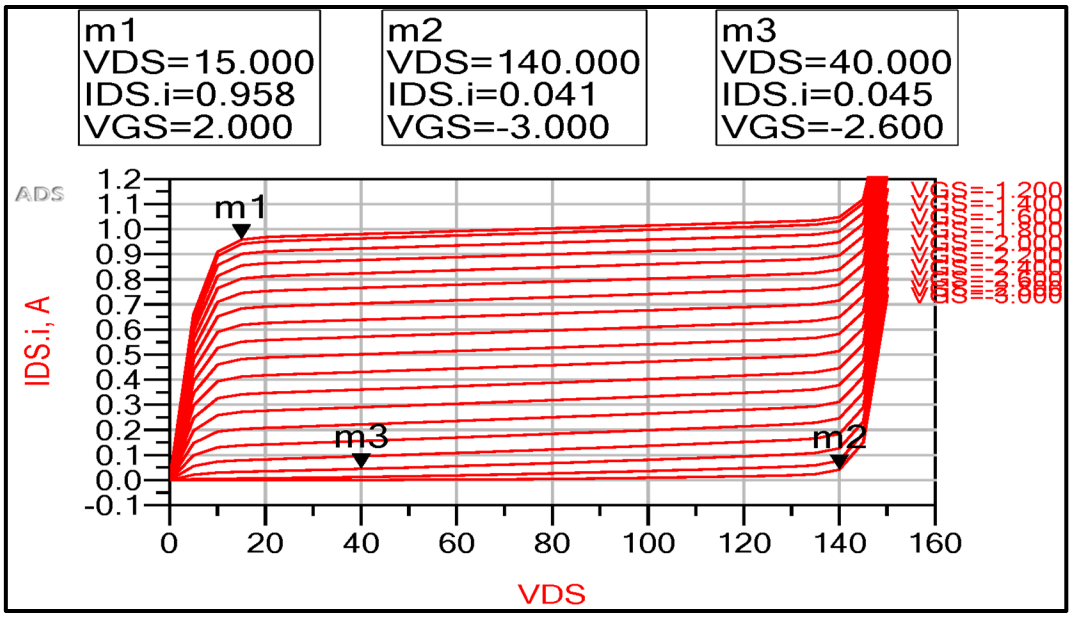

Figure 2.6 IV curves of the transistor

2.6.2 S-parameters Verification

After choosing a suitable DC bias condition, the next step is to verify the simulated S-parameters and compare with the set provided in the datasheet. There are S- parameters provided in the datasheet under two different DC bias conditions. In the datasheet, only the values of drain voltage and current are given for the measurement. Therefore, one should find the corresponding gate voltage in order to generate the same drain current in simulation. The transistor is terminated with 50ohms at the input and output. The 3 DC bias conditions verified in the simulation are shown below:

1st condition: Vds=40 v, Ids=30 mA ,Vgs=-2.65v

2nd condition: Vds=40v, Ids=60mA, Vgs=-2.5 v

Since the X-parameter file for large signal is not available from manufacturer. Small-signal S-parameters will be used instead during the design process. The ADS simulated S-parameters of the transistor under the two different DC bias conditions are shown in Table

3.3 and Table 3.4 The simulated S-parameters from the ADS model including the magnitude and phase are really close to the experimental S-parameters provided in datasheet. It can be assumed that the CGHV1J006D transistor model using S-parameters for computation is accurate enough so that the simulated results will be able to accurately describe the actual PA performance.

Table 2.4 Simulated s-Parameters with VDS=40V,VGS=-2.65,IDS=30mA

freq	mag(S(1,1))	phase(S(1,1))	mag(S(2,1))	phase(S(2,1))	mag(S(1,2))	phase(S(1,2))	mag(S(2,2))	phase(S(2,2))
500.0 MHz	0.987	-38.451	15.214	156.572	0.013	67.130	0.822	-14.030
1.000 GHz	0.962	-69.963	13.043	137.142	0.022	48.260	0.764	-25.262
1.500 GHz	0.940	-93.119	10.841	122.353	0.027	34.031	0.711	-33.669
2.000 GHz	0.925	-109.724	9.030	111.066	0.030	23.304	0.676	-40.387
2.500 GHz	0.915	-121.839	7.622	102.119	0.032	14.919	0.655	-46.264
3.000 GHz	0.909	-130.950	6.530	94.723	0.033	8.084	0.644	-51.720
3.500 GHz	0.906	-138.024	5.671	88.382	0.033	2.306	0.641	-56.929
4.000 GHz	0.904	-143.681	4.984	82.789	0.033	-2.724	0.642	-61.950
4.500 GHz	0.903	-148.323	4.423	77.747	0.033	-7.201	0.647	-66.798
5.000 GHz	0.903	-152.222	3.959	73.129	0.032	-11.254	0.654	-71.472
5.500 GHz	0.903	-155.561	3.568	68.846	0.032	-14.969	0.662	-75.969
6.000 GHz	0.904	-158.471	3.235	64.838	0.031	-18.408	0.671	-80.287
6.500 GHz	0.904	-161.047	2.949	61.060	0.031	-21.615	0.681	-84.424
7.000 GHz	0.905	-163.358	2.700	57.480	0.030	-24.621	0.692	-88.384
7.500 GHz	0.906	-165.454	2.483	54.072	0.029	-27.452	0.702	-92.170
8.000 GHz	0.908	-167.377	2.290	50.818	0.029	-30.128	0.713	-95.789
8.500 GHz	0.909	-169.156	2.120	47.702	0.028	-32.662	0.723	-99.246
9.000 GHz	0.910	-170.815	1.968	44.711	0.027	-35.068	0.733	-102.550
9.500 GHz	0.911	-172.374	1.832	41.833	0.026	-37.356	0.743	-105.707
10.00 GHz	0.912	-173.847	1.709	39.060	0.026	-39.536	0.752	-108.726
10.50 GHz	0.914	-175.248	1.599	36.384	0.025	-41.614	0.761	-111.615
11.00 GHz	0.915	-176.586	1.498	33.798	0.024	-43.597	0.770	-114.380
11.50 GHz	0.916	-177.871	1.407	31.295	0.023	-45.490	0.778	-117.029
12.00 GHz	0.917	-179.108	1.324	28.870	0.023	-47.300	0.786	-119.569
12.50 GHz	0.918	179.696	1.247	26.518	0.022	-49.030	0.794	-122.006
13.00 GHz	0.919	178.537	1.178	24.234	0.021	-50.684	0.801	-124.347
13.50 GHz	0.920	177.409	1.113	22.013	0.020	-52.266	0.807	-126.598
14.00 GHz	0.921	176.309	1.054	19.853	0.020	-53.778	0.814	-128.763
14.50 GHz	0.922	175.235	1.000	17.748	0.019	-55.224	0.820	-130.849
15.00 GHz	0.922	174.182	0.950	15.696	0.018	-56.605	0.826	-132.861
15.50 GHz	0.923	173.150	0.903	13.694	0.018	-57.922	0.831	-134.802
16.00 GHz	0.924	172.135	0.860	11.739	0.017	-59.179	0.836	-136.677
16.50 GHz	0.924	171.135	0.819	9.828	0.016	-60.374	0.841	-138.490
17.00 GHz	0.925	170.150	0.782	7.959	0.016	-61.510	0.845	-140.245
17.50 GHz	0.926	169.177	0.747	6.128	0.015	-62.586	0.850	-141.945
18.00 GHz	0.926	168.215	0.715	4.335	0.014	-63.601	0.854	-143.593

Table 2.5 Simulated s-Parameters with VDS=40V,VGS=-2.5,IDS=60mA

freq	mag(S(1,1))	phase(S(1,1))	mag(S(2,1))	phase(S(2,1))	mag(S(1,2))	phase(S(1,2))	mag(S(2,2))	phase(S(2,2))
500.0 MHz	0.984	-43.625	18.155	154.021	0.012	64.602	0.775	-15.640
1.000 GHz	0.956	-77.575	15.053	133.542	0.020	44.710	0.706	-27.314
1.500 GHz	0.935	-101.068	12.181	118.772	0.025	30.526	0.650	-35.506
2.000 GHz	0.922	-117.179	9.972	107.876	0.027	20.216	0.616	-41.924
2.500 GHz	0.914	-128.600	8.327	99.384	0.028	12.311	0.598	-47.582
3.000 GHz	0.909	-137.039	7.086	92.409	0.029	5.925	0.590	-52.903
3.500 GHz	0.906	-143.522	6.128	86.436	0.029	0.542	0.590	-58.027
4.000 GHz	0.905	-148.674	5.371	81.160	0.029	-4.143	0.594	-62.992
4.500 GHz	0.904	-152.888	4.759	76.391	0.028	-8.318	0.601	-67.796
5.000 GHz	0.904	-156.423	4.254	72.007	0.028	-12.106	0.610	-72.432
5.500 GHz	0.905	-159.451	3.832	67.928	0.028	-15.588	0.620	-76.890
6.000 GHz	0.905	-162.093	3.474	64.096	0.027	-18.818	0.631	-81.167
6.500 GHz	0.906	-164.436	3.167	60.474	0.027	-21.836	0.643	-85.262
7.000 GHz	0.907	-166.542	2.900	57.030	0.026	-24.671	0.655	-89.178
7.500 GHz	0.908	-168.458	2.667	53.742	0.025	-27.346	0.667	-92.919
8.000 GHz	0.909	-170.219	2.462	50.594	0.025	-29.877	0.679	-96.493
8.500 GHz	0.910	-171.854	2.280	47.572	0.024	-32.277	0.690	-99.906
9.000 GHz	0.911	-173.384	2.117	44.664	0.023	-34.558	0.702	-103.167
9.500 GHz	0.913	-174.826	1.972	41.860	0.023	-36.727	0.713	-106.283
10.00 GHz	0.914	-176.193	1.841	39.153	0.022	-38.793	0.723	-109.262
10.50 GHz	0.915	-177.496	1.723	36.535	0.021	-40.762	0.734	-112.112
11.00 GHz	0.916	-178.745	1.615	34.001	0.021	-42.639	0.743	-114.841
11.50 GHz	0.917	-179.947	1.518	31.545	0.020	-44.429	0.753	-117.456
12.00 GHz	0.918	178.892	1.428	29.161	0.019	-46.136	0.762	-119.964
12.50 GHz	0.919	177.766	1.347	26.845	0.019	-47.763	0.770	-122.371
13.00 GHz	0.920	176.671	1.272	24.594	0.018	-49.313	0.778	-124.684
13.50 GHz	0.921	175.604	1.203	22.402	0.017	-50.789	0.786	-126.909
14.00 GHz	0.921	174.561	1.140	20.267	0.017	-52.192	0.793	-129.050
14.50 GHz	0.922	173.539	1.082	18.186	0.016	-53.524	0.800	-131.114
15.00 GHz	0.923	172.536	1.028	16.154	0.016	-54.787	0.806	-133.104
15.50 GHz	0.924	171.550	0.978	14.170	0.015	-55.980	0.812	-135.026
16.00 GHz	0.924	170.578	0.931	12.231	0.014	-57.104	0.818	-136.883
16.50 GHz	0.925	169.620	0.888	10.334	0.014	-58.157	0.824	-138.679
17.00 GHz	0.925	168.673	0.848	8.476	0.013	-59.140	0.829	-140.419
17.50 GHz	0.926	167.736	0.810	6.657	0.013	-60.049	0.834	-142.105
18.00 GHz	0.927	166.808	0.775	4.873	0.012	-60.883	0.839	-143.740

2.6.3 Stability Analysis and Stabilize The Transistor

The early design stages of a PA should focus on stability analysis. This is because the active device's S-parameter response is a function of bias points, which means that stability issues need to be simulated according to operating bias conditions.

Figure 2.7 shows the MAG and k-factor, configured here as a function of frequency. In order to find the regions that will likely be unstable, the stability analysis step has to be performed starting with low frequencies and moving up to high frequencies. Because the k-factor is framed as a stability criterion, the circuit stabilizes as the k-factor increases, but there is still an inverse proportionality between the MAG and k-factor. In fact, the k-factor needs to remain around 1 on the frequency band of interest while staying relatively large out of band in order to obtain high gain while preventing out-of-band oscillations. Figure 3.5 illustrates the stability of the active device only over 8.2 GHz. Consequently, a stability circuit is needed to provide stability across the other frequencies.

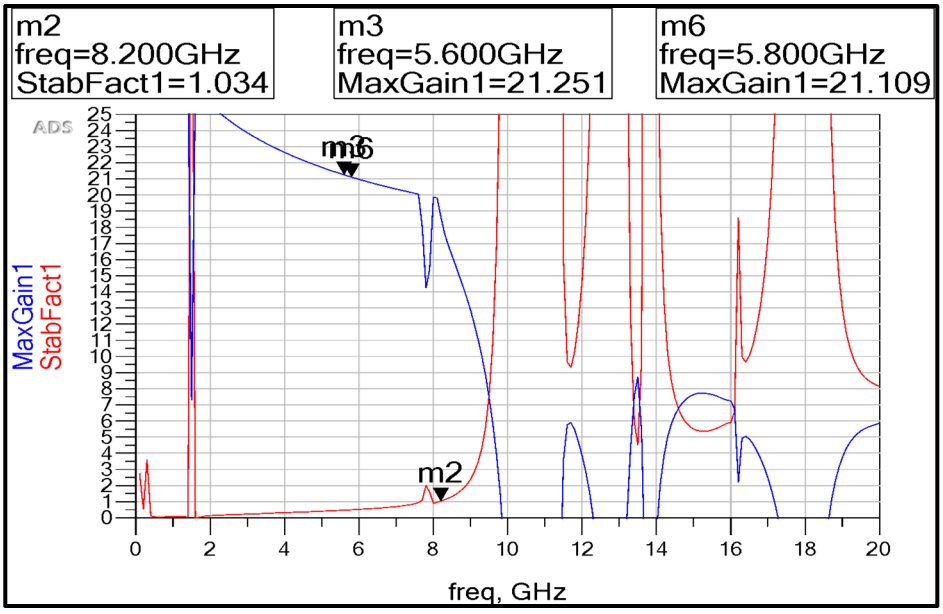

Figure 2.7 The k-factor and maximum available gain

Stability networks are able to maintain stability across frequencies through utilizing resistance against matching networks. Stability circles can be used to find the resistance value required by an active device to create unconditional stability. Figure 2.8 presents the input and output stability circles for an active device. As can be seen, the stability circles show is the device as being unstable when inside the stability circles but stable when at other areas in the Smith chart. In order to achieve stability across frequencies, the stability circles need to go beyond the chart, which would give the device not only added resistance in low frequencies but also low resistance in high frequencies. Thus, by expanding to include any necessary series resistances, impedance values on the input side of the active device would be confined with so-called safe regions on the chart.

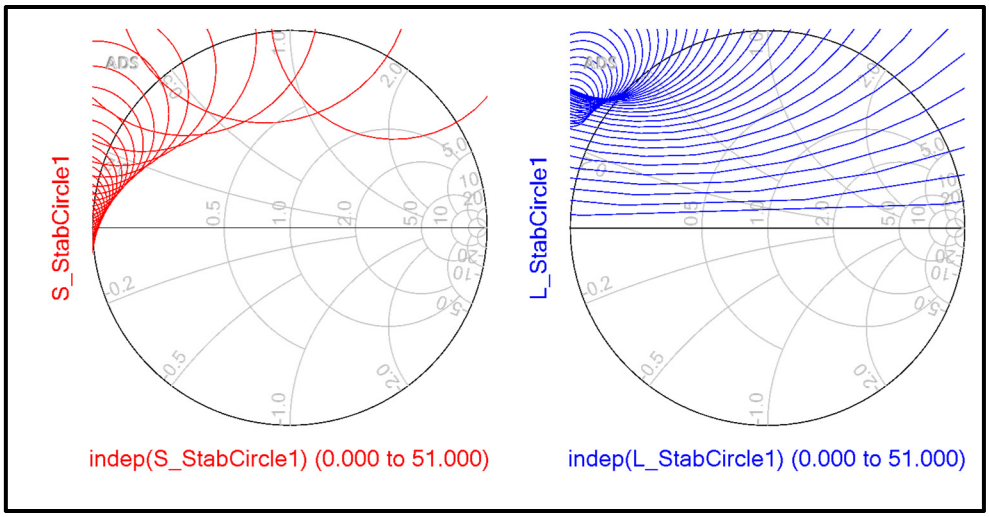

Figure 2.8 Input and output stability circles

Intentional loss is added to the PA in order to stabilize it. With this in mind, stability network need to give high gains along with unconditional stability. To achieve this, the maximum available gain and stability factor have to be watch closely to prevent loss of control in the loss frequency band of interest's loss level. Figure 2.9 depicts an ideal circuit in relation to unconditional stability. As can be seen, it is basically a parallel connected RC circuit.

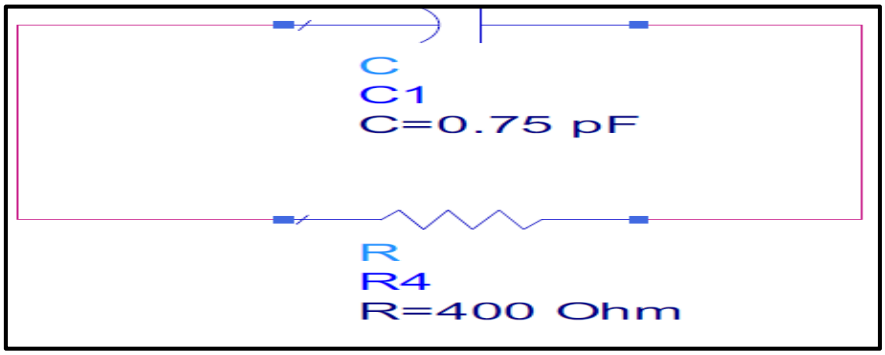

Figure 2.9 Proposed ideal stability network

Next, Figure 2.10 illustrates the maximum available gain and stability factor, but the circuit elements are ideal and there are no parasitic elements in the network. On the contrary, the actual model does reveal some parasitic capacitances and inductances as well as some resistances between the elements and the ground layer. Moreover, the capacitors and

inductors create resonant frequencies which could lead to high loss. All of these circumstances point to the necessity of having an actual 3D model with a simulated circuit that has all of the parasitic effects mentioned above. Such a model would be able to show actual circuit response.

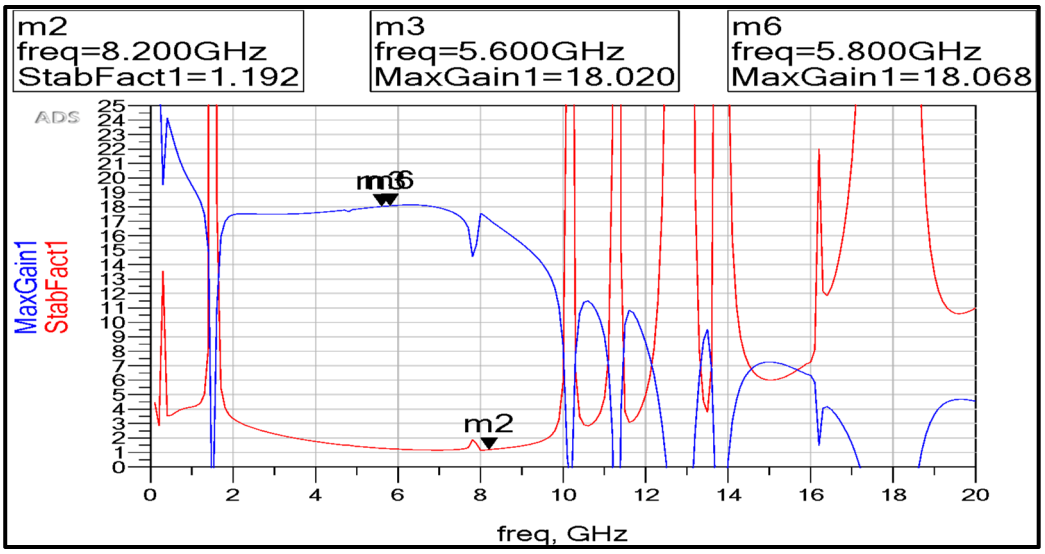

Figure 2.10 k-factor and maximum available gain with ideal network

The constructed 3D model of the proposed ideal network is shown in Figure 2.11. Instead of ideal capacitor, printed capacitor was used. The bottom side of the capacitor is printed to the fourth layer of microstrip and connected to the circuit using vias and upper side is printed to the fifth layer of microstrip under the physical resistor and connected to the circuit using vias. The resistor is modeled as a KOA resistor. Gate bond wires between stability network and transistor die is also included in the stability network model to have a better accuracy.

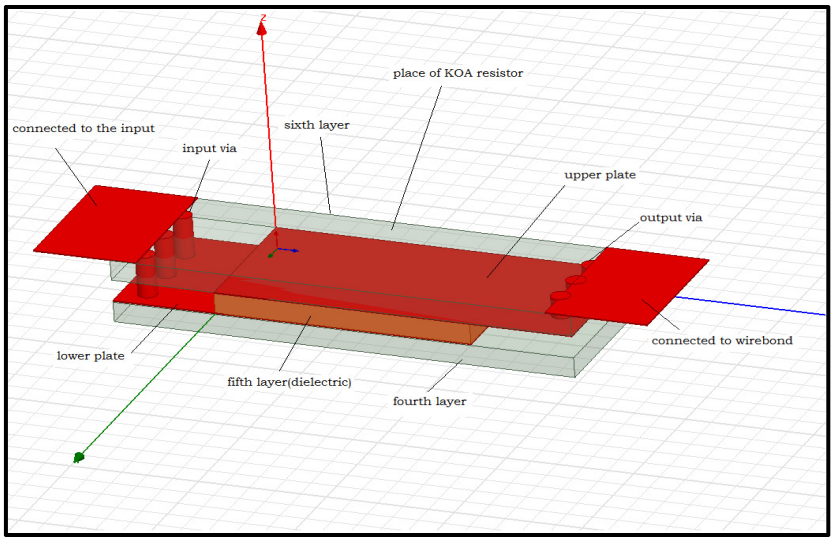

Figure 2.11 3D capacitor

Figure 2.12 shows the simulation result of the capacitor built in figure 2.11 using ANSYS. as shown in the figure the value of capacitor is 0.76 pf it is close to the value that we simulated before in stability network (figure 2.7) and give the same result.

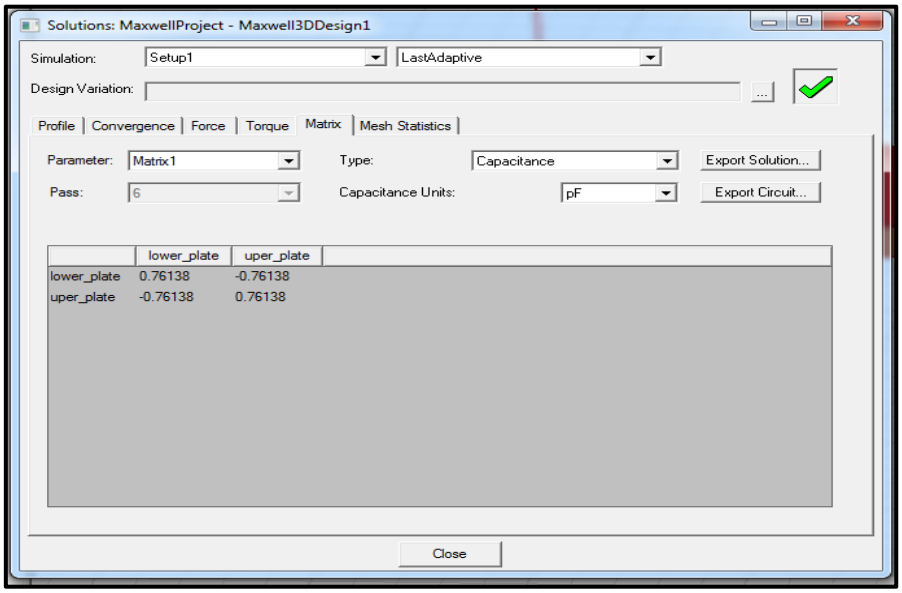

Figure 2.12 Simulation result of figure 2.9

2.7 Power Amplifier Design

The design and simulation are done by using Advanced Design System (ADS) from Agilent. There are some important features provided by ADS that enable Class F amplifier simulation:

- **Load-pull / Source-pull Analysis** - Determines the optimum source and load impedance terminations at the fundamental and harmonic frequencies;
- **Harmonic balancing** – Simulates the circuit using non-linear transistor model with harmonics taken into account;
- **Schematic optimization**- Optimizes the value of discrete components such as capacitors and inductors, and also distributed element values such as transmission line length and width based on the requirement specified by the designer;
- **Momentum EM simulation** - A planar electromagnetic (EM) simulator, which simulates the circuit with electromagnetic coupling and radiation taken into account. The simulated results of Momentum are expected to be more accurate than those of schematic simulation. However, it takes much longer computational time to simulate than schematic simulation does;
- **Momentum Optimization** - The schematic of a component can be transformed from the layout and used in Momentum optimization. This feature is especially useful when designing distributed element filters;

2.7.1 Multi Harmonicas Source-Pull and Load-Pull Analysis

In this work, third harmonic peaking configuration will be used due to the negligible improvement from terminating higher order harmonics. Thus, only second and third harmonic will be controlled at both the input and output for shaping the waveforms.

After determining the DC bias condition and analyzing the stability circles, computing the optimum source and load termination impedances for harmonics and the fundamental signal will be the next. According to the competition rules, PAE is the only metric used to evaluate

the PA performance. Therefore, each participant should only concentrate on designing input and output networks that generate the highest PAE while keeping the termination impedances out of the unstable region.

One of the features of ADS is source / load-pull analysis, which allows designer to determine the optimum source and load termination impedances in order to maximize the performance in terms of PAE, (Mengistu, 2008). This feature doesn't just compute the impedance for the fundamental signal, but for all involved harmonics being controlled. The source/load-pull simulator treats all impedances as variables in terms of the reflection coefficient S11. During the process, the simulator sweeps S11 within a specified circular region with a certain number of sweeping points, radius /center of the region and the system impedance [9]. Then, the simulator will calculate the PAE and output power for every swept point and generates the PAE and output power contour plot. The procedure of source/load pull analysis will be demonstrated next to determine the optimum termination impedances for the fundamental tone, second and third harmonics.

The procedure of source-pull and load-pull analysis for harmonics and fundamental is outlined below.

1. Initially, set the second harmonic load impedance to a low impedance such as 0.01Ω. Set the third harmonic load impedance to a high impedance such as 2500Ω. Set all other harmonic impedances to 50Ω. Perform load-pull analysis for the first harmonic;
2. Set the second harmonic source impedance to a low impedance such as 0.01Ω. Set the third harmonic source impedance to a high impedance such as 2500Ω. Set the first harmonic load impedance computed in step 1 and perform source-pull analysis for the first harmonic;
3. Set the first harmonic source impedance computed in step 2 and perform load-pull analysis for the first harmonic;
4. Repeat step1, step2 and step3 up to there is no change in PAE. After that fixed first harmonic load impedance and first harmonic source impedance;
5. Set the second harmonic load impedance to 50Ω. Perform load-pull analysis for the second harmonic;

6. Set the second harmonic source impedance to 50Ω. Set the second harmonic load impedance computed in step 5 and perform source-pull analysis for the second harmonic;
7. Set the second harmonic source impedance computed in step 6 and perform load-pull analysis for the second harmonic;
8. Repeat step5, step6 and step7 up to there is no change in PAE. After that fixed second harmonic load impedance and second harmonic source impedance;
9. Set the third harmonic load impedance to 50Ω. Perform load-pull analysis for the third harmonic;
10. Set the third harmonic source impedance to 50Ω. Set the third harmonic load impedance computed in step 9 and perform source-pull analysis for the third harmonic;
11. Set the third harmonic source impedance computed in step 10 and perform load-pull analysis for the second harmonic;
12. Repeat step9, step10 and step11 up to there is no change in PAE. After that fixed third harmonic load impedance and third harmonic source impedance;

After all steps are completed, the input and output impedances for the fundamental tone and second and third harmonics can be determined based on the harmonic input and output impedances computed in step 4 and step 8 and step 12 above. Figure 2.13 show the PAE contours (blue) and the output power contours (red) as the results of source/load-pull analysis for step 12.

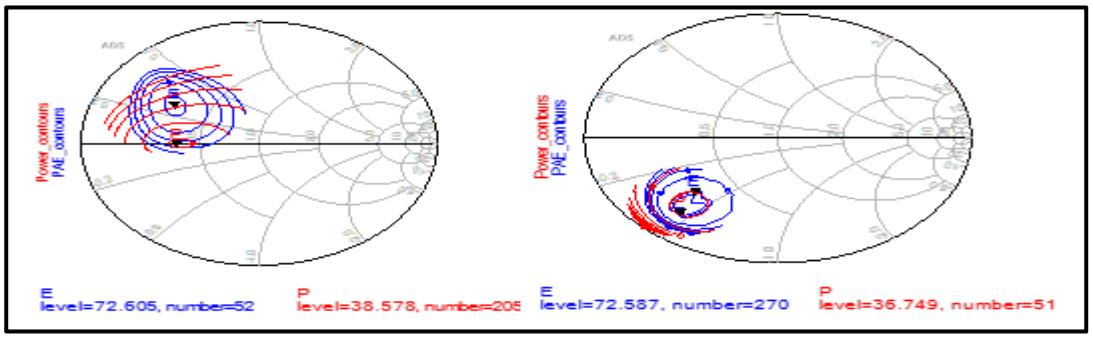

Figure 2.13 The PAE contours and the output power contours as the results for step 12

Table 2.6 summarizes input and output impedance values. Using these impedances, it is expected to reach a PAE higher than 72.605 %.

Table 2.6 Input and output impedances

Frequency	Load impedances	Source impedances
fundamental	14.733+j*13.815	5.707-j*3.013
Second harmonic	0.0.001-j*18.472	0.0005-j*62.248
Third harmonic	0.141-j*97.346	0.095+j*110.175

2.7.2 Wave Shaping Networks

The wave-shaping network is a sub-network used to shape a particular voltage and current waveforms at the transistor drain or gate by terminating harmonics with specified impedances. In Class F amplifiers, the output wave-shaping network should shape a square waveform for the voltage and a half-sine waveform for current at the transistor drain. Moreover, a distorted sine voltage waveform should be seen at the gate because of the existence of the second and third harmonics.

As shown in Figure 2.14, the Class F amplifier is composed of the input/output sub-matching networks and the input/output wave-shaping networks, which are part of the matching-networks. The wave-shaping networks must be taken into account when performing the source/load-pull analysis for the fundamental tone.

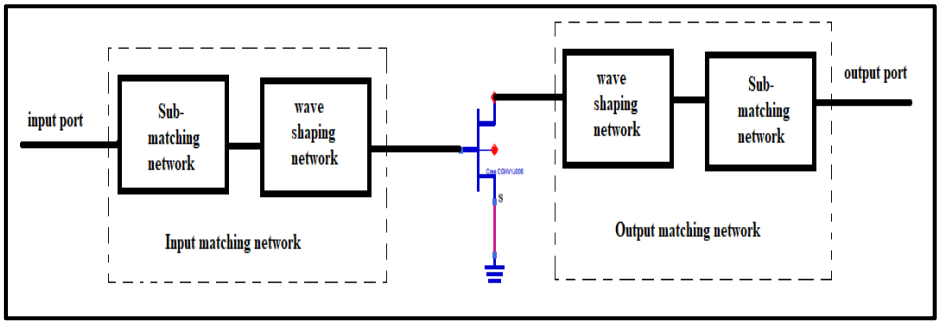

Figure 2.14 Block diagram of input and output matching network

2.7.2.1 Output Matching Network

The output matching network used in this work is illustrated in Figure 2.15. As can be seen, the network enables load-matching at fundamental frequencies and at 2nd / 3rd harmonics. Furthermore, the length or width of the lines can be determined through isolating short circuit conditions for second and third order harmonics. Because a λ/12 wavelength open stub for fundamental frequencies has been applied here, we can get a short circuit from the third harmonic on point A. In so doing, the circuit's other portion, such as the left part, has no impact on third harmonic impedance. Because length L1 can create impedance near ZL3, we apply an additional quarter wavelength grounded stub for the fundamental frequency. Next, we get a short circuit for the second harmonic for point B. Length L2 has been chosen to get impedance near ZL2. Thus, in creating an optimal load for the fundamental frequency, we need to add a sub-matching network. However, when designing the sub-matching network, it is important to keep in mind the impacts of circuits needed to create second and third load impedances.

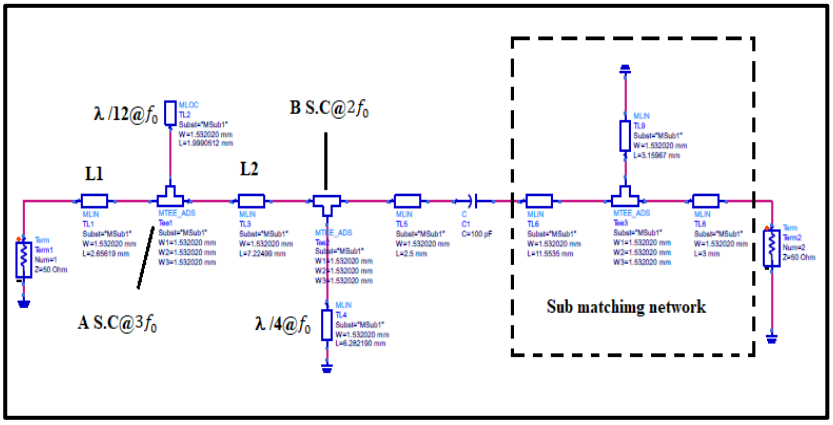

Figure 2.15 Output matching network

In Figure 2.16, we can see the outcome from the previous figure's output matching network. Using adequate tuning, we got impedances quite near in value to what was needed for: fundamental frequency (ZL1), 2nd harmonic (ZL2) and third harmonic (ZL3).

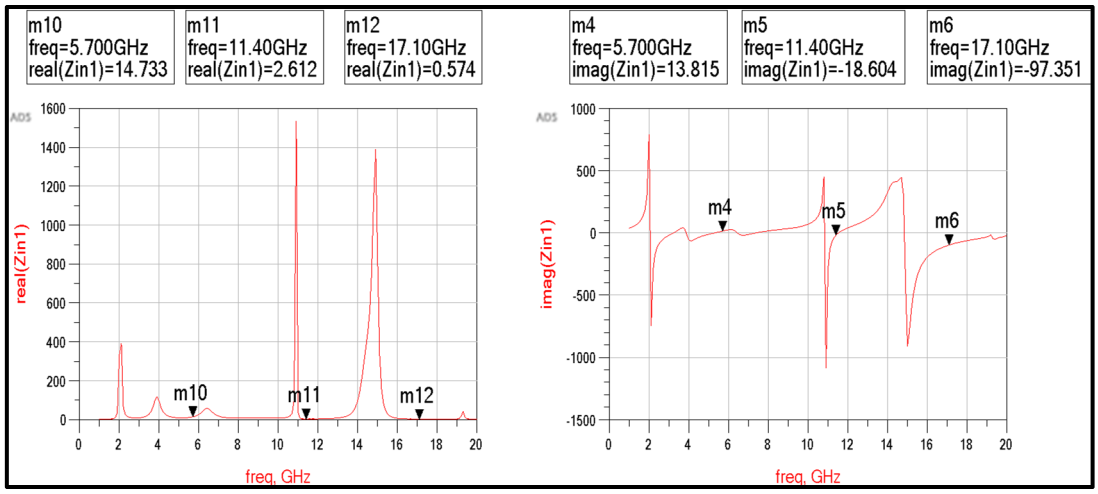

Figure 2.16 Output matching network response

2.7.2.2 Input Matching Network

In creating our input matching network, we employed a technique very similar to the one we employed when designing the output matching network. Accordingly, open and grounded stubs (quarter wavelength) were utilized and short circuits on $3f_0$ as well as $2f_0$ were gained, respectively, on point D and point C. Next, we chose transmission lines lengths that could create source second and third harmonic impedances. To get the necessary source impedance for the fundamental frequency, we chose to include an input sub matching network. The input matching network is depicted in detail in Figure 2.17.

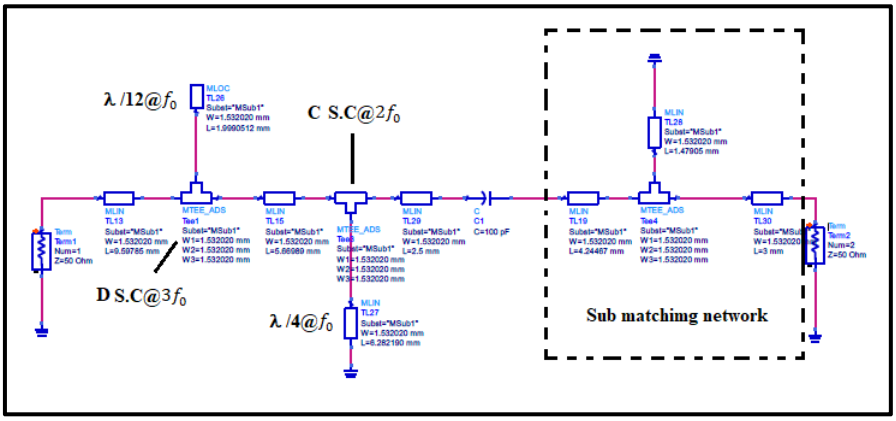

Figure 2.17 Detailed input matching network

The response of the input matching network is depicted on Figure 2.18. The obtained impedances are very close to the source impedances of Table 2.6.

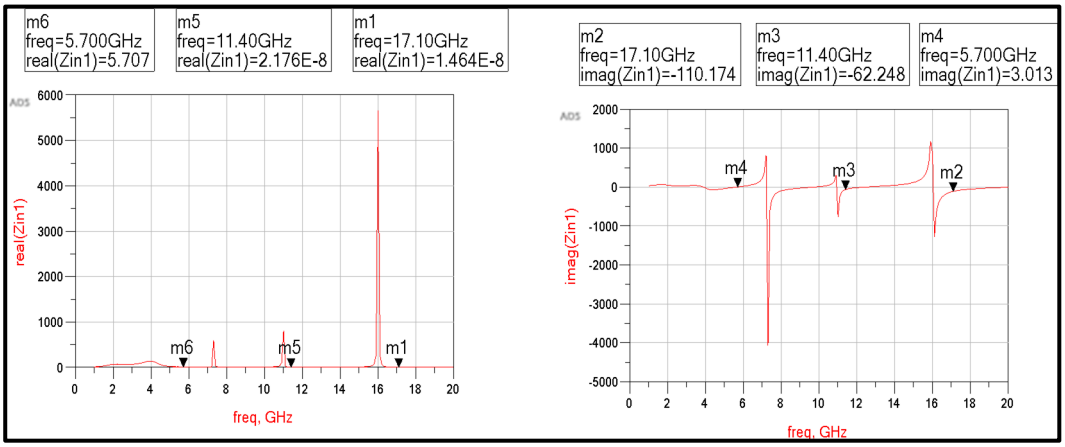

Figure 2.18 Input matching network response

2.8 Simulation Results

When the design process of the matching networks, stability and bias networks are finished, the circuit blocks are connected to each other to simulate the complete PA as shown in Figure 2.19.DC block capacitors are positioned on all sides of the amplifier, the purpose of these capacitors is to block any DC component in the incoming and outgoing signals, and thus to permit the propagation of RF signals only.

The nonlinear model of the transistor provides the capability of realizing nonlinear simulations such as output power, harmonic distortion.

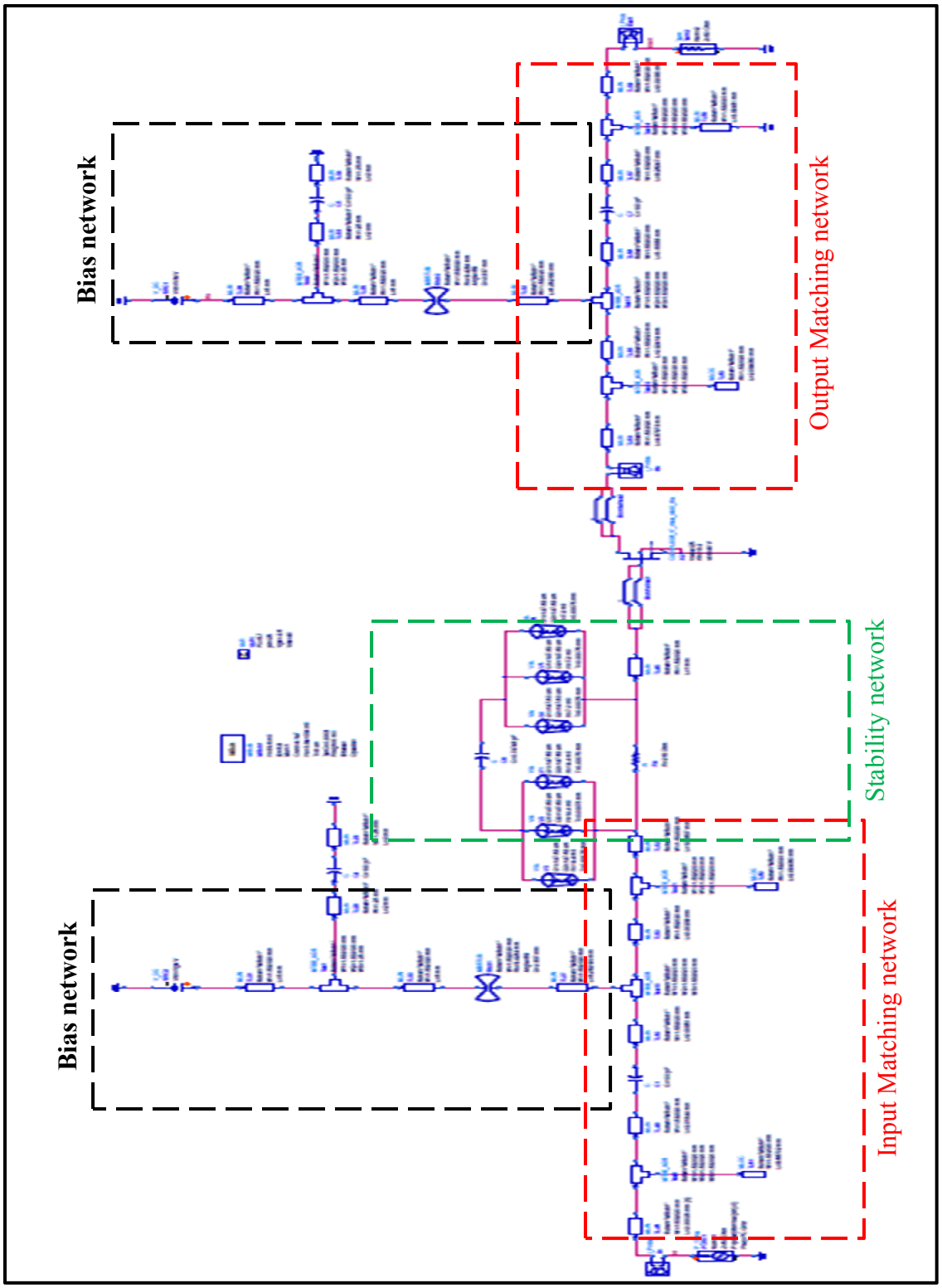

Figure 2.19 Full power amplifier design

2.8.1 One Tone Simulation of Power Amplifier

Figure 2.20 shows small signal simulation outcomes for the PA. As can be seen, the amplifier's gain stands at around 18.380 dB for center frequencies. Additionally, the PA input return loss value exceeds -10 dB, while the output return loss value measures around -23.998 Db.

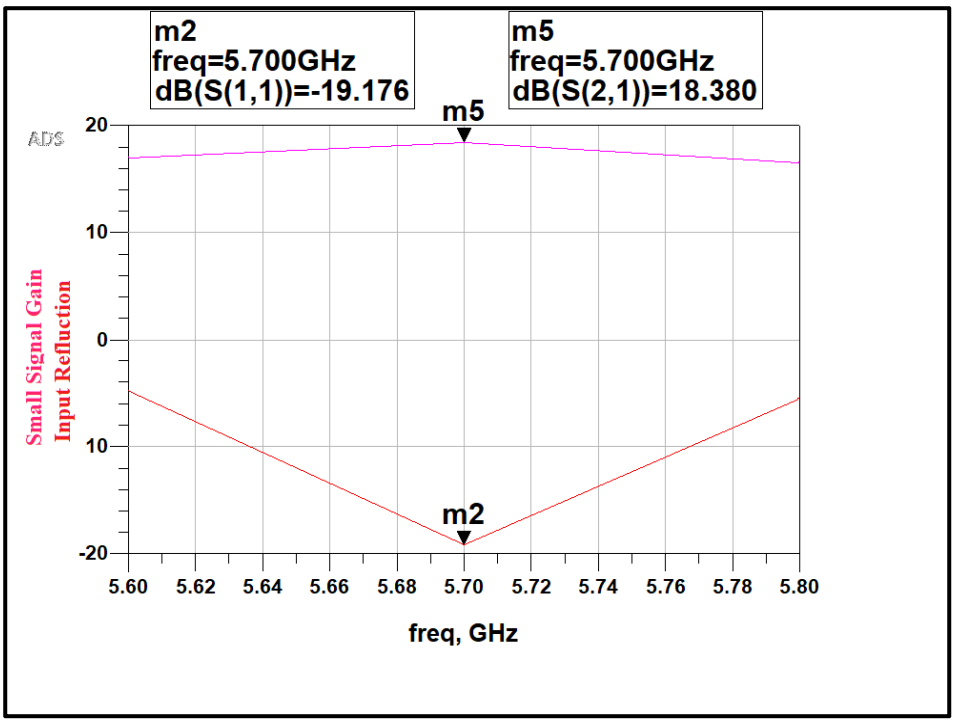

Figure 2.20 Simulated small signal parameters

Figure 2.21 depicts measurements for power gain, percentages of PAE and output power. Input power remains constant (25 dBm) across the frequencies, with power gain measuring 12 dB (m19), PAE measuring around 68% (m17), and output power measuring 37 dBm (5.23 W) (m18).

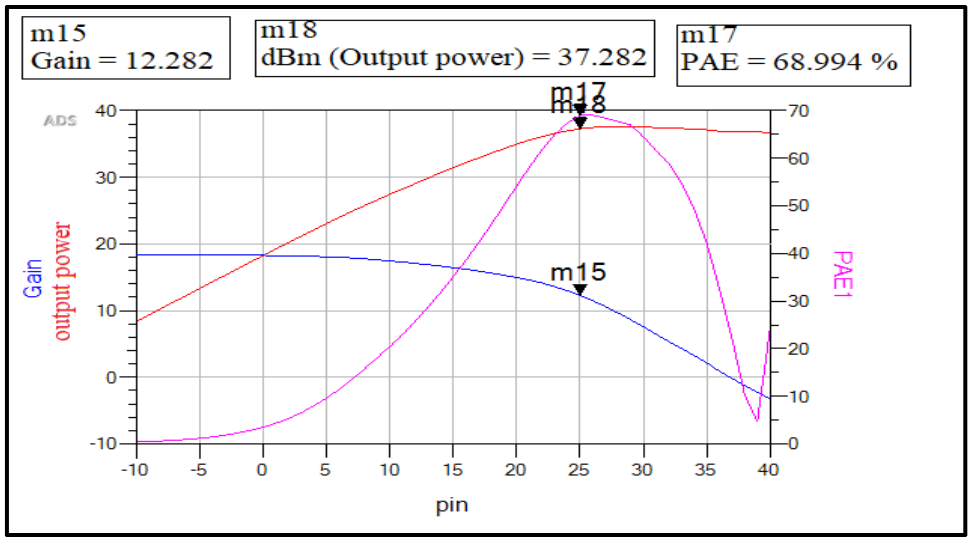

Figure 2.21 output power, PAE (%) and power gain at 25 dBm input power

The parameter of harmonic distortion provides data on a PA's nonlinearity. Figure 2.22 shows the second harmonic level at the 5.7 GHz fundamental frequency. Working from Equation (1-13), we can formulate second and third harmonic distortions as expressed below:

$$HD2nd, dB = 37.282 - 6.112 = 31.17$$

$$HD3th, dB = 37.188 - 8.410 = 28.774$$

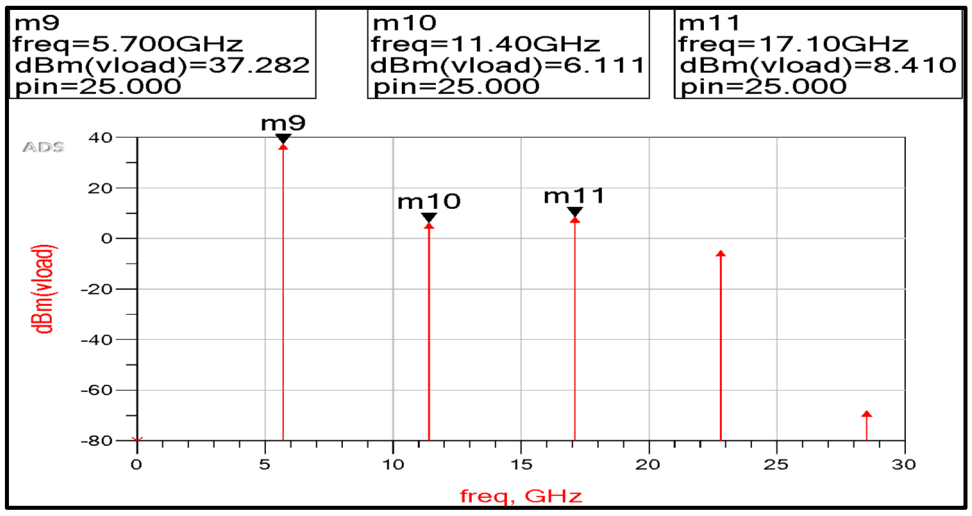

Figure 2.22 Simulated second and third harmonic distortion

Such a high value of PAE is reached based on shaping the drain voltage and current waveforms. Figure 2.23 shows that the overlapping area between these two curves is minimised. This explicit class-F behavior of the designed PA allows to reduce the DC power dissipated in the transistor and hence improve the device efficiency.

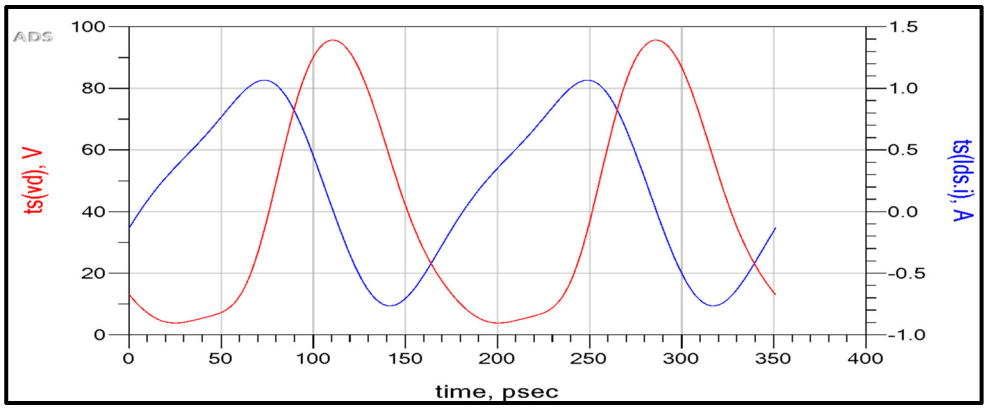

Figure 2.23 Drain voltage (red) and current (blue) waveforms

The simulated output power as a function of the input power is shown in figure 2.24. The small signal gain of the designed class-F PA is approximately equal to 18.380 dB. The PA starts to compress at 5 dBm (m19) as input power. Its P-1dB is approximately equal to 12 dBm. The compression point corresponding to the input power where the PAE is maximum Pin =25 dBm is 6.088dB.

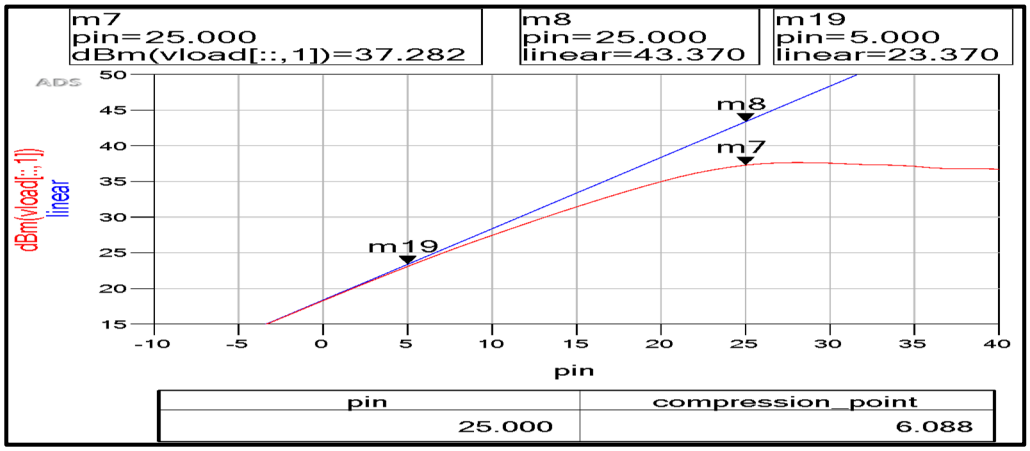

Figure 2.24 Output power versus input power

The relationship between input power in watt and output power in watt and DC power in watt is shown in figure 2.25. as shown in figure there is approximately 2 watts dissipated as heat, this value we will treat it in the next chapter. Also from the figure we can calculate the drain efficiency using equation 1-4, the drain efficiency is equal 73.56%

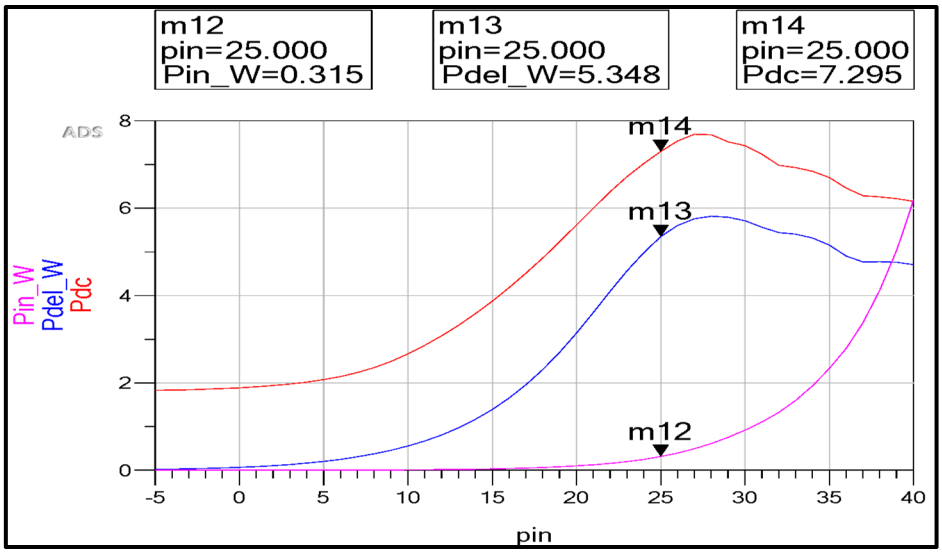

Figure 2.25 input, output and DC power

2.8.2 Two Tone Simulation of Power Amplifier

Two tone simulations of amplifiers is recommended analysis to find out IMD performance of the designed power amplifier which also provides clear indication of ACPR (adjacent channel power rejection) in case of modulated signal.

IMD occurs when more than one input frequency component is present in the PA input. Two tone simulations are generally performed with two closely spaced input frequencies. In two tone test the frequency spacing is swept between the input tones. 5.7 GHz is our fundamental RF signal, assume the spacing is 20 MHz so the two frequencies are:

$$F1 = \text{RF frequency} - \text{f spacing}/2 = 5700 - 20/2 = 5.69 \quad (2.1)$$

$$F2 = \text{RF frequency} + \text{f spacing}/2 = 5700 + 20/2 = 5.71 \quad (2.2)$$

With the input power value set at 19 dBm (6 dBm below our 1-tone input power), Figure 2.26 shows inter modulation products up to the 7th order. Here (f1+f2) is second order, (2f1-f2) is third order, (3f1-2f2) is fifth order, and so on.

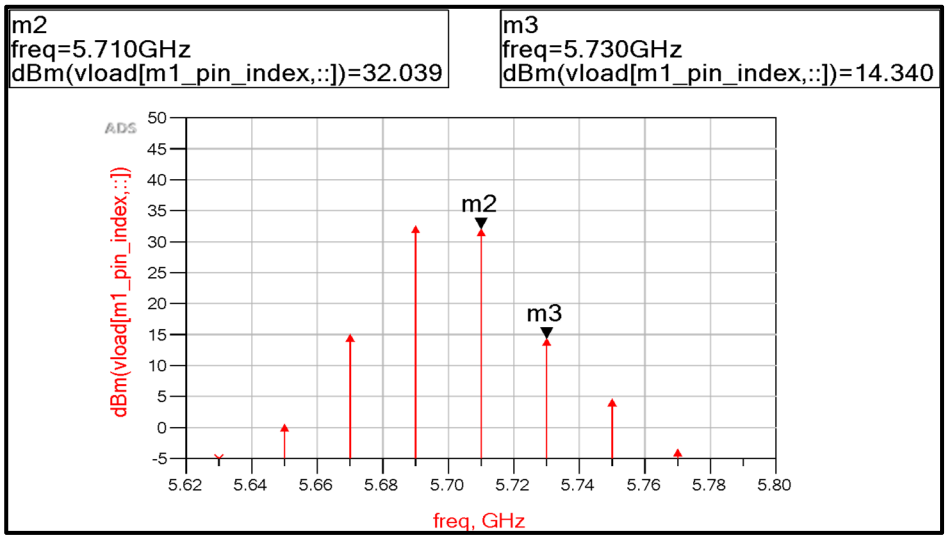

Figure 2.26 Intermodulation products of two tone simulation

From the figure we can calculate:

IMD = m2-m3 = 17.699 (-17.699 dBc)

IIP3 = pin + IMD/2 = 25 + 8.8495 = 33.84

2.8.3 Modulated Signal Analysis of Power Amplifier

Automatic verification and Ptolemy co-simulation modeling are employed here to obtain data for the desired power output. QPSK modulation will be used for signal modulation. In quadrature phase-shift keying (QPSK), which is a type of phase-shift keying where two bits can be modulated simultaneously, one in potentially four carrier phase shifts (i.e., 0, 90, 180, and 270 degrees) can be selected. Using QPSK, the signal can hold double the amount of

data compared to a conventional PSK. A QPSK source schematic for the PA is illustrated in Figure 2.27 below:

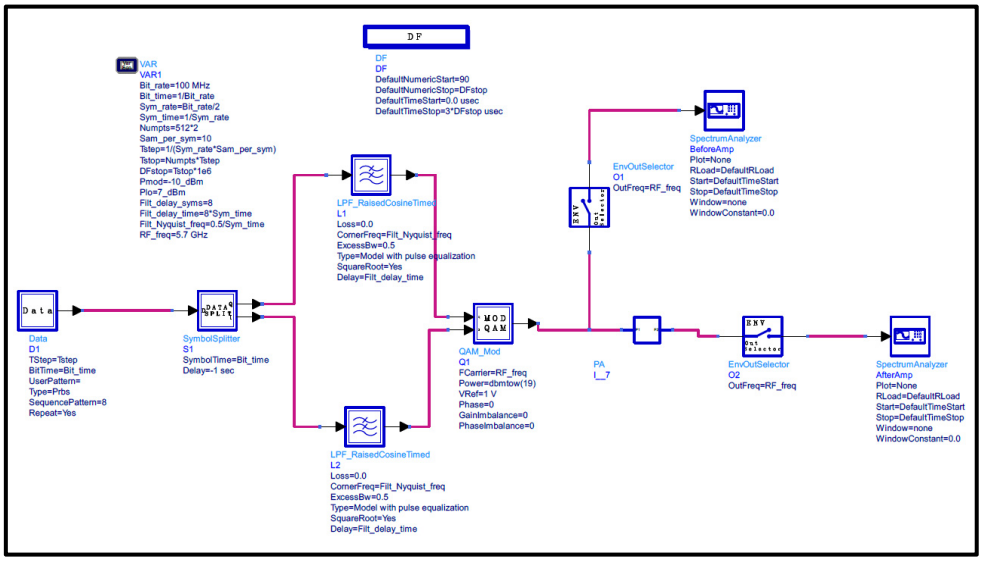

Figure 2.27 QPSK source schematic and power amplifier

The screens of the two-spectrum analyzer before the power amplifier and after the power amplifier are shown in figure 2.28

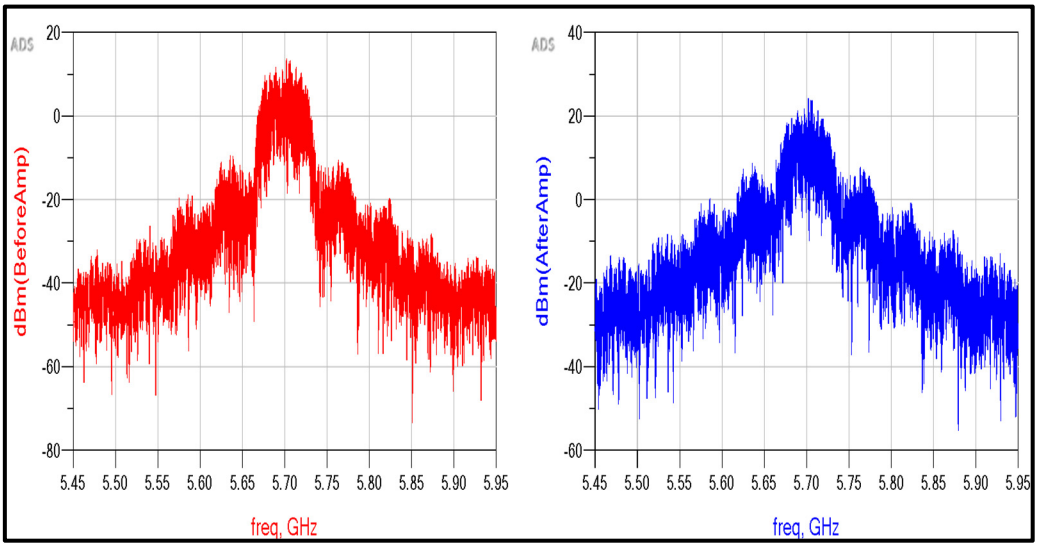

Figure 2.28 before(red) and after(blue) power amplifier modulated signal

ACPR is a key metrics for Wireless modulated signals and this gives the power in adjacent band of the operating PA. Figure 2.29 shows the equations and the values of ACPR.

Eqn Adj_Ch_Lower=spec_power(dBm(AfterAmp),5.55GHz,5.65GHz)

Eqn Adj_Ch_Upper=spec_power(dBm(AfterAmp),5.75GHz,5.85GHz)

Eqn ACPR_Lower=PA_OP_Power-Adj_Ch_Lower

Eqn ACPR_Upper=PA_OP_Power-Adj_Ch_Upper

PA_IP_Power	PA_OP_Power	ACPR_Lower	ACPR_Upper
29.045	39.061	16.336	16.535

Figure 2.29 ACPR values

2.9 Layout Generation and Momentum Simulation

After verifying the impedances in schematic, the circuit layout in Figure 2.30 can be directly translated from ADS schematic. Note that metal pads have been added in the layout as ground plane and power supply connection in the layout.

Next, the EM simulator Momentum can be used to accurately calculate the input and output impedances with electromagnetic coupling effect taken into account. First, all capacitors, resistors and grounds must be removed in the schematic before the layout is generated. Then, port terminations are defined using port editor in the layout with specified termination impedances. Ports with low impedance, for example 0.001Ω, are used to replace all grounds. Ports with 50Ω are used as RF input and output terminations.

There are 2 simulation models; Microwave mode and RF mode can be selected in Momentum. Microwave mode is only used when designs require full-wave electromagnetic simulation that involves radiation effects. The RF mode is used for designs that are geometrically complex, but do not radiate. The RF mode provides much faster computation than Microwave mode does. In this work, RF Mode was chosen instead of Microwave mode for faster computation since this power amplifier is assumed to not radiate.

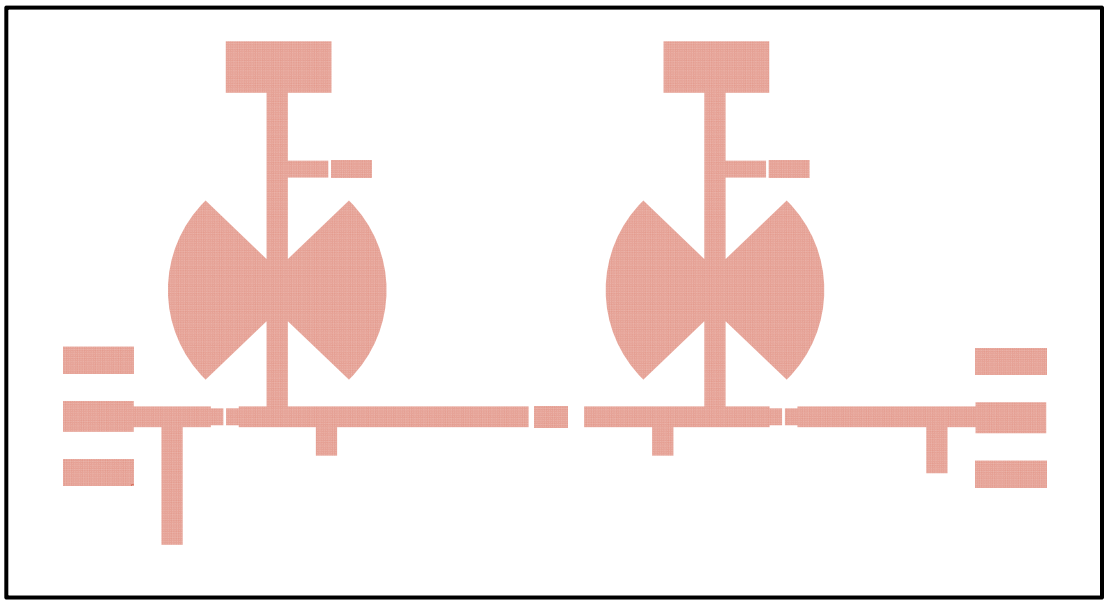

Figure 2.28 Layout of the power amplifier

CHAPTER 3

THERMAL DESIGN OF CLASS F POWER AMPLIFIER

3.1 Introduction

When laying the groundwork for developing a power amplifier, designers should include prototyping along with electrical design. Consideration should be given to elements like how to attach the active device to LTCC and the heatsink, what type of RF connectors are most suitable, metal housing, and thermal precautions. Deciding on the design of the metal heatsink can be especially crucial because this element serves a number of important purposes, such as electrically isolating the power amplifier from interference signals, acting as infrastructure for various components (e.g., supply circuits and RF connectors used to construct the PA module), and dispersing and/or transferring any PA-produced heat. Heatsinks are commonly made from aluminum because that material is lightweight, inexpensive, and easy to process; it also has good thermal and electrical conductivity. In the majority of cases, the aluminum intended for heatsinks is often plated with a gold or silver layer, along with a nickel seed layer between them, (Walker , 2012).

Figure 3.1 depicts what a standard thermal stack-up looks like. As can be seen, the heatsink transforms heat to amps via surface touch. Then, when the material's thermal conductivity rises and thermal resistance decreases, the heat moves faster, lowering the transistor junction's equilibrium temperature. Along with thermal conductivity, i.e., thermal resistance, the heatsink material's density is likewise crucial because denser materials have greater thermal capacitance, producing faster heat transference. At the same time, however, consideration should be given to weight. In fact, the overall weight of the module is directly tied to the type of heatsink material used. So, for example, compared to aluminum, copper displays relatively high thermal conductivity and higher density, but copper is also cost more than aluminum and increases the PA module's weight. Because of weight restrictions and other factors, the material chosen for heatsinks must be suitable for the intended applications.

To attach LTCC and active devices to heatsinks, industrial glues and metal carriers should be used for mounting. However, metal carriers function only as options for mounting because LLTC and transistors are easily bonded to metals through the employment of thermal and conductive epoxy materials. At the same time, it is worth noting that metal carriers offer enhanced production and maintenance flexibility by effectively becoming a fully separate section on the power amp module. This feature is advantageous if, for example, an active device becomes burnt out. In this case, the metal carrier can be removed, and the active device replaced. Alternatively, a new metal carrier could also be mounted on the heatsink.

Industrial glues, such as epoxies, serve as thermally and electrically conductive adhesives. In PA modules, metal-backed LTCCs as well as transistors (die format) can be glued to the metal carriers or heatsinks. The thermal conductivity feature of the adhesive results in low levels of thermal resistance between the backside metals and the semiconductor, while the electrical conductivity grounds the active devices. The epoxy can also add some flexibility, as metals and semiconductor thermal expansion coefficients rarely match. Thus, the rising heat caused by increased power dissipation leads to thermal expansion of the materials used. Flexible adhesives, which can form an interface between metals and semiconductors, will prevent mechanical stress and breaks caused by different levels of thermal expansion.

The cold plate can be cooled down through the incorporation of an active cooling technique like fluid or air flow.

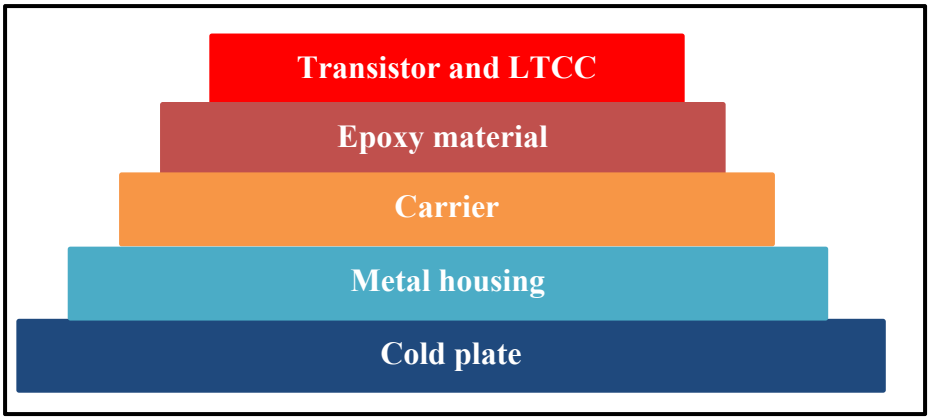

Figure 3.1 Typical thermal stack-up

3.2 Thermal Analysis

In order to evaluate the thermal characteristics of the designed power amplifier, a thermal model is constructed in ANSYS transit thermal. The overall model includes three parts: first one is the active device (transistor) and the second one is the power amplifier housing on which the PA mounted and the third is the heat sink.

3.2.1 Mechanical Housing

Figure 3.2 shows the house of the power amplifier constructed in HFSS. As shown in the figure the power amplifier circuit is divided into two parts input part which includes input matching and stability circuit and gate bias, the output part includes output matching network and drain bias, the line in the middle is the bed of the transistor and designed as a line to dissipate the heat in all directions.

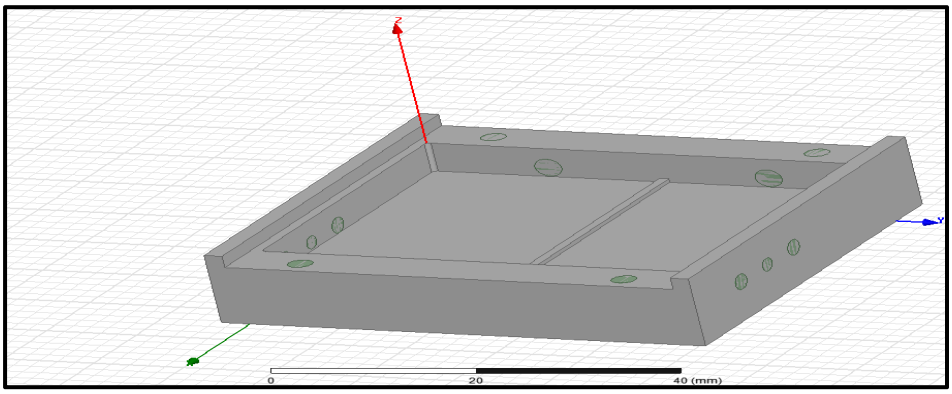

Figure 3.2 power amplifier house

3.2.2 Thermal Simulation

A schematic drawing of each layer is illustrated in figure 3.3. The top layer represents the main heat source which contains the active device. Then, an adhesive layer of solder material (AuSn) is used to mount the active device onto the top of copper diamond layer. Finally, the transistor and the copper diamond layer is fixed on a aluminum platform using silver epoxy

solder. The simulation is done in three aspects. First with active device only and the second with attachment thermal material and the last one with heat sink.

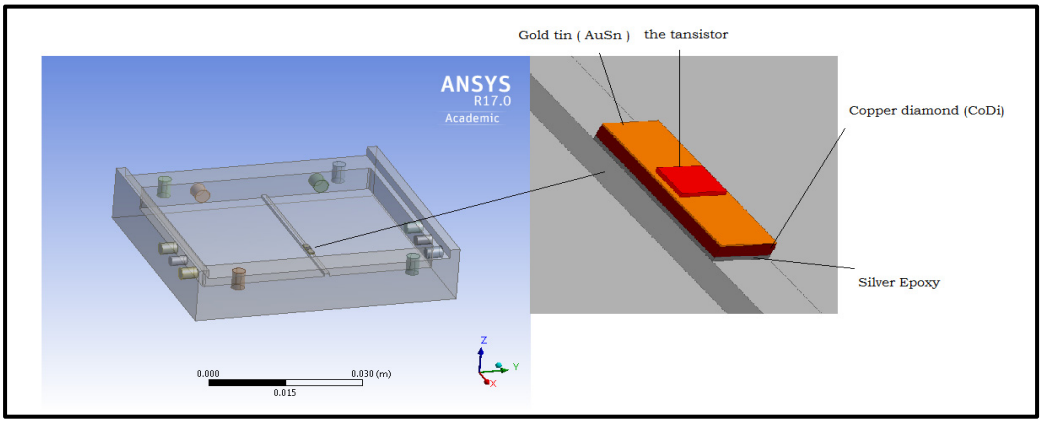

Figure 3.3 Schematic drawing of each layer for the simulation model

3.2.2.1 Option 1: Thermal Analysis With Active Device

Figure 3.4 shows the case where only the active device is simulated without any other materials just silver epoxy to sold it on platform. The highest temperature is approximately 99.71C.

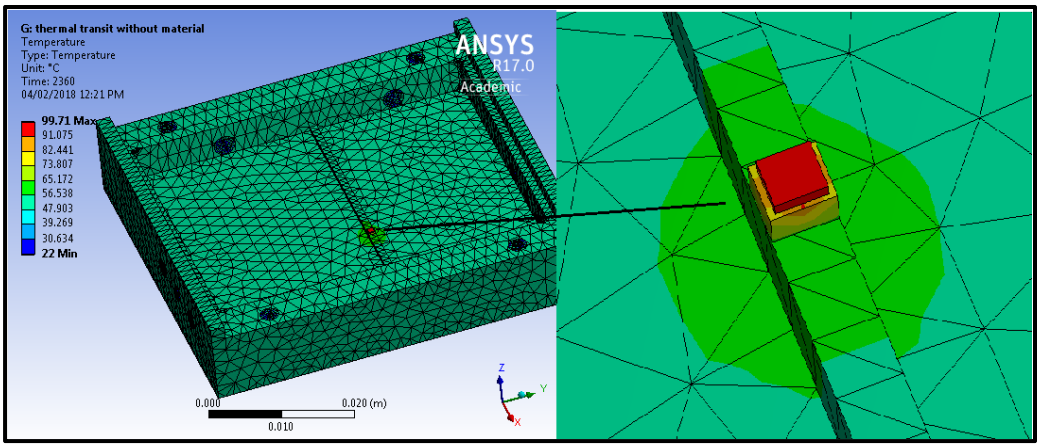

Figure 3.4 Thermal simulation of the PA with only the active device

Figure 3.5 shows the relationship between the temperature and time. We can see the transistor was 63C at starting point and got the highest temperature after 53 minutes.

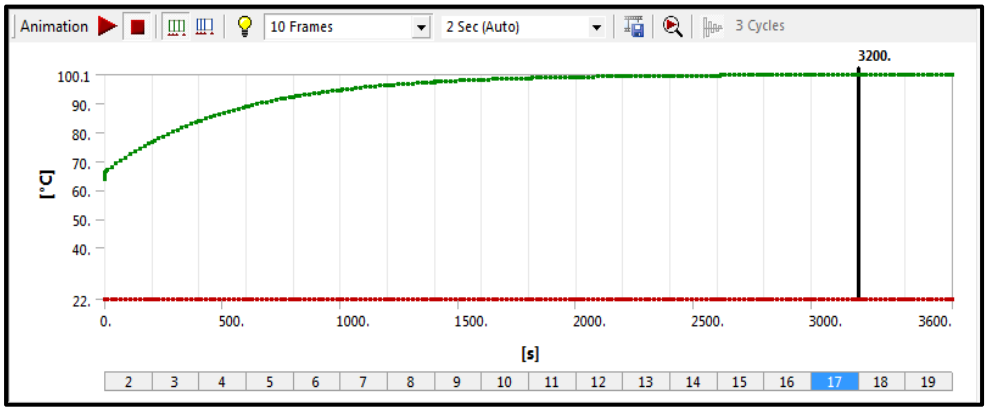

Figure 3.5 The relationship between the temperature and time at case1

3.2.2.2 Option 2 : Thermal Analysis When Active Device Attached to The Materials

Figure 3.6 demonstrates the simulation result of the active device with all materials. The hottest area is where the transistor is with a temperature of 64.65C which is responsible for delivering the requirement power to the output of the circuit. There is a 35.06C difference from the previous section. This is due to that some of the heat has been dissipated from the transistor to the back metal.

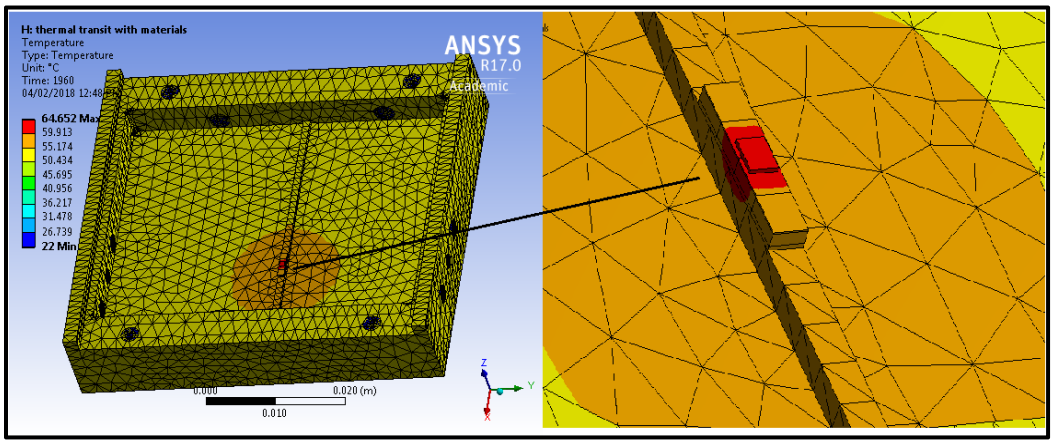

Figure 3.6 Thermal simulation of the PA with all layers.

The relationship between the temperature and time is shown in Figure 3.7. We can see the transistor was 29.571C at starting point and got the highest temperature after 40 minutes.

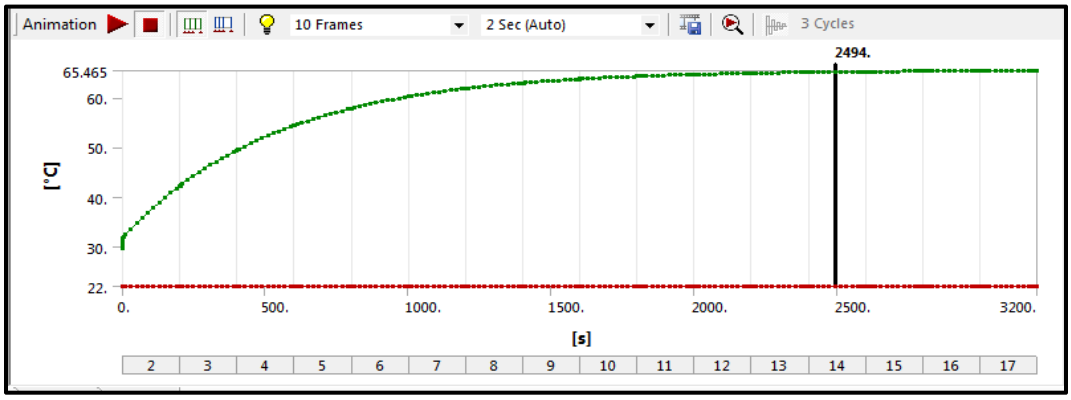

Figure 3.7 The relationship between the temperature and time case 2

3.2.2.3 Option 3: Thermal Analysis With Heat Sink

The last aspects is adding a heatsink to improve the heat dissipation, in this section we will simulate the thermal with two types of heatsink, circular plate and rectangular plate, figure 3.8 shows the result when we added a circular plate heatsink, as shown the hottest area is approximately 44.62C, There is a 20C difference from the previous section. This is due to some of the heat has been dissipated due to the heat sink.

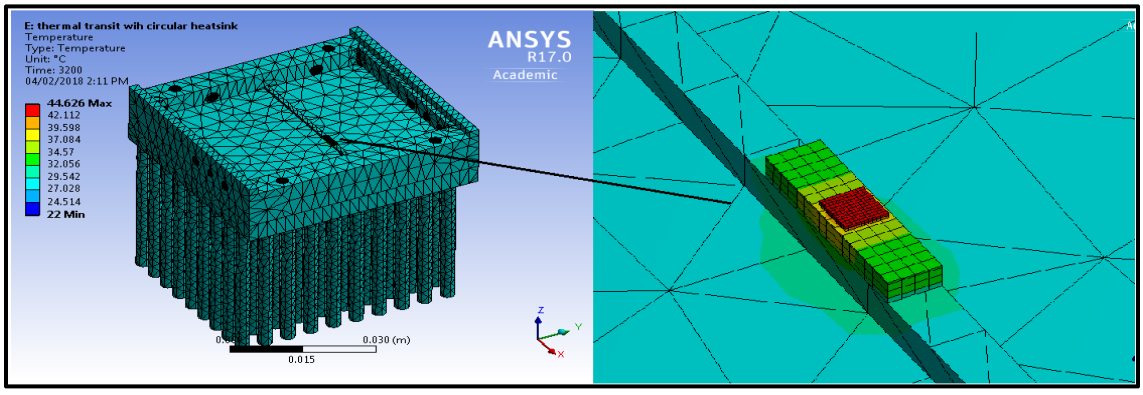

Figure 3.8 Thermal simulation of the PA with circular plate heatsink

The relationship between the temperature and time is shown in Figure 3.9. We can see the transistor was 36.64C at starting point and got the highest temperature after 15 minutes.

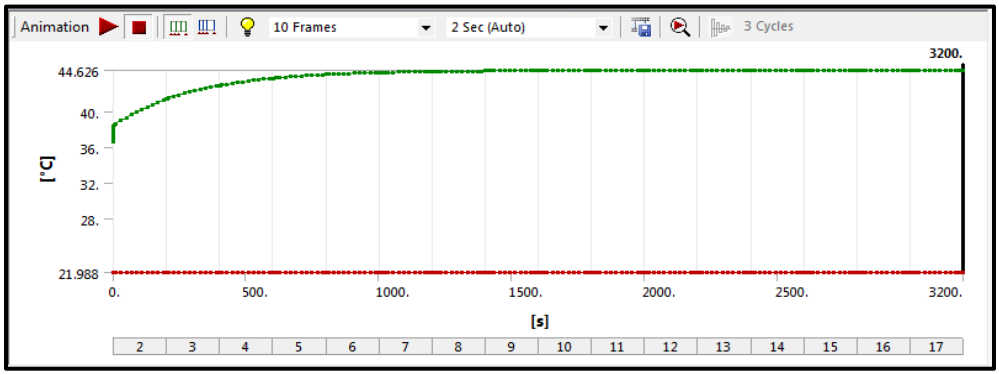

Figure 3.9 The relationship between the temperature and time in case 3

Figure 3.10 shows the result when we added a rectangular plate heatsink, as shown the hottest area is approximately 38.826C, There is a 6C difference from the circular plate heatsink.

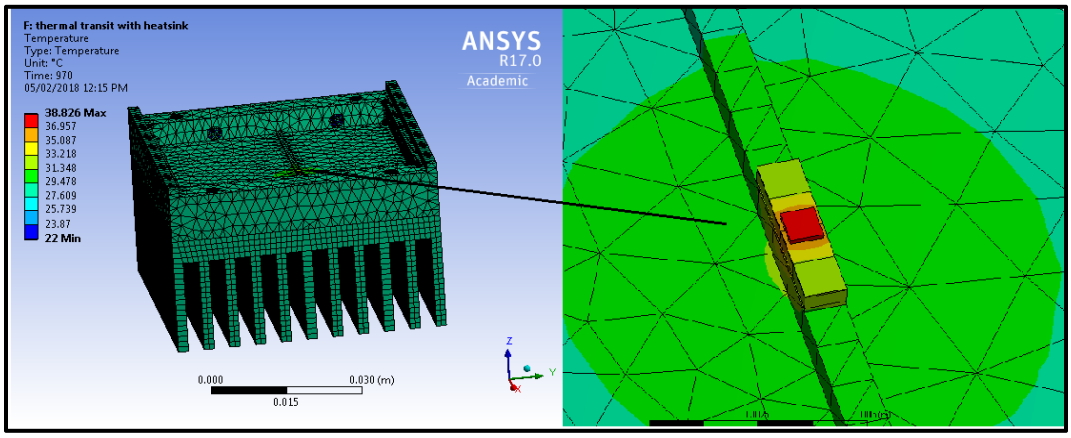

Figure 3.10 Thermal simulation of the PA with rectangular plate heatsink.

The relationship between the temperature and time is shown in Figure 3.11. We can see the transistor was 29.59C at starting point and got the highest temperature after 36 minutes.

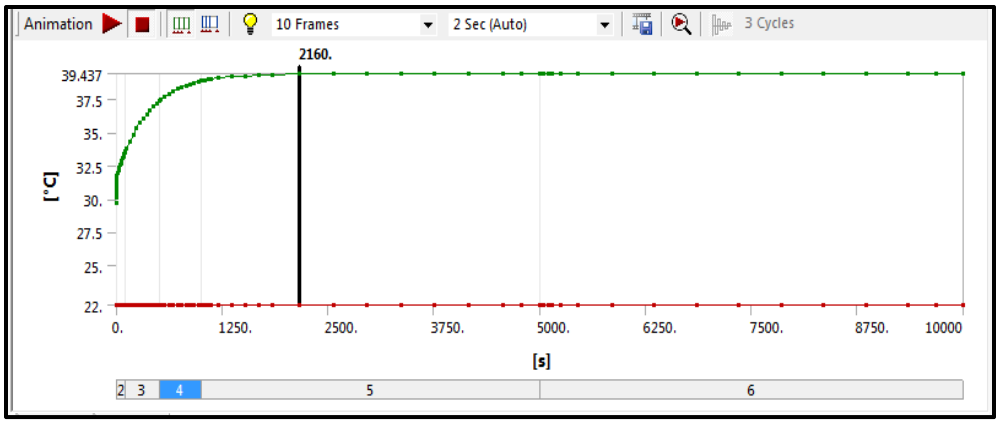

Figure 3.11 The relationship between the temperature and time case 3

3.3 Result Discussion and Comparison

To keep the same performance of the designed power amplifier, the temperature should not go more than 60 C, and with previous results we can note that the first option is not practical for our power amplifier,

In the previous steps, heat convection was assumed to be 10 w/m2. Table 3.1 charts the various values for heat convections as given by the thermal simulations. Clearly, the heat convection exerts a significant impact on the results. In raising the heat convection value, the maximum temperature then decreases. Furthermore, even though the starting temperatures are the same for the heat convection values, the amount of time it takes to attain maximum temperature is different. Hence, the heat transfer equation can be expressed as:

$$Q = h * S * (Tp – Ta) \quad (3.1)$$

Where:

Q : heat transferred J/s = w

H : heat transfer coefficient, w/(m2 k)

S : transfer surface, m2

Tp: plate temperature, k

Ta : air temperature, k

Table 3.1 Summarizes the thermal simulation for all options

The option / parameter	Heat convection	option 1	option 2	Option 3	
				circular plate	rectangular plate
Maximum temperature	10 w/m2	99.71 c	64.65 c	44.62 c	38.82 c
Starting point temperature		63 c	29.57 c	36.64 c	29.59 c
Time to get highest temp.		53 min	40 min	15 min	36 min
Maximum temperature	15 w/m2	88.85 c	54.28 c	42.534 c	35.52 c
Starting point temperature		63.64 c	29.57 c	36.64 c	29.59 c
Time to get highest temp.		25 min	23 min	10 min	30 min
Maximum temperature	20 w/m2	83 c	48.67 c	41.562 c	32.11 c
Starting point temperature		63.601	29.57 c	36.63	29.59 c
Time to get highest temp.		20 min	16 min	6 min	26 min

CHAPTER 4

REALIZATION AND MEASURMENTS

4.1 Introduction

Chapter 2 presented a Class-F PA which was designed with A6M Rogers substrate material and a GaN discrete transistor. This PA design made use of a nonlinear transistor model that could performe small and large signal measurements. In the present chapter, we fabricate and test the PA from Chapter 2. Our aim is to gauge the PA's electrical performance parameters while also comparing the measurement results to those of the simulation.

As a first step, we discuss the measurement approach as well as its set-up. Then we operate the PA according to CW operational conditions, measuring the PA's gain, output power, and efficiency parameters.

4.2 Prototyping

For the prototype PA, we fabricate the biasing circuits and matching networks over an A6M Rogers substrate with LTCC technology. The mechanical housing mentioned in Chapter 3 is also included in the PA. Figure 4.1 below shows the newly fabricated PA, while Figure 4.2 shows more details of the PA. As can be seen, we have used wire bounding to join the transistor to the output matching network and input stability circuit. This mechanical structure forms a thermal stack-up like the one depicted in Figure 3.4, as certain materials (e.g., gold, diamond, and copper) were unavailable. Note the close placement of the temperature sensor to the transistor die. This is done as a means to obtain more accurate readings of the die's base temperature.

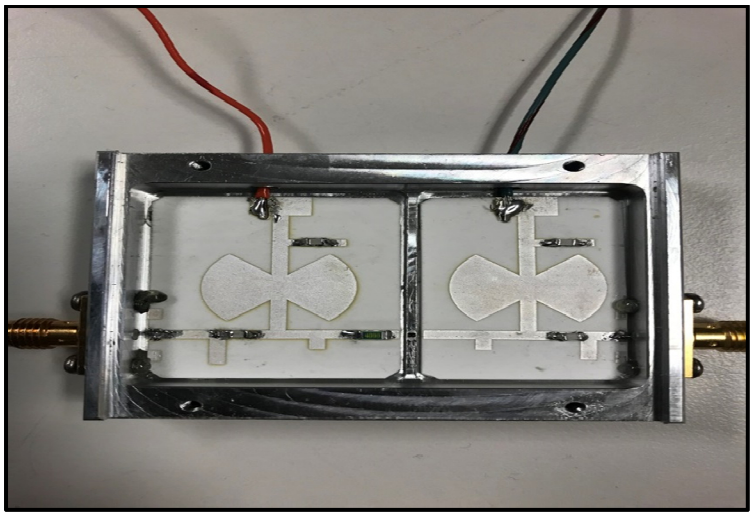

Figure 4.1 Fabricated Power Amplifier

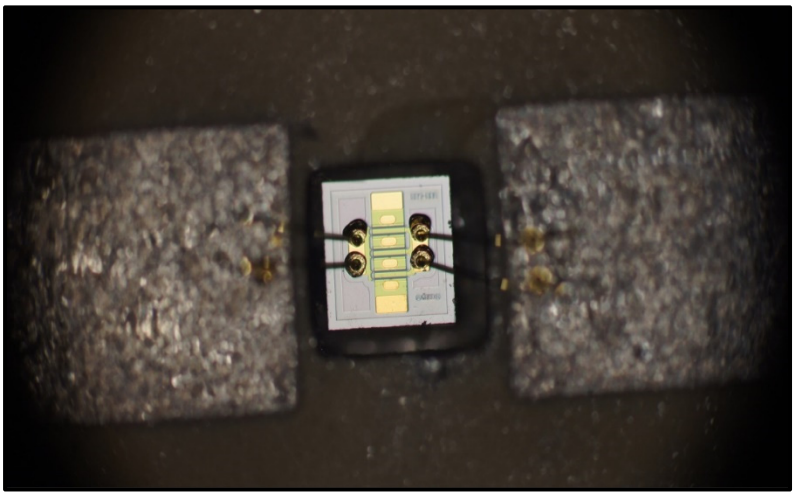

Figure 4.2 wire bound connection

4.3 Description Of Measurements Setup

Figure 4.2 depicts the measurement setup in the form of a block diagram. Along with the PA, the figure shows a network analyzer (NA), which is used for measuring S-parameters. Figure 4.2 also shows an attenuator, which is added as a protective element for the NA, to keep it from being compromised or damaged by the high power levels being generated. Because we can carry out our CW measurements with the assistance of the NA, the measurements are

performed in the measurement setup that employs the large and small signal drive. Figure 4.2 illustrates how this particular setup enables the measurements of the S-parameters to proceed as functions of the input power for predefined frequencies between the A' and B' planes.

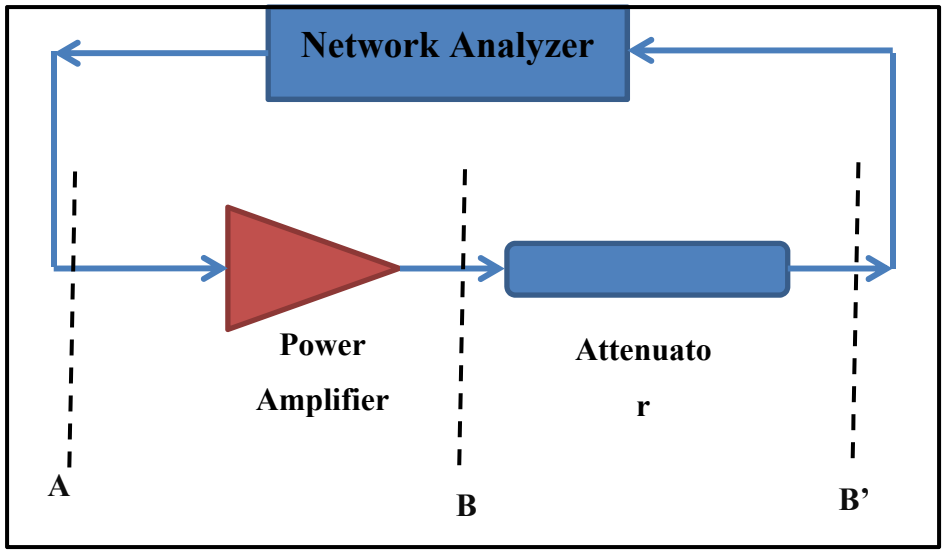

Figure 4.3 measurements setup of fabricated PA

Picture of the real measurement setup is shown in Figure 4.4. In addition to measurement devices, there are also cooling equipment to prevent the temperature to reach excessive levels for the PA.

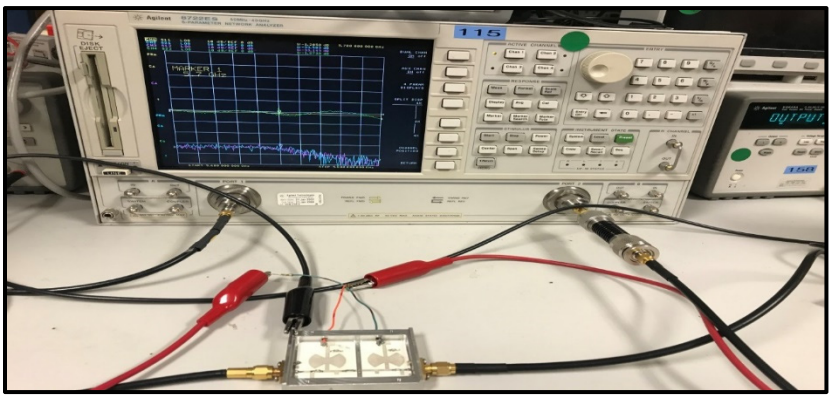

Figure 4.4 Real measurements setup of fabricated PA

4.4 CW Fundamentals Measurements

By working in CW mode, the RF input signal, along with the drain and gate bias voltages, can be continuously applied in the PA. Note that the PA is biased in class F mode during the CW measurements process. In this mode, the quiescent drain current is typically situated between the drain bias currents emitted by Class AB and Class B. The bias parameters for Class F CW mode measurements are given in Table 4.1 below.

Table 4.1 Bias voltage and current values

Gate Voltage (VGS)	**Drain Voltage (VDS)**	**Drain bias current (Ids)**
-2.6 V	40 V	45 mA

4.4.1 Small Signal Measurements Results

First of all, to validate if the PA is functioning as anticipated (e.g., whether or not it is stable), we measure the PA using small signal conditions. An unstable PA could indicate the presence of possible ripples in the drain current, a lower than expected small signal gain, or even PA burn-out. In Figure 4.5 below, the PA small signal measurement results are given for CW operational mode. No stability issues are evident and the PA appears to be functioning as anticipated. The only difference is that the small signal gain is somewhat lower than that of the simulation results. This difference in performance is likely due to matching network loss that has been inaccurately simulated by the EM simulators. Other potential sources of loss are the inclusion of RF connectors and microstrip lines in the PA. A few other losses have been added to the results; however, any transition occurring between microstrip lines and matching networks might lead to a mismatch loss caused by 50-ohm features that are imperfect.

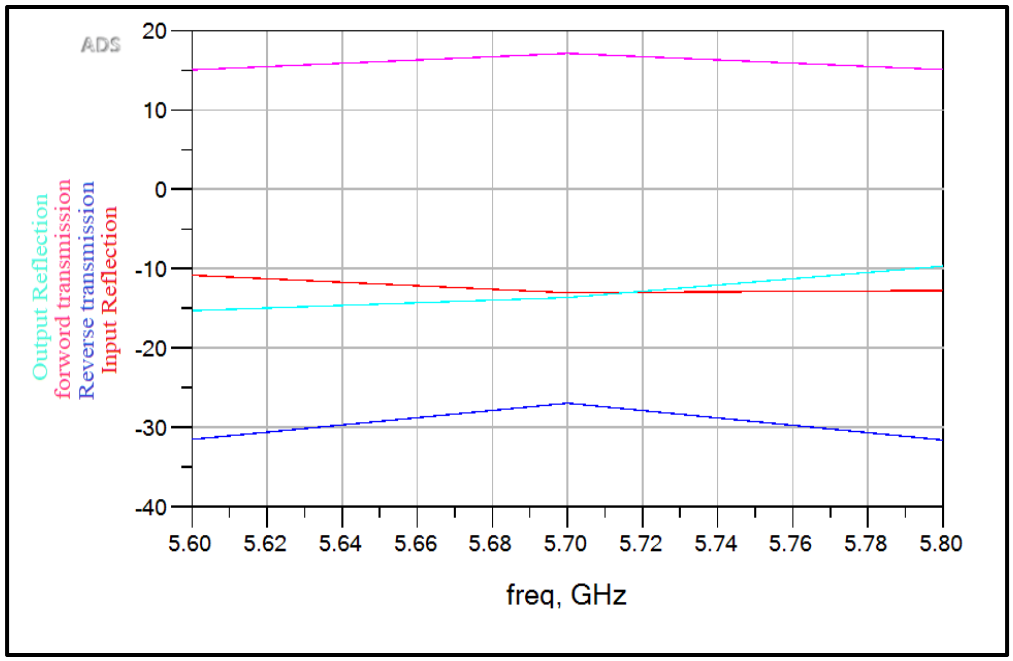

Figure 4.5 small signal S-parameters of the fabricated PA in CW

4.4.2 Measurements of PAE, Drain Efficiency and Gain

Measurement of PAE, efficiency and gain will be illustrated in this section. According to the simulated result, the maximum PAE is expected to be 69% with input power of 25dBm. This is consistent and confirmed in the experimental measurement shown in Figure 4.6, where the maximum PAE of 54.36% is reached at 25dBm input power level. In theory, PAE would increase as the input power increases. However, the PAE starts decreasing as the input power goes beyond 25dBm, which implies that the signal is being clipped and the PA becomes saturated. Moreover, the efficiency is also shown in Figure 4.6. At Pin=25dBm, the measured efficiency of the PA are 58.79 % .

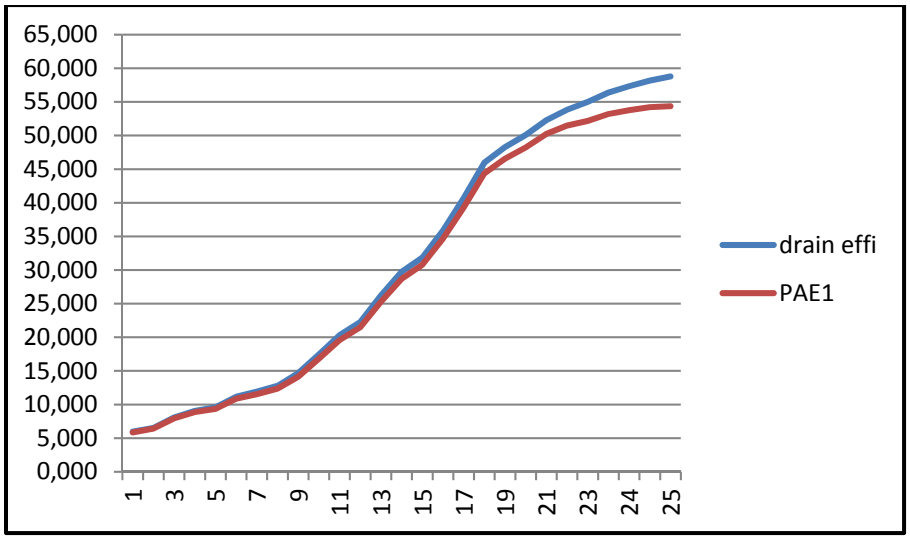

Figure 4.6 PAE and drain efficiency

The gain is also shown in figure 4.7. The measured gain of the amplifier at pin = 25 dBm is 11.23, the gain of the PA is expected to be 12dB as mentioned in section 2.8.1.

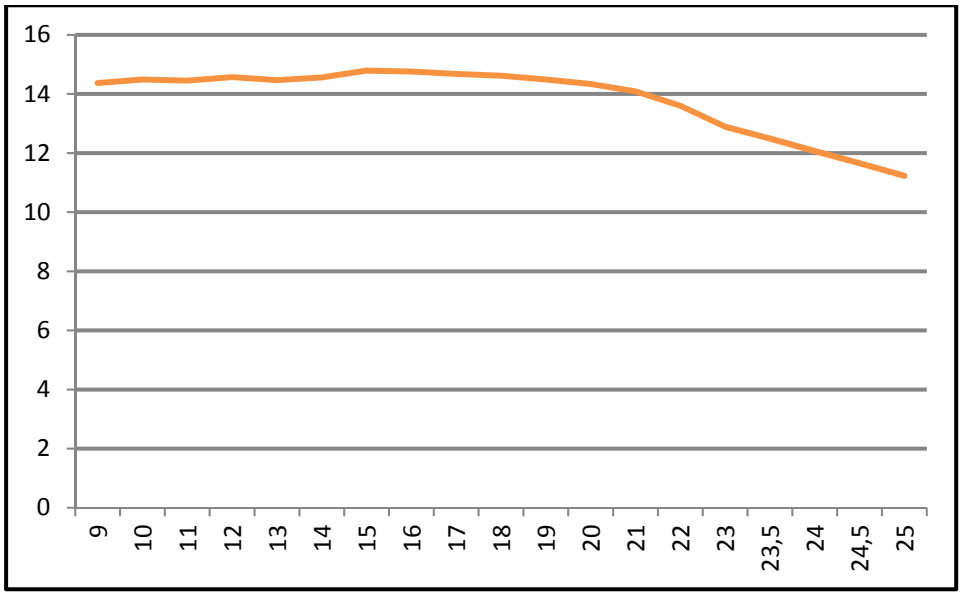

Figure 4.7 the gain of PA

Furthermore, the PAE and output power are shown in Figure 4.8. The maximum PAE is obtained with output power of 36.23dBm.

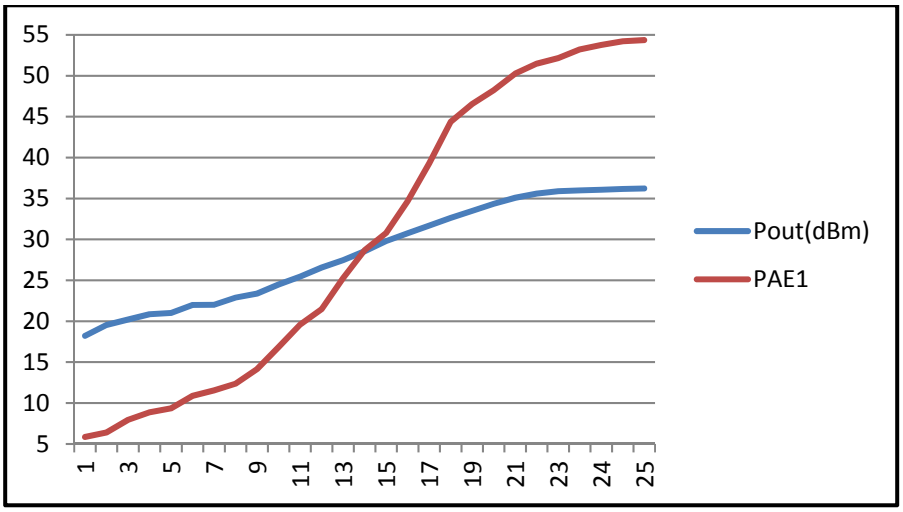

Figure 4.8 PAE and output power

Next, the 1 dB compression point is measured in order to find out when the PA starts to become saturated. Figure 4.9 shows that the 1 dB compression point of the system. The measured input P_1dB is 11.5dBm.

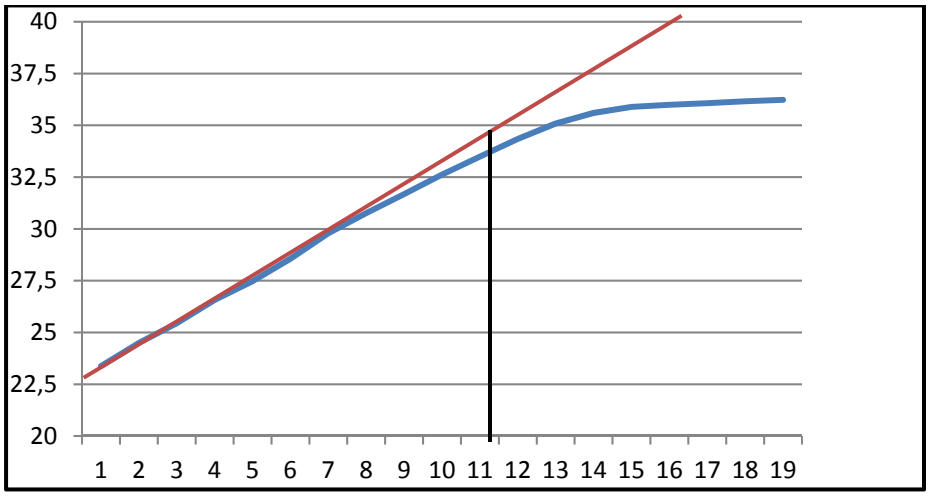

Figure 4.9 1-dB compression point

Picture of the real measurement setup is shown in Figure 4.10. as shown in the figure the output of the power amplifier connected to the attenuator then power detector then to the power meter, and the input of the power amplifier connected directly to the signal generator which can only output a maximum power of 25 dBm.

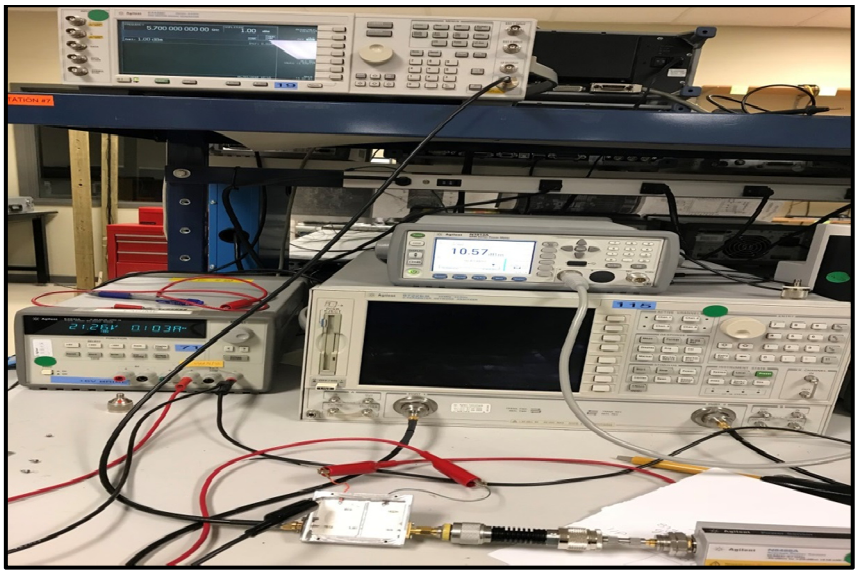

Figure 4.10 picture of the lab test setup

Next table shows the comparison between the simulation result and experimental result.

Table 4.2 comperasion between simulation and experiments results

Measurements	**Pin**	**Put**	**PAE**	**Drain Efficiency**
Simulation	25 dBm	37.28 dBm	68.99 %	73.31 %
Experiments	25 dBm	36.23 dBm	54.36 %	58.79 %

4.5 Result Discussion

as charted in Table 4.2. As was shown, the simulated PAE measured 68.99% compared to the lab-measured PAE of 54.36%, giving a difference of nearly 15%. This difference was likely due to errors in component values and calibration inaccuracies in the lab equipment used for taking measurements. Moreover, because of the heat generated within the power attenuator

when attenuating such a high power from the power amp, the attenuation may not be constant as the temperature increases. This attenuation variation of the power attenuator will impact the PAE measurement extremely. Because, in the simulation, components like resistors and capacitors are considered ideal (i.e., present no equipment errors), the PAE for the simulation shown in Table 4.2 is ideally optimal. Nevertheless, we can still consider the simulated circuit to be a good model of the actual PA, as the output power, amplifier drain current, and transistor S-parameters are not far off from those obtained in the simulation

CONCLUSION

A power amplifier was designed and prototyped at 5.7 GHz and a thermal reliability analysis method based on ANSYS was proposed and used to evaluate the PA thermal characteristics the use of high thermal conductivity materials, like copper diamond was investigated and found to yield improved thermal performance.

A mechanical housing was designed based on the thermal simulations and the entire PA was assembled and tested, the simulated performance was compared with experimental measurements and some differences were observed. The amplifier provided a measured PAE of 54 % at an input power of 25dBm with an output power of 36dBm.

As a conclusion, for the systems that require high efficiency, GaN technology is ideal the candidate for the future systems. However, it should also be noted that while providing high power density devices, GaN materials do not provide significant efficiency improvement so that the generated heat by the PA is remarkably increased. Therefore, reliability problems might occur if thermal management is not proper. Furthermore, the fabricated PA does not have a strongly linear operation region so that GaN based power amplifiers are not proper for the use in the systems which are expected to operate linearly

FUTURTE WORK

- The measurement made in this thesis covers small signal and one tone large signal measurements. A good extension of this work would be to make further investigations of amplifier such as two tone and modulated signal measurements.
- In order to make more accurate measurements, a driver amplifier of more than 25 dBm at 5.7 GHz is needed and should be developed.
- Improving the linearity of the designed PA should be undertaken.

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