TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

Page

LIST OF ABREVIATIONS

AC	Alternate Current
BTB	Back To Back
CSC	Current Source Converter
DB	Dead Beat
DC	Direct Current
ETS	École de Technologie Supérieure
FFT	Fast Fourier Transform
GCT	Gate Commutated Turn-Off Thyristor
HCC	Hysteresis Current Control
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Insulated Gate Commutated Turn-Off Thyristor
GTO	Gate Turn Off Thyristor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LCC	Line Commutated Converter
MMC	Modular Multilevel Converter
NPC	Neutral Point Clamped
PI	Proportional Integral
PLL	Phase Lock Loop
PWM	Pulse Width Modulation

SPS	SimPowerSystem
SPWM	Sine-wave Pulse Width Modulation
STATCOM	Static Compensator
THD	Total Harmonics Distortion
UHVDC	Ultra-High Voltage Direct Current
VSC	Voltage Source Converter

LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

A	ampere
C	reactor capacitance
C_{l}	DC cable capacitance
C_j	reactor capacitance of the j^{th} converter
$e_{\mathrm{a,b,c}}$	voltages from the AC system referred to VSC side of the transformers
F	farad
f_{c}	triangle carrier frequency
f_{m}	modulating frequency
$\mathrm{F_c}$	effective/equivalent frequency
H	henry
H*z*	hertz
i_{a}	*a*-phase AC network current
i_{b}	*b*-phase AC network current
i_{c}	*c*-phase AC network current
i_{aref}	*a*-phase reference current
i_{bref}	*b*-phase reference current
i_{cref}	*c*-phase reference current
$i_{\mathrm{a}j}$	*a*-phase current of the j^{th} converter
$i_{\mathrm{b}j}$	*b*-phase current of the j^{th} converter
$i_{\mathrm{c}j}$	*c*-phase current of the j^{th} converter
i_{dc}	DC current
i_{d}	*d*-axis current

i_q	*q*-axis current
i_{dref}	*d*-axis reference current
i_{qref}	*q*-axis reference current
$i_{dc\text{-}j}$	DC current of the j^{th} converter
i_{DC}	DC bus current
i_{djref}	reference value of the *d*-axis current for the j^{th} converter
i_{qjref}	reference value of the *q*-axis current for the j^{th} converter
$K_{p\text{-}voltage}$	proportional coefficient of voltage
$K_{I\text{-}voltage}$	integral coefficient of voltage
$K_{P\text{-}voltage}j$	proportional coefficient of the j^{th} converter voltage
$K_{I\text{-}voltage}j$	integral coefficient of the j^{th} converter voltage
$K_{P\text{-}power}$	proportional coefficient of active power
$K_{I\text{-}power}$	integral coefficient of active power
$kg{\cdot}m^2$	kilo· square metre
km	kilo meter
kV	kilo volts
kW	kilo watt
L	reactor inductance
L_l	DC cable inductance
L_j	reactor inductance of the j^{th} converter
M	the modulation index
m_{aj}	*a*-phase modulating signal
m_{bj}	*b*-phase modulating signal

m_{cj}	*c*-phase modulating signal
mΩ	milli ohm
mH	milli henry
MVA	maga vlots ampere
MW	megawatt
N	numbers of voltage source converters
P	active power
P_{ref}	reference active power
P_{meas}	measured active power
pu	per unit
Q	reactive power
Q_{ref}	reference reactive power
Q_{meas}	measured reactive power
R	reactor resistance
R_l	DC cable resistance
R_j	reactor resistance of the j^{th} converter
s	second
S_{base}	base power
s_j	switching function
t	time
T	sampling period
u_{sa}	*a*-phase AC network voltage
u_{sb}	*b*-phase AC network voltage

u_{sc}	*c*-phase AC network voltage
u_{ca}	*a*-phase VSC-output PWM voltage
u_{cb}	*a*-phase VSC-output PWM voltage
u_{cc}	*a*-phase VSC-output PWM voltage
u_{dc}	DC bus voltage
u_{dcref}	DC bus reference voltage
u_{d}	*d*-axis voltage
u_{q}	*q*-axis voltage
u_{dcref}	DC base / reference voltage
$u_{dc\text{-}j}$	DC voltage of the j^{th} converter
U_s	line-to-line AC bus voltage
U_c	converter AC voltage
V	volts
$V_{tot\text{-}2}$	total DC voltage of the AC system 2
V_{tot}	total DC voltage
δ	phase angle of the fundamental component of PWM
Δe_{pj}	difference value of the active power for the j^{th} converter
Δe_{dcj}	difference value of the dc voltage for the j^{th} converter
$\Delta^{*} e_{dcj}$	difference value of the compensation dc voltage for the j^{th} converter
Δi_{dj}	difference value of the compensation *d*-axis current for the j^{th} converter
θ_{Δ}	phase shifting angle of the triangle carrier signals
Ω	Ohm

INTRODUCTION

This chapter describes the research background, problem statements, main objectives, contributions, and the outline of this thesis.

Background

The high voltage direct current (HVDC) transmission technology has been developed due to its recognized significant economic and technical advantages for certain specific power system transmission and interconnection applications such as offshore wind farms, solar plants, different far distant AC systems, and so on (Sood, 2004). Rapid development of modern power electronics technology makes voltage source converter (VSC) based high voltage direct current transmission become an economic way for delivering electric power over long distances (Weimers, 1998). The VSC-HVDC system which employs insulated gate bipolar transistor (IGBT) and Pulse Width Modulation (PWM) switching techniques offers a number of advantages over the conventional line commutated HVDC systems (Ooi et Wang, 1990), such as no need of external voltage source for commutation, fast and independent control of reactive and active power, independent control of reactive power flow at each AC network, feeding weak AC systems or even passive loads, high quality power with less harmonics distortion (Asplund, 2000; Venkataramanan et Johnson, 2003). Therefore, VSC-HVDC transmission system is a competitive way for grid connection over long distance. Modeling, control, and application of VSC-HVDC systems were reported in (Casoria, 2009) , (Chen et al., 2006), (Du, Agneholm et Olsson, 2008), and (Fu et al., 2011) and so on. More articles work on the control of the VSC-HVDC system since a good control system acts like “core chip” which is one of the most important parts for the whole VSC-HVDC system. Nowadays the installations of VSC-HVDC systems at commercial level can be found in Sweden, Australia, the U.S., Mexico, Norway, China and etc.

The demand for power keeps increasing at a scale and speed all over the world in the past latest years. Growing renewable energy sources with power generation becomes increasingly

distributed and a growing number of generation facilities located far away from load centers. What's more, demanding economic objectives and obligations to reduce greenhouse gas have to be met (SIEMENS, 2015). To satisfy these demands, it is necessary to study higher voltage level HVDC power transmission technology-Ultra-High Voltage Direct Current (UHVDC) power transmission technology. In 2010, the first commercial thyristor-based UHVDC transmission system is in operation in China. So far, there are several thyristor converter based UHVDC projects in use by 2015. For example, ±800 kV Xiangjiaba Shanghai UHVDC link is with rated power of 6,400 MW and a transmission distance of 1,935 km (Yang et al., 2011b); ±800 kV Yunnan-Guangdong UHVDC link is with rated power 5,000 MW and a transmission distance of 1,373 km (Rao, 2012); and in India, Champa-Kurukshetra project using 800 kV UHVDC technology transfer rated power 3,000 MW and with a transmission distance of 1365 km (ALSTOM, 2016). More projects are either in planning or under construction in China, India, Brazil, and some other countries. Here, motivated by the success of the thyristor-UHVDC technology and the benefits of VSC-based HVDC technology, VSC modules based UHVDC transmission system will be firstly studied in Chapter 4.

Problem statements

The statement of the problem A): So far, many literatures about VSC-HVDC control strategies have been developed, such as PI control scheme (Yin, G. Y. Li et T. Y. Niu, 2005; Zheng et Zhou, 2006) in *dq* coordinates, direct current control strategy by regulating the amplitude and phase of the AC side currents, direct power control method (Rahmati, Abrishamifar et Abiri, 2006) using hysteresis with random switching frequency and a nonlinear control scheme in (Chen, Zheng et Fan, 2006). Most of these controllers are based on *dq* coordinates and the variables such as the voltages and currents in this controller need use abc/dq and dq/abc coordinates transformation several times, which results in the resutls of control performance more impacted by the performance of phase lock loop (PLL). Usually, it needs to tune four control coefficients for a double close-loop PI control scheme and it is

not an easy task. Some other nonlinear control schemes are with complex control algoriths and not easy to design.

Therefore, in order to further exploit the benefits of VSC-HVDC system and improve the dynamic performance of the VSC-HVDC system, it is expeceted to develop some control scheme with easy to design and simple control structure to reach good dynamic performance and good steady-state tracking accuracy behavior.

The statement of the problem B): Most of converter stations for UHVDC operations in the existing projects are thyristor-based converter stations, which usually is a series connection of a two 12-pulse bridges with 400kV rated voltage each to each the rated DC voltage of 800 kV per pole. The innovative solutions of thyristor-based UHVDC have been implemented to fully meet the extended requirements for ultra-high voltage bulk power transmission. However, thyristor-based converters have well-known weaknesses: (a) commutation failures; (2) expensive filters on the AC side and DC side; (3) power flow reversal needs interruption to change voltage polarity mechanically; (4) and no independent active and reactive power control.

In order to address those problems, a solution of two modular multilevel converters (MMC) connected in series per pole was presented for UHVDC application in (Wang, Hao et Ooi, 2013) and each 3-phase MMC based on single-phase H-bridge modules in series. MMC has the advantages over conventional thyristor-based HVDC. However, MMC for UHVDC applications, the weight and size of the power module capacitors of the converters have to be considered since a large quantity of capacitors is needed to form the whole converter stations. At the same time, MMC cell capacitor only conducts single phase AC current, which is one drawback of MMC topology. Besides, the series connection MMC faces the individual DC voltage unequal. Therefore, compared with 12-pulse bridge thyristor-based converter and MMC stations, in this research two-level VSC module based stations are proposed for UHVDC operation.

Project objectives

The research mainly focuses on the control of VSC-HVDC transmission system and the application of VSC-HVDC system to UHVDC operation with series-connected VSC modules. The main objectives of the project are described below:

Control of the VSC-HVDC systems): To present good control scheme for the VSC-HVDC system to reach good dynamic response and steady-state tracking accuracy behavior.

Application of the VSC-HVDC systems): Based on the success in thyristor-UHVDC depends on industry having the technical knowledge in insulation so as to connect four 200 kV thyristor-based converter stations in series to bring the DC voltage up to 800 kV or more, in this part, the objectives are: to propose two-level VSC modeules based UHVDC transmission system; then, to develop the corresponding control system for the proposed UHVDC transmission system; lastly, to verify the validation of two-level VSC modules based UHVDC by demanding tests such as active and reactive power step change test and reversal of direction power flow test.

Contributions

The main contributions of this research are as follows:

- Deadbeat current control scheme in *abc* coordinates with its simple control structure and determined parameters is developed for the VSC-HVDC system, which improves the dynamic responses and the steady-state tracking accuracy behavior of the system;

- Two-level VSC modules based UHVDC transmission system is proposed first time, and this research reports on the first step which is series connecton VSC modules for UHVDC operation is trouble free;

- To improve the stability of the DC voltages, the corresponding control system with DC voltage compensation equalizer is developed for the series-connected VSC modules based UHVDC system. Details test the feasibility of the VSC-UHVDC transmission system for the future "energy high way".

Two Journal and three conference papers have been submitted for review, they include:

Fu, Xiaofan**,** L.-A. Dessaint, B. T. Ooi. 2016. « Feasibility Study of Series Connection VSCs for UHVDC Operation ». Submitted to *IEEE Trans. Industrial. Electronics*, Aug. 2016. (Resubmitted).

Fu, Xiaofan, L.-A. Dessaint, et R. Gagnon. 2016. « Coordinated Control of Offshore Wind Farm Connected to the Grid with DC Series Connection ». Submitted to *IEEE Trans. Sustainable Enegy*, Aug. 2016. (Submitted)

Fu, Xiaofan, L.-A. Dessaint, R. Gagnon, K. Zhou, et M. Cheng. 2012. « A Comparative Study of Control Schemes for VSC-HVDC Transmission System ». *38th Annual Conference of the IEEE Industrial Electronics Society, IECON* 2012, Montreal, Canada, (Oct. 25-28, 2012) p: 2096-2103.

Fu, Xiaofan, L.-A. Dessaint et R. Gagnon. 2011. « Grid-connection of offshore wind farms using VSC-HVDC systems ». *in Proc. 10th Int. Workshop Large-Scale Integr. Wind Power into Power Syst. Transm. Netw. Offshore Wind Farms,* (Oct. 25-26, 2011) Aarhus, Denmark.

Fu, Xiaofan, L.-A. Dessaint, R. Gagnon, K. Zhou et M. Cheng. 2011. « Modeling and simulation of VSC-HVDC with current deadbeat control ». In *Electrical Machines and Systems (ICEMS), 2011 IEEE International Conference on*. Beijing, China (20-23 Aug. 2011), p. 1-6.

Thesis outline

This thesis is organized as follow:

Chapter 1 Literature review: This chapter mainly reviews on control and application of the VSC-HVDC system. Firstly, the topology and basic principle of VSC-HVDC are introduced, and then different control systems of two-terminal VSC-HVDC are reviewed. The application of VSC-HVDC, especially for UHVDC and offshore wind farms, is also presented and reviewed at the end.

Chapter 2 A comparative studies of control schemes for VSC-HVDC transmission system: this chapter we briefly review the control schemes for the VSC-HVDC system. Then, present conventional PI decoupling control, hysteresis current control and deadbeat current control schemes for the VSC-HVDC transmission system connecting two AC grids. Furthermore, compare their advantages and disadvantages in the VSC-HVDC control systems. Finally, Case of two-terminal VSC-HVDC system is developed in MATLAB/SimPowerSystems and the dynamic performance of the system is evaluated during system start up, grid voltage sags and power reversal changes. Simulation results show that these three control schemes for VSC-HVDC system can offer good dynamic performance when system start up, voltage sags in the grid and power reversal in the system. Different control schemes have different responses performance in the system. Thus, we can choose different control schemes according to the system control requirements and applications.

Chapter 3 Study on VSC-HVDC system with current deadbeat control: In this chapter, a double-loop control scheme is proposed for the VSC-HVDC transmission system connecting two AC grids. A conventional PI controller is used in the outer loop and a current deadbeat controller is presented in the inner loop in order to achieve fast dynamic response, high tracking accuracy and robustness. Cases of two-terminal VSC-HVDC system are developed in MATLAB/SimPowerSystems (SPS) to verify the validity of the proposed control strategy.

Simulation results show that the proposed control scheme provides a high performance control solution to the VSC-HVDC system.

Chapter 4 Application of VSC-HVDC: Feasibility study of series connection VSCs for UHVDC operation: Existing Ultra-High Voltage Direct Current (UHVDC) Transmission at 800 kV is based on line-commutated thyristor technology. As HVDC based on Voltage Source Converter (VSC) technology has already reached 350 kV DC voltage, this chapter examines the feasibility of connecting four Voltage Source Converter (VSC) HVDC stations, each rated at 200 kV DC voltage, in series to form a pole UHVDC of 800 kV DC voltage. Feasibility is demonstrated by simulations using the software of MATLAB/SPS.

Conclusion The final chapter concludes with a synopsis of the thesis and identifies topics for further studies.

CHAPTER 1

LITERATURE REVIEW

1.1 Introduction

This Chapter mainly reviews the control and application of the VSC-HVDC system. Firstly, the topology and basic principle of VSC-HVDC are introduced, and then different control schemes for two-terminal and multi-terminal VSC-HVDC are reviewed. The applications of VSC-HVDC transmission, especially for UHVDC and offshore wind farms, are also presented and reviewed in detail at the end.

1.2 Configuration and basic principle of VSC-HVDC

The configuration of a typical two-terminal VSC-HVDC system is shown in Figure 1.1. The configuration of VSC-HVDC system includes Voltage Source Converters (VSC), Converter Reactors (*R*, *L*), Transformers (T_1, T_2), AC Filter and DC Capacitor etc. Each VSC station is regulated by a corresponding control regulator (Asplund, 2000; Venkataramanan et Johnson, 2003; Weimers, 1998).

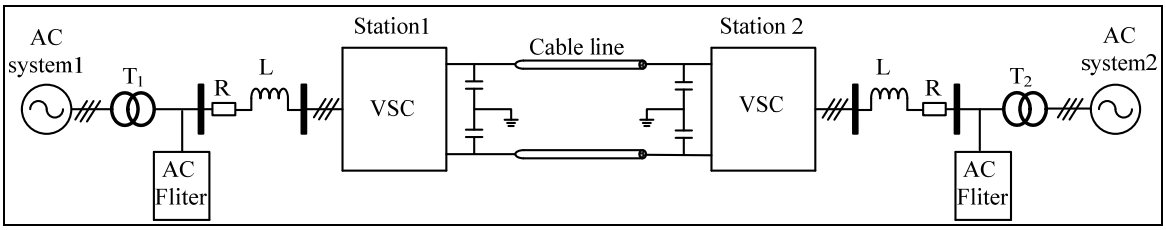

Figure 1.1 A VSC-HVDC system

The two sets of converter (station1, station2) shown in Figure 1.1 are VSCs whose bridge arms are based on IGBT. The VSC could be a two-level converter, a three-level converter, or a multi-level converter. Each of its bridge arms is a series of a number of IGBTs and its parallel diodes, so as to enhance the capacity of converters and system voltage under high

voltage and high power condition (Sood, 2004). Number of its series is relied on converter's rated power, voltage level and power electronic devices electric capability and compressive strength. The reactors are used for performance control of active and reactive power during the power transfer process. At the same time, inhibit switching frequency harmonics in converter output current and voltage in order to obtain the expected fundamental current and fundamental voltage. Also, it can inhibit short-circuit current (Sood, 2004). T1 and T2 in Figure 1.1 are transformers which are used to transform AC voltage into secondary voltage adapted to DC link in converter. Transformers can be eliminated when the AC system at low voltage. AC filter is used for the elimination of their output harmonics (Kim, 2009). DC capacitor is converter's DC-link storage elements, it can buffer the impact of current in bridge arm breaking; reduce DC voltage harmonic (Arrillaga, 2008).

The topologies of two converters of the VSC-HVDC system have been studied in (Andersen et al., 2002; Portillo et al., 2006; Xu et Agelidis, 2007). Different converters are used in the VSC-HVDC system and the two-level bridge is the simplest circuit configuration. Recent practices have extended the principle to multi-level converters by using of capacitors and diodes to increase the number of levels. The voltages can be clamped for different levels such as a three-level neutral point clamped voltage source converter (Noroozian et al., 2003; Yazdani et Iravani, 2006; Zhang et al., 2008) and a three-level flying capacitor voltage source converter (Xu et Agelidis, 2007). The multi-level converters provide improved waveform quality and reduced power losses. Recent years more and more modular multilevel converters (MMC) based HVDC such as (Li et al., 2013), (Wang et al., 2014), (Li et al., 2015), (Beddard, Barnes et Preece, 2015), and (NgTrinh et al., 2016) is developing and blooming. However, due to the increased complexity in converter control with multilevel converters the two-level converter technology is still the most commonly used in practical applications.

In addition, for completeness review, multi-terminal VSC-HVDC is introduced briefly here. As we know, a VSC-HVDC system can achieve a reversal of the power flow by simply reversing the direction of the DC current without changing the polarity of the DC voltage

(Chen et al., 2006; Li et al., 2007), this feature is critical for multi-terminal DC system, namely, multi-terminal VSC-HVDC (Chen et al., 2006; Li et al., 2007; Lu et Ooi, 2003). In fact, the multi-terminal VSC-HVDC system is a natural extension of two-terminal VSC-HVDC. The converters in a multi-terminal VSC-HVDC system can be either an inverter or a rectifier, depending on its power direction. Figure 1.2 shows a four-terminal VSC-HVDC transmission system. In Figure 1.2, each terminal connects to the AC system which also can be the interfaces of the integrations of offshore wind farms, solar plants, and other renewable energy resources.

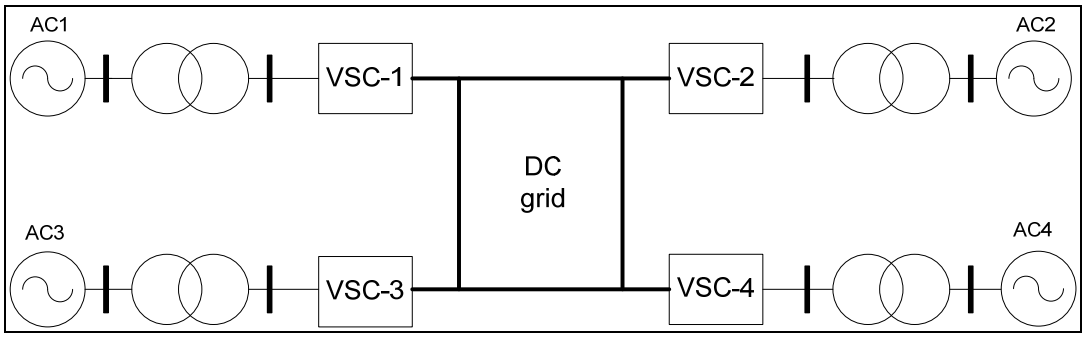

Figure 1.2 A four-terminal VSC-HVDC system

1.3 Control of VSC-HVDC

Generally, for a VSC-HVDC system, there are three control modes: *a*) constant DC voltage control; *b*) constant DC current or active power; *c*) constant AC voltage control (Asplund, 2000; Flourentzou, Agelidis et Demetriades, 2009; Sood, 2004). Figure 1.3 shows the overall control scheme of the two-terminal VSC-HVDC system.

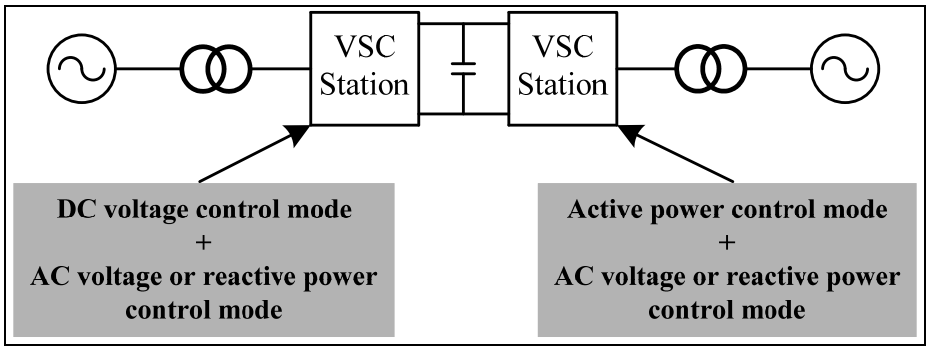

Figure 1.3 Overall control scheme of the two-terminal VSC-HVDC

In mode *a*) and *b*), the reactive power sent to the AC system by the VSC is also controlled. Mode *c*) is usually used when the VSC-HVDC system feeds power to a passive network. Mode *a*) and *b*) are adopted for connecting an active AC network and mode *c*) is suitable for connecting a passive AC network (Flourentzou, Agelidis et Demetriades, 2009; Mauricio et Exposito, 2006).

Many literatures associated with the modeling and control of VSC-HVDC systems. To exploit the benefits of VSC-HVDC, many control strategies have been developed, such as PI control scheme (Yin, G. Y. Li et T. Y. Niu, 2005; Zheng et Zhou, 2006) in dq coordinates, direct current control strategy by regulating the amplitude and phase of the AC side currents, direct power control method (Rahmati, Abrishamifar et Abiri, 2006) using hysteresis with random switching frequency. Recently various nonlinear controllers have been investigated in (Liang et al., 2005), (Liu et Cai, 2008b), and (Rashed, El-Anwar et Youssef, 2008). In (Lindberg et Lindberg, 1995) and (Ouquelle, Dessaint et Casoria, 2009) an inner current control loop is designed for a digital control implementation and for a dead-beat control of the converter current when the converter is connected to a very strong AC network. An ancillary damping fuzzy control is proposed to change the active power reference dynamically and system stability is improved with the proposed ancillary damping fuzzy control in (Li et al., 2008). In (Du et al., 2007), the control strategy is to regulate the AC and DC voltages on the rectifier side and to control the AC voltage and frequency at the inverter side for improving the quality of power supply to industrial plants. An optimal control

strategy based on Newton-Raphson OPF algorithm is proposed in (Pizano-Martinez et al., 2007).

Moreover, there are some further possibilities for the improvement control of VSC-HVDC system. In (Jowder et Ooi, 2004) the static synchronous series compensation (SSSC) is embedded in the VSC-HVDC station to improve the dynamic characteristics of the VSC-HVDC link. In (Du, Sannino et Bollen, 2005), it has been investigated what happens when the VSC-HVDC is designed to supply an established AC system by using power flow and AC voltage control. The current limit, as also shown in (Du, Sannino et Bollen, 2005), (Du et al., 2007), and (Du, Agneholm et Olsson, 2008) which are aimed to protect the VSC-HVDC valves, has a significant impact on the dynamics of a VSC-HVDC supplied system. A control system for the VSC-HVDC during island operation and under three-phase balanced fault was investigated in (Du et Bollen, 2006), and it has been found that the current limit of the converters has a significant influence on the dynamic response of the system. Reference (Du, Agneholm et Olsson, 2008) presents three different frequency controllers and their effects on the voltage disturbance ride-through capability of a VSC-HVDC supplied industrial system.

As VSCs are modeled as ideal current sources on their DC sides, they are eminently suited for parallel connection across a pair of DC bus. The possible implementation of a multi-terminal HVDC system and various aspects related to the multi-terminal HVDC system have been studied in (Li et al., 2007), (Ding et al., 2009), and (Lu et Ooi, 2002). In (Li et al., 2007) a linear decoupling control is studied and the multi-terminal VSC-HVDC is presented to interconnect wind farms to AC grids. This method highlights the control at the level of wind generator cluster that comprises several permanent magnet synchronous generators without the primary converters on themselves. Multi-terminal VSC-HVDC system is able to connect each doubly-fed induction generator located at different site respectively, and transmit electrical power into main grid (Ding et al., 2009). In (Lu et Ooi, 2002) it describes the optimal acquisition and aggregation of wind power by multi-terminal high voltage direct current based on Sine-wave Pulse Width Modulation (PWM), three-phase VSCs connected at their AC terminals to the wind turbine generators.

It should be mentioned that converters in a multi-terminal VSC-HVDC system can be either inverter or rectifier, depending on its power direction. Therefore, in order to maintain power balance in the DC grid, at least one VSC must be assigned to operate as a DC voltage regulator, which automatically functions as a power slack and ensures that the power balance requirement of the DC grid is satisfied (Egea-Alvarez et al., 2013).

1.4 Applications of VSC-HVDC

The VSC-HVDC transmission has a number of technical features that make it especially attractive for many applications such as feeding into passive networks, transmission to/from weak AC systems, enhancement of an AC system, land cable systems, supply of offshore loads, connection to wind farms (on-shore or off-shore) or wave power generation (Sood, 2004; Tang et Ooi, 2007; Xu et al., 2010), *etc*. Two commercial VSC-HVDC transmission systems projects, Gotland and Tjæreborg, are feeding onshore wind power to the AC system. These projects have shown that VSC-HVDC is capable of handling wind power and reacting rapidly enough to counteract voltage variations in an excellent way.

On the other hand, the fact that neighboring energy sources have already been exploited, so the future power has to be transmitted from very remote locations to consumers. The long transmission distances of large countries like China, India, and Brazil justify the use of Ultra High Voltage DC transmission (UHVDC) at transmission voltages of ±600 kV to ±800 kV (Astrom et al., 2010; Kumar et al., 2009b). So far, all the UHVDC transmission lines are based on thyristor converters. Here, VSC-HVDC based UHVDC will be proposed in this research work. The following sections focus on reviewing the application of VSC-HVDC system for UHVDC operation.

The main feature of UHVDC is the potentiality of long-distance, high-capacity, and low-loss power transmission. Thus, UHVDC offers the promise to meet the aforementioned challenge. Some UHVDC projects are already in operation. For example, the ±800 kV Xiangjiaba-Shanghai UHVDC link, which is the first UHVDC project in the world to go into commercial

operation in July 2010, with a rated power of 6,400 MW, transmit power over a distance of 1935 km (Yang et al., 2011a). Yunnan - Guangdong ±800 kV UHVDC link, owned by China Southern Power Grid, rated for 5000 MW to transmit power over a distance of 1418 km (Rao, 2012). Jingping-Sunan ±800 kV HVDC transmission (JPS800) project is rated for 7200 MW to transmit power over a distance of 1935 km, owned by State Grid Corporation of China (Astrom et al., 2010). More UHVDC projects are under construction in India, China and some European countries.

The main advantage of UHVDC is overall transmission loss is low at high transmission voltage of 800 kV. Most of converter stations for UHVDC in the above existing projects are thyristor based converter stations, which usually is a series connection of two 12-pulse bridges with 400 kV rated voltage, and each 12 pulse bridge consists of two 6-pulse bridges of 200 kV each. On their AC sides, one bridge has a wye-delta transformer connection and the other a wye-wye connection to achieve a 30 degree phase shift to eliminate the 6^{th} harmonic. Thyristor based converter for UHVDC applications, innovative solutions have been implemented to fully meet the extended requirements for ultra high voltage bulk power transmission (Rao, 2012). Figure 1.4 shows the basic arrangements of transformers and converters for thyristor-based UHVDC (one pole).

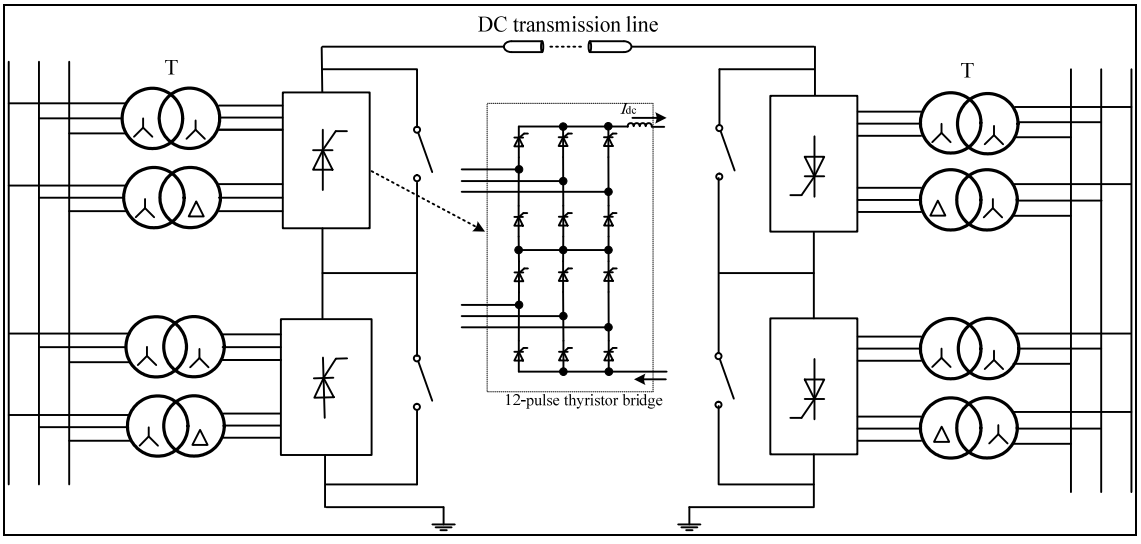

Figure 1.4 Basic arrangements of transformers and converters for thyristor-based UHVDC (one pole)

However, thyristor-based UHVDC has some disadvantages as well, such as facing the risk of commutation failure, needing communication between stations, cannot connect to weak AC system and reactive power and active power cannot control independently. One solution of two modular multilevel converters (MMC) connected in series per pole was presented in (Wang, Hao et Ooi, 2013) for higher voltage HVDC application and each 3-phase MMC based on single-phase H-bridge modules in series. MMC has the advantages over conventional thyristor HVDC in that: (i) there is no commutation failure; (ii) power reversal takes place by reversal of current direction; (iii) costly DC-side and AC-side filters are not required (Wang, Hao et Ooi, 2013). Three-parallel phase MMC stations based HVDC (one pole) is shown in Figure 1.5.

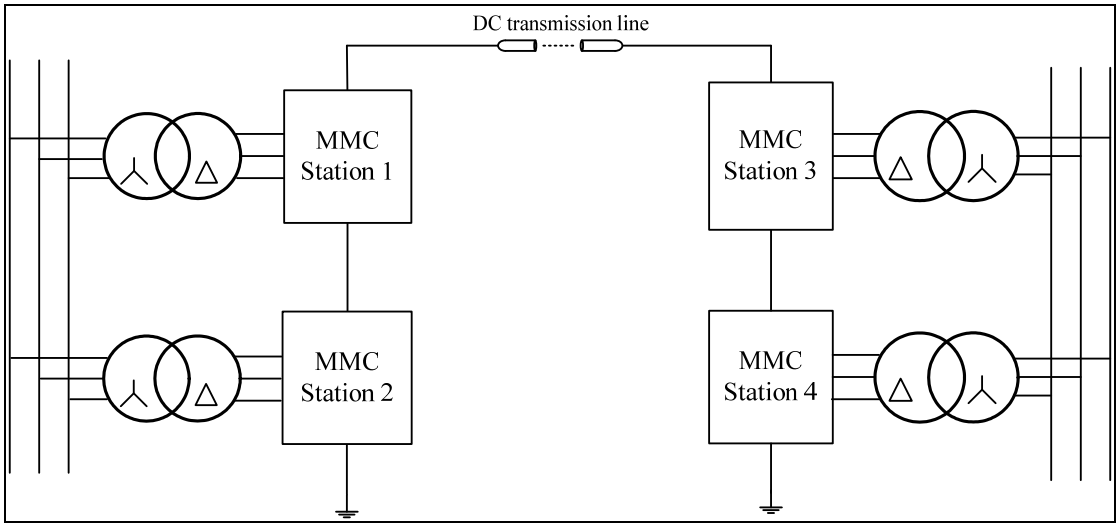

Figure 1.5 Three-parallel phase MMC stations based HVDC (one pole)
Adapted from Wang, Hao et Ooi (2013)

However, MMC for UHVDC applications, the weight and size of the power module capacitors of the converters are big trouble since a large quantity of capacitors is needed to form the whole converter stations. At the same time, MMC cell capacitor only conducts single phase AC current, which is intrinsic drawback of MMC topology. Therefore, compared with 12-pulse bridge thyristor converter and MMC stations for UHVDC application, two-level VSC modules based station is a good option.

The success in UHVDC depends on industry having the knowledge in insulation and co-ordination in connecting two 400 kV or 500 kV thyristor converter stations in series to bring the DC voltage up to 800 kV or more, for example. In particular, the transformer insulation of the converter station of the higher DC voltage level must be able to withstand the peak AC voltage together with the 400 or 500 kV DC upon which the converter station is connected to. This knowledge on high voltage insulation already exists and in view of the fact that VSC-HVDC stations are reaching high power and high DC voltage ratings. For example, the Caprivi Link is rated at 600 MW at ±350 kV (Magg et al., 2012b) and the EirGrid East-West Interconnector is rated at 500 MW, at ±200 kV (Egan et al., 2013). Hence, the feasibility study of connecting VSC-HVDC stations in series to form VSC-based UHVDC is one of the research contents, which will be presented in Chapter 4.

CHAPTER 2

A COMPARATIVE STUDY OF CONTROL SCHEMES FOR VSC-HVDC TRANSMISSION SYSTEM

2.1 Introduction

Voltage Source Converter (VSC) based High Voltage Direct Current (HVDC) transmission is an electrical transmission technology that has received considerable attention due to the rapid development of modern power electronics technology (Asplund, 2000; Bahrman et Johnson, 2007; Zhang, Harnefors et Nee, 2011). The VSC-HVDC system which employs Insulated Gate Bipolar Transistor (IGBT) and Pulse Width Modulation (PWM) switching techniques, offers a number of advantages over the conventional Line Commutated Converter based HVDC (LCC-HVDC) systems (Mauricio et Exposito, 2006; Venkataramanan et Johnson, 2003; Weimers, 1998), such as no need of external voltage source for commutation, fast and independent control of reactive and active power, independent control of reactive power flow at each AC network, feeding weak AC systems or even passive loads, high quality power with less harmonics distortion, and so on.

To date, many articles related to the modeling, control, and application of VSC-HVDC systems were reported. For example, a dynamic model for a back-to-back HVDC system based on the three-level neutral point diode Clamped (NPC) topology was presented in (Yazdani et Iravani, 2006) and (Zhang et al., 2008). In (Zheng et Zhou, 2006), a small signal dynamic model of VSC-HVDC is established. Reference (Yin, G. Y. Li et T. Y. Niu, 2005) presents an equivalent continuous time state-space model of VSC-HVDC in the synchronous dq reference frame. Moreover, many control strategies for VSC-HVDC systems have been developed in (Yin, G. Y. Li et T. Y. Niu, 2005), (Zheng et Zhou, 2006), and (Casoria, 2009). Most of which are double-loop PI controllers. Also, some various nonlinear controllers (Li et al., 2008; Liu et Cai, 2008a; Rashed, El-Anwar et Youssef, 2008) have been investigated. An inner current control loop was designed for a digital control implementation when the converter is connected to a very strong AC network in (Lindberg et Lindberg, 1995), and

(Ouquelle, Dessaint et Casoria, 2009). And an outer PI controller combination of an inner deadbeat current controller is used for power converters in (Fu et al., 2011) to reach good performance for VSC-HVDC system. Recently, power-synchronization control is investigated for VSC-HVDC links connected to weak AC system (Zhang, Harnefors et Nee, 2011). So far, on the practical application side most of the VSC-HVDC projects are still point-to-point DC transmission. Reference (Prieto-Araujo et al., 2011) mentioned some important projects involving HVDC multi-terminal transmission are currently under study.

As reviewed above, the control system of the VSC-HVDC is based on an inner current control loop and slower outer controllers. Due to the choice of outer controllers depending on the application (Du, Agneholm et Olsson, 2008), the focus of this chapter is devoted to comparative study on inner control algorithms. The objective of the comparative study is to show the good dynamic behavior of the VSC-HVDC systems.

This Chapter is organized as below: Section 2.2 briefly describes the configuration and modeling of the VSC-HVDC system. Three inner control schemes are presented and compared in section 2.3. In section 2.4, case studies on three control schemes for the VSC-HVDC system under different operating conditions are done to show the good dynamic behavior of the VSC-HVDC systems. Finally, conclusions are drawn in section 2.5.

2.2 Configuration and modeling

2.2.1 VSC-HVDC configuration

The configuration of a typical two-terminal VSC-HVDC system is shown in Figure 2.1. The VSC-HVDC has two identical back-to-back VSC stations, which are linked with a DC bus. Reactors are the ties of power changes between VSC and AC system. The AC filters are placed to absorb high frequency harmonics.

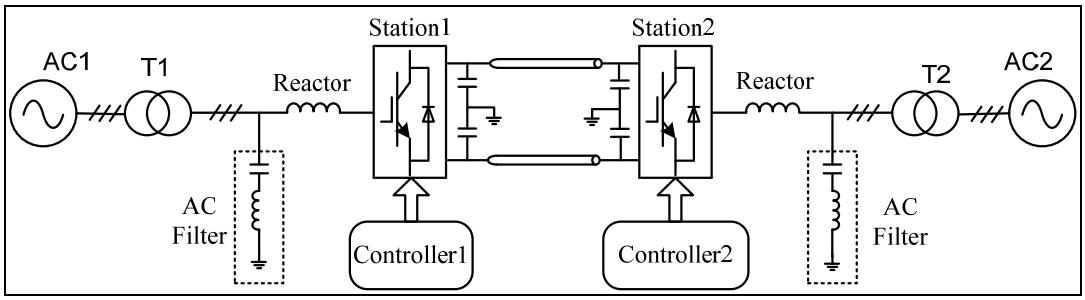

Figure 2.1 Configuration of a two-terminal VSC-HVDC system

2.2.2 Dynamic model of VSC

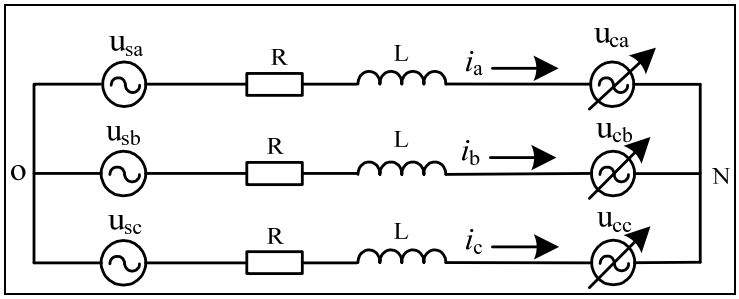

Figure 2.2 Equivalent circuit of VSC

Figure 2.2 shows a general equivalent circuit for the VSC used in the above HVDC transmission system, where u_{sa}, u_{sb} and u_{sc} are balanced three-phase AC network voltages with $u_{sa} + u_{sb} + u_{sc} = 0$; u_{ca}, u_{cb} and u_{cc} are the VSC's output PWM voltages; N is the midpoint DC bus; L is the reactor inductance; R is the reactor resistance; and the VSC could be a two-level converter, a three-level converter, or a multi-level converter. Therefore, the dynamic model of VSC as shown in Figure 2.2 can be described as follows:

$$\begin{pmatrix} \dot{i}_a \\ \dot{i}_b \\ \dot{i}_c \end{pmatrix} = \begin{pmatrix} -R/L & 0 & 0 \\ 0 & -R/L & 0 \\ 0 & 0 & -R/L \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + \begin{pmatrix} (u_{sa} - u_{ca})/L \\ (u_{sb} - u_{cb})/L \\ (u_{sc} - u_{cc})/L \end{pmatrix} \tag{2.1}$$

The output equation can be written as:

$$y = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \tag{2.2}$$

The output PWM voltages of VSC can be expressed as:

$$u_{cj} = (1/2) u_{dc} s_j \tag{2.3}$$

Where, u_{dc} is DC bus voltage and s_j (j = a, b, c) are switching functions. For a two-level PWM modulator, the switching functions s_j = +1 or s_j = -1 (shown in Figure 2.3 a)); for a three-level PWM modulator, s_j = +1, s_j = 0 or s_j = -1 (shown in Figure 2.3 b)). The amplitude and phase angle of the three-phase AC currents i_a, i_b and i_c can be controlled by regulating the fundamental components in VSC's output PWM voltages. Therefore, the active and reactive power flow can be controlled by regulating the outputs of VSC.

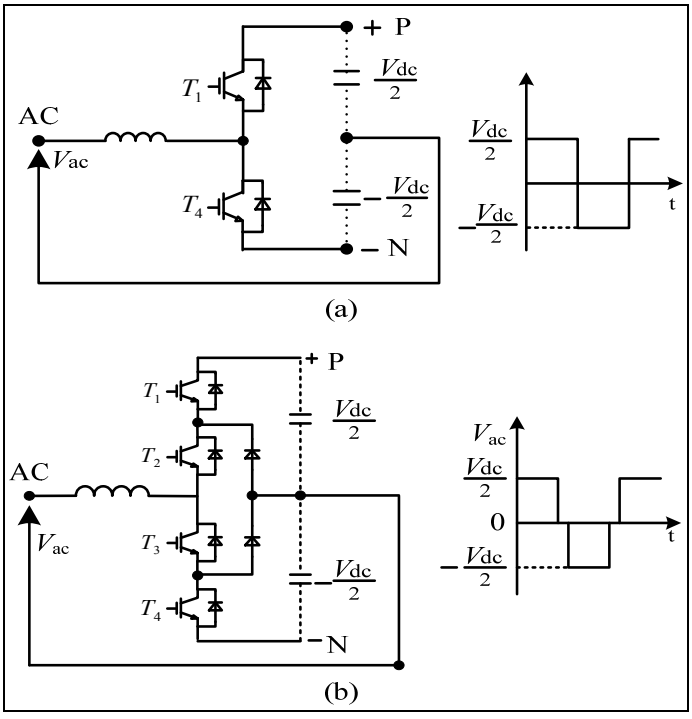

Figure 2.3 Principle of VSC
(a) Principle of the 2-level VSC; (b) Principle of the 3-level VSC

2.3 Control scheme for VSC-HVDC system

2.3.1 Overall control description

Generally speaking, the control system of the VSC-HVDC is based on fast inner current loop and slower outer power or DC voltage control, which supply the current references for the inner control loop (Du et al., 2007; Du, Agneholm et Olsson, 2008). For a normal operation of two terminal VSC-HVDC transmission, one VSC station will work in DC voltage and reactive power or AC voltage control mode, where VSC is used to maintain constant DC bus voltage and send required reactive power to its connected AC power network; whereas the other VSC station will operate in active power and reactive power or AC voltage control mode, where VSC is employed to regulate active and reactive power flow as required. The overall control of the two-terminal VSC-HVDC system is already shown in Figure 1.3 in Chapter 1.

According to the three-phase instantaneous power theory, the active power P and reactive power Q on the AC side of VSC, which is in the *abc* coordinates, can be expressed as:

$$\begin{cases} P = u_{sa}i_a + u_{sb}i_b + u_{sc}i_c \\ Q = \left[\left(u_{sa} - u_{sb}\right) i_c + \left(u_{sb} - u_{sc}\right) i_a + \left(u_{sc} - u_{sa}\right) i_b \right] / \sqrt{3} \end{cases} \tag{2.4}$$

Using coordinates transformation, (2.4) in the synchronous rotating *dq* coordinates can be rewritten as:

$$\begin{cases} P = u_{sd}i_d + u_{sq}i_q \\ Q = u_{sq}i_d - u_{sd}i_q \end{cases} \tag{2.5}$$

Where, u_{sd} and u_{sq} are the *d*-axis component and *q*-axis component of AC network voltage vector. Since the three-phase voltages of the AC network are assumed to be balanced, we

will have $u_{sd} = U_s$ and $u_{sq} = 0$, where U_s is the length of $\vec{U}_s$. Therefore, (2.5) can be deduced as:

$$\begin{cases} i_d = (1/u_{sd})P \\ i_q = -(1/u_{sd})Q \end{cases} \tag{2.6}$$

From (2.6), it can be seen that the active power P and the reactive power Q on AC side of VSC can be independently controlled by regulating i_d and i_q respectively (Flourentzou, Agelidis et Demetriades, 2009).

In the following sections, we focus on developping the conventional PI decoupling control scheme, hysteresis current control scheme, and deadbeat current control scheme for the VSC-HVDC system.

2.3.2 Conventional PI decoupling control scheme

The PI control scheme, which is adopted for comparison is given in Figure 2.4 and Figure 2.5. L_{id} and L_{iq} are decoupling compensation components; u_{sd} and u_{sq} are feed forward compensation components. As known to all, the transformation matrices are required to transform voltages and currents in the *abc* coordinate to the synchronously rotating *dq* coordinate and later to make the inverse transformation of the current references in the *dq* coordinate back to the *abc* coordinate.

In this control scheme, the voltages and currents need to be transformed several times. One side VSC works in VQ mode for the regulation of DC bus voltage V_{dc} and reactive power Q, and the other side VSC will operate in PQ mode for the regulation of active power P and reactive power Q, and vice versa. The PI control scheme achieved decoupled control of active and reactive power.

According to (2.6), reference currents (i_{dref}, i_{qref}) can be obtained from the corresponding reference active and reactive power (P_{ref}, Q_{ref}). Then, i_{dref} and i_{qref} are inputs of the inner PI current controller. The diagram of PI decoupling control scheme for VSC in PQ control mode is shown in Figure 2.4.

At the same time, the function of VSC in VQ control mode is to maintain constant DC bus voltage and regulate the reactive power Q as required. Figure 2.5 shows the PI control scheme for VSC in VQ control mode. The proposed control scheme is a double-loop PI control structure: a PI controller is used for outer-loop DC voltage regulation, and a PI current controller is used for inner-loop current regulation. The *d*-axis reference current i_{dref} is the output of outer-loop PI controller as follows:

$$i_{dref} = K_p(u_{dcref} - u_{dc}) + K_I \int (u_{dcref} - u_{dc})dt \tag{2.7}$$

Where, u_{dcref} is the DC bus reference voltage. And the Q control mode is the same as VSC in PQ control mode. The signal θ comes from phase locked loop (*PLL*) which generates signals synchronized to the AC network voltages.

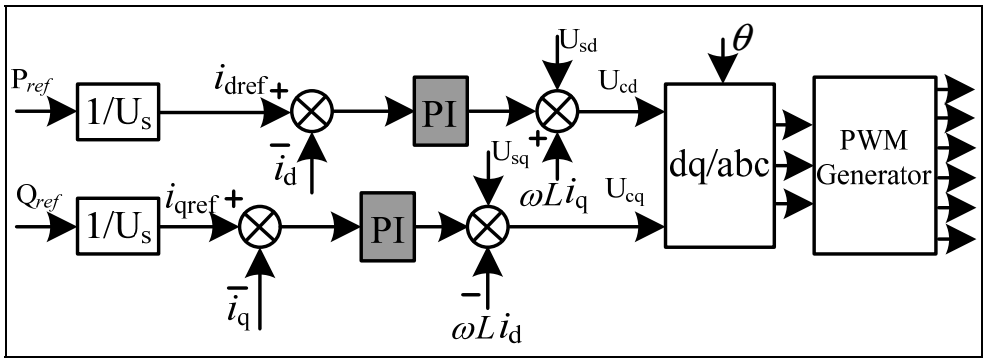

Figure 2.4 PI control scheme for VSC in PQ control mode

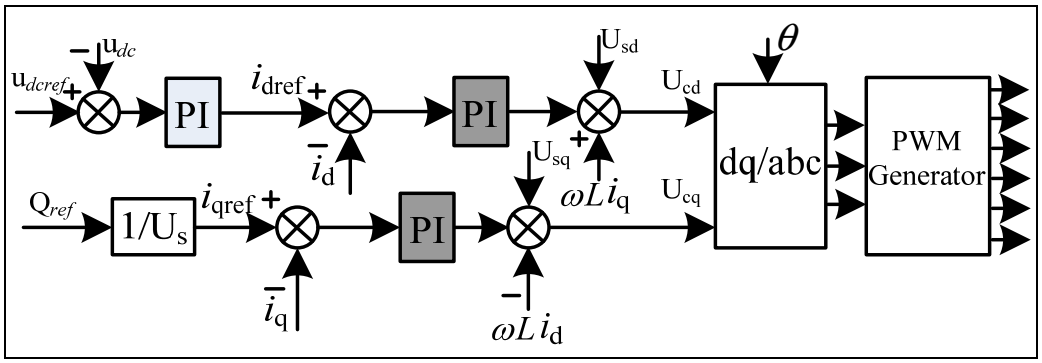

Figure 2.5 PI control scheme for VSC in VQ control mode

2.3.3 Hysteresis current control scheme

The hysteresis current control (HCC) scheme, which is adopted for comparison, is given in Figure 2.6 and Figure 2.7. Where, Figure 2.6 shows the diagram of HCC scheme for VSC in PQ control mode and Figure 2.7 shows the diagram of HCC scheme for VSC in VQ control mode.

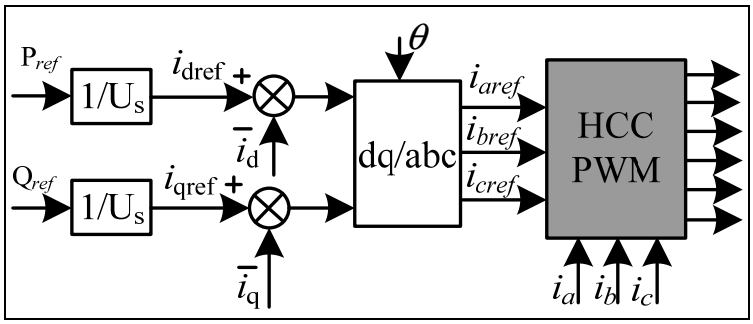

Figure 2.6 HCC scheme for VSC in PQ control mode

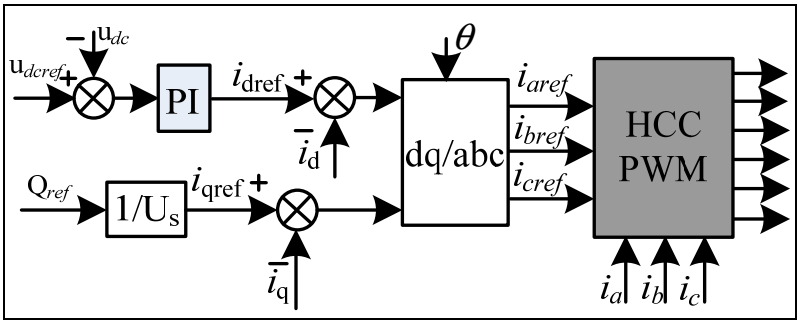

Figure 2.7 HCC scheme for VSC in VQ control mode

The source of the reference currents (i_{dref}, i_{qref}) not only in PQ control mode but also in VQ control mode is obtained in the same way as described in conventional PI decoupling control scheme section. But here the reference currents (i_{dref}, i_{qref}) should be further transformed into reference currents (i_{aref}, i_{bref}, i_{cref}) by using dq/abc transformation in order to provide the reference current inputs of the inner hysteresis controller.

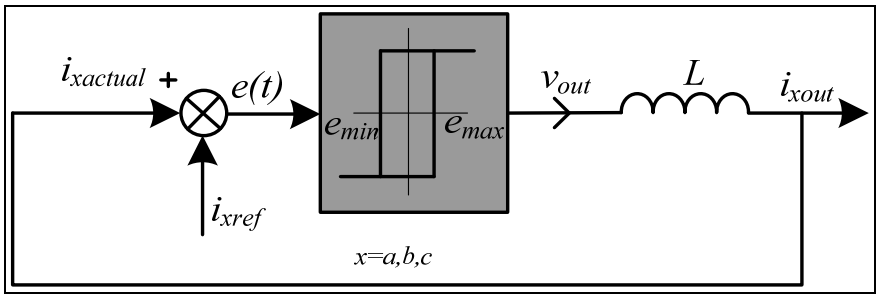

Figure 2.8 Diagram of hysteresis current controller

The hysteresis current controller is implemented with a closed loop control system and the diagram of hysteresis current controller is shown in Figure 2.8. The error signal, $e(t)$, is the difference between the reference current, i_{xref}, and the measured current, $i_{xactual}$. When error reaches an upper limit e_{max}, the transistors are switched to force the current decrease, and when the error reaches a lower limit the current is forced to increase. Hysteresis band, which is the difference between the maximum value of the error signal and the minimum value of the error signal, directly decides the amount of ripple in output current. Similarly, the signal θ comes from PLL. By using PLL, the effect of signal interference between phases can be reduced.

2.3.4 Deadbeat current control scheme

The deadbeat (DB) current control scheme, which is adopted for comparison is given in Figure 2.9 and Figure 2.10.

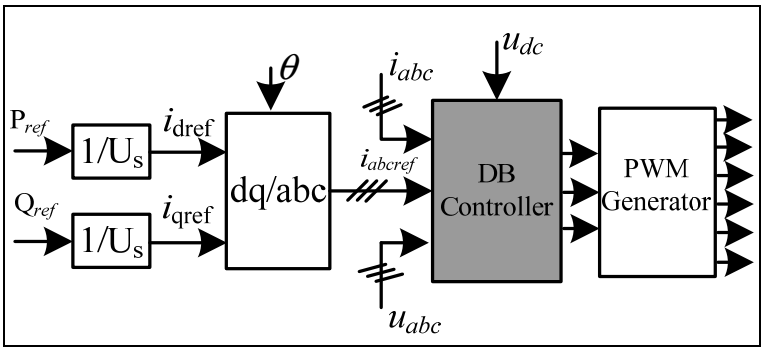

Figure 2.9 DCC scheme for VSC in PQ control mode

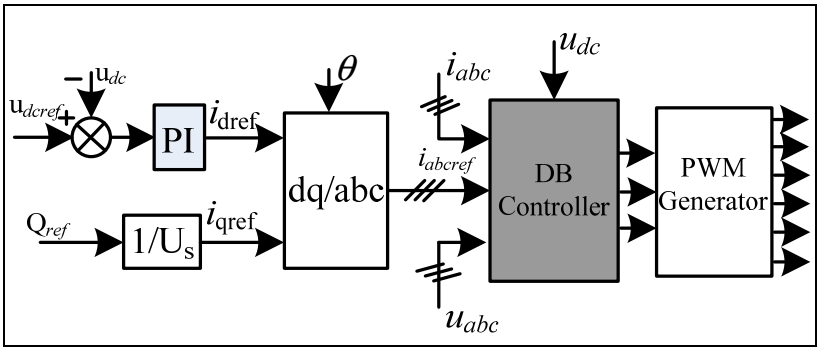

Figure 2.10 DCC scheme for VSC in VQ control mode

In this control scheme, the outer controller of deadbeat current control scheme is exactly the same as for the hysteresis current control scheme, as seen in the Figure 2.9 and Figure 2.10. The inner is a deadbeat current controller and the controller is designed as below.

At the time $t = (n + 1)$ T, the corresponding sampled-data equations of (2.1) can be expressed as follows:

$$i_j(n+1) = ((b_1 - b_2)/b_1) * i_j(n) + \left(u_{sj}(n) - v_j(n) * (u_{dc}(n)/2)\right)/b_1 \qquad (2.8)$$

where $v_j(n)$ is the phase j output control signal at the time $t = n$ T with $-1 \leq v_j(n) \leq 1$ and the subscript $j = a, b, c$; $u_{dc}(n)$ is DC bus voltage at the time $t = n$T; $b_1 = Ln/T$; $b_2 = Rn$; Ln and Rn are the nominal value of L and R respectively as shown in Figure 2.2; T is the sampling

period. Obviously, equation (2.8) can be regarded to be three independent subsystems. From (2.8), the corresponding transfer function of the current loop can be expressed as follows:

$$G_i(z) = i_j(z) \big/ i_{jref}(z) = 1/z \tag{2.8}$$

Thus, a deadbeat current controller is obtained:

$$v_j(n) = 2\left(u_{sj}(n) - b_1 i_{jref}(n) + (b_1 - b_2) i_j(n)\right) \big/ u_{dc}(n) \tag{2.9}$$

A more detailed description of the inner deadbeat current control system can be found in (Fu et al., 2011).

2.3.5 Comparison of the three control schemes

In the above paragraphs of this section, we present the PI decoupling control scheme, hysteresis current control scheme, and deadbeat current control scheme respectively.

PI control is one of the most popular control schemes applied for most industrial control systems. The characteristics of PI controller have zero steady state error, maximum overshoot and high settling time. Generally, PI control requires tuning several control coefficients, especially for double close-loop PI control, which is not an easy task.

For comparison, HCC scheme are studied for VSC-HVDC system due to its excellent dynamic performance and low complexity of implementation (Dalessandro et al., 2005). However, it will increase switch loss in the converter with random switching frequency.

Furthermore, compared with the above two methods, the third control scheme deadbeat current control scheme as shown in (2.10) is investigated. The advantages of the deadbeat current control scheme for the VSC-HVDC system is that it offers fast dynamic response and high steady-state tracking accuracy with only one sampling time delay. Moreover, the

promising advantages of deadbeat current control are simple control structure and algorithms. However, the deadbeat current controller is based on an accurate nominal model of the converter (Zhou et Danwei, 2001). In practice, there may be uncertainties in the converter parameters.

From the three control schemes comparison, we can see that the HCC and deadbeat control scheme take less coordinate transformation steps, and thus less impact by the PLL performance than PI controller does. In view of the different characteristics of these three control schemes, a further comparison study of the three control schemes in the same VSC-HVDC system are presented in the following section.

2.4 Case studies

This section shows the dynamic behavior of the system during startup, AC voltage sags and power reversal. A case of two-terminal IGBT VSC-HVDC system as shown in Figure 2.1 is developed in MATLAB/Simulink, where VSC station 1 will work in VQ control mode and VSC station 2 will operate in PQ control mode. In this case, note that the AC filters are excluded in the simulation system. Different operation cases are studied and described in the following subsections with PI decoupling control scheme, hysteresis current control scheme, and deadbeat current control scheme, respectively. A comparison analysis is made between these three control schemes.

The parameters of the VSC-HVDC systems are listed in Table 2.1.

Table 2.1 Parameters of the VSC-HVDC system

Parameters	**Unit**	**Value**
AC rated voltage(U_{s1})	*kV*	100
Reactor resistance (*R*)	Ω	0.075
Reactor inductance (*L*)	*H*	0.0024
DC base voltage (U_{dcref})	kV	100
DC capacitance (*C*)	*F*	70e-6
DC-cable resistance (R_1)	Ω/km	13.9e-3
DC-cable inductance (L_1)	H/km	0.159e-3
DC-cable capacitance (C_1)	F/km	2.3e-3
Base power (S_{base})	MVA	100

2.4.1 Startup and steady state response test

Figure 2.11 to Figure 2.13 show the startup responses with PI decoupling control scheme, HCC scheme, and deadbeat control scheme respectively. From the simulation results, it can be seen that although the DC voltage has a reasonable over voltage at the beginning, all the controlled variables P_2, Q_2, Q_1, and U_{1dc} follow their reference values in good dynamic performance and in good decoupling control of active and reactive power. In comparison, the waveforms of voltage and power with the deadbeat control scheme are smoother than the others does.

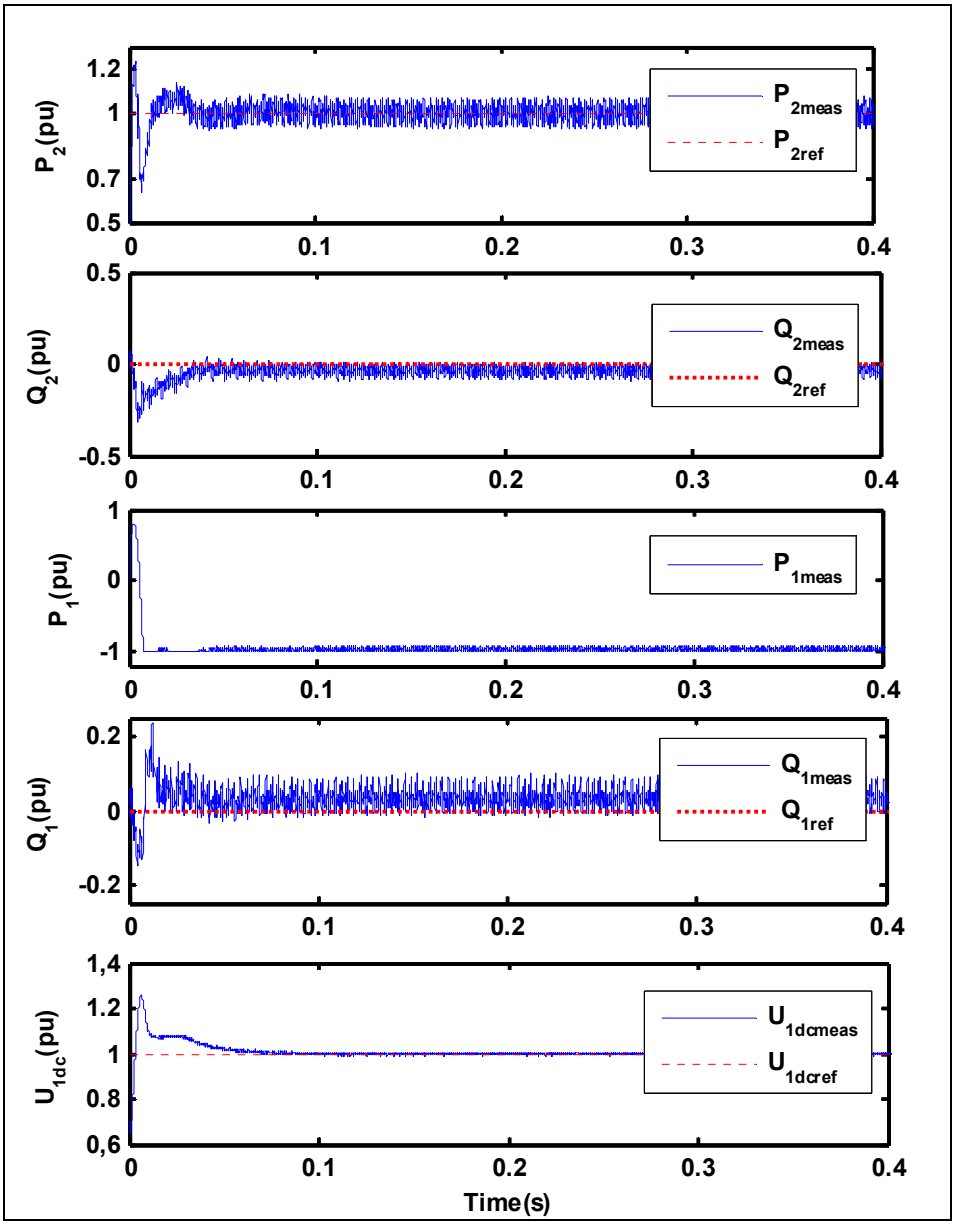

Figure 2.11 Startup and steady state responses for PI decoupling control scheme

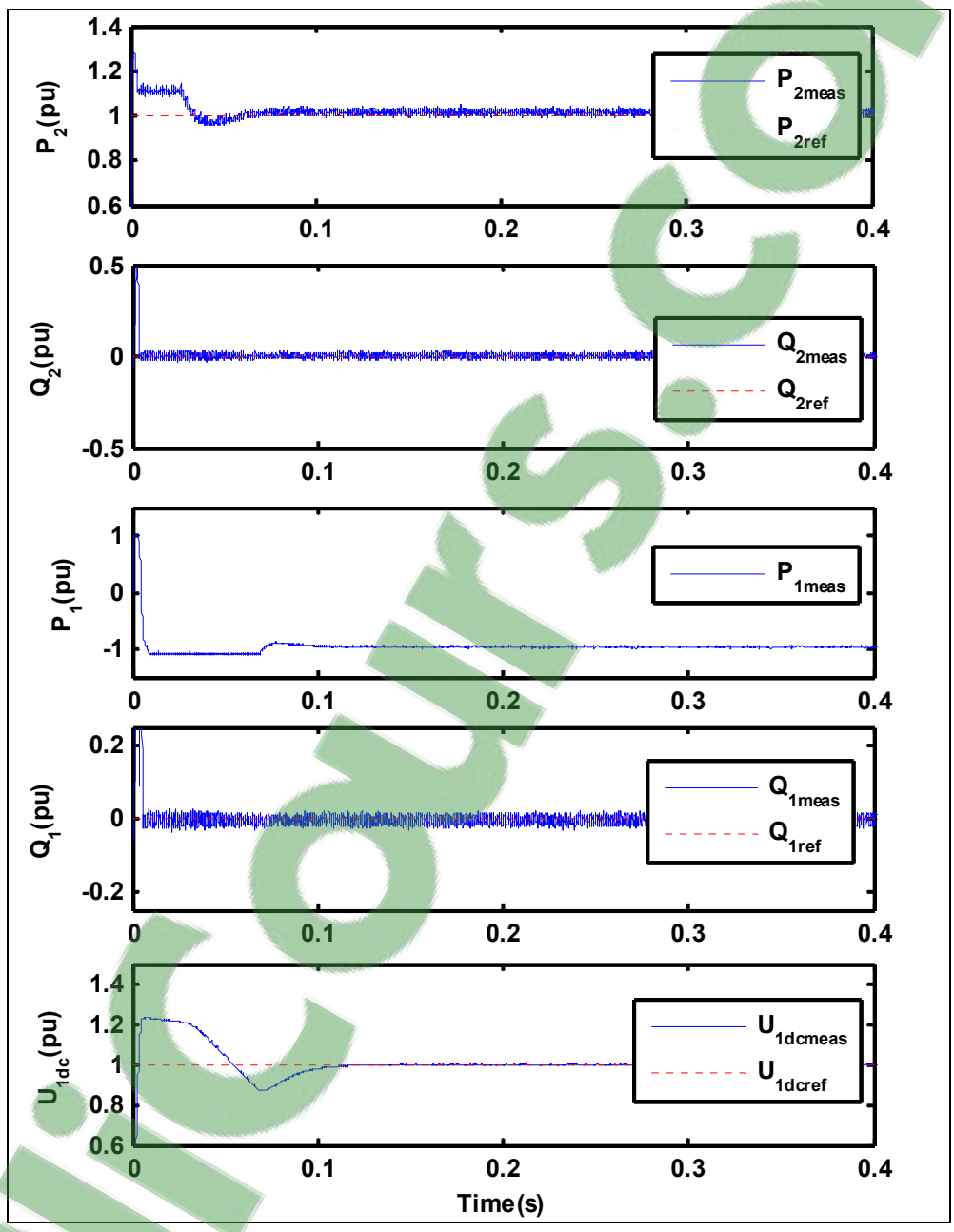

Figure 2.12 Startup and steady state responses for HCC scheme

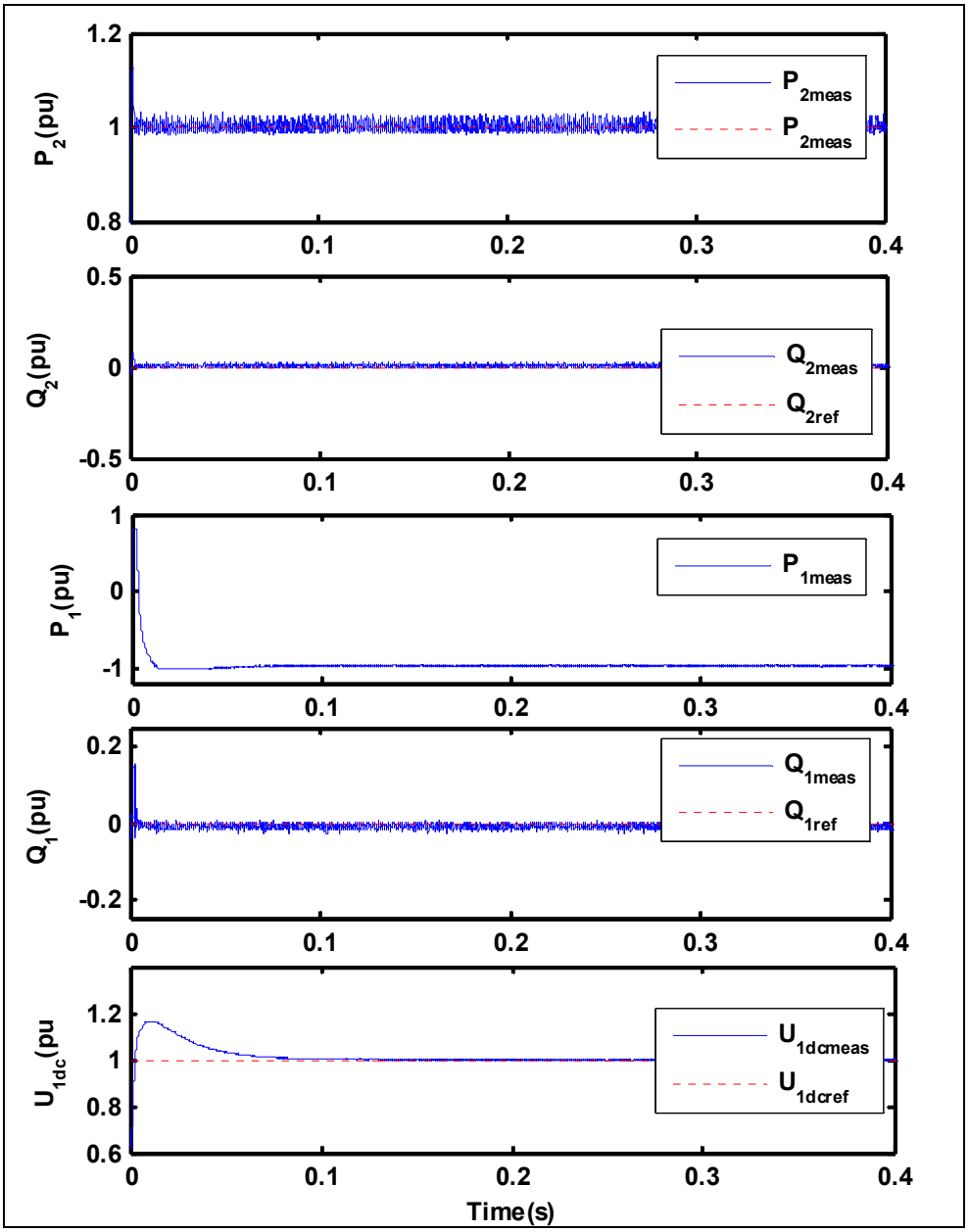

Figure 2.13 Startup and steady state responses for DB control scheme

2.4.2 AC Side voltage sag test

Figure 2.14 to Figure 2.16 show the AC voltage sag responses with PI decoupling control scheme, HCC scheme, and deadbeat control scheme respectively. In this test, the AC voltage

sag (0.5 pu) is applied to VSC 2 AC voltage magnitude for time period of 100 *ms*. The voltage step change started at t = 0.5 *s* and removed at t = 0.6 *s*.

From the results, it can be seen that the controlled variables has better dynamic performance for the deadbeat control scheme than for the other conventional PI control scheme and HCC scheme.

Notice that when the AC voltage sags, the active power has corresponding sags which result from direct implementation of (2.6) instead of an outer power feedback controller.

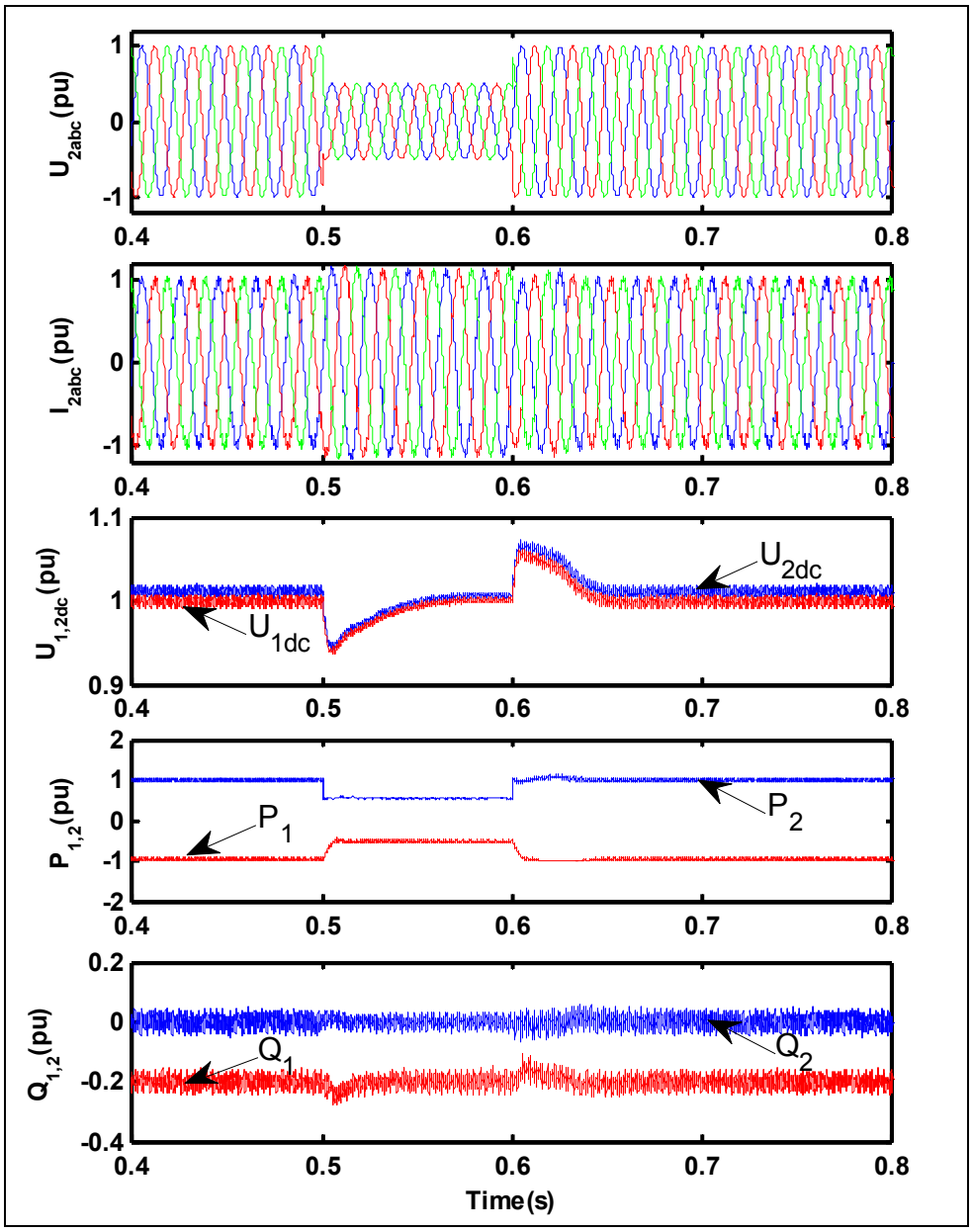

Figure 2.14 AC voltage sag test for PI decoupling control scheme

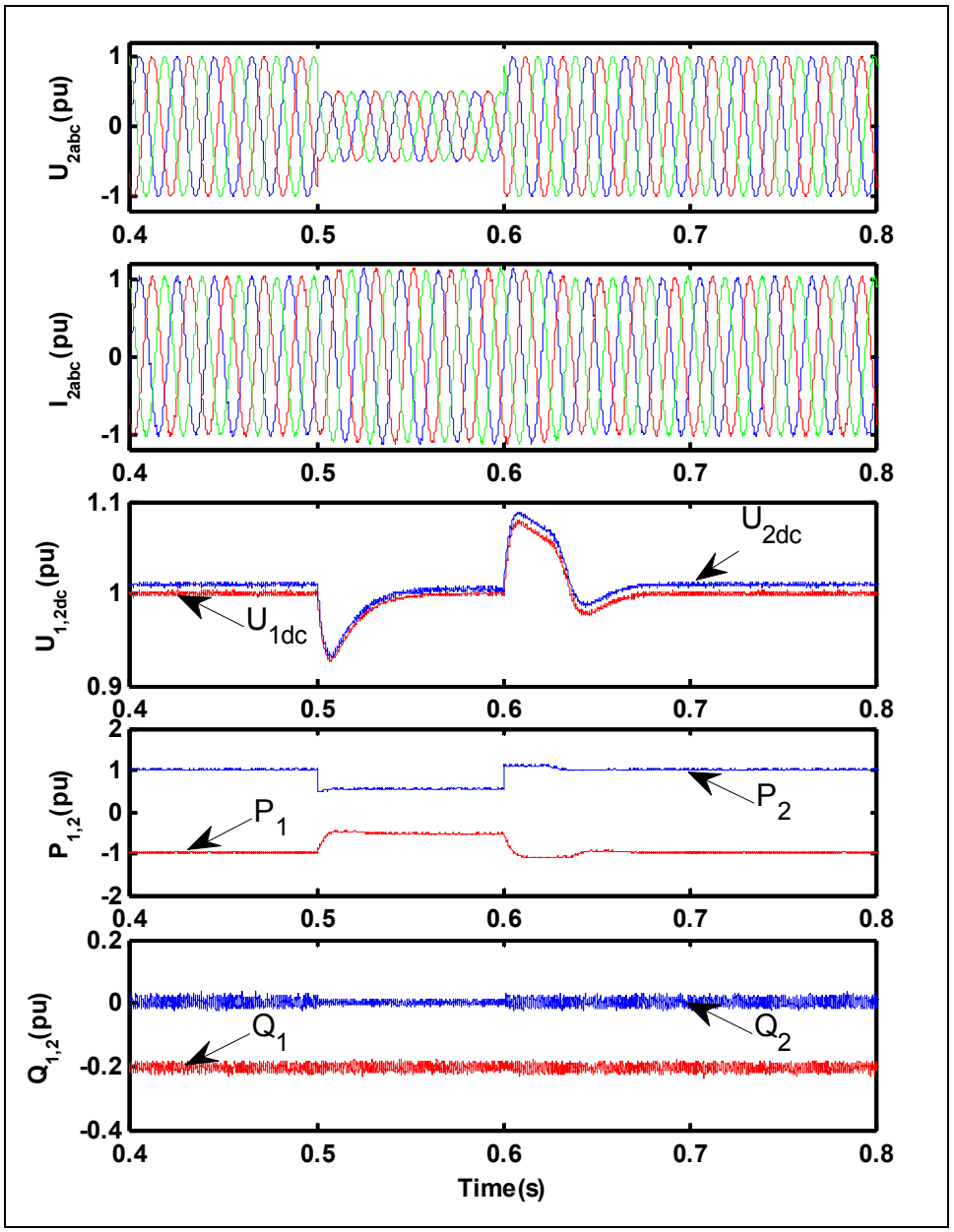

Figure 2.15 AC voltage sag test for HCC scheme

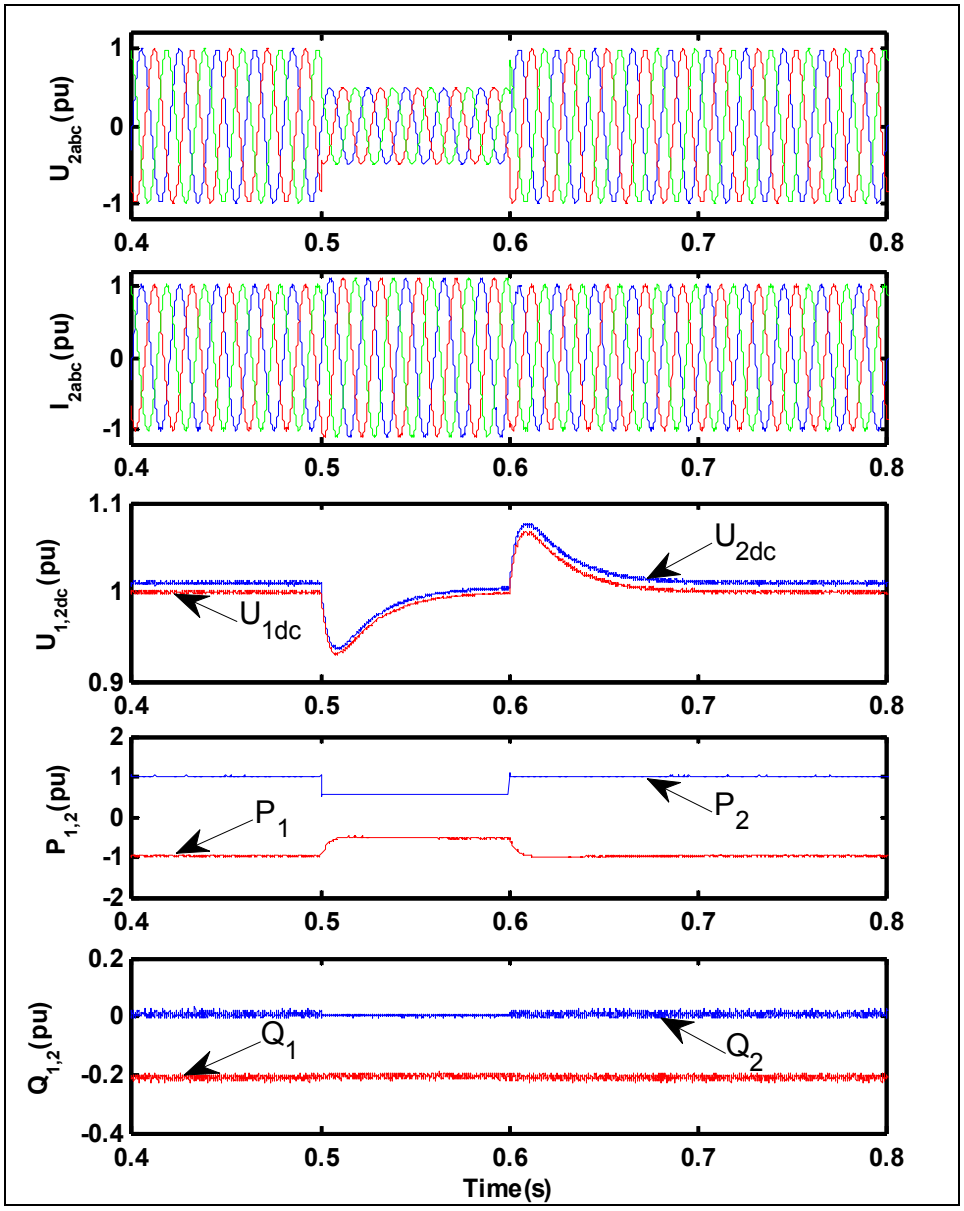

Figure 2.16 AC voltage sag test for DB control scheme

2.4.3 Power reversal test

Figure 2.17 shows the power reversal under sudden changes of active power flows for the conventional PI decoupling control scheme. At t = 0.6 s, the reference value of P_2 is suddenly reversed from 1.0 pu to −1.0 pu and then returned back to its original value at t = 0.8 s. Under the same operating conditions, the active power reversal test has been performed for

HCC scheme and deadbeat control scheme respectively in the VSC-HVDC system as shown in Figure 2.18 and Figure 2.19.

It is noted that P and Q exactly reach their reference values in the transient and steady state expect undesirable spikes exist in Q_2 at $t = 0.6$ s and $t = 0.8$ s. It is also noted that undesirable spikes exist in Q_2 and Q_1 waveforms and 0.3 pu DC voltage fluctuations exists in U_{1dc} after the second power reversal at $t = 0.8$ s. So, it is obvious from the results that the deadbeat control scheme works best and has better dynamic performance during active power reversal period and dynamic performance of HCC scheme is similar but worse with that of deadbeat control scheme.

Moreover, the decoupling performance of the P and Q are better with deadbeat control scheme for this system.

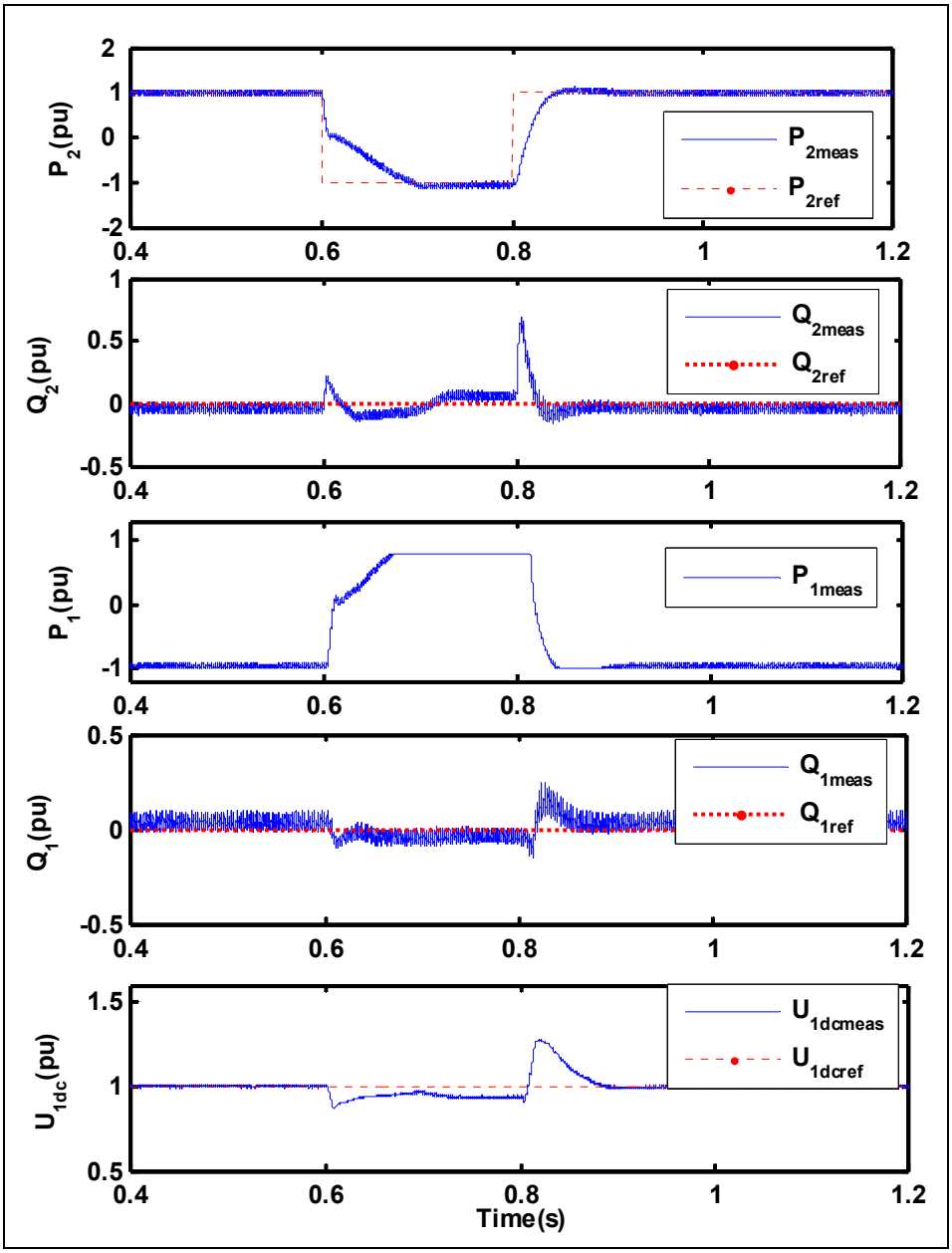

Figure 2.17 Power reversal test for PI decoupling control scheme

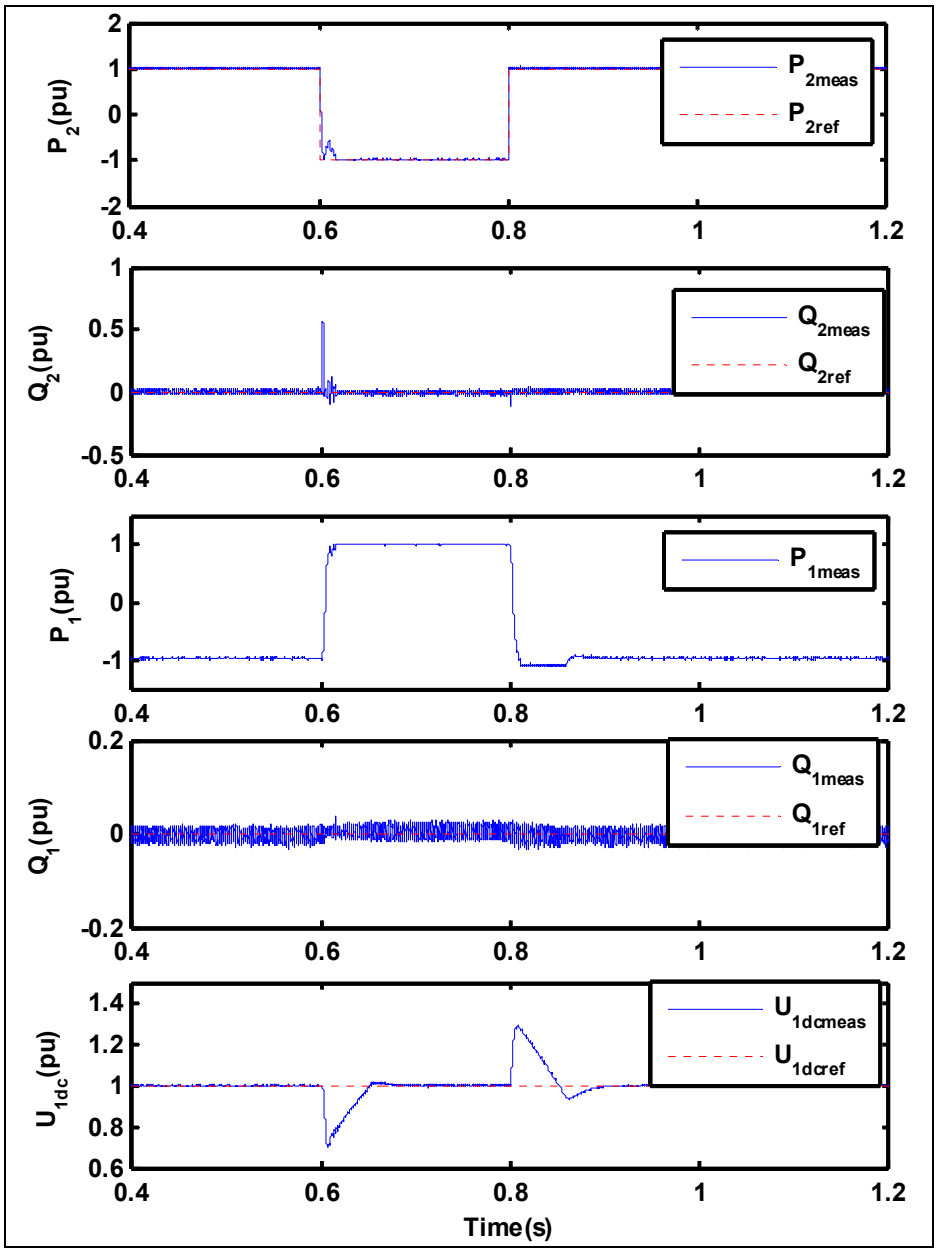

Figure 2.18 Power reversal test for HCC scheme

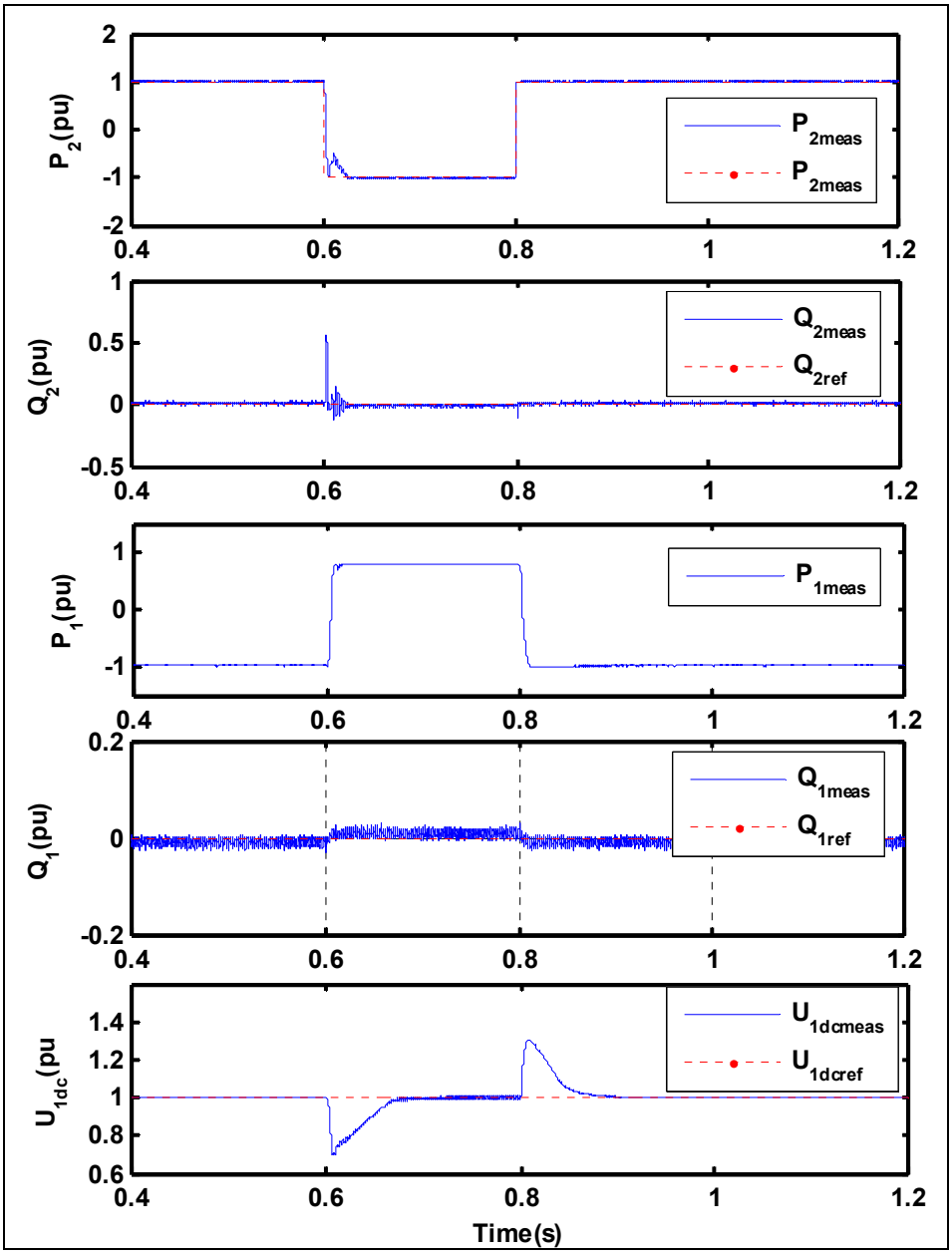

Figure 2.19 Power reversal test for DB control scheme

In short, from Figure 2.11 to Figure 2.19, we can conclude that the deadbeat control scheme for the VSC-HVDC works best and offers high tracking accuracy, fast dynamic response, and the best *P* and *Q* decoupling control. What's more, the dynamic performances of HCC scheme and deadbeat control scheme are more or less similar in three simulated cases.

Though PI control scheme for the VSC-HVDC works well, but the dynamic performance for PI control scheme is not as good as for the deadbeat control scheme.

2.5 Conclusion

In this chapter, a comparison of the conventional PI decoupling control scheme, hysteresis control scheme, and deadbeat control scheme is presented for the VSC-HVDC system and the system is implemented under different operating conditions to show the different dynamic performances. The following conclusions are drawn by the analysis:

1) In comparison, the conventional PI controller performs relatively poor.
2) The dynamic performances of hysteresis control scheme and deadbeat control scheme are more or less similar in the simulated cases. However, the deadbeat control scheme shows the merits of not only the best dynamic performance but also the best decoupling performance, which provides a good high performance control solution to VSC-HVDC systems.

CHAPTER 3

STUDY ON VSC-HVDC SYSTEM WITH CURRENT DEADBEAT CONTROL

3.1 Introduction

Due to the High Voltage Direct Current (HVDC) transmission has the "firewall" function in preventing cascaded AC system outages spreading from one system to another system (Bahrman et Johnson, 2007; Zhang, Harnefors et Nee, 2011); more and more cases such as wind farms, solar power plants use HVDC transmission systems to deliver energy. However, the conventional Line Commutated Converter based HVDC (LCC-HVDC) which commutation of the converter valve is dependent on the stiffness of the alternating voltage supplied by the AC system. Also, the converter cannot work properly if the connected AC system is weak (Zhang, Harnefors et Nee, 2011).

Thus, Voltage Source Converter based HVDC (VSC-HVDC) becomes popular for delivering electric power over long distances (Asplund, 2000; Mauricio et Exposito, 2006; Venkataramanan et Johnson, 2003; Weimers, 1998). The VSC-HVDC which employs Insulated Gate Bipolar Transistor (IGBT) and Pulse Width Modulation (PWM) switching techniques offers some potential advantages over the conventional LCC-HVDC, such as no need of external voltage source for commutation, fast and independent control of reactive and active power, independent control of reactive power flow at each AC network (Schettler, Huang et Christl, 2000), and feeding weak AC systems or even passive loads (Flourentzou, Agelidis et Demetriades, 2009).

So far, many articles associating with the modeling and control of VSC-HVDC system were reported. For instance, a dynamic model for a back-to-back HVDC system based on the three-level neutral point diode Clamped (NPC) topology was presented in (Yazdani et Iravani, 2006) and (Zhang et al., 2008). In (Zheng et Zhou, 2006), a small signal dynamic model of VSC-HVDC is established. Reference (Yin, G. Y. Li et T. Y. Niu, 2005) presents an equivalent continuous time state-space model of VSC-HVDC in the synchronous *dq*

reference frame. Correspondingly, many control strategies of VSC-HVDC systems have been developed, such as PI control scheme (Casoria, 2009; Yin, G. Y. Li et T. Y. Niu, 2005) in *d-q* coordinates, direct current control strategy by regulating the amplitude and phase of the AC side current, and direct power control method (Rahmati, Abrishamifar et Abiri, 2006) using hysteresis with random switching frequency. However, these double-loop PI controllers require tuning four control coefficients, which is not an easy task. And it will increase switch loss in the converter with random switching frequency. Also, various nonlinear controllers (Chen, Zheng et Fan, 2006; Liang et al., 2005; Liu et Cai, 2008a; Rashed, El-Anwar et Youssef, 2008) have been investigated, but the algorithm is complicated. Recently, an inner current control loop was designed for a digital control implementation when the converter is connected to a very strong AC network in (Lindberg et Lindberg, 1995) and (Ouquelle, Dessaint et Casoria, 2009) and a predictive current controller is presented in (Fu, Zhou et Cheng, 2008). However, reference (Fu, Zhou et Cheng, 2008) is more suitable for AC balance system operation, when the AC voltage sags or other perturbations happen the control scheme needs to be improved.

In this chapter, combination of PI controller and advantages of the deadbeat controller such as fast dynamic response, high tracking accuracy, and simple control structure and algorithms with determined parameters, a conventional PI controller is used in the outer loop and a current deadbeat controller is presented in the inner loop. Thus, the VSC-HVDC transmission system not only can achieve fast dynamic response and high tracking accuracy but also can improve the robustness of the control system.

This chapter is organized as follows: Section 3.2 briefly describes the configuration and modeling of the VSC-HVDC system. The proposed control scheme for VSC-HVDC system is developed in section 3.3. In section 3.4, case studies on the VSC-HVDC system are done to evaluate the proposed scheme. Finally, conclusions are drawn in section 3.5.

3.2 Configuration and modeling of VSC-HVDC

A typical VSC-HVDC system is shown in Figure 3.1. The VSC-HVDC has two identical back-to-back VSC stations, which are linked with a DC cable. Reactors are the ties of power exchanges between VSC and AC system. The AC filters are placed to absorb high frequency harmonics. T1 and T2 in Fig.1 are transformers which are used to transform AC voltage into secondary voltage adapted to DC link in converter (Schettler, Huang et Christl, 2000). Transformers can be eliminated for low voltage AC system.

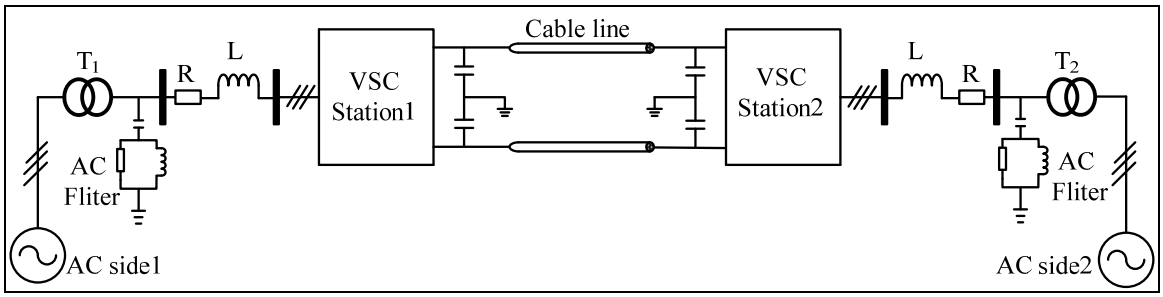

Figure 3.1 Configuration of the VSC–HVDC system

In Figure 3.1 AC side and VSC converter side having the line-to-line AC bus voltage (U_s) and converter AC voltage (U_c) respectively, are interconnected by a line with the reactance X. In steady state ignoring the harmonic components and resistance R, the active power P and reactive power Q absorbed by the VSC, and the voltage U_c are given by the following relations (Flourentzou, Agelidis et Demetriades, 2009; Schettler, Huang et Christl, 2000):

$$P = \frac{U_s U_c}{X} \sin\delta \tag{3.1}$$

$$Q = \frac{U_s\left(U_s - U_c \cos\delta\right)}{X} \tag{3.2}$$

$$U_c = \frac{M}{\sqrt{2}} U_d \tag{3.3}$$

Where U_d is the DC voltage, δ is the phase angle of the fundamental component of PWM, and M is the modulation index of PWM. Thus, it is possible to control P and Q independently by δ and U_c, respectively. The relation between two AC voltages interconnected through a reactor is shown in Figure 3.2. When VSC operates as a rectifier, the converter output AC voltage lags AC bus voltage by an angle δ; When VSC operates as an inverter the converter output AC voltage leads by an angle δ.

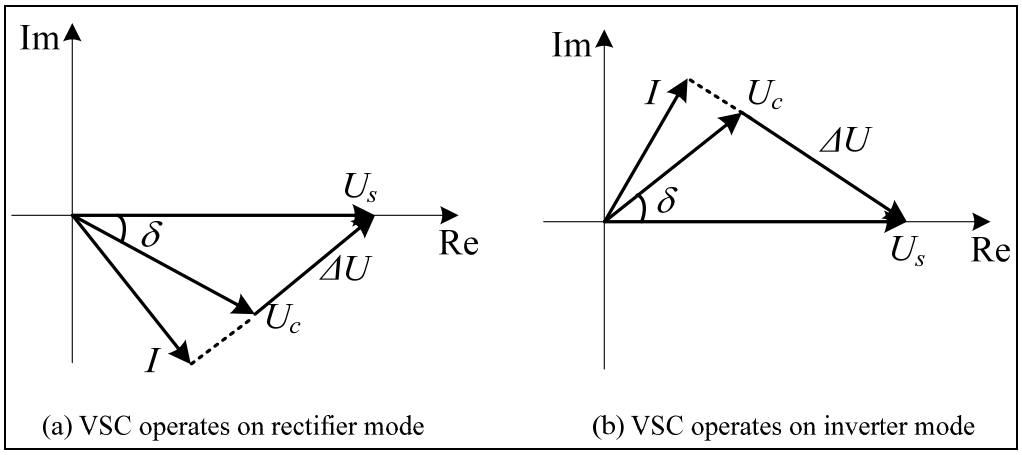

Figure 3.2 Phasor diagram of between U_s and U_c interconnected through a reactor

Figure 3.3 shows the active and reactive power capabilities of the VSC-HVDC system. The VSC can be operated with 1.0 per unit (pu) value being the megavolt amperes rating of each converter (assuming that the HVDC operates in ideal conditions) (Flourentzou, Agelidis et Demetriades, 2009). Comparing with conventional LCC-HVDC transmission, one of the advantages of the VSC-HVDC is the four-quadrant operation which contributes to the VSC-HVDC system having a more flexible controllability.

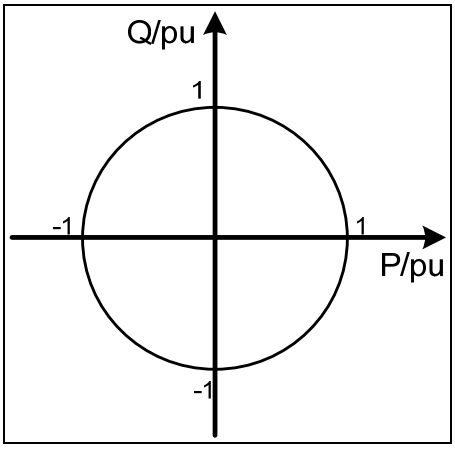

Figure 3.3 P-Q characteristics of
the VSC-HVDC system

For a general VSC used for the above HVDC transmission system, the VSC could be a two-level converter, a three-level converter, or a multi-level converter (Fu, Zhou et Cheng, 2008). The dynamic model of VSC can be described as follows:

$$\begin{pmatrix} \dot{i}_a \\ \dot{i}_b \\ \dot{i}_c \end{pmatrix} = \begin{pmatrix} -\mathrm{R}/L & 0 & 0 \\ 0 & -\mathrm{R}/L & 0 \\ 0 & 0 & -\mathrm{R}/L \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + \begin{pmatrix} (u_{sa} - u_{ca})/L \\ (u_{sb} - u_{cb})/L \\ (u_{sc} - u_{cc})/L \end{pmatrix} \tag{3.4}$$

Where, u_{sa}, u_{sb}, and u_{sc} are balanced three-phase AC network voltages with $u_{\mathrm{sa}} + u_{\mathrm{sb}} + u_{\mathrm{sc}} = 0$; u_{ca}, u_{cb}, and u_{cc} are the VSC's output PWM voltages; L is the reactor inductance; R is the reactor resistance. Therefore, the output PWM voltages of VSC can be expressed as:

$$u_{cj} = (1/2)\, u_{dc} s_j \tag{3.5}$$

Where u_{dc} is the DC bus voltage and s_j (j = a, b, c) are switching functions. The amplitude and phase angle of the three-phase AC currents i_{a}, i_{b}, and i_{c} can be controlled by regulating the fundamental components in VSC's output PWM voltages. Therefore, the DC voltage,

active power and reactive power can be controlled by regulating the outputs of VSC.

3.3 Control scheme for VSC-HVDC

3.3.1 Overall control description

Generally speaking, the control system of the VSC-HVDC is based on a fast inner current control loop controlling the AC current and slower outer controllers, which supply the current references for the inner control loop (Du et al., 2007; Du, Agneholm et Olsson, 2008). For a normal operation of two terminal VSC-HVDC transmission, one VSC station will work in DC voltage and reactive power or AC voltage control mode, where VSC is used to maintain constant DC bus voltage and send required reactive power to its connected AC power network; whereas the other VSC station will operate in active power and reactive power or AC voltage control mode, where VSC is employed to regulate active and reactive power flow as required. The overall outer control system of the two-terminal VSC-HVDC system can refer Figure 1.3 in Chapter 1.

Power-angle control and vector control are the popular existing control methods for VSC-HVDC systems (Zhang, Harnefors et Nee, 2011). In this research, the conventional PI control scheme is used in the outer loop, and the current deadbeat control scheme is presented in the inner loop in order to achieve the fast dynamic response and high tracking accuracy. In the following subsection the outer loop and inner loop controllers are explained in detail.

3.3.2 Outer loop controller

As previously described, the outer loop control mode could be DC voltage, active power, and reactive power or AC voltage control mode. In our case, if VSC station 1 works in DC voltage and reactive power control mode (VQ control mode), VSC station 2 will work in active power and reactive power control mode (PQ control mode); and vice versa. Figure 3.4

shows the outer PI controllers of the VSC-HVDC system. The DC voltage, active power and reactive power control loops are illustrated in Figure 3.4 (a), (b), and (c) respectively.

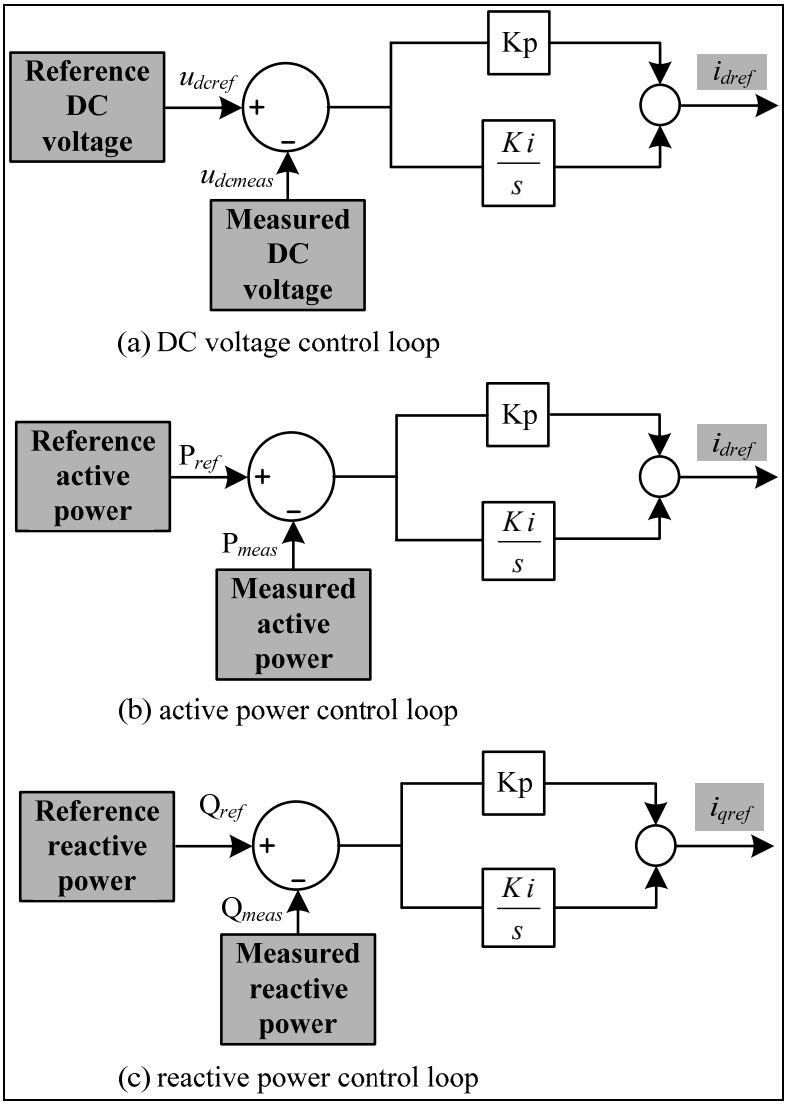

Figure 3.4 Outer loop controllers

The function of VSC in VQ control mode is to maintain constant DC bus voltage and regulate the reactive power Q as required. A PI controller is used for outer-loop DC voltage regulation. The d-axis reference current i_{dref} at this terminal is the output of outer-loop PI controller as follows:

$$i_{dref} = K_p(u_{dcref} - u_{dcmeas}) + K_I \int (u_{dcref} - u_{dcmeas})dt \tag{3.6}$$

Where u_{dcref} and u_{dcmeas} are the DC bus reference voltage and measured voltage, respectively. At the same time, the function of VSC in PQ control mode is employed to regulate active and reactive power flow as required. Also, a PI controller is used for outer-loop active power regulation. The *d*-axis reference current i_{dref} at this terminal is the output of outer-loop PI controller as follows:

$$i_{dref} = K_p(P_{ref} - P_{meas}) + K_I \int (P_{ref} - P_{meas})dt \tag{3.7}$$

Where, P_{ref} and P_{meas} are the reference active power and measured active power, respectively.

The reactive power control loops at each terminal are similar to the active power control loop, except that the P_{ref}, P_{meas}, and i_{dref} are replaced by Q_{ref}, Q_{meas}, and i_{qref}, respectively. However, their control purposes are different. At the PQ control mode terminal, the VSC generates reactive power to ensure that the source voltage and current are in phase, whereas the VQ control mode terminal, the purpose of the reactive power injection is to keep the terminal voltage at the specified level (Liu, Arrillaga et Watson, 2007).

3.3.3 Inner loop current controller

The outputs of the outer loops are the current i_{dref} and i_{qref} which can be further transformed into reference currents (i_{aref}, i_{bref}, i_{cref}) by using dq0/abc transformation as follows:

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta & 1/\sqrt{2} \\ \cos(\theta - 120^\circ) & -\sin(\theta - 120^\circ) & 1/\sqrt{2} \\ \cos(\theta + 120^\circ) & -\sin(\theta + 120^\circ) & 1/\sqrt{2} \end{bmatrix} \tag{3.8}$$

Where θ is phase angle of $\vec{U}_s$. Therefore, the independent regulation of the active power P and the reactive power Q can be implemented by forcing the three-phase AC currents (i_a, i_b, and i_c) to track the reference currents (i_{aref}, i_{bref}, and i_{cref}) in the static abc coordinates. We know, at the time $t = (n + 1)$ T, the corresponding sampled-data equations of (3.4) can be expressed as follows (Wu, Dewan et Slemon, 1991):

$$i_j(n+1) = \frac{b_1 - b_2}{b_1} i_j(n) + \frac{1}{b_1}\left[u_{sj}(n) - \frac{u_{dc}(n)}{2} v_j(n)\right] \tag{3.9}$$

where $v_j(n)$ is the phase j output control signal at the time $t = n\ T$ with $-1 \leq v_j(n) \leq 1$ and the subscript $j = a, b, c$; $u_{dc}(n)$ is DC bus voltage at the time $t = nT$; $b_1 = L_n/T$; $b_2 = R_n$; L_n and R_n are the nominal value of L and R respectively; T is the sampling period. Obviously, equation (3.9) can be regarded to be three independent subsystems. From (3.9), if $i_j(n+1) = i_{jref}(n)$, the corresponding transfer function of the current loop can be expressed as follows:

$$G_i(z) = i_j(z) / i_{jref}(z) = 1/z \tag{3.10}$$

Thus, a current deadbeat controller is obtained:

$$v_j(n) = \frac{2}{u_{dc}(n)}\left[u_{sj}(n) - b_1 i_{jref}(n) + (b_1 - b_2) i_j(n)\right] \tag{3.11}$$

Figure 3.5 shows the current loop deadbeat controller. The current deadbeat controller in (Fu, Zhou et Cheng, 2008)is called the current predictive controller. It takes one sampling period for the 3-phase current (i_a, i_b, i_c) to track their reference commands (i_{aref}, i_{bref}, i_{cref}).

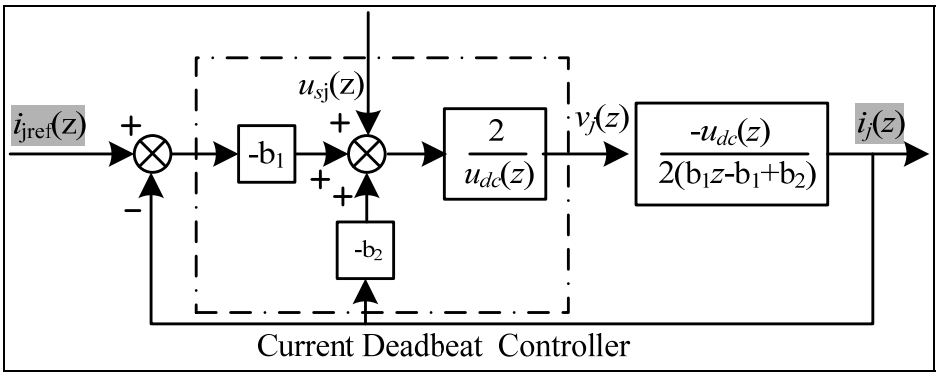

Figure 3.5 Inner current-loop controllers

In short, the proposed control scheme for the VSC-HVDC system is an outer PI controller plus an inner current deadbeat controller for each terminal VSC. But their control purposes are different, as mentioned above. As shown in (3.11), it is an easy design for the inner current controller due to its simple structure with determined parameters.

3.4 Case studies

To evaluate the effectiveness of the proposed control scheme, cases of two-terminal IGBT VSC-HVDC system is developed in MATLAB. The power system simulator /SimPowerSystems toolbox and Simulink are used for system modeling and simulation, where VSC station 1 works in VQ control mode and VSC station 2 works in PQ control mode as described in section-III. The parameters of VSC-HVDC system for simulation are used the same as Table 2.1 in Chapter 2.

3.4.1 Case 1

Figure 3.6 shows the startup and steady-state responses of the VSC-HVDC system with reference commands u_{dcref1} = 1 pu, Q_{ref1} = 0 pu for VSC 1 and reference commands P_{ref2} = 1 pu, Q_{ref2} = 0 pu for VSC 2. Note that the DC side capacitors have been charged to $\sqrt{2}U_s$ (U_s is the RMS value of AC network line to line voltages) through the diodes in VSC before the startup of VSCs. In order to prevent the VSC-HVDC system from over-voltage and over-

current during the startup, a ramp reference active power P_{ref2} is given instead of a step one. VSC station 1 in VQ control mode will start at time $t = 0$, and VSC station 2 will start until the DC bus voltage reach 90 % of DC base value. From simulation results in Figure 3.6, it can be seen that the VSC-HVDC system start softly and the outputs at VSC1 and VSC2 exactly reach the set reference values in the steady state.

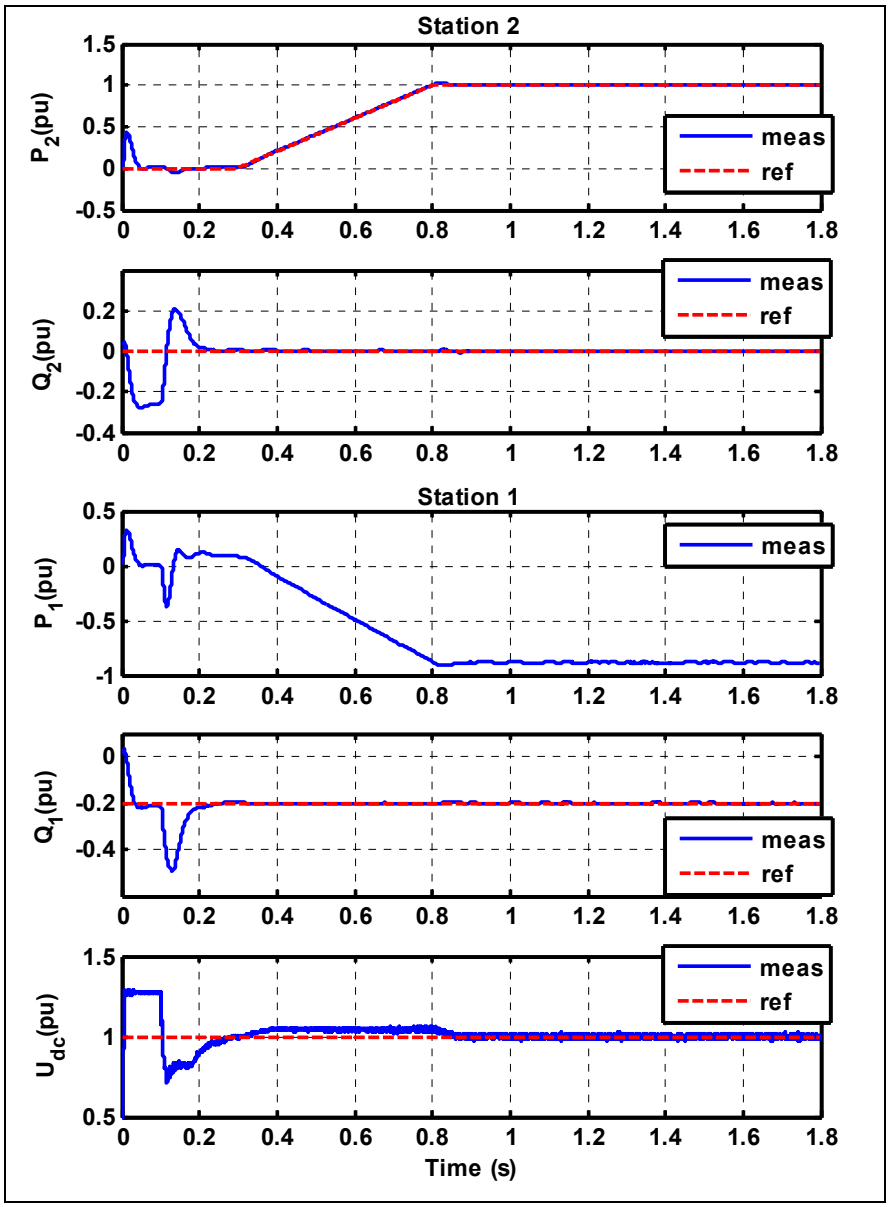

Figure 3.6 Startup and steady-state responses

3.4.2 Case 2

Figure 3.7 shows the active power and reactive power step responses. At the beginning, the active power is transmitted from VSC2 to VSC1. The reference active power P_{ref2} is reduced from 0.5 pu to −0.2 p.u. at time t = 1.4 s, and it takes about 130 *ms* for the measured active power P_{meas2} at VSC2 changes to −0.2 pu. Correspondingly, the measured active power P_{meas1} at VSC1 changes around from −0.48 pu to 0.22 pu. At the same time, the active power flow reverses with the DC current direction change. However, the reactive powers Q_1 and Q_2 at VSC1 and 2 do not change.

When the reactive power Q_1 is changed from 0 pu to −0.4 pu at time t = 1.3 s, and the reactive power Q_2 is changed from 0 to −0.2 pu at time t = 1.65 *s*, we can see that it has a good tracking accuracy. However, variables P_1 and P_2 are not affected at all.

Obviously, the reactive power flow can be independently controlled at each AC network, and the reactive power and the active power control is independent. Notice that, considering the loss in the transmission cables, the sending active power equals the receiving active power plus the loss power in the cable.

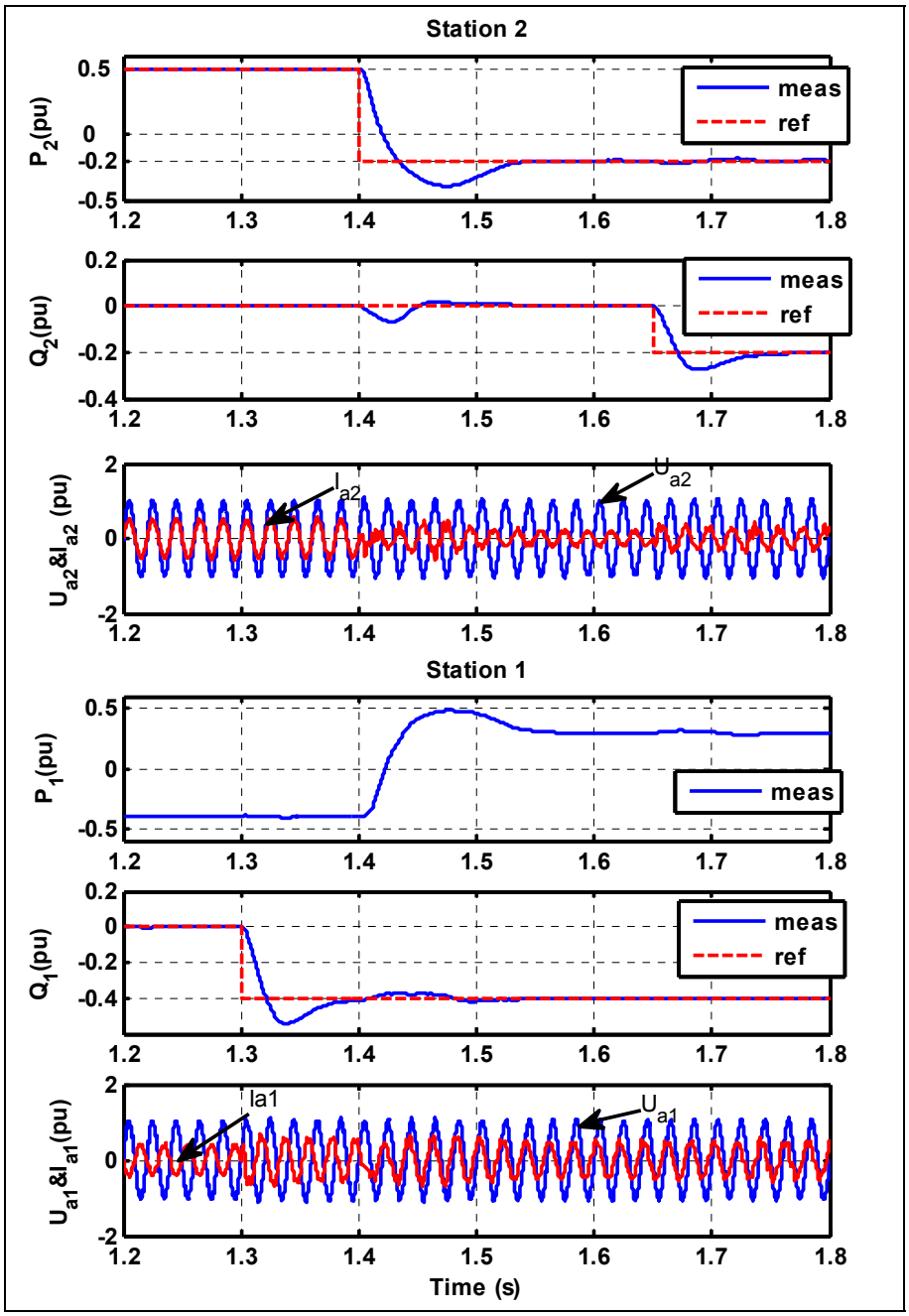

Figure 3.7 Active and reactive power step responses

3.4.3 Case 3

A three-phase voltage sag is applied at station 2 AC bus shown as Figure 3.8. The AC voltage sag with −0.1 pu voltage amplitude is applied at the time between 1.4 s and 1.55 s.

The results show that the active and reactive power deviation from the first disturbance is less than 0.1 pu and 0.05 pu respectively. It takes about 100 *ms* to recover the steady state before the next perturbation initiation.

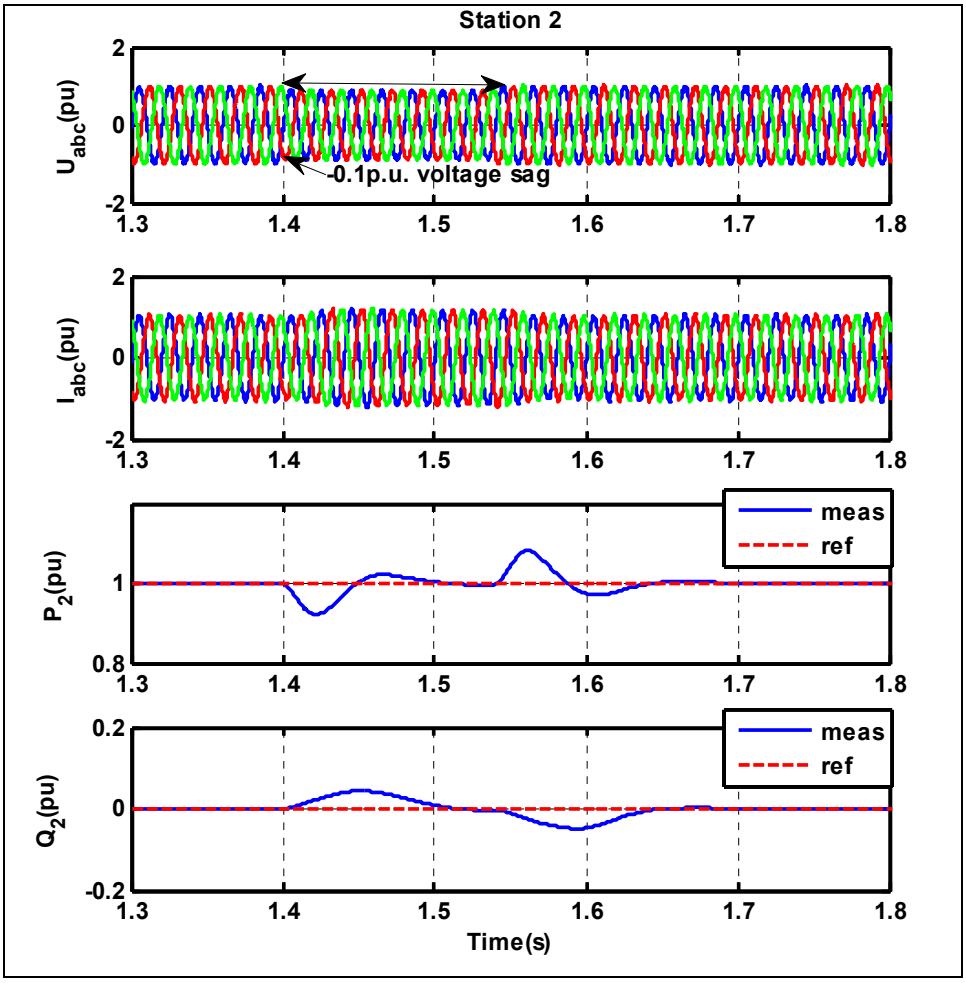

Figure 3.8 Voltage sag on station 2 AC bus

3.4.4 Case 4

A three-phase to ground fault is applied at station 1 AC bus shown as Figure 3.9. The fault is applied at t = 1.4 *s* during 100 *ms*. Note that during the three-phase fault, the transmitted DC power is almost zero. At this moment the two VSC stations can be considered as independent STATCOMs. The system recovers well after the fault within 0.2 s.

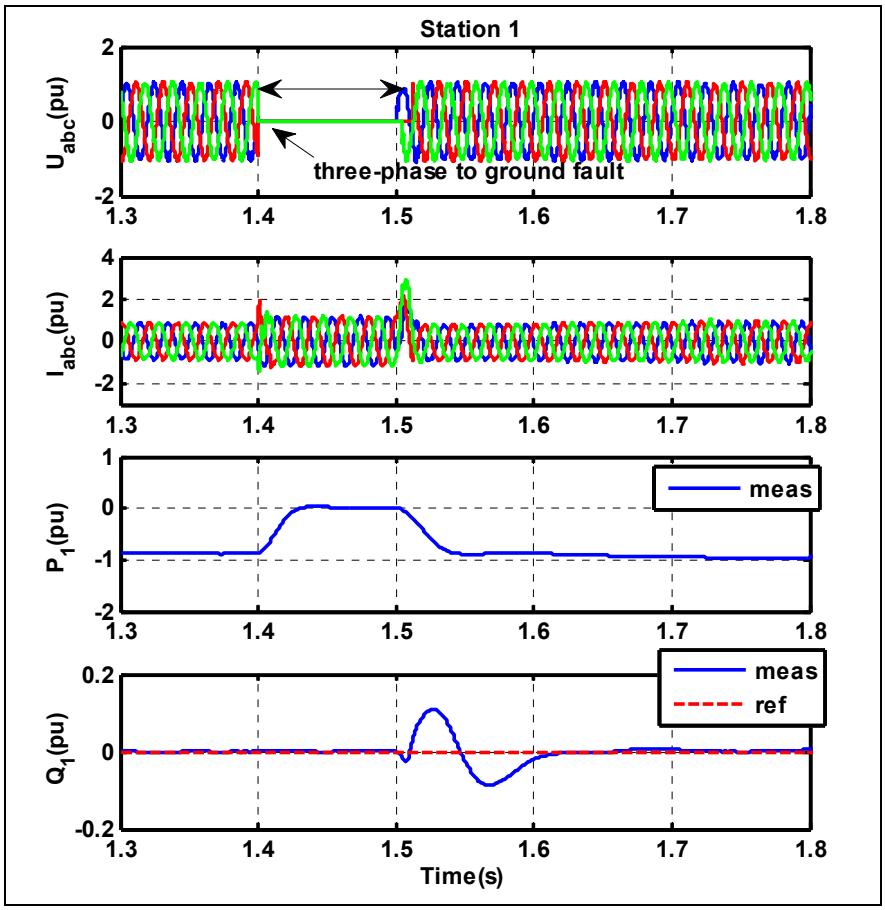

Figure 3.9 Three-phase to ground fault on station 1 AC bus

3.5 Conclusion

In this chapter, a current deadbeat control scheme is proposed for the VSC-HVDC system. The proposed control scheme for the VSC-HVDC system shows some attractive advantages: offering high tracking accuracy, fast dynamic response and good robustness behavior. Cases of two-terminal VSC-HVDC system are studied in MATLAB/SPS to testify the validity of the proposed control strategy. Simulation results indicate that the proposed control scheme provides a high performance control solution to the VSC-HVDC system.

CHAPTER 4

APPLICATION OF VSC-HVDC: FEASIBILITY STUDY OF SERIES CONNECTED VSC MODULES FOR UHVDC OPERATION

4.1 Introduction

Due to the fact that neighboring energy sources have already been exploited, future power has to be transmitted from more remote locations to consumers. The long transmission distances of large countries like China, India, and Brazil justify raising the DC transmission voltage of HVDC from ±600 kV to ±800 kV (Astrom et al., 2005; Kumar et al., 2009a).

There are already Ultra-High Voltage DC transmission (UHVDC) projects in operation, for example:(1) ±800 kV Xiangjiaba Shanghai UHVDC link, rated power of 6,400 MW, transmission distance of 1935km (Yang et al., 2011b); (2) ±800 kV Yunnan-Guangdong UHVDC link, rated power 5000 MW, transmission distance of 1373 km (Rao, 2012). More UHVDC projects are under construction in India, China and some European countries.

The advantages of UHVDC are: (1) overall transmission loss is low at high transmission voltage of 800 kV; (2) the right-of-way land requirement for a ±800 kV, 6400 MW UHVDC scheme is about half that required for two 500 kV parallel HVDC or about one fifth of that required for five ±500 kV parallel HVAC alternative (AlstomCorp., 2015).

So far, the existing UHVDC projects are based on line-commutated thyristor technology (Rao, 2012; Yang et al., 2011b). Typically a single pole rated at 800 kV is based on two 12-pulse bridges rated at 400 kV. Each 12 pulse bridge consists of two 6-pulse bridges of 200 kV each. On their AC sides, one bridge has a wye-delta transformer connection and the other, a wye-wye connection to achieve a 30 degree phase shift to eliminate the 6^{th} harmonic. Effectively, they consist of four 6-pulse modules in series on the DC side (Beaty et Fink, 2012).

Thyristor converters have well known weaknesses: (a) commutation failures; (2) expensive filters on the AC side and the DC side; (3) power flow reversal needs interruption to change voltage polarity mechanically; (4) and no independent active and reactive power control (Arrillaga, 2008; Kim, 2009; Sood, 2004).

As voltage source converter (VSC) based HVDC are free from the weaknesses, this paper examines the feasibility of connecting VSC-HVDC stations in series to form VSC-Ultra HVDC. This is in view of the fact that VSC-HVDC stations are reaching high power and high DC voltage ratings. For example, the Caprivi Link is rated at 600 MW at ±350 kV (Magg et al., 2012a) and the EirGrid East-West Interconnector is rated at 500 MW, at ±200 kV (Egan et al., 2013).

The success in thyristor-UHVDC depends on industry having the technical knowledge in insulation so as to connect four 200 kV thyristor converter stations in series to bring the DC voltage up to 800 kV or more. This is because the transformer insulation of the converter stations at the higher DC voltage levels must be able to withstand the peak AC voltage together with the DC voltages of 200 kV, 400 kV, and 600 kV to which the converter stations are connected (Guo et al., 2012; Sheng et al., 2010). As this knowledge already exists, it can be applied to the VSC-UHVDC of this proposal.

The VSC-UHVDC proposed in this research is guided by thyristor-UHVDC (Astrom et al., 2005; Kumar et al., 2009a; Rao, 2012; Yang et al., 2011a). On both sides of the transmission line, each station consists of four two-level VSC modules in series to form a single pole. As VSC modules have never been connected in series on the DC-sides for UHVDC before, this research shows that series connection is trouble free.

Prior to feasibility demonstration by simulations, analysis of the equations modeling the series connection of VSC modules, shows that the ultra high dc voltage can be shared equally by the modules provided the voltages across the DC capacitor of every module can be

equalized. The paper shows that equalization can be accomplished by negative feedback (Wang, Hao et Ooi, 2013).

Multi-Modularity raises the concern of reliability. On this point, the authors are guided by the practice of thyristor-UHVDC. In the event of failure in any VSC, there is a switch across its DC terminals, which closes to isolate it. On the other end of the DC transmission line, a VSC module is also isolated by its switch to maintain symmetry. Hence, in our case the VSC-UHVDC continues to operate with DC voltage reduced by 0.25 %.

As a single station, VSC is well-known to have flexibility such as: (1) decoupled P-Q control; (2) capability to reverse direction of power flow; (3) low total harmonic distortion (THD) (Casoria, 2013; Egea-Alvarez et al., 2013; Saeedifard, Iravani et Pou, 2009; Yousefpoor, Narwal et Bhattacharya, 2015). This paper shows that the desirable features are incorporated in the VSC-UHVDC. In fact, the series connection VSCs topology allows the phase-shifted triangle carrier Sinusoidal Pulse Width Modulation (SPWM) technique to be applied to reduce switching losses significantly to improve efficiency (Townsend, Summers et Betz, 2015; Tu, Xu et Xu, 2011).

The existing great interest in Modular Multilevel Converter (MMC) is one driving force for the research of this research. The competition from MMC obliges partisans of VSC to examine if the excellent characteristics of VSC-HVDC can be more fully realized by adopting the methods of multi-modularity. In fact, Ultra-High Voltage DC based on MMC in (Wang, Hao et Ooi, 2013) is one challenge.

This Chapter is organized as follows: The configuration of VSC-UHVDC is described in Section 4.2. Circuit analysis of VSC-UHVDC to establish feasibility of series-connection VSCs is presented in Section 4.3. In Section 4.4, the control of VSC-UHVDC is developed in details. In Section 4.5, the method of applying phase shifted triangle carrier SPWM technique to series-connected VSC modules to reduce switching losses is presented. Simulation results are presented in Section 4.6. In Section 4.7, continuity of power supply during VSC fault is

presented briefly. In Section 4.8, how higher modularity will improve the performance of VSC-UHVDC is discussed. Finally, conclusions are made in Section 4.9.

4.2 VSC-UHVDC topology

Figure 4.1 shows one pole of the proposed topology of VSC- UHVDC. AC System 1 and AC System 2 are interconnected by a DC transmission line. The DC station at the ends consists of a series connection of four modules of two-level VSCs rated at 200 kV each. The series connected modules enable the DC voltage to reach 800 kV. Isolation on the AC-side is by Y/Δ transformers (Guo et al., 2012; Sheng et al., 2010). Because VSC-13, VSC-12 and VSC-11, for example, are respectively 400 kV, 600 kV and 800 kV above ground voltage, the transformer winding insulation must have voltage withstand of the peak AC voltage together with the DC voltages. As existing thyristor-UHVDC has the same problem, manufacturers know how to insulate the transformers.

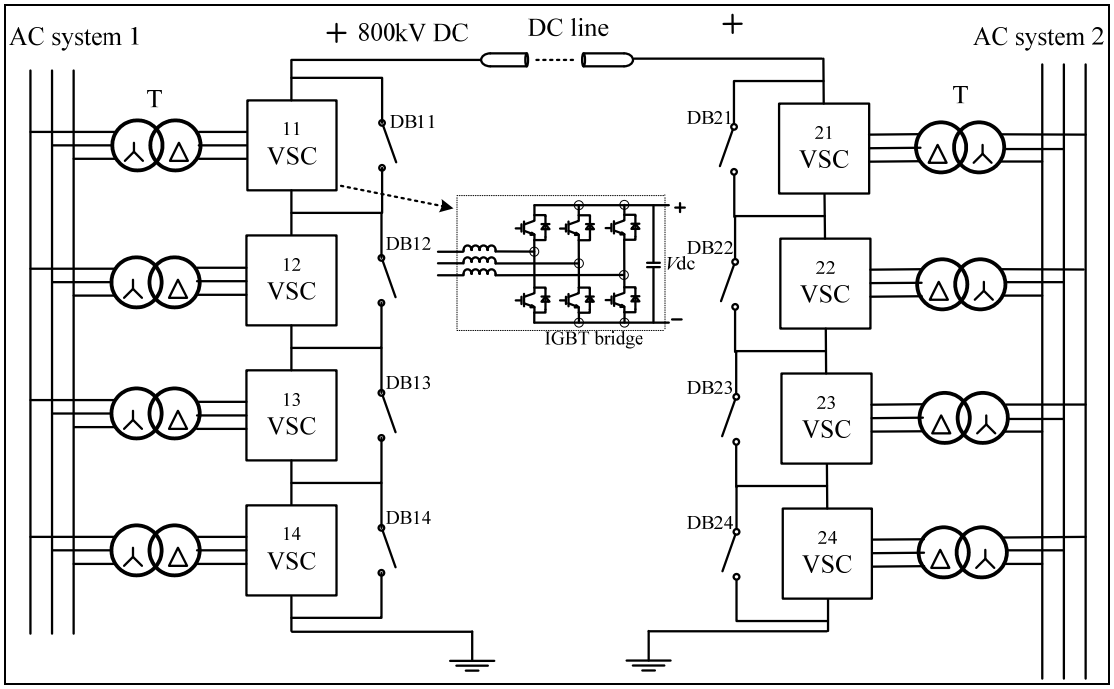

Figure 4.1 Proposed VSC-UHVDC transmission (one pole)

For reliability, DB switches across the DC terminals of each VSC applies short-circuit across the VSC when it fails so that the pole continues to operate, but from 800 kV to a lower voltage of 600 kV.

4.3 Circuit analysis of VSC-UHVDC

The analysis of this section shows that existing technical expertise can realize the VSC-UHVDC. The analysis begins with assigning unequal inductance and resistance values and controlling variables to the j^{th} VSC module. For instance, the circuit equations from Kirchhoff's Voltage Law applied to each of *a*, *b* and *c* phases are:

$$L_j \frac{di_{aj}}{dt} + R_j i_{aj} = e_a - \frac{m_{aj} U_{dc-j}}{2} \tag{4.1}$$

$$L_j \frac{di_{bj}}{dt} + R_j i_{bj} = e_b - \frac{m_{bj} U_{dc-j}}{2} \tag{4.2}$$

$$L_j \frac{di_{cj}}{dt} + R_j i_{cj} = e_c - \frac{m_{cj} U_{dc-j}}{2} \tag{4.3}$$

where e_a, e_b and e_c are the voltages from the AC system referred to VSC side of the transformers. i_{aj}, i_{bj} and i_{cj} are the three phase currents. m_{aj}, m_{bj} and m_{cj} are the modulating signals. U_{dc-j} is the voltage across the DC capacitor. C_j, L_j and R_j are the equivalent inductance and resistance on the AC side.

From the view of power balance, the DC current of the VSC is:

$$i_{dc-j} = \frac{m_{aj} i_{aj} + m_{bj} i_{bj} + m_{cj} i_{cj}}{2} \tag{4.4}$$

Assuming that the DC line current is i_{DC}, the voltage across the capacitor C_j is:

$$C_j \frac{dU_{dc-j}}{dt} = i_{dc-j} - i_{DC} \tag{4.5}$$

The DC voltage across 4 VSCs is:

$$V_{tot} = \sum_{j=1}^{4} U_{dc-j} \tag{4.6}$$

Let the currents i_{aj}, i_{bj} and i_{cj} on the Δ side of the transformers be transformed to i_{aj}^{1}, i_{bj}^{1} and i_{cj}^{1} on the Y side.

From Kirchhoff's Current Law, the AC bus currents from the Y transformer windings are:

$$i_a = \sum_{j}^{j=4} i_{aj}^{1} \qquad i_b = \sum_{j}^{j=4} i_{bj}^{1} \qquad i_c = \sum_{j}^{j=4} i_{cj}^{1} \tag{4.7}$$

In general, manufacturers have the ability to produce N units of VSCs which meet identical specifications. This is because they can meet tight tolerances so that $L_j \cong L$, $R_j \cong R$ and $C_j \cong C$ for j = 1, 2, 3, 4 and likewise for the modulating signals $m_{aj} \cong m_a$, $m_{bj} \cong m_b$ and $m_{cj} \cong m_c$ for j = 1, 2, 3, 4.

The four VSCs would operate identically provided in (4.1), (4.2) and (4.3). $U_{dc-j} = U_{dcref}^{*}$, where j = 1, 2, 3, 4. The DC voltage acrosses each VSC is presented below.

$$U_{dcref}^{*} = \frac{V_{tot}}{4} \tag{4.8}$$

This equalization can be achieved by negative feedback using compensation equalizer blocks, which will be designed in the following Section.

4.4 Control of VSC-UHVDC System

4.4.1 Control of UHVDC

In existing VSC-HVDC transmission, one terminal operates as a Power Dispatcher and the other as a DC Voltage Regulator (Saeedifard, Iravani et Pou, 2009). The same control principle is adopted as illustrated in Figure 4.2. The control of VSC modules in AC system 1 is to maintain constant DC voltage and regulate the reactive power Q as required. The reactive power Q is used to support the magnitude of AC voltage. Each VSC module operates with decoupled U_{dc}-Q control.

The control of VSC modules in AC systems 2 is to regulate the active and reactive power flow as required (Egea-Alvarez et al., 2013; Yousefpoor, Narwal et Bhattacharya, 2015). The reactive power Q is used to support the magnitude of AC voltage. Each VSC module operates with decoupled P-Q control.

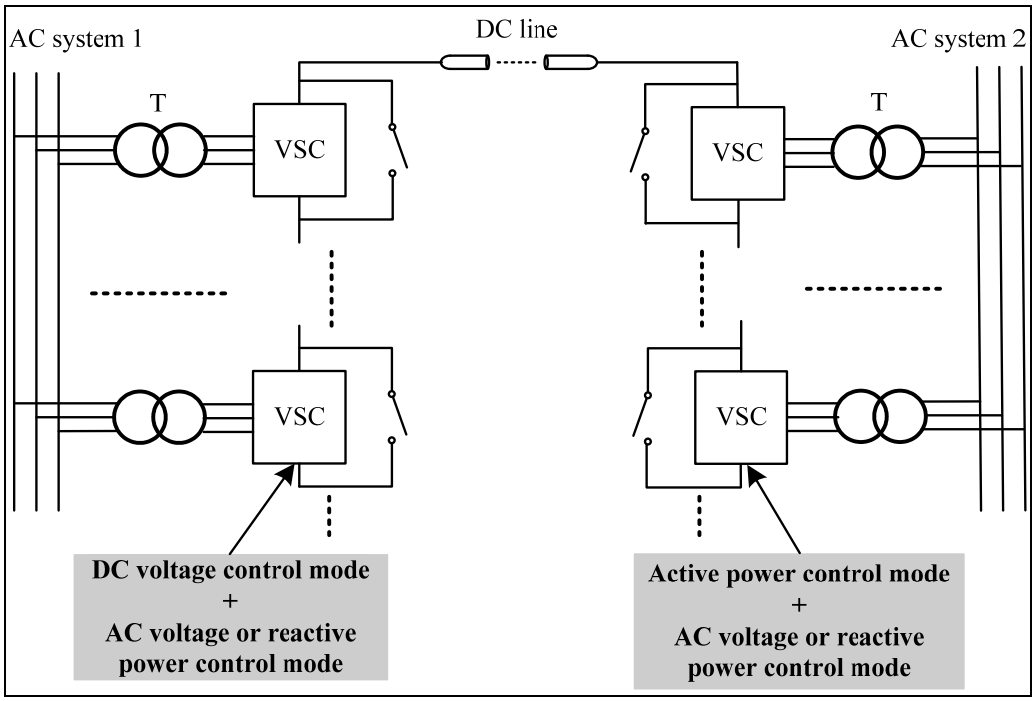

Figure 4.2 Overall control system of the VSC-UHVDC transmission system

4.4.1.1 U_{dc}-Q Control Mode (AC System 1)

VSC control methods are already well-known in (Casoria, 2013; Fu et al., 2011). For completeness, the schematic of the j^{th} VSC of N VSCs is shown in Figure 4.3. The overall references U_{dcref} and Q_{ref} , $U_{dcjref} = U_{dcref} / N$ and $Q_{jref} = Q_{ref} / N$ are the DC voltage reference and the reactive power reference of the j^{th} converter, respectively. Likewise their measured values are $U_{dcjmeas}$ and Q_{jmeas}, respectively.

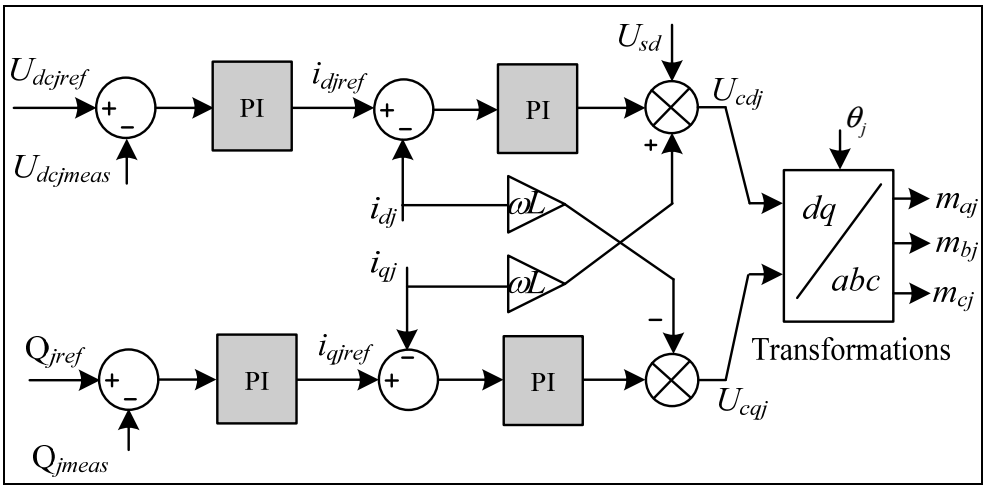

Figure 4.3 Decoupled U_{dc}-Q control schemes for VSC modules

4.4.1.2 P-Q Control Mode (AC System 2)

Figure 4.4 shows the schematic of P-Q control for the j^{th} converter of AC system 2. $P_{jref} = P_{ref} / N$, $Q_{jref} = Q_{ref} / N$ are the j^{th} VSC references of active and reactive powers, respectively. P_{jmeas} and Q_{jmeas} are the measurements of active and reactive powers, respectively.

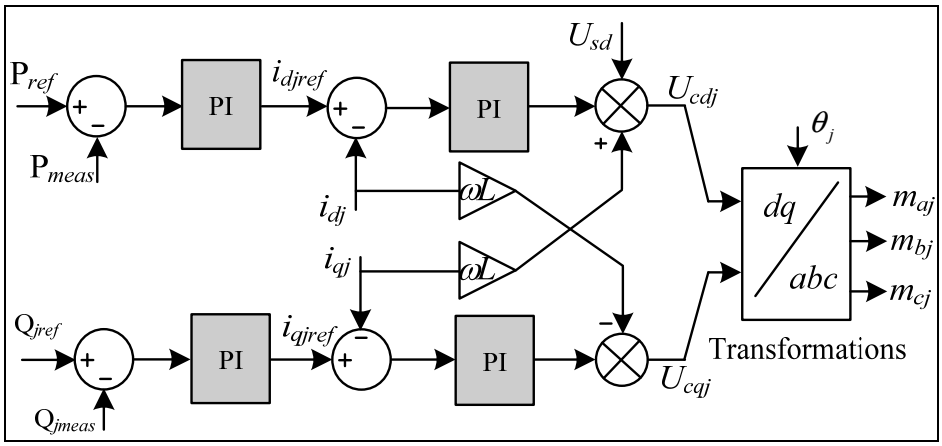

Figure 4.4 Decoupled P-Q control schemes for VSC modules

4.4.2 Equalization of DC Voltages of Series-Connection VSCs

4.4.2.1 Power Dispatcher (AC System 2)

Figure 4.5 shows the DC voltage compensation equalizer block. In decoupled P-Q control without voltage equalization, i_{djref} is sent to command the j^{th} VSC to produce power so that the error Δe_{pj} is nulled. With voltage equalization, a corrective signal Δi_{dj} is added to i_{djref} so that the command is i^*_{djref}. The size of the corrective signal Δi_{dj} is based on the error Δe^*_{dcj} being nulled by the negative feedback.

The DC voltage across the j^{th} VSC at P-Q side is measured as $U_{dcjmeas-2}$. The measurements are summed as:

$$V_{tot-2} = \sum_{j=1}^{N} U_{dcjmeas-2} \tag{4.9}$$

In this case, the equalization reference is $0.25V_{tot-2}$ in the negative feedback block of Figure 4. 5. In general, this reference is V_{tot-2} / N when N VSCs are connected in series.

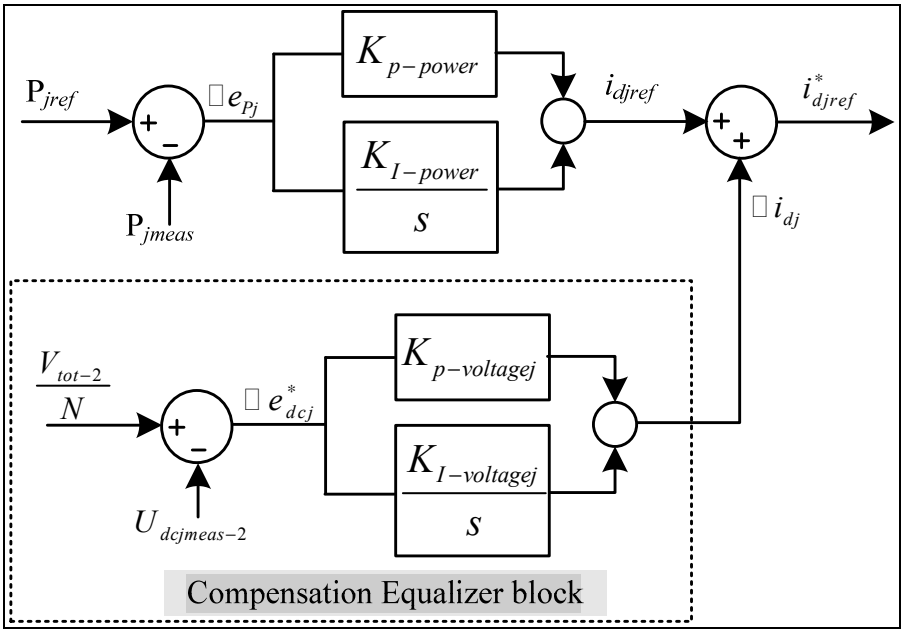

Figure 4.5 DC voltage compensation equalizer block for P-Q control side

4.4.2.2 DC Voltage Regulator (AC System 1)

Figure 4.6 shows the same design for the DC Voltage Regulator. The changes required in the upper blocks are: P_{jref} is replaced by U_{dcjref} and P_{jmeas} is replaced by $U_{dcjmeas-1}$. The DC voltage across the j^{th} VSC at U_{dc}-Q side is measured as $U_{dcjmeas-1}$. The measurements are summed as:

$$V_{tot-1} = \sum_{j=1}^{N} U_{dcjmeas-1} \tag{4.10}$$

Here, the voltage compensation reference for each VSC is V_{tot-1}/N.

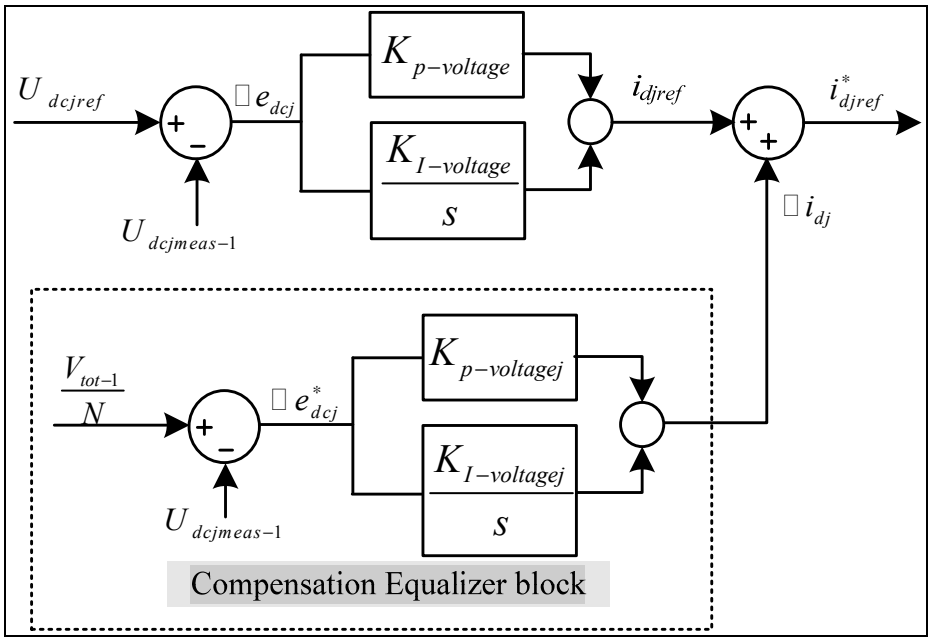

Figure 4.6 DC voltage compensation equalizer block for U_{dc}-Q control side

4.5 Reduction of Switching Losses

4.5.1 SPWM based on Phase Shifted Triangle Carrier

In this research, the phase shifted triangle carrier technique is adopted to reduce switching losses (Townsend, Summers et Betz, 2015), (Deng et Chen, 2015), and (Lim, Maswood et Ooi, 2015). As illustrated in Figure 4.7, each triangle carrier of frequency f_c has a period of $1/f_c$ second. When N = 4 VSCs form one UHVDC station, each VSC receives its carrier C_1, C_2, C_3 and C_4, as illustrated in Figure 4.7 (a). The carriers have phase shifting of $\theta_\Delta = 2\pi/(4f_c)$.

Figure 4.7 (b) shows the carriers used when one VSC is short-circuited by a DB switch in Figure 4.1. The carriers are C_1, C_2, and C_3 and the carriers have phase shifting of $\theta_\Delta = 2\pi/(3f_c)$.

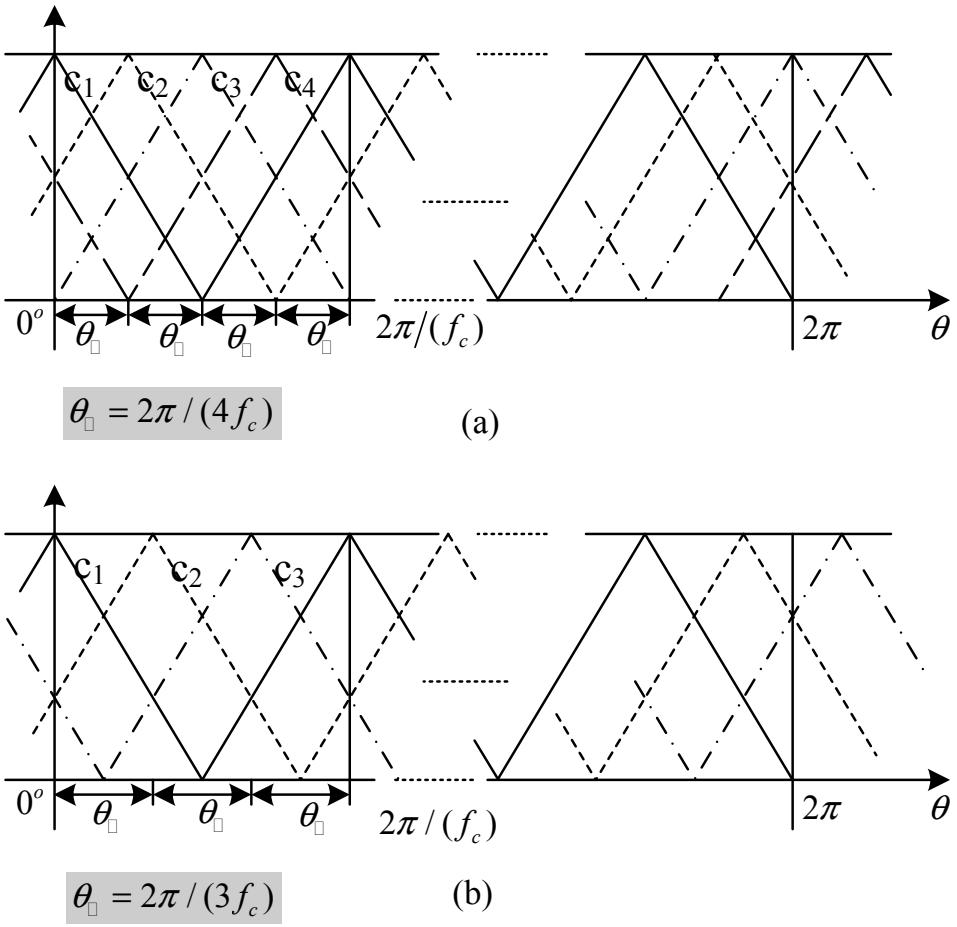

Figure 4.7 Phase shifted triangular carriers
(a) for N=4 VSCs; (b) for N=3 VSCs

In conventional SPWM implementation, the effective carrier frequency becomes $F_c = Nf_c$ when each of the N VSC modules uses a carrier frequency of f_c. Switching losses are proportional to f_c of each VSC module.

When effective carrier frequency F_c is high enough to meet THD and other harmonic standards, switching losses are reduced by increasing N because of $f_c = F_c / N$.

4.6 Simulation studies

The simulation studies show that the proposed VSC-UHVDC of Figure 4.1 is feasible because: (i) it operates with equalized DC voltages; (ii) it has bi-directional power transfer capability and independent control of active and reactive power; (iii) it has reduced switching losses while satisfying harmonic and THD requirements; (iv) and it continues to operate after one VSC has failed.

The main data for the simulation of the proposed VSC-UHVDC system is shown in Table 4.1.

Table 4.1 Main data for the UHVDC system used in the simulation

Parameters	**Value**	**Unit**
Total base power (S_{base})	800	MVA
AC bus rated voltage (Us_1)	230	kV
VSC module Reactor resistance(R)	0.075	Ω
VSC module Reactor inductance (L)	0.0024	H
VSC module DC capacitance (C)	70e-6	F
VSC module DC base voltage(U_{dcjref})	200	kV
Total DC bus base voltage (U_{dcref})	800	kV
DC-cable resistance (R_1)	6.95e-3	Ω/km
DC-cable inductance (L_1)	3.18e-4	H/km
DC-cable capacitance (C_1)	2.3e-7	F/km
VSC module base power (S_{jbase})	200	MVA
Length of cable (l)	1000	km
Switching frequency (f_c)	1440	Hz

4.6.1 Equalization of DC voltages of power dispatcher (AC system 2)

The simulation of Figure 4.8 shows that the VSC modules do not have self-DC voltage equalization mechanism especially when power reversal happens. The DC voltage across this station V_{tot-2} is measured and $0.25V_{tot-2}$ is compared with the voltages across each VSC module.

However, with the DC voltage compensation equalizer block of Figure 4.5 (a), the DC voltages across each VSC equalize. As shown in Figure 4.9. The measured DC voltages across each VSC module and $0.25V_{tot-2}$ overlap well.

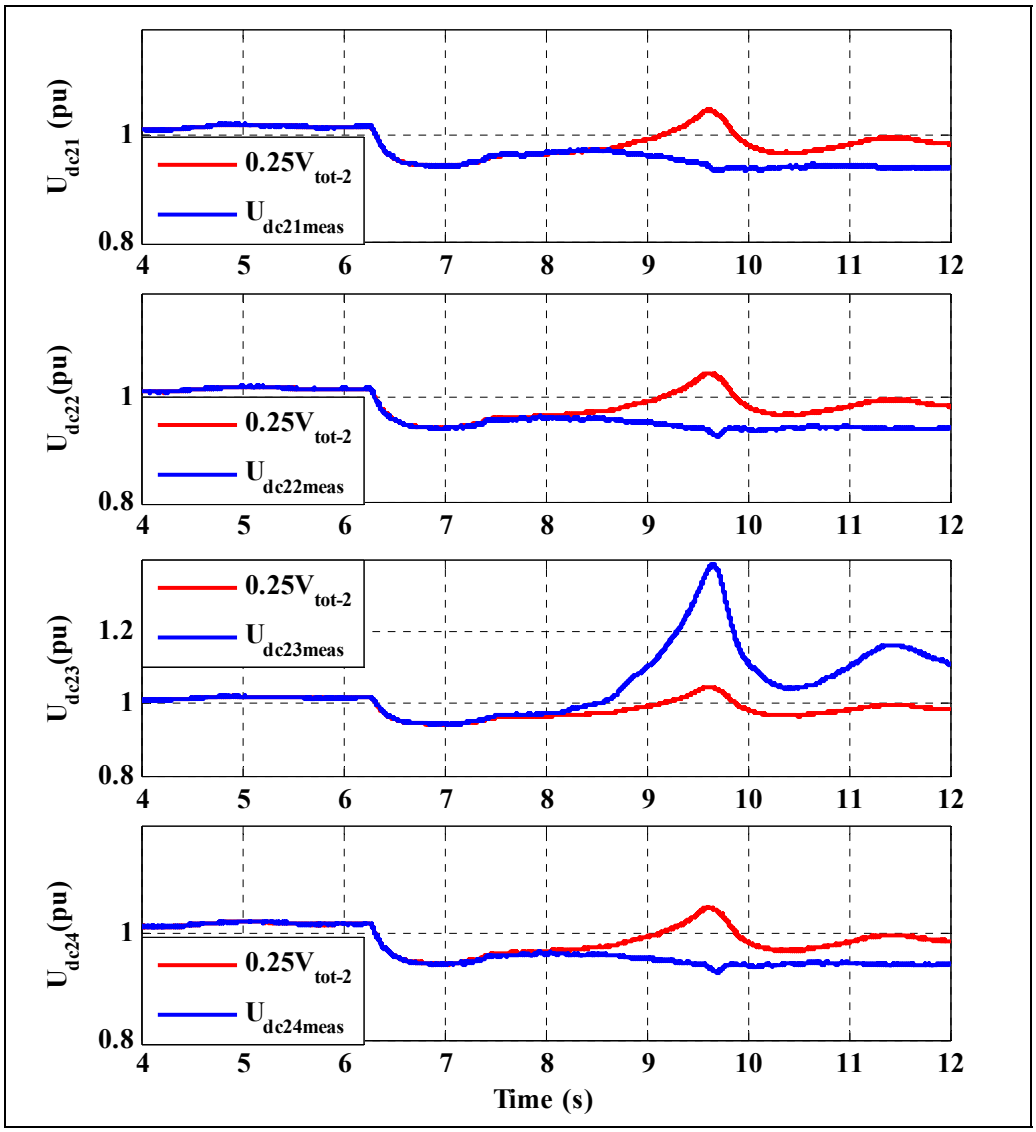

Figure 4.8 DC voltages of each VSC at P-Q side without DC voltage compensation equalizer control

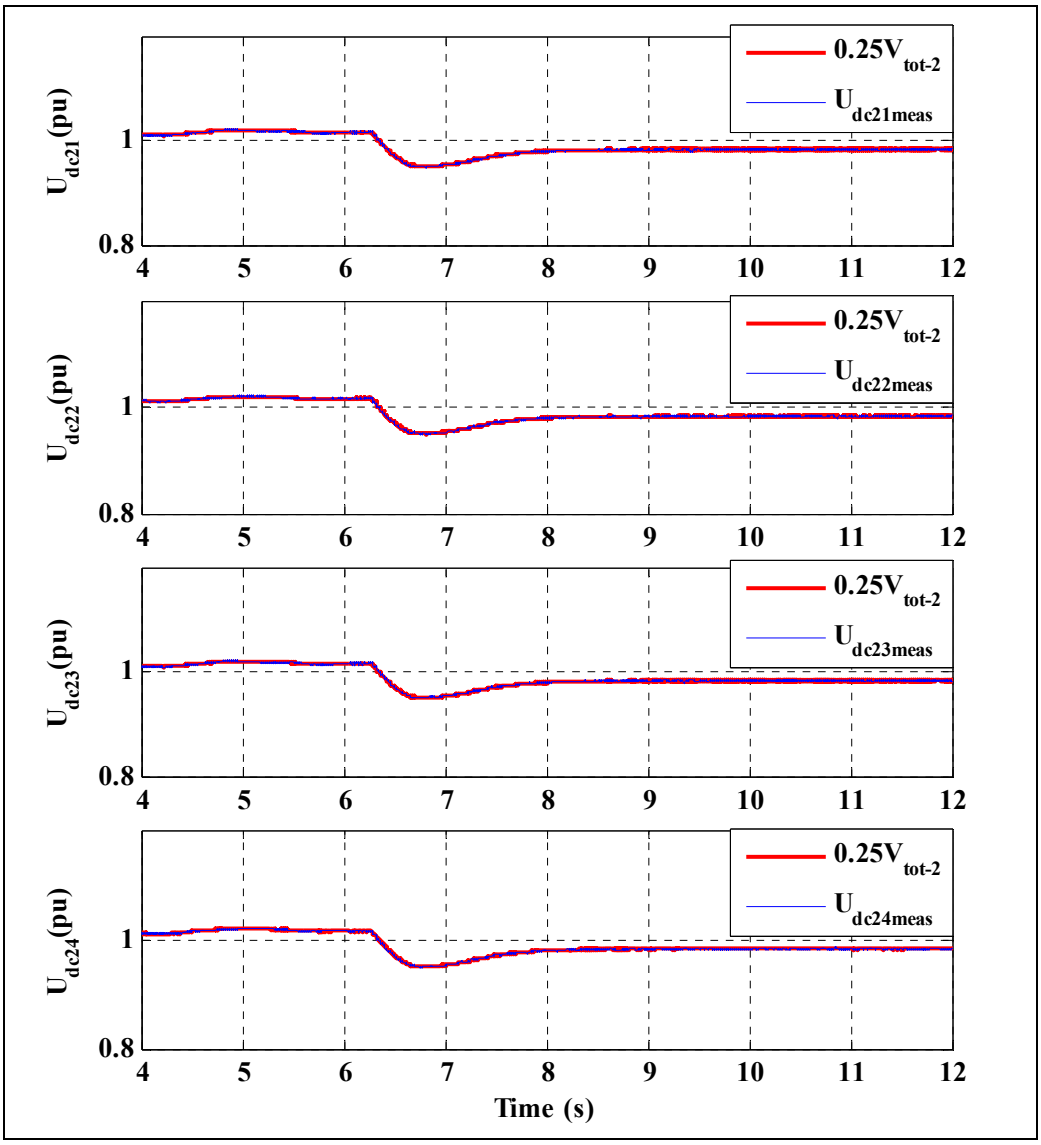

Figure 4.9 DC voltages of each VSC at P-Q side with DC voltage compensation equalizer control

4.6.2 Test on overall control system

Coordinated control of the point-to-point system of Figure 4.1 is as follows: As Power Dispatcher, AC system 2 makes use of P-control to assign the size of active power through the dc line; As DC-Voltage Regulator, AC system 1 makes use of P-control to regulate the dc voltage across its dc terminals thereby ensuring active power balance.

Figure 4.10 and Figure 4.11 present simulation results which show that the coordinated control is accomplished. As shown in Figure 4.10 (a) Pref of AC side 2 is given a step change at t = 5 s and t = 7.5 s. Figure 4.11(a) shows the corresponding active power changes on AC side 1 which indicate active power balance.

The test results show that decoupled P-Q control is achieved. The Q-curve in Figure 4.10 (b) shows insensitivity to P-changes. Figure 4.11 (b) shows that a test step change in Q_{ref} is introduced at t = 9 s. The P-curves in Figure 4.10 (a) and Figure 4.11 (a) are not affected by the step change in Q_{ref} at t = 9 s.

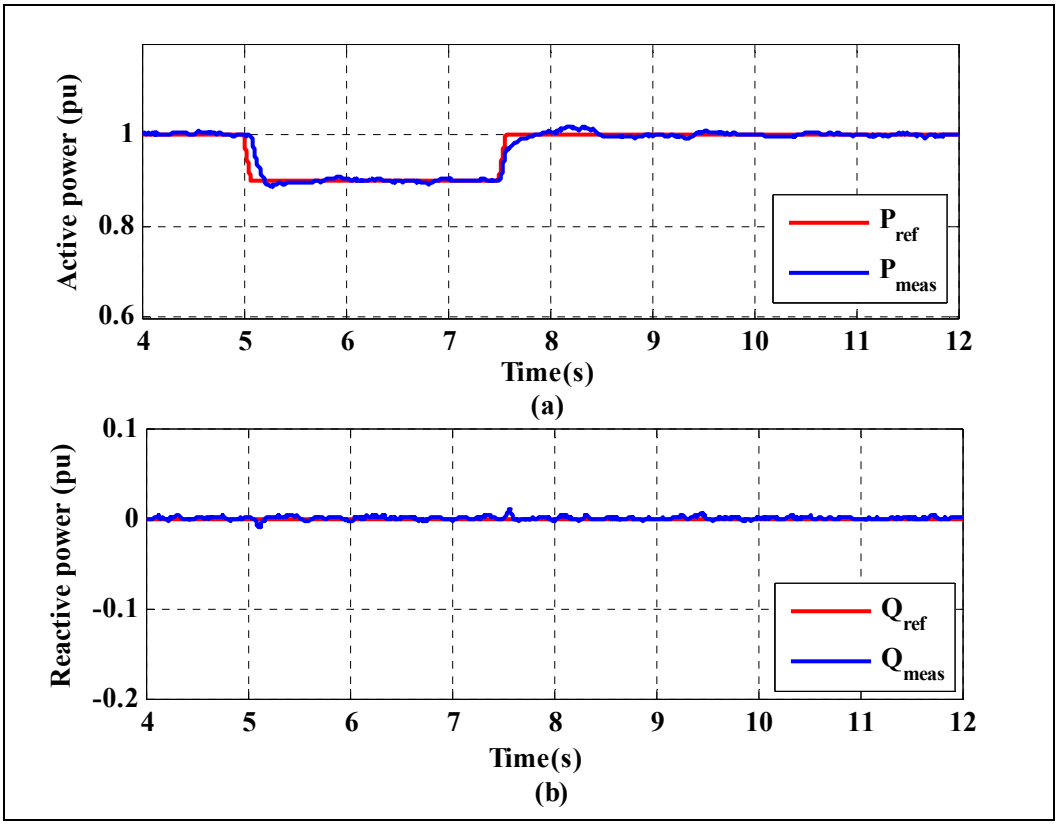

Figure 4.10 (a) Active power and (b) reactive power at P-Q control side

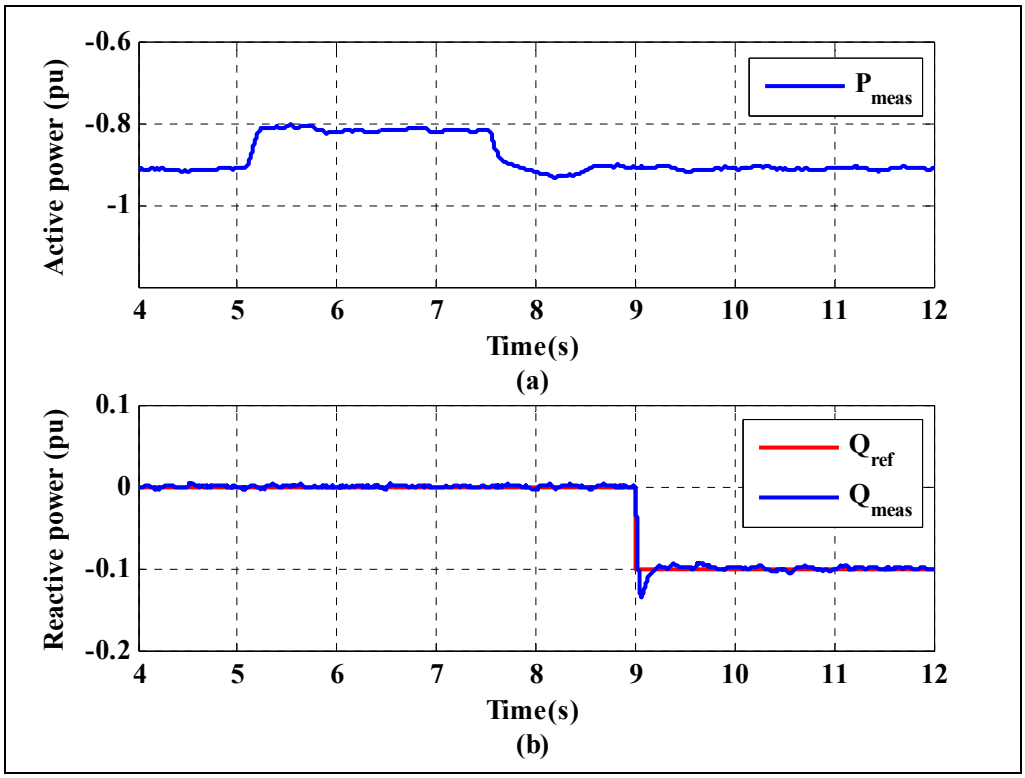

Figure 4.11 (a) Active power and (b) reactive power at U_{dc}-Q control side

4.6.3 Power reversal

Figure 4.12 to Figure 4.14 show that the VSC-UHVDC system has bidirectional power capability. Figure 4.12 (a) shows P_{ref}, the power reference (in red) changing from 1.0 pu to −1.0 pu in a ramp. The measured power (in blue) tracks its reference. In Figure 4.12 (b), the measured reactive power Q_{meas} tracks the reference $Q_{ref} = 0$.

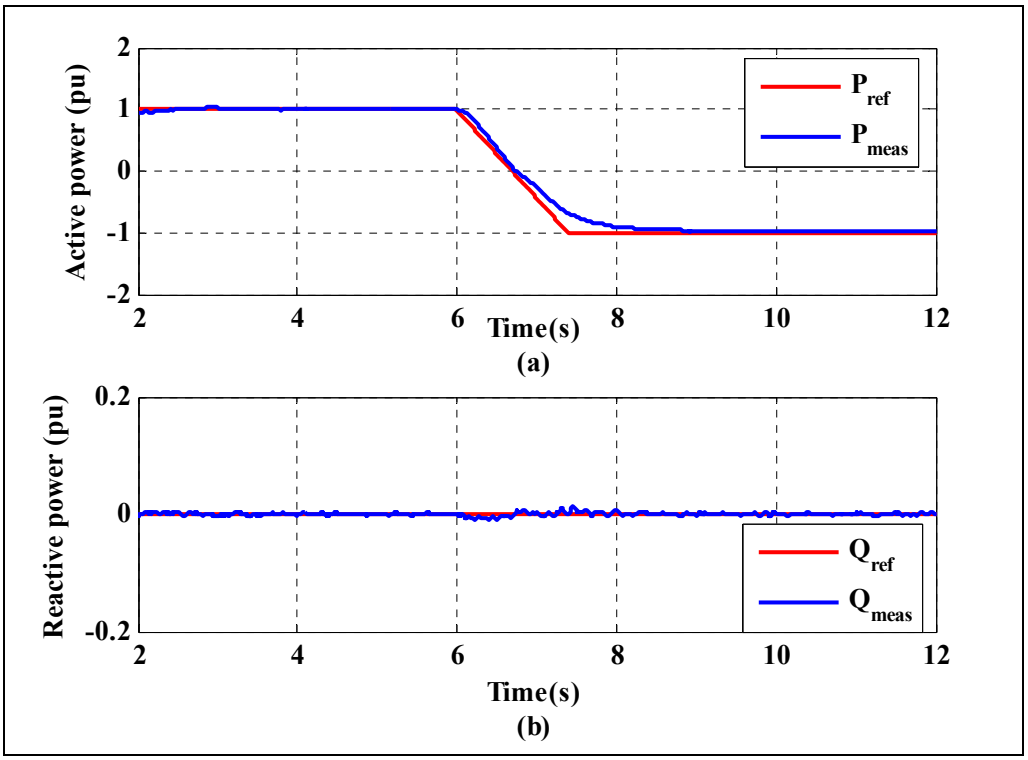

Figure 4.12 (a) Active power and (b) reactive power at P-Q control side

On the DC Voltage Regulator side, Figure 4.13 (a) shows that the active power commanded by the Power Dispatcher side is automatically adapted by the DC Voltage Regulator which adjusts its P_{ref} control to null the DC voltage error. At the same time, the measured reactive power tracks its reference $Q_{ref} = 0$ shown in Figure 4.13 (b).

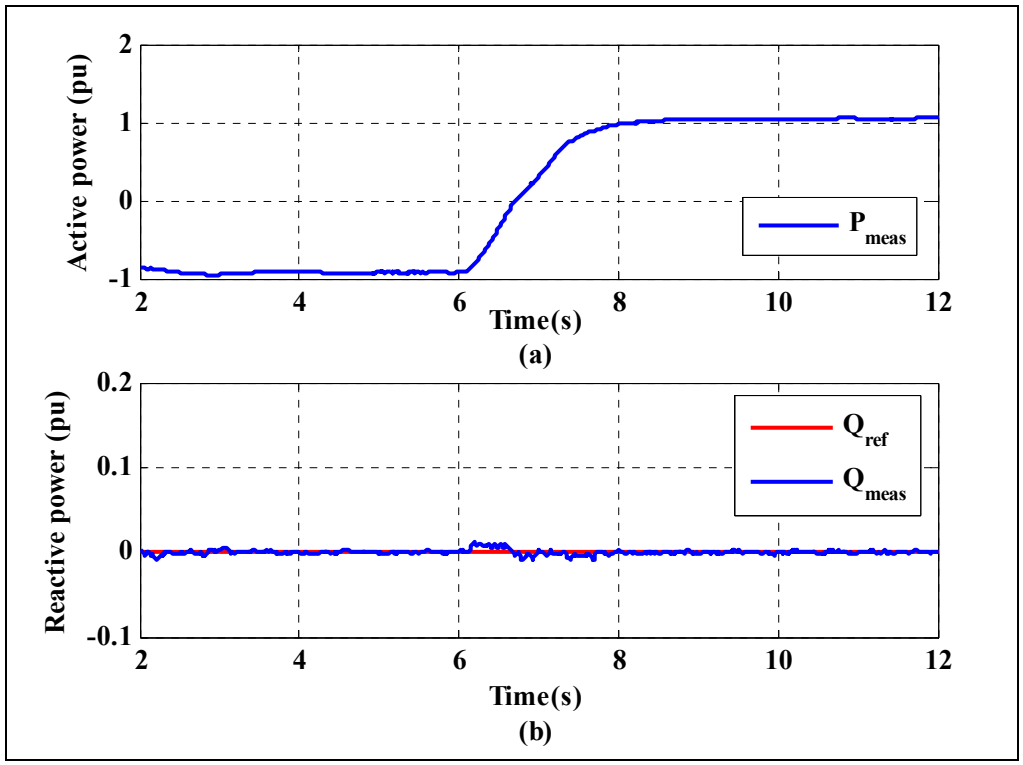

Figure 4.13 (a) Active power and (b) reactive power at U_{dc}-Q control side

Figure 4.14 (a) shows the DC voltage dip during the power reversal. This voltage dip causes the DC Voltage Regulator to supply the active power requested by the Power Dispatcher. Figure 4.14 (b) shows that power reversal is reached by reversal of the direction of current flow, while the DC voltage is kept substantially constant.

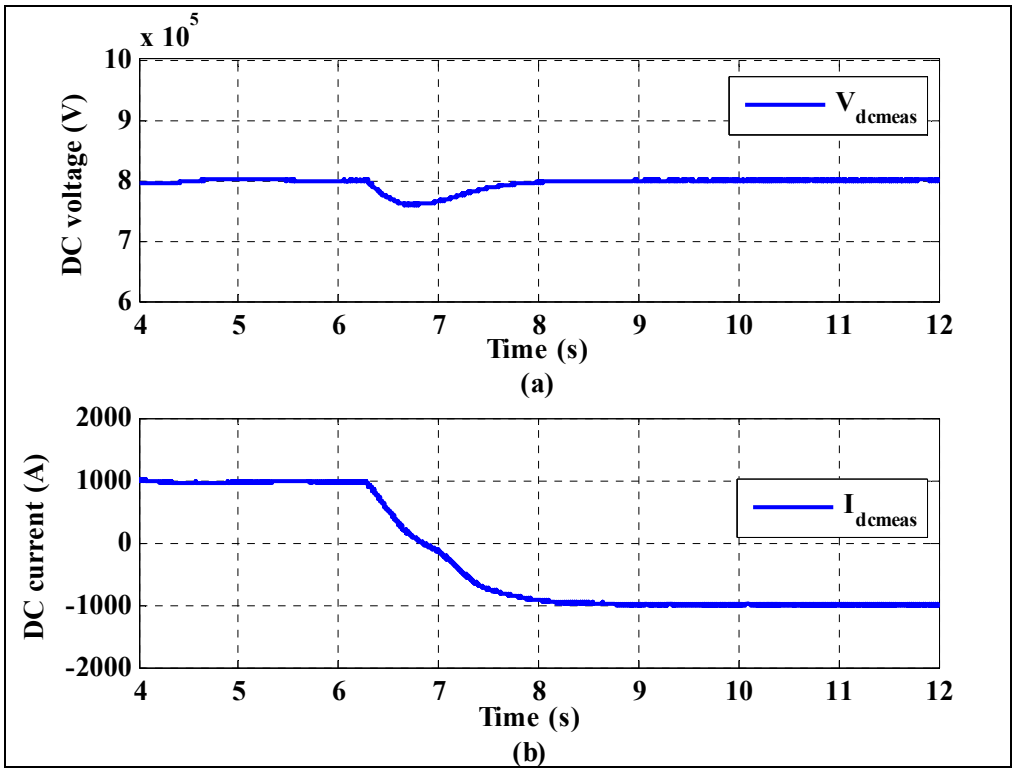

Figure 4.14 (a) DC voltage and (b) DC current when power reversal happens

Figure 4.15 shows that the voltage dip of Figure 4.14 (a) is equalized across VSC modules on AC System 1 side (operating as DC voltage regulator) using compensation equalizer blocks of Figure 4.6 Successful DC voltage equalization on AC System 2 side has already been demonstrated in Figure 4.9.

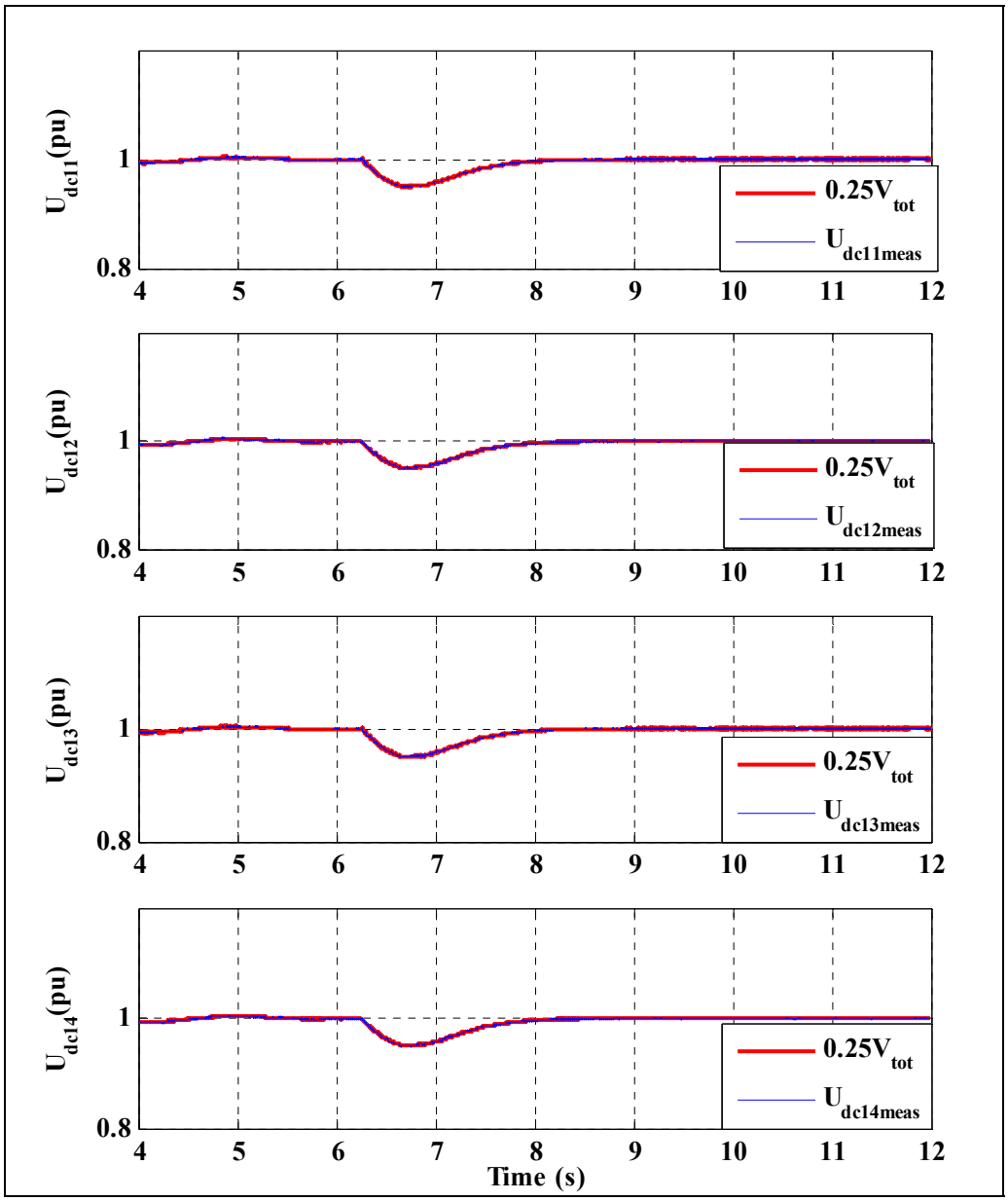

Figure 4.15 DC voltages of each VSC module at Udc-Q side

4.6.4 Harmonics and Total Harmonic Distortion

4.6.4.1 SPWM Strategy with Phase-Shifted Carrier Strategy

Applying the well-known Sinusoidal Pulse Width Modulation (SPWM) technique, the current waveform for carrier frequency f_c = 1440 Hz and its harmonic spectrum from Fast Fourier Transform analysis (FFT) are shown in Figure 4.16. The 24th harmonic is the carrier and the 20th harmonic is the lower sideband. Their magnitudes are given as % of the fundamental. The THD is 9.46 %. Better waveforms are obtainable by increasing the carrier frequency.

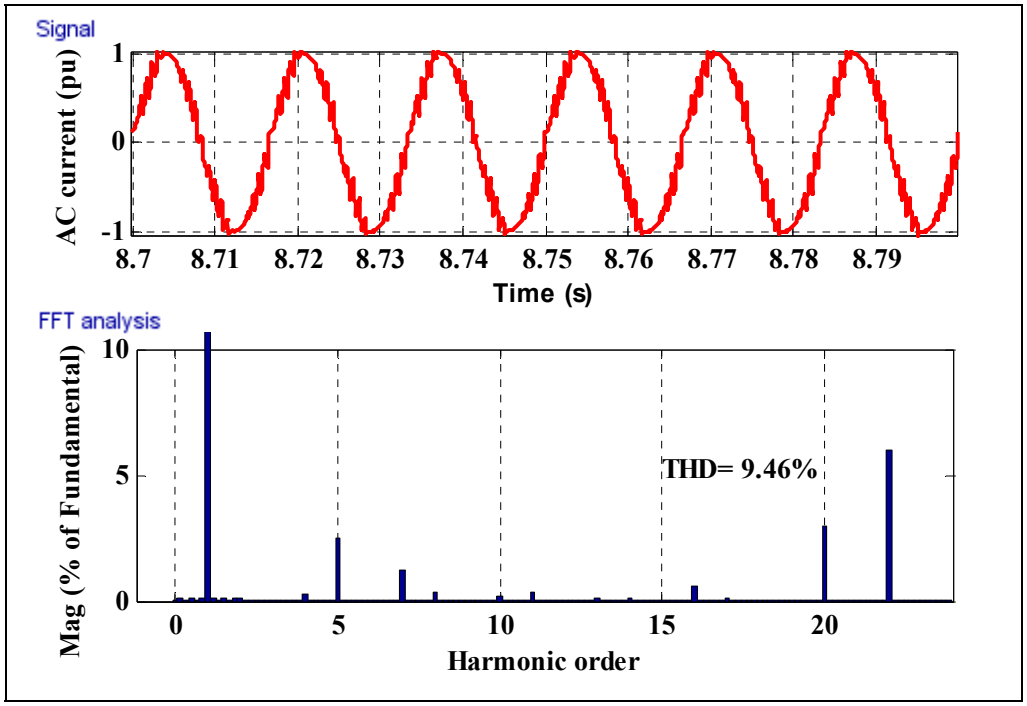

Figure 4.16 AC bus current of four VSC module and harmonic spectrum with the conventional SPWM

By using phase shifted triangle carrier as illustrated in Figure 4.7 (a), it is well-known that the equivalent carrier frequency is increased by 4 to $4f_c = 5769$ Hz. Figure 4.17 shows the AC current waveform of the four VSC modules and the harmonic spectrum. The 20^{th} and 24^{th} harmonics of Figure 4.16 are eliminated in the spectrum and the THD is reduced to 2.97 %. The switching losses remain the same as $f_c = 1440$ Hz.

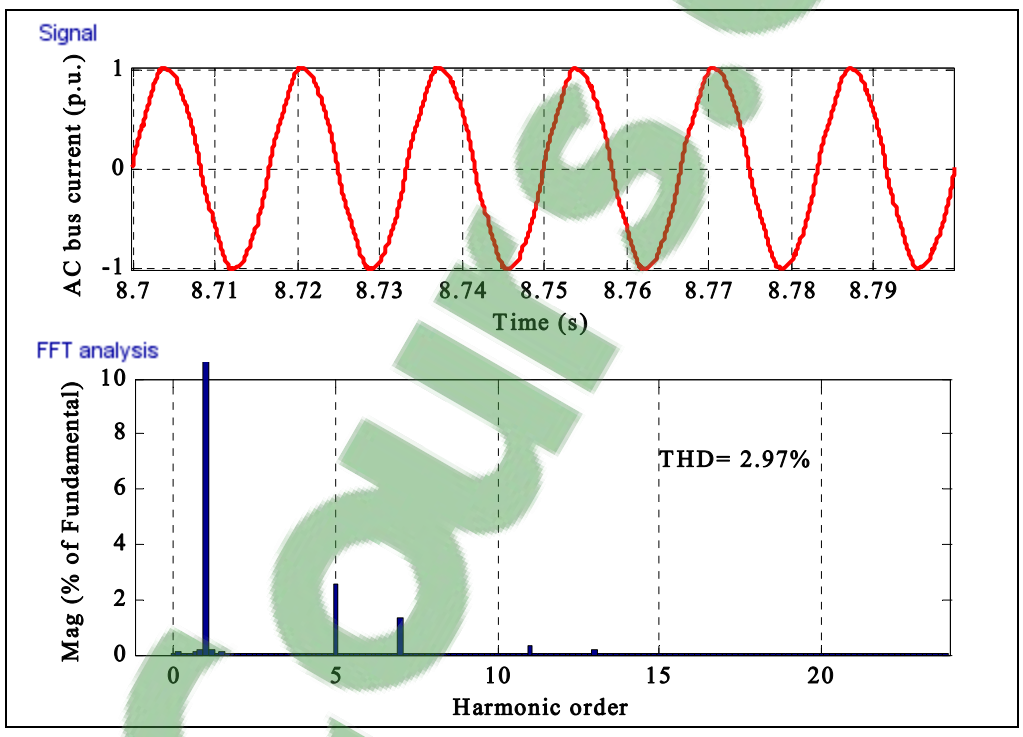

Figure 4.17 AC bus current of four VSC modules and harmonic spectrum with the phase shifted carrier SPWM

The corresponding waveform of the voltage and spectrum on the DC side are shown in Figure 4.18.

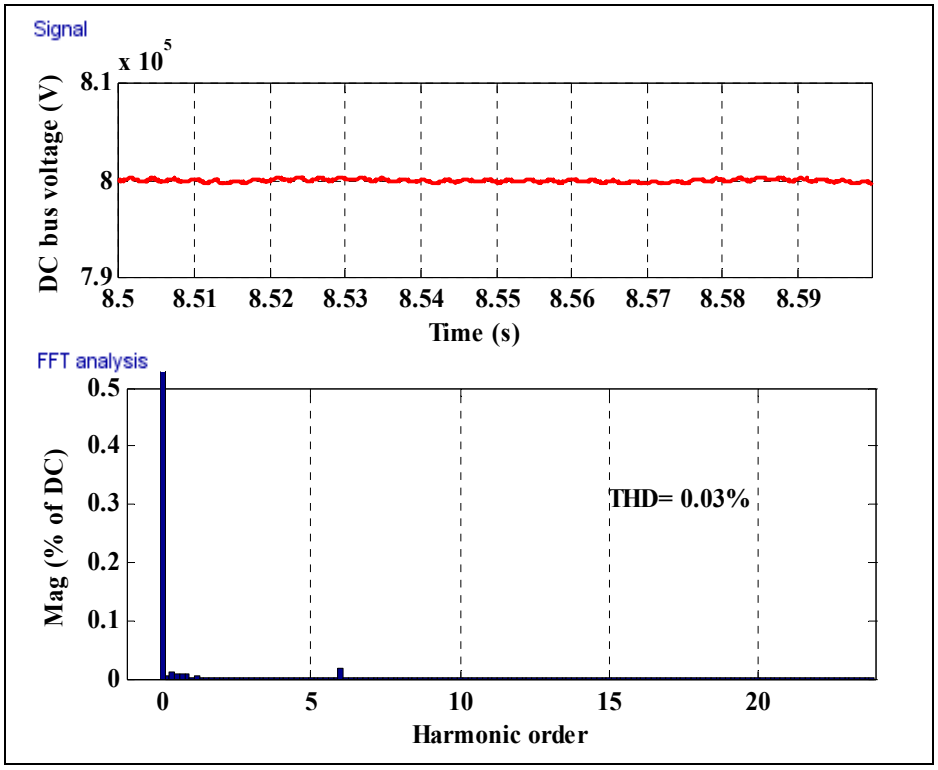

Figure 4.18 THD of DC bus voltage with the phase shifted carrier SPWM

4.7 Continuity of power supply after fault in VSC module

The method of ensuring continuity of power supply in the event of failure in any VSC module is by using bypass switches DBs, illustrated in Figure 4.1. When one of VSC module has a fault, it is taken out of service by closing the bypass switch. A VSC-module at the other end of the transmission is likewise bypassed so that the DC voltage is lowered by the same amount. In thyristor-UHVDC, there is a brief interruption of service for the fault to be located and switches to be manually reconnected. It is assumed that the same interruption is acceptable in VSC-UHVDC.

The remaining 3 VSC modules continue to use phase shifted triangle carriers of Figure 4.7 (b). Figure 4.19 shows the current waveform and the harmonic spectrum.

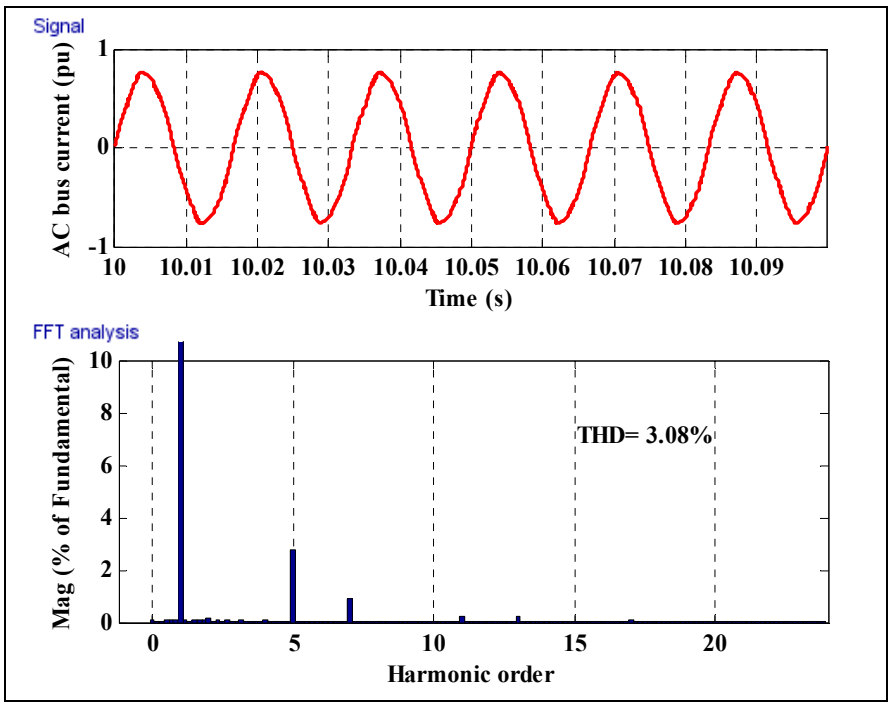

Figure 4.19 AC bus current of three VSC modules and harmonic spectrum

4.8 Higher Level of Modularity

The authors have used 4 VSC modules in series because they have followed the example of thyristor UHVDC as a guide. In view of the successful simulation of the proposed topology of Figure 4.1 and in view that the analysis of Section 4.3 does not impose any limit, there are good reasons to use as large a number of VSC modules as physical space consideration allows.

One benefit relates to the DC voltage, when one VSC is incapacitated, is that the DC voltage is lowered by a factor of (N-1)/N. Another benefit is the reduction of switching losses with increasing the number of modules by using the phase shifted triangle carrier technique.

The large number of modular levels is one of the reasons for the attractiveness of modular multilevel converters (MMC) (Bergna et al., 2013; Solas et al., 2013; Wang, Hao et Ooi, 2014). It should be noted that although MMC reduces high frequency harmonics, large capacitors are required to filter the 2nd and other low order harmonics which come under the name of "circulating current" (Tu, Xu et Xu, 2011).

Although there is research in using feed-forward and feedback methods (Wang, Hao et Ooi, 2014) to suppress the "circulating current" to enable capacitor size to be reduced, one has to wait for the feed-forward and/or feedback methods to be put into practice. MMC is relatively new and not fully understood. In addition, the mathematical equations and modeling MMC are highly nonlinear.

On the other hand, VSC is known to operate as switch mode linear amplifiers and control techniques from linear system theory can be implemented by VSCs (Mwinyiwiwa, Wolanski et Ooi, 1996).

Physical space consideration is related to coping with the large number of connecting cables. Figure 4.1 shows 4 separate transformers. When the size of a VSC is reduced, the number of turns in the windings for the VSC AC output is reduced so that one transformer iron core can fit insulated windings from a few VSCs.

4.9 Conclusion

This chapter shows that UHVDC based on VSCs technology is feasible. Feasibility is demonstrated by:

1. Circuit theory analysis which shows that operating of N modules of VSCs connected in series on their DC sides is no different from operating the N modules of VSCs separately. The VSC modules will produce identical AC currents and DC voltages, provided the voltages across the DC terminals are maintained equal. This research has

shown that feedback circuits can equalize the DC voltages of the series connected VSC modules. As VSC modules can be produced by manufacturers which yield AC currents and DC voltages to very fine tolerance, VSC-UHVDC is feasible when equalization feedback is incorporated.

2. The VSC-UHVDC model passes two demanding tests: response to step active and reactive power test and reversal of direction power flow test. The tests make use of simulation by MATLAB/SPS.

The research shows that N VSC modules connected in series, it is possible to maintain THD standards while lowering switching losses by N. The success demonstrated by tests on the 4-VSC UHVDC suggests that future VSC-UHVDC should consist of larger number of VSC modules to reduce switching losses further. There is an upper limit possibly due to physical space to connect cables.

CONCLUSION

This work aims at the control and application of VSC-HVDC system for grid connection. Firstly, in order to exploit the benefits of VSC-HVDC system and improve the dynamic performance of the VSC-HVDC system, the conventional PI current control scheme, hysteresis current control scheme and the developed *abc* coordinates deadbeat current control scheme were implemented under the same conditions in the VSC-HVDC control system. These three different current control schemes, their advantages and disadvantages are analyzed and compared in details. Case of two-terminal VSC-HVDC system is developed in MATLAB/SPS and the dynamic performance of the system is evaluated during system start up, steady state, grid voltage sags, and power reversal changes. Simulation results show that these three control schemes for VSC-HVDC system can offer good dynamic performance when system start up and steady state, voltage sags in grid side AC voltages, and power reversal happening. Different control schemes have different responses performance in the system. Thus, we can choose different control schemes according to the system control requirements and applications.

Based on the above analysis of the inner control scheme for VSC-HVDC system, it is easy to know that the deadbeat current control scheme in *abc* coordinates is a good option. In the above research, we assume that the two-terminal AC systems are balanced three phase AC system, so the power feedback loop we did not use the power feedback regulators. In order to further improve the control system of the VSC-HVDC system, we added a power negative feedback regulator control for the outer loop. Combined with PI controller and the advantages of the deadbeat controller such as fast dynamic response, high tracking accuracy, and simple control structure and algorithms with determined parameters, a conventional PI controller is used in the outer loop for regulate the power flow and a current deadbeat controller is presented in the inner loop. Series simulation studies, such as start up and steady state, voltage sags, power step change, and the three-phase to ground fault, shows the developed *abc* coordinates deadbeat current control scheme provides a high performance control solution to the VSC-HVDC system.

As for the application of VSC-HVDC, due to the demand for power keeps increasing at a scale and speed all over the world in the past latest years. Growing renewable energy sources with power generation becomes increasingly distributed and a growing number of generation facilities located far away from load centers. It is necessary to study higher voltage level HVDC power transmission technology - UHVDC power transmission technology. In this research, two-level VSC modules based UHVDC transmission system is proposed first time, and this research reports on the first step which is series connection VSC modules for UHVDC operation is trouble free; Besides, to increase the stability of the DC voltages, the corresponding control system with DC voltage compensation equalizer is developed for the series-connected VSC modules based UHVDC system.

The series-connected VSC modules based UHVDC model passes two demanding tests: response to step active and reactive power test and reversal of direction power flow test. The tests make use of simulation by MATLAB/SPS. Some conclusions are drawn by this simulation study and analysis: 1) Lots of advantages of VSCs over thyristor based converters for HVDC application still take effective roles in this proposed UHVDC system, which has a simple configuration and clear control scheme. 2) By series connection of VSC modules, the DC voltage capacity is increased to the level required by the UHVDC. 3) And what's more, the robustness of the proposed system is improved by adding the proposed compensation DC voltage equalizer block to the control system. The voltages across the DC terminals are maintained equal. 4) Furthermore, it shows that N VSC modules connected in series, it is possible to maintain THD standards while lowering switching losses by N. 5) The success demonstrated by tests on four series-connected VSC modules based UHVDC suggests that future VSC-UHVDC should consist of larger number of VSC modules to reduce switching losses further. There is an upper limit possibly due to physical space to connect cables. This research has provides a simple and feasible solution for UHVDC power transmission and also offers one of the new energy highways for the future.

Some Challenges for Series Connected VSC modules

The challenges related to the series-connected VSC modules based UHVDC system will be met by manufacturers who have the know-how on transformer insulation to withstand the peak AC voltage together with the DC voltages of 200 kV, 400 kV and 600 kV from the four VSC modules. It should be pointed out that these manufacturers also have the know-how on auxiliary R-L-C circuits to equalize the voltages across hundreds of IGBTs connected in series so that they switch in unison to withstand the ultra-high voltages during steady-state and transient operation.

The attraction of MMC is to new comers in high voltage power electronic industries in China, India, Turkey, Iran and emerging nations who do not have the know-how on designing auxiliary R-L-C circuits to equalize IGBT voltages. If the inherent weakness problem related to "circulating current" cannot be solved economically, their alternative is to use the multi-VSC-modular approach of this research. The challenge in extending N = 4 to N = 100 is to reduce the large number of transformers. There are two ways to meet the challenge:

(A) One way to reduce the number of transformers is by connecting the AC outputs of the VSC modules to multiple units of galvanically isolated secondary windings of the same iron core. The method is used in ROBICON Perfect Harmonic medium voltage drives, which are vended by Siemens.

(B) As the cost of developing the know-how on auxiliary R-L-C circuits which can equalize the voltages across five or ten IGBTs connected in series is more affordable than for 100 IGBTs, the number of VSC modules can be reduced to N = 10, for example. The number of transformers and secondary windings can therefore be reduced.

A combination of (A) and (B) offers a solution. There will still be the challenge of having the know-how to insulate transformer windings with ac voltages riding on dc voltages. So far, the challenges discussed above are related to ultra-high voltage HVDC of this research in Chapter 4.

Future work

From the practical industry application view, there are still more work need to be further studied on series-connected VSC modules for UHVDC operation. For example, how the arm inductor should be arranged to avoid problems with voltage slopes; and how different fault cases would be handled in order to avoid excessive over-heating of power semiconductor devices or over-voltage in submodule capacitors, etc. It is believed that this issues listed above will ultimately be addressed by researchers in the future.

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